WHITE PAPER

From Complicated to Simple with Single-Chip Silicon Clock Generation

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While communications equipment manufacturers have aggressively pushed integrated circuit (IC) suppliers to combine features and functionalities onto a single chip in an effort to reduce footprint and design costs, performance and reliability concerns have meant timing sources have remained as standalone components. Traditionally, a large number of clock oscillators, crystals and fixed frequency clock generator and multiplier ICs have been required to satisfy the diverse clocking requirements of every major component on the PCB, including the CPU, memory, DSPs, framers, PHYs and mappers.

Today, new single-chip silicon clock generation products can effectively manage and control dataflow across multiple components for a range of applications. Beyond board space advantages, these single-chip solutions reduce power consumption, ease system validation, simplify frequency margining and help improve overall reliability. Most important, these new devices are designed with a unique architecture that supports any rate to any rate frequency translation, where traditional M/N and Fractional-N multiplication have frequency and performance limitations.

This flexibility is critical for high-speed optical transport networks (OTN) that transport a wide range of services, such as storage, SONET/SDH, digital video, Ethernet and more. OTN offers Transparent Transport of Client signal and Forward Error Correction (FEC), requiring unconventional rate conversion that cannot be achieved by traditional M/N divide or Fractional-N multiplication.

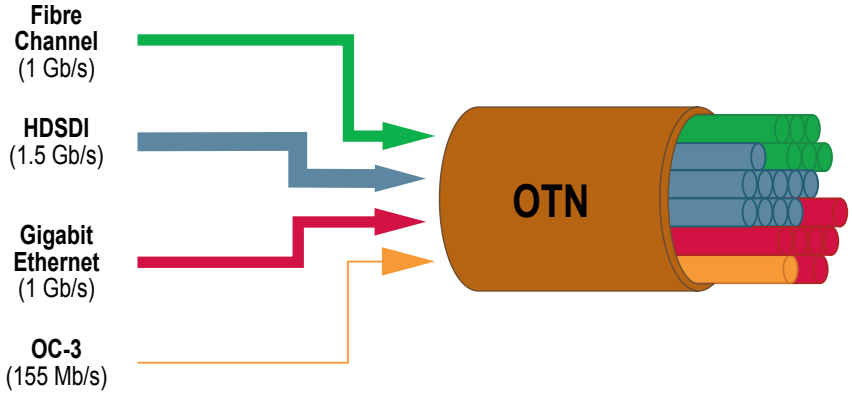
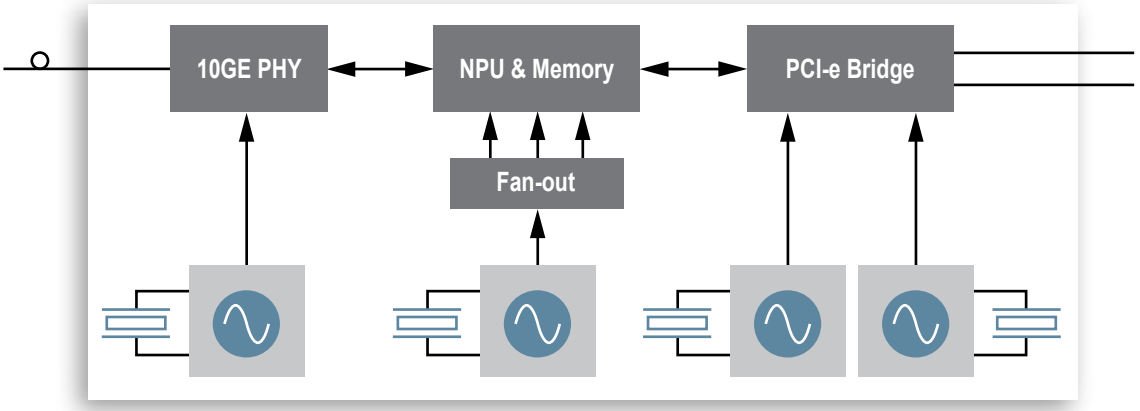


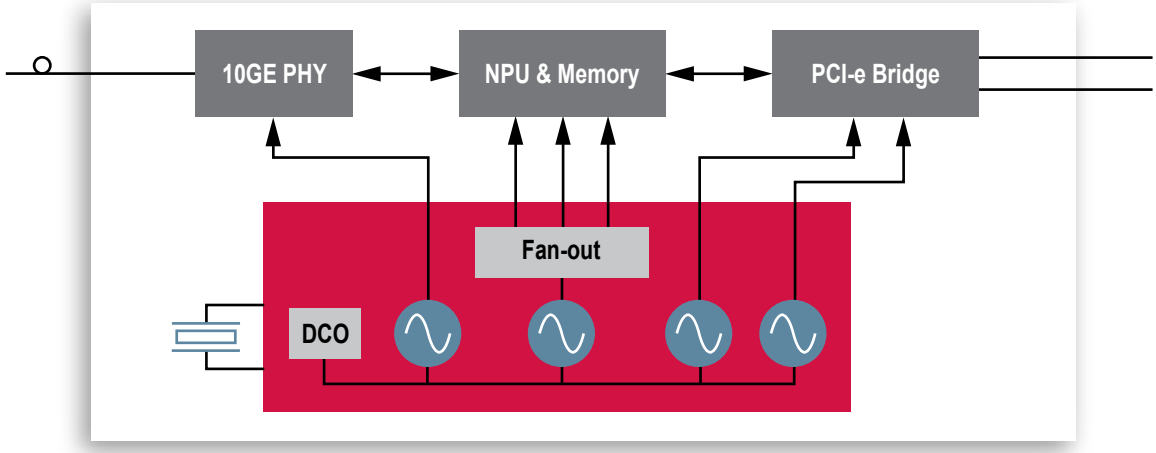
Figure 1—Optical Transport Network

The ability to replace multiple clock oscillators and fan-out circuitry with a single chip offers obvious savings in terms of PCB real estate and power consumption, especially if it can reduce the number of the large, power hungry, high-stability oscillators such as Oven Controlled Crystal Oscillators (OCXOs).

Reliability in the clocking subsystem is significant. The timing source often provides mission-critical functionality, such as clocking the CPU, where a single failure can bring down an entire system. Using an integrated silicon solution in place of a discrete solution (Figure 2) can improve the overall system reliability. For example, silicon ICs based on standard CMOS processes provide improved reliability compared with a quartz-based oscillator, with FIT rates that are routinely an order of magnitude or more better versus a crystal oscillator. In addition, the ability to replace four or more of crystals with a single silicon chip further amplifies the gains in reliability that can be achieved.



Discrete Oscillator Solution



Integrated Silicon Solution

Figure 2—Integrating timing solutions on a single chip

The flexibility and programmability of the clock generators allow designers to translate, generate and synthesize any output frequency required from a single fixed frequency oscillator. As a result, there is no need to maintain dozens of oscillators and crystals on the approved parts list manufacturers, allowing manufacturers to dramatically simplify inventory and reduce the Bill of Materials (BOM) complexity.

The powerful and flexible timing block can also be repurposed across multiple designs targeting applications with differing timing requirements. The programmability of the clock generator also allows a single design to target different applications without the need of multiple stuffing options on the BOM. For example, a 10G PHY can operate in LAN PHY mode at 10.3125 Gb/s or in WAN PHY mode (9.953 Gb/s) in order to interoperate with OC-192 SONET/ STM-64 SDH equipment. To operate in the different modes, the PHY requires a different reference clock, typically 156.25 Mhz for WAN mode and 155.52 MHz for LAN mode. With a programmable clock generator providing the low jitter reference clocks, a simple register write is all that is needed to change the configuration and enable the PHY to operate in a different mode.

A single-chip clock generation approach also helps speed design validation and system characterization. Frequency margining tests the frequency ranges for all onboard clock oscillators over which a system operates correctly and determines the margins between the allowed clock oscillator frequency ranges and the oscillator tolerances. It is useful in the validation phase to test onboard FPGAs and validate pull-in ranges of certain phase-locked loop (PLL) or voltage control crystal oscillator (VCXO) timing circuitry. Frequency margining can also be used to characterize the system response to various clock frequencies and offsets.

This can be a very time consuming task that requires populating a board with oscillators with known frequency offsets or using an external frequency generator to replace the onboard oscillators. In comparison clock generator ICs can dynamically support precise frequency offsets through a simple serial interface, meaning the entire system can be validated and characterized efficiently without extra time or cost.

New single-chip silicon clock generation products provide designers with the flexibility, programmability, performance, reliability and integration density required to simplify design, BOMs and validation. As these new devices replace costly, more complicated approaches to manage multiple components, timing solution providers are now helping meet manufacturers' demands for "smaller, cheaper and less power."

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