Unraveling Buck Converter Efficiency and Maximizing Performance

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Introduction

The first step we have taken towards systematically understanding the topic of Buck efficiency is to write a detailed Mathcad model of virtually each significant loss. We are deliberately ignoring smaller losses, those which we know barely affect overall efficiency. For example, we know that the RMS current in the output caps very small in a Buck, and we have disregarded that specific loss component. We have also disregarded core losses, since up to 1 MHz, they are usually relatively very small in a Buck. We have also made some "convenient" assumptions, since we do not want to be guilty of mistaking the forest for the trees. So, for example, the transition (crossover) time is set *equal*, for turn-on and for turn-off transitions. We have disregarded smaller losses from the charging and dumping of parasitic capacitances, such as those present across the FETs and the inductor. We have also assumed a Schottky of diode drop 0.6 V across each FET during the deadtime. In reality, the body diode may be conducting instead (if the Schottky is not present, or it is not placed properly on the PCB directly across the FET with very low-inductance traces). The R_{DS} used and stated in our calculations and graphs is not the nominal datasheet value, or some arbitrarily scaled temperature -compensated value, but the actual value present. We have included controller losses however, as this can rather dramatically affect efficiency at very light loads. We are ignoring pulse-skip modes as they are very implementation-dependent, and difficult to model, and not universally applicable either. But we have included the possibility of running the converter either in forced continuous conduction (i.e., full synchronous) mode at light loads (which we call "FCCM"), or in diode emulation mode (we call it "DCM", for discontinuous conduction mode).

Note that all our familiar converter design equations typically involve the parameter "r", the current ripple ratio, defined in general, as $\Delta I/I_{COR}$, where ΔI is the entire current swing (not *half* of the swing as sometimes used in literature), and I_{COR} is the "center-of-ramp" current value, which for a Buck is simply the load current I_O. We know that when r=2, we are in critical conduction mode. We may not realize it, but in fact, all our usual CCM (continuous conduction mode) equations apply even when r exceeds 2, *provided we are in FCCM*. So all the usual CCM equations were extrapolated in our spreadsheet down to very light loads (r > 2) in the FCCM/CCM case. However, in diode emulation mode, we enter DCM after the r=2 boundary is reached (for light loads). For DCM, we do have to use the correct DCM equations. In this manner we can finally describe the performance of the converter under changes in load or line for either operating mode.

But we can also "assemble" each loss one by one starting from the "ideal converter", at 100% efficiency. In this manner we can examine how each loss them affects the "shape" of the efficiency curve. This in turn leads us to understanding exactly how to raise the efficiency curve at different load or line conditions.

Only One Loss term at a time: Understanding each

Our base example is a 5V to 1.8V converter, with max load I_{OMAX} equal to 10A. We start with no losses. In Fig. 1 we introduce only crossover (switch transition) loss. The first thing we vary is the crossover loss itself, by varying the crossover time t_{CROSS}. We also vary frequency, input voltage, load, and "r_{SET}". This is the set "r" at max load and at max line. Of course, if we change application conditions, by slowly reducing the input voltage for example, or reducing the load, "r" will vary from the set point. But we are interested in knowing what will be the difference in the efficiency curves, if we set "r" to 0.5, versus say, 0.2, *at the design entry point of max line and max load*. And that set design value is "r_{SET}" here.

Note: In general, *efficiency curves are plotted in two ways: efficiency versus load current (for various constant input voltages), or efficiency versus line voltage (for various constant loads).* Our curves follow the former method of display. We also use the log scale for load current (x-axis) for greater "visibility" of the situation at light loads, so the curves may "look different". But they actually have the same basic shape as standard datasheet efficiency curves as we will soon see.

Crossover losses:

From Fig. 1 we see that these losses all stay flat with respect to load current, right up to the point where r exceeds 2 and the curves suddenly fall off. So switching losses seriously affect efficiency below the critical conduction point, and more so for FCCM/CCM mode rather than DCM. This realization allows us to significantly reduce the sudden dip in efficiency at light loads. But it is important we do not increase DCR in the process of going to larger inductances to reduce r. Otherwise, the improvement in switching losses at light loads will be swamped out by the increased conduction loss due to higher DCR. In Table 1 we summarize our observations and provide detailed suggestions to reduce the crossover losses.

Deadtime Losses:

These are actual a mix of what we may call switching losses and conduction losses. They are proportional to frequency, but also depend on the deadtime itself, and the (assumed 0.6V) drop across each FET during the deadtime. In Fig. 2 we plot the efficiency versus load current for only deadtime losses. The findings, and suggestions for improvement, are tabulated in Table 2. Note they are very similar to the crossover losses, except for one notable exception: deadtime losses do not depend on input voltage. That would be one way of trying to gauge on the bench, whether the low-efficiency at light loads is due to crossover losses or deadtime losses.

Input Cap ESR Losses:

In Fig. 3 we plot the variations of these, and summarize the conclusions in Table 3. Note that, as for all conduction losses, changing the underlying resistance (the ESR_IN in this case), causes the most impact on efficiency at high loads. Changing V_{IN} in this case has a U-turn effect: it maxes out at $V_{IN} = 2\times V_O$, corresponding to highest RMS currents at D = 0.5. We know that is true for a Buck input cap. (For a Boost, the input cap RMS is very small, so we can ignore that usually. For a Buck-Boost, the input cap RMS increases dramatically and steadily for all duty cycles from 0 to 1).

Note that changing r_{SET} will not noticeably affect the efficiency at max loads, and also not at light loads for DCM, but in the mid-current range, there is some effect. As expected, since this is a pure conduction loss term, it is unaffected by frequency.

Conduction Losses (R_{DS} and DCR):

In Fig. 4 we show that DCR and R_{DS} variations behave similar to ESR_IN conduction losses. One key point to note is that if we set R_{DS_BOT} as zero, then as we increase the input, efficiency improves. That is understandable because as input increases, the duty cycle pinches OFF, and so less time is spent by the inductor current in the dissipative element (the top FET). Similarly, if we only have R_{DS} present in the bottom FET (R_{DS_TOP} is zero), then as we increase the input, efficiency falls as more time is spent in the dissipative element (the bottom FET). In practice, when both R_{DS} terms are present, what happens to overall efficiency with respect to V_{IN}, depends on which R_{DS} is bigger: the top FET or the bottom FET.

But there is another important lesson here. If we have a system with D<0.5 (say 5V to 1.8V), and we want to "distribute" a net R_{DS} (and die cost) appropriately between top and bottom FET positions, we are better off allocating lower R_{DS} to the *bottom* FET, since the current spends more time in the lower FET. However, if we have a case where D>0.5 (such as 5V to 3.3V), we design our system more optimally by allocating lower R_{DS} to the *top* FET. In fact, in general, we can proportion the two R_{DS}'s to be inversely proportional to the conduction time of each FET, so the losses will be well-distributed (and minimum overall). In Tables 4, 5 and 6 we have summarized the trends for the R_{DS} terms ad DCR for completeness sake. In Fig. 5, we compare the relative effect of these conduction loss terms too.

Controller IC Losses:

We are assuming the controller IC draws a fixed current "I_{CONT}", irrespective of input voltage. We see that this has a gradually increasing significant effect at light loads as expected. We have seen that all the conduction loss terms do NOT cause the efficiency to fall below r=2 boundary unless we are in CCM/FCCM. If the chip is DCM-enabled, the drop in efficiency below r=2 boundary occurs only due to switching losses. And it occurs right from the r=2 boundary. However if we minimize all switching losses, there will still be a "hump" in efficiency ar very light loads --- and this is due to I_{CONT} losses. The "hump" due to this is not related at all to r_{SET} (or where exactly the r=2 boundary is). This becomes clearer when we cumulate the losses next.

Cumulating Losses: Adding them up One-by-One

In Fig. 6 we now cumulate the loss terms one by one, showing at each step what the impact on efficiency is. So we are in effect constructing the efficiency onion (reverse-peeling). We also plot the same without log scales to show the familiar shape of published efficiency curves. We learn that:

The fall in efficiency at max load regions is primarily due to conduction losses, whereas the fall at lighter loads is more due to switching losses, and that occurs most significantly below the r=2 boundary. However, by decreasing r_{SET}, from the usual "optimum of r = 0.4", to say 0.2 or even 0.1, ***but without increasing DCR losses****, will cause a dramatic increase in the maximum efficiency, simply because the switching-loss related hump moves to lower and lower load currents, and that just allows the conduction loss rising curve (for currents to the right of the r=2 boundary) to naturally keep rising more and more before r=2 is encountered and the efficiency falls off.*

This effort continues to Fig. 7 where we learn to look at the efficiency curves and immediately figure out if the losses are primarily conduction loss related (curves drooping at max load), or switching loss related (curves drooping at mid to light loads). One particular case, where we see a constantly rising efficiency curve right up till I_{OMAX}, actually indicates an excessively large r_{SET} value. The solution to that is to increase the inductance (decrease r_{SET}), *but without significantly increasing DCR*. That will yield big benefits to efficiency. In Fig. 8, we take the "onion" and show the direct impact on this curve by various maneuvers/stratagems to increase overall efficiency. We show what happens as we change r_{SET}, or frequency and so on.

The Underlying Buck Spreadsheet

In Fig. 9 we share all the equations used in the spreadsheet used for all the efficiency curves. These incorporate the relevant DCM equations.

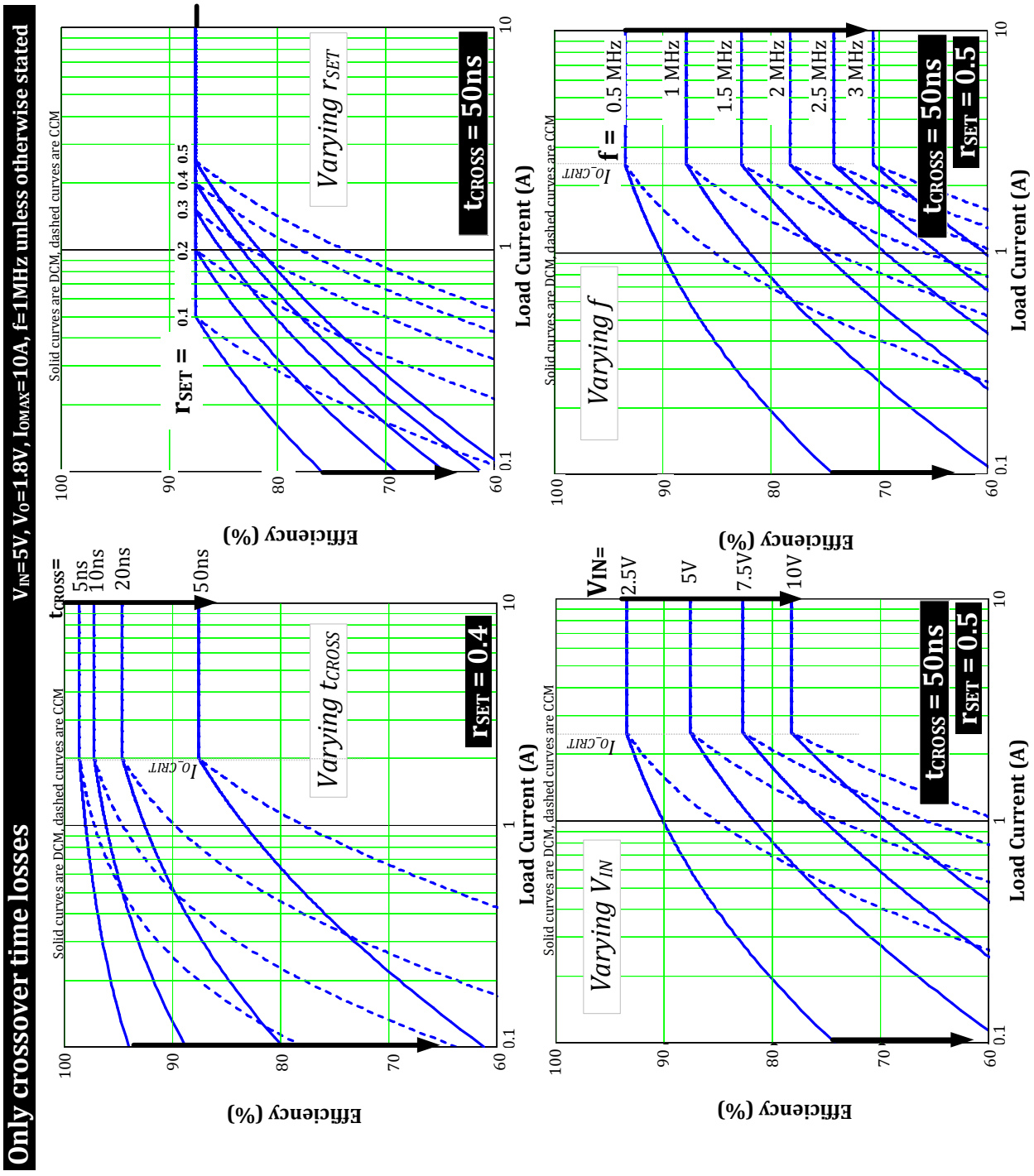

Fig. 1: Effect of crossover time only (starting with ideal converter)

Crossover time profile (one change at a time)		
Parameter	**Effect**	**Suggestion and Impact**
Increasing t_{CROSS}	Efficiency will fall as expected --- but the fall is equal in the region from I_{OMAX} to critical load I_{O_CRIT}. Below I_{O_CRIT} it will have an increasingly significant effect on efficiency, but more for FCCM than for DCM	Reduce t_{CROSS} if possible. Will improve efficiency for all loads
Increasing V_{IN}	Efficiency will fall as expected --- but the fall is equal in the region from I_{OMAX} to critical load I_{O_CRIT}. Below I_{O_CRIT} it will have an increasingly significant effect on efficiency, but more for FCCM than for DCM	Reduce V_{IN} if possible. Will improve efficiency for all loads
Increasing f	Efficiency will fall as expected --- but the fall is equal in the region from I_{OMAX} to critical load I_{O_CRIT}. Below I_{O_CRIT} it will have an increasingly significant effect on efficiency, but more for FCCM than for DCM	Reduce frequency is possible. Will improve efficiency for all loads
Increasing r_{SET} *(r_{SET} is the set r at max load, max input)*	Changing r_{SET} (different inductance, but maintaining low-enough DCR as we change r_{SET}), will not affect the efficiency between I_{OMAX} to I_{O_CRIT}. But since efficiency drops below I_{O_CRIT} simply on account of crossover loss in general, higher r_{SET} will have an increasingly bad effect on efficiency at light loads (both for DCM and for FCCM). So, decreasing r_{SET}, will reduce the impact of crossover loss significantly at light loads, even for the same crossover time. To reduce r_{SET}, we need a higher inductance. So long as this is not accompanied by an increase in DCR, then from the DCR efficiency curves we see that reducing r_{SET} will not affect efficiency at max loads, but will cause great improvement in light-load efficiency on account of the DCR versus r_{SET} plots too. So by lowering r_{SET} *without increasing DCR*, will cause a great improvement in light load efficiency on account of the profiles of crossover loss and DCR loss.	Reduce r_{SET} if possible. Will improve efficiency significantly at light loads

Table 1: Effect of crossover time only, and suggestions to improve efficiency

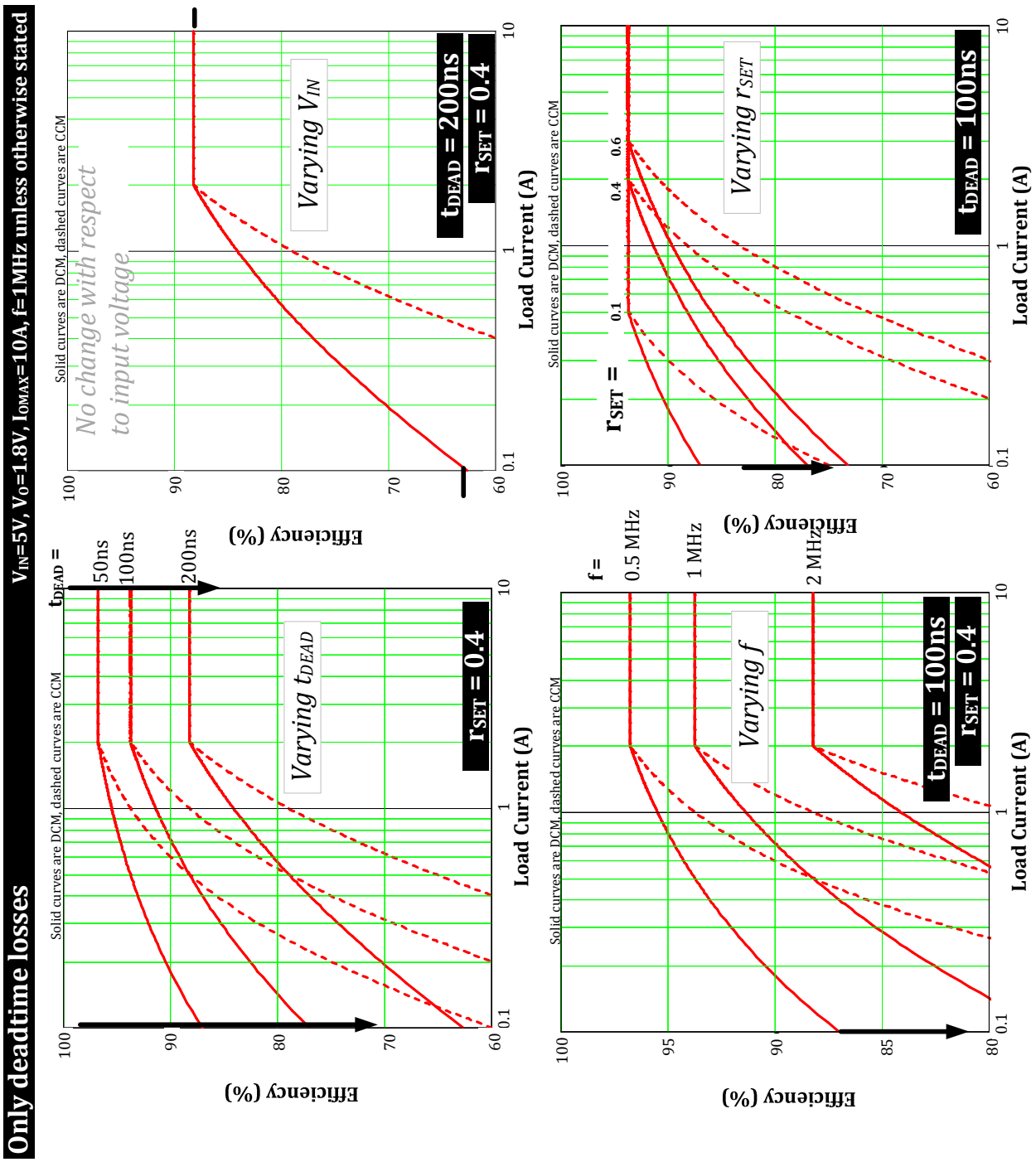
Only deadtime losses
VIN=5V, VO=1.8V, IOMAX=10A, f=1MHz unless otherwise stated
Varying VIN
No change with respect to input voltage
tDEAD = 200ns
rSET = 0.4
Varying rSET
tDEAD = 100ns
rSET =
0.1
0.4
0.6
Varying tDEAD
tDEAD =
50ns
100ns
200ns
rSET = 0.4
Varying f
f =
0.5 MHz
1 MHz
2 MHz
tDEAD = 100ns
rSET = 0.4
Solid curves are DCM, dashed curves are CCM
Efficiency (%)
Load Current (A)

Fig. 2: Effect of deadtime only (starting with ideal converter)

Deadtime time profile (one change at a time)		
Parameter	**Effect**	**Suggestion and Impact**
Increasing t_{DEAD}	Efficiency will fall as expected --- but the fall is equal in the region from I_{OMAX} to critical load I_{O_CRIT}. Below I_{O_CRIT} it will have an increasingly significant effect on efficiency, but more for FCCM than for DCM	Reduce t_{DEAD} if possible. Will improve efficiency for all loads
Increasing V_{IN}	Efficiency does not depend on V_{IN}, since the drop across the FET during the deadtime ("V_{DEAD}") is fixed (we have assumed a default of 0.6V for the curves). Only changing that voltage drop will affect efficiency results	Reduce V_{DEAD} if possible. That will improve efficiency for all loads
Increasing f	Efficiency will fall as expected --- but the fall is equal in the region from I_{OMAX} to critical load I_{O_CRIT}. Below I_{O_CRIT} it will have an increasingly significant effect on efficiency, but more for FCCM than for DCM	Reduce frequency is possible. Will improve efficiency for all loads
Increasing r_{SET} *(r_{SET} is the set r at max load, max input)*	Changing r_{SET} (different inductance, but maintaining low-enough DCR as we change r_{SET}), will not affect the efficiency between I_{OMAX} to I_{O_CRIT}. But since efficiency drops below I_{O_CRIT} simply on account of deadtime loss in general, higher r_{SET} will have an increasingly bad effect on efficiency at light loads (both for DCM and for FCCM). So, decreasing r_{SET}, will reduce the impact of deadtime loss significantly at light loads, even for the same deadtime. To reduce r_{SET}, we need a higher inductance. So long as this is not accompanied by an increase in DCR, then from the DCR efficiency curves we see that reducing r_{SET} will not affect efficiency at max loads, but will cause great improvement in light-load efficiency on account of the DCR versus r_{SET} plots too. So by lowering r_{SET} *without increasing DCR*, will cause a great improvement in light load efficiency on account of the profiles of deadtime loss and DCR loss.	Reduce r_{SET} if possible. Will improve efficiency significantly at light loads

Table 2: Effect of deadtime only, and suggestions to improve efficiency

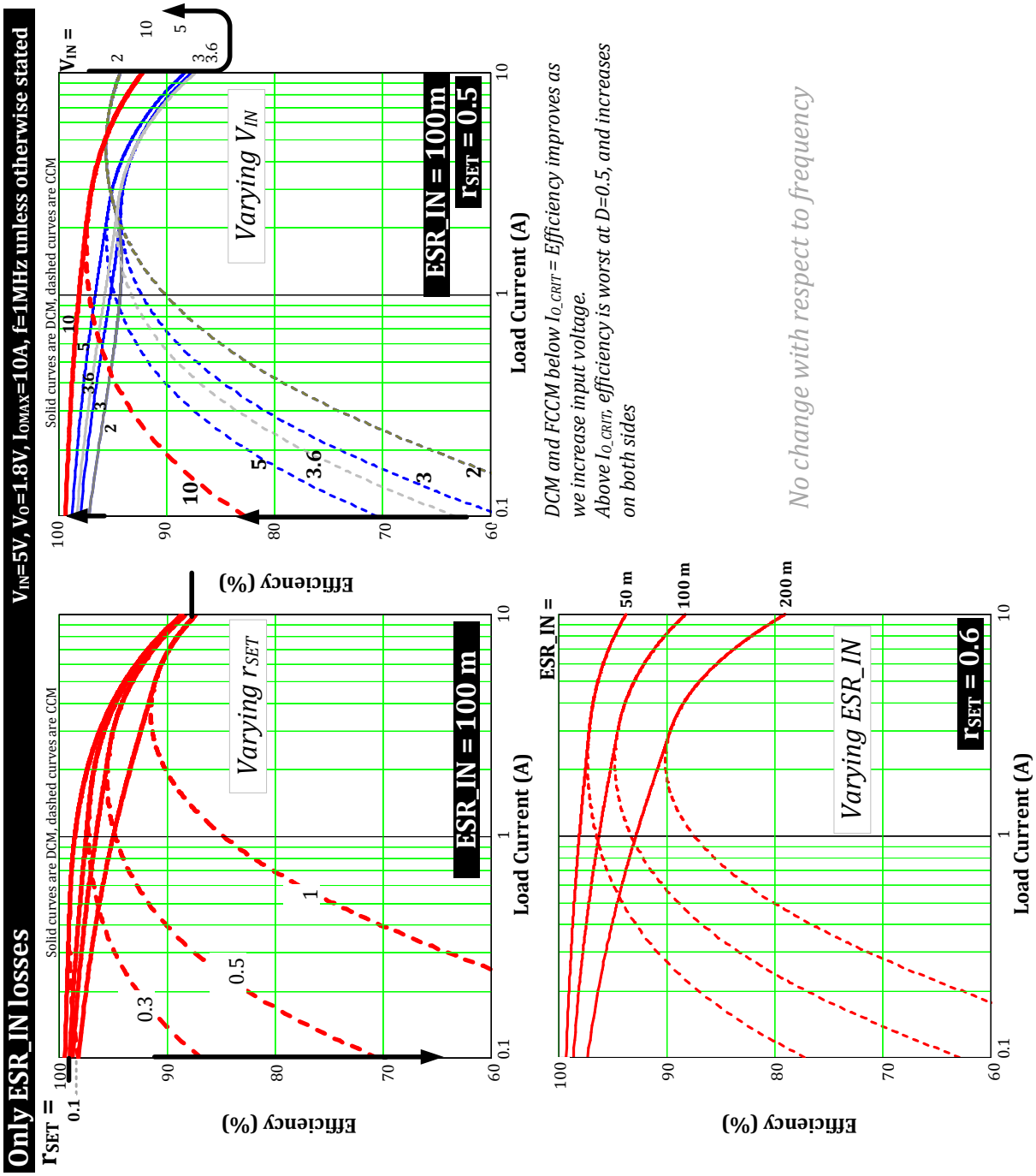
Only ESR_IN losses
VIN=5V, VO=1.8V, IOMAX=10A, f=1MHz unless otherwise stated
rSET = 0.1
Solid curves are DCM, dashed curves are CCM
Varying rSET
ESR_IN = 100 m
0.3
0.5
1
Efficiency (%)
Load Current (A)
VIN =
2
3
3.6
5
10
Varying VIN
ESR_IN = 100m
rSET = 0.5
DCM and FCCM below IO_CRIT = Efficiency improves as we increase input voltage.
Above IO_CRIT, efficiency is worst at D=0.5, and increases on both sides
No change with respect to frequency
ESR_IN =
50 m
100 m
200 m
Varying ESR_IN
rSET = 0.6

Fig. 3: Effect of ESR_IN only (starting with ideal converter)

Input Cap ESR profile (one change at a time)		
Parameter	**Effect**	**Suggestion and Impact**
Increasing ESR_IN	Efficiency will fall as expected --- but the fall is most at max loads. For DCM there is almost no effect on efficiency at light loads. For FCCM, there is an increasingly bad effect on efficiency at light loads, but the least effect of ESR_IN is in the region of I_{O_CRIT}.	Reduce ESR_IN to improve high-load efficiency in any mode, and light-load efficiency in FCCM mode
Increasing V_{IN}	Efficiency does not depend on V_{IN} at light loads in DCM. In FCCM at light loads, increasing input voltage improves efficiency (lower input current). In CCM, at max loads, the effect actually depends on duty cycle. When input voltage is twice the output voltage (D =0.5), there is maximum impact on efficiency on account of ESR_IN, the effect decreasing on either side of input range.	Increase V_{IN} to improve the efficiency at light loads in FCCM, and to improve efficiency at max loads in CCM too for input voltages greater than $2 \times V_O$.
Increasing f	Efficiency does not change	No effect
Increasing r_{SET} *(r_{SET} is the set r at max load, max input)*	Increasing r_{SET} (different inductance, but maintaining low-enough DCR as we change r_{SET}), will barely affect max load efficiency for CCM. It will barely affect light-load efficiency in DCM either, but in CCM/FCCM, it will cause significant worsening of light-load efficiency, and to a lesser extent, some efficiency loss in the region of I_{O_CRIT}.	Reduce r_{SET} if possible, to improve efficiency at mid and light loads in CCM/FCCM modes.

Table18.3: Effect of ESR_IN only, and suggestions to improve efficiency

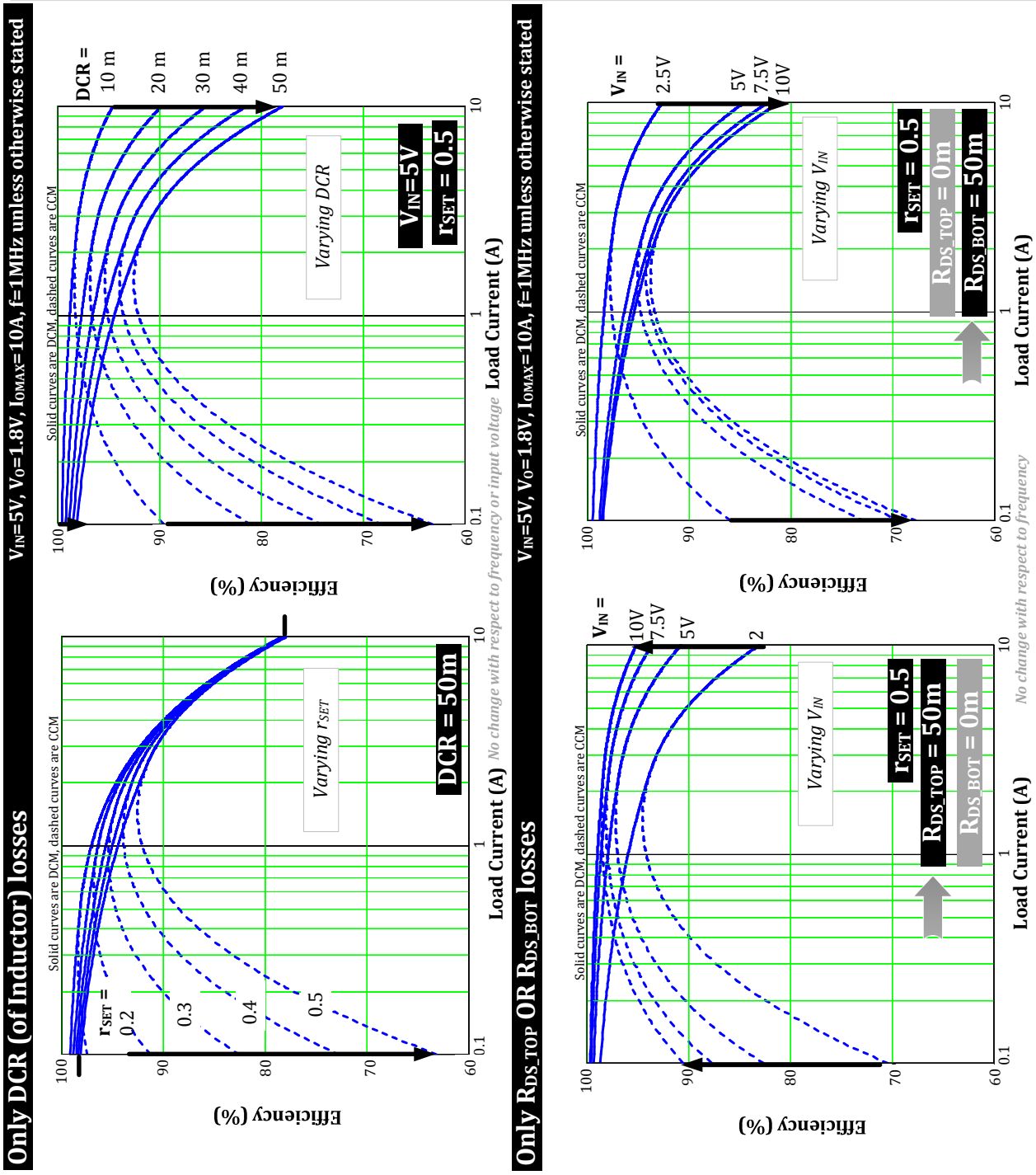

Fig. 4: Effect of R_{DS_TOP}, R_{DS_BOT} and DCR only (starting with ideal converter)

Inductor DCR profile (one change at a time)		
Increasing DCR	Efficiency will fall as expected --- but the fall is most at max loads. For DCM there is almost no effect on efficiency at light loads. For FCCM, there is an increasingly bad effect on efficiency at light loads, but the least effect of DCR is in the region of I_{O_CRIT}.	Reduce DCR to improve high-load efficiency in any mode, and light-load efficiency in FCCM mode
Increasing V_{IN}	Efficiency does not depend on V_{IN}	No effect
Increasing f	Efficiency does not change	No effect
Increasing r_{SET} *(r_{SET} is the set r at max load, max input)*	Increasing r_{SET} (different inductance, but maintaining low-enough DCR as we change r_{SET}), will barely affect max load efficiency for CCM. It will barely affect light-load efficiency in DCM either, but in CCM/FCCM, it will cause significant worsening of light-load efficiency, and to a lesser extent, some efficiency loss in the region of I_{O_CRIT}.	Reduce r_{SET} if possible, to improve efficiency at mid and light loads in CCM/FCCM modes.

Table 4: Effect of DCR only, and suggestions to improve efficiency

UPPER MOSFET RDS (R_{DS_TOP}) profile (one change at a time)		
Increasing R_{DS_TOP}	Efficiency will fall as expected --- but the fall is most at max loads. For DCM there is almost no effect on efficiency at light loads. For FCCM, there is an increasingly bad effect on efficiency at light loads, but the least effect of DCR is in the region of I_{O_CRIT}.	Reduce R_{DS_TOP} to improve high-load efficiency in any mode, and light-load efficiency in FCCM mode
Increasing V_{IN}	Efficiency improves at max load (CCM), and at light loads in FCCM/CCM	Increase V_{IN} to improve the efficiency at light loads in FCCM, and to improve efficiency at max loads in CCM too
Increasing f	Efficiency does not change	No effect
Increasing r_{SET} *(r_{SET} is the set r at max load, max input)*	Increasing r_{SET} (different inductance, but maintaining low-enough DCR as we change r_{SET}), will barely affect max load efficiency for CCM. It will barely affect light-load efficiency in DCM either, but in CCM/FCCM, it will cause significant worsening of light-load efficiency, and to a lesser extent, some efficiency loss in the region of I_{O_CRIT}.	Reduce r_{SET} if possible, to improve efficiency at mid and light loads in CCM/FCCM modes.

Table 5: Effect of R_{DS_TOP} only, and suggestions to improve efficiency

LOWER MOSFET RDS (R_{DS_BIT}) profile (one change at a time)		
Increasing R_{DS_BOT}	Efficiency will fall as expected --- but the fall is most at max loads. For DCM there is almost no effect on efficiency at light loads. For FCCM, there is an increasingly bad effect on efficiency at light loads, but the least effect of DCR is in the region of I_{O_CRIT}.	Reduce R_{DS_BOT} to improve high-load efficiency in any mode, and light-load efficiency in FCCM mode
Increasing V_{IN}	Efficiency worsens at max load (CCM), and at light loads in FCCM/CCM	Reduce V_{IN} to improve the efficiency at light loads in FCCM, and to improve efficiency at max loads in CCM too
Increasing f	Efficiency does not change	No effect
Increasing r_{SET} *(r_{SET} is the set r at max load, max input)*	Increasing r_{SET} (different inductance, but maintaining low-enough DCR as we change r_{SET}), will barely affect max load efficiency for CCM. It will barely affect light-load efficiency in DCM either, but in CCM/FCCM, it will cause significant worsening of light-load efficiency, and to a lesser extent, some efficiency loss in the region of I_{O_CRIT}.	Reduce r_{SET} if possible, to improve efficiency at mid and light loads in CCM/FCCM modes.

Table 6: Effect of R_{DS_BOT} only, and suggestions to improve efficiency

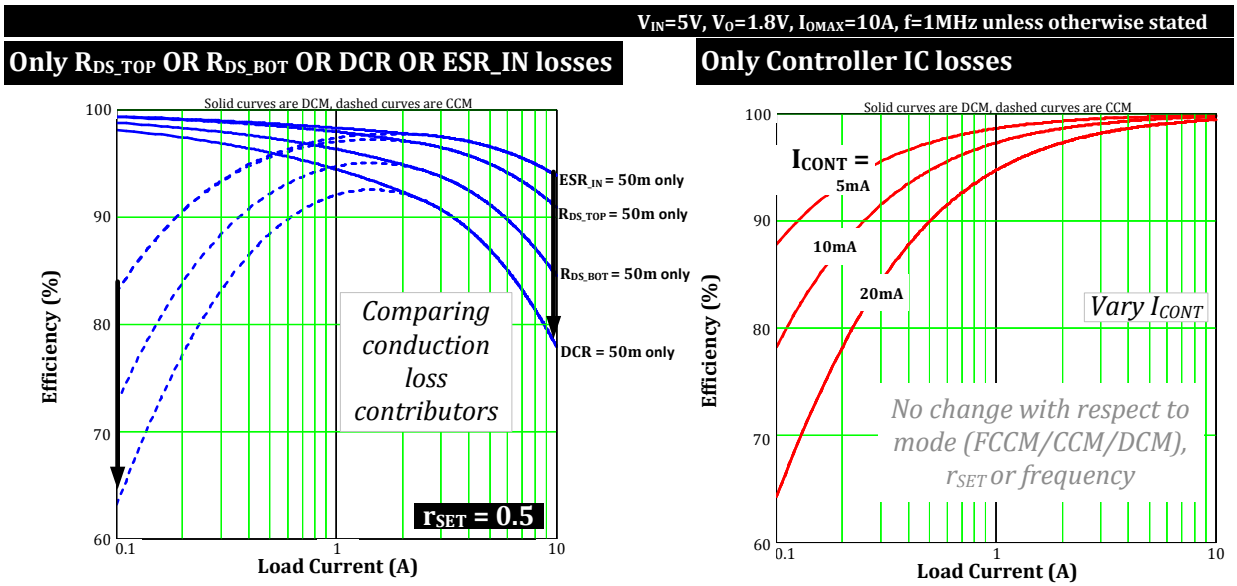

Fig. 5: Comparing effect on efficiency of conduction loss contributors and the IC (controller) current

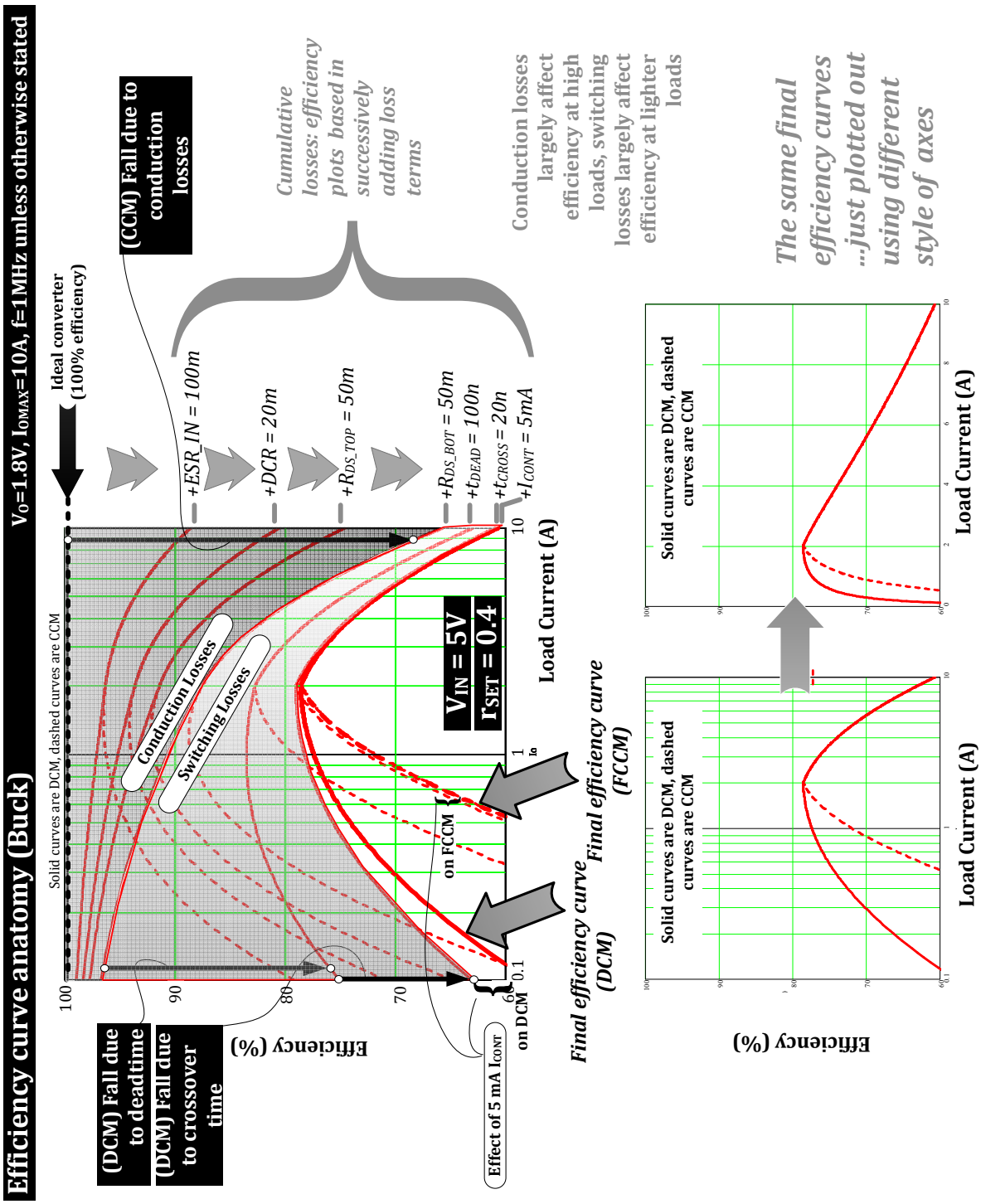

Fig. 6: Anatomy of efficiency curves: each loss term included successively

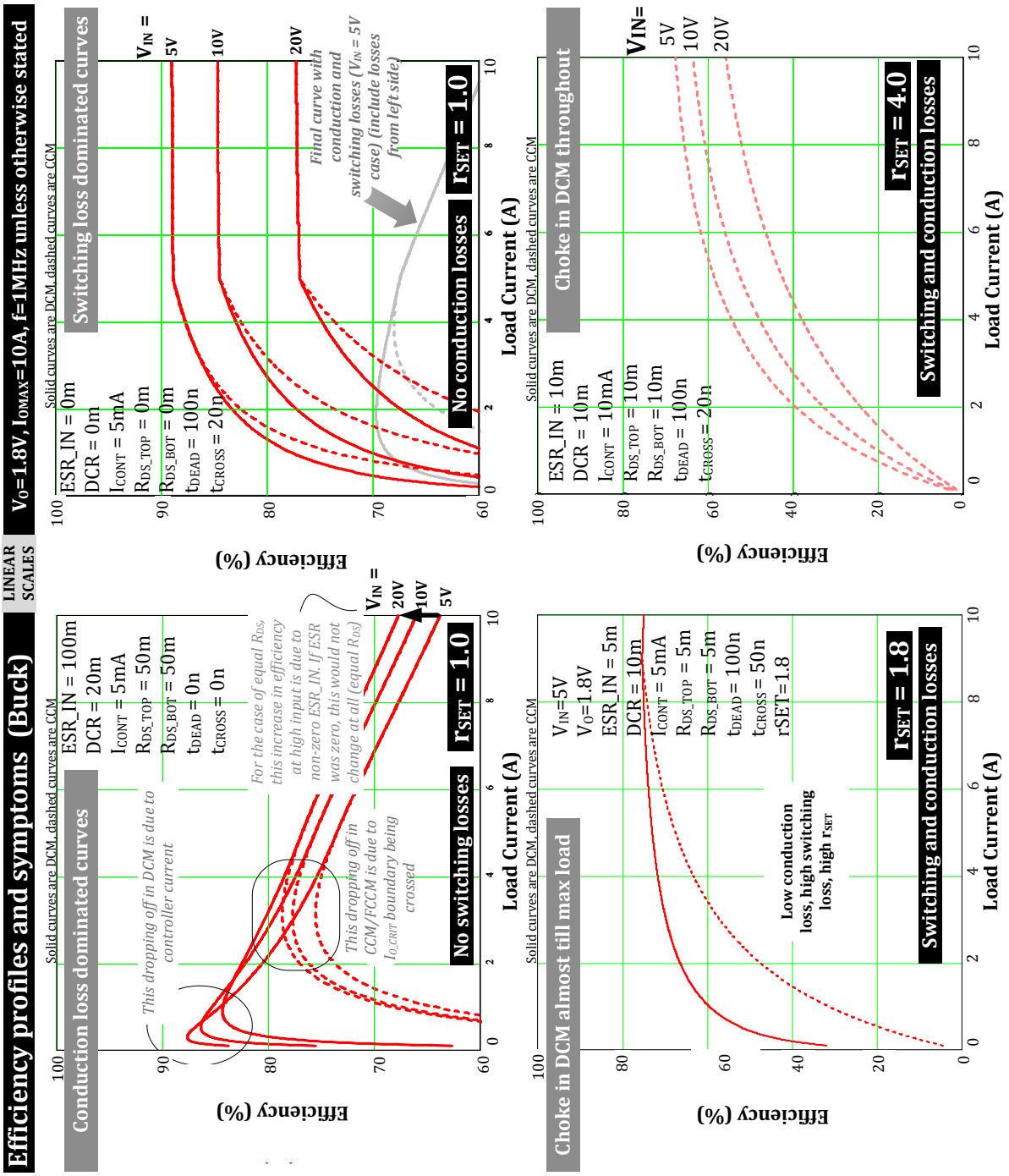

Fig. 7: Recognizing profiles of measured efficiency and knowing what to fix

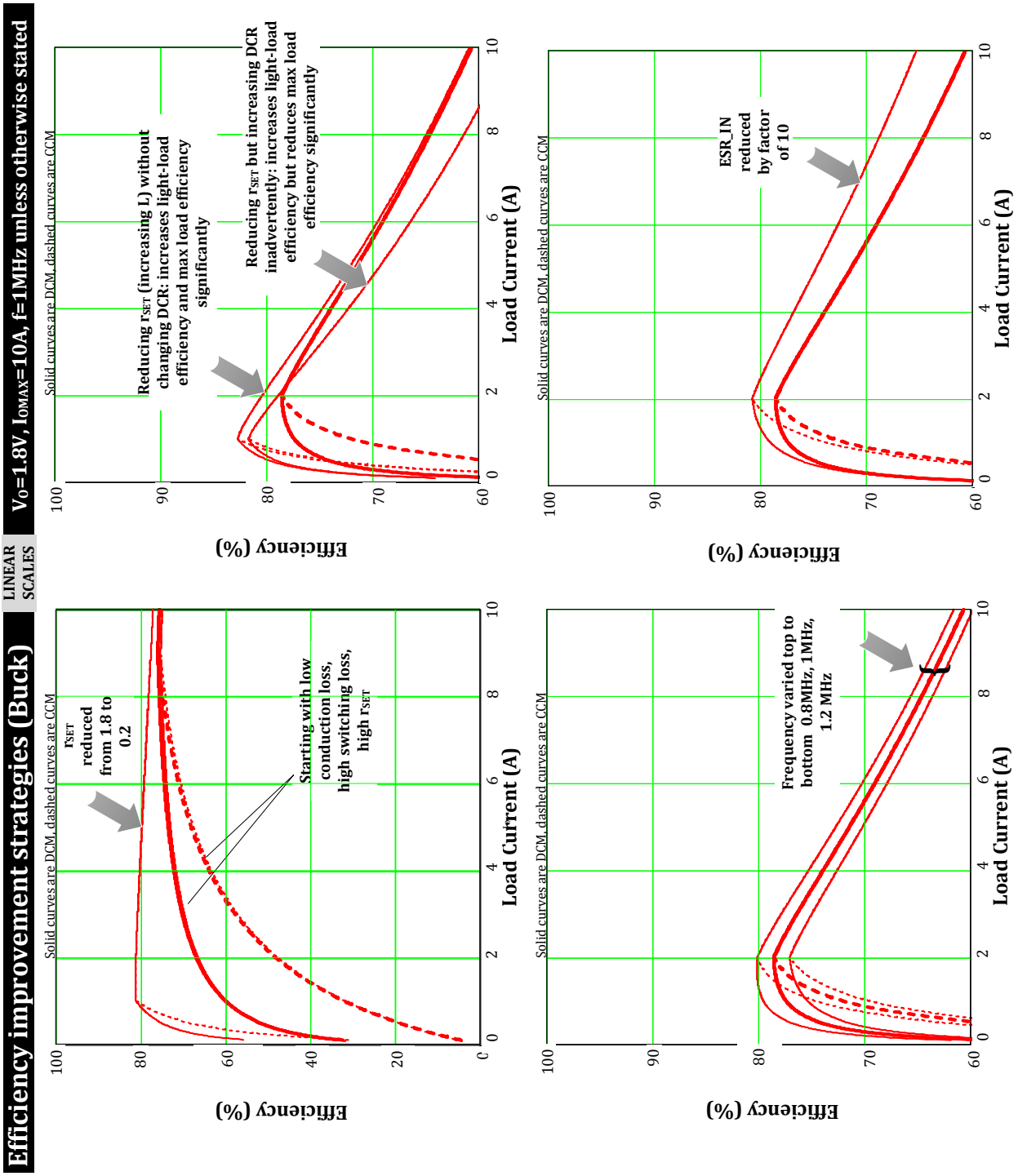

Fig. 8: Suggestions for Improvement in efficiency without major re-design

Buck efficiency calculations ("Full Buck Model")

CCM/FCCM Efficiency

$D = \frac{V_O}{V_{IN}}$; D′=1-D

$L = \frac{V_O}{I_{OMAX} \times r_{SET} \times f}(1-D)$ (set r to r_{SET} at max load, max input, and find L)

$r = \frac{V_O}{I_O \times L \times f}(1-D)$ (actual variation of r with load and D)

Conduction Losses (in CCM/FCCM)

$I_{RMS\_TOP} = I_O\sqrt{D\left(1+\frac{r^2}{12}\right)}$ (RMS current in top FET)

$I_{RMS\_BOT} = I_O\sqrt{D'\left(1+\frac{r^2}{12}\right)}$ (RMS current in bottom FET)

$I_{RMS\_IND} = I_O\sqrt{\left(1+\frac{r^2}{12}\right)}$ (RMS current in inductor)

$I_{RMS\_CIN} = I_O\sqrt{D\left(1-D+\frac{r^2}{12}\right)}$ (RMS in input cap)

$P_{TOP} = I_{RMS\_TOP}^{\ 2} \times R_{DS\_TOP}$; $P_{BOT} = I_{RMS\_BOT}^{\ 2} \times R_{DS\_BOT}$

$P_{IND} = I_{RMS\_IND}^{\ 2} \times DCR$; $P_{CIN} = I_{RMS\_CIN}^{\ 2} \times ESR_{IN}$

Switching loss (crossover term):

$P_{SW} = \frac{V_{IN}I_O}{2} \times \left(1+\frac{r}{2}\right) \times (f \times t_{CROSS}) + \frac{V_{IN}I_O}{2} \times \left|\left(1-\frac{r}{2}\right)\right| \times (f \times t_{CROSS})$

(for FCCM, allow r to exceed 2, so we need to use magnitude sign above)

Deadtime Loss:

Assume Schottky across both FETs, so $V_{DEAD} = 0.6$ typ

$P_{DEAD} = \frac{V_{DEAD}I_O}{2} \times \left(1+\frac{r}{2}\right) \times (f \times t_{DEAD}) + \frac{V_{DEAD}I_O}{2} \times \left|\left(1-\frac{r}{2}\right)\right| \times (f \times t_{DEAD})$

t_{DEAD} is deadtime (same for each transition).

Controller IC loss: assume constant current drawn I_{CONT}

$P_{CONT} = V_{IN} \times I_{CONT}$

Total loss in CCM/FCCM

$P_{CCM} = P_{TOP} + P_{BOT} + P_{IND} + P_{CIN} + P_{SW} + P_{DEAD} + P_{CONT}$

Efficiency in CCM:

$\eta_{CCM} = \frac{V_O I_O}{V_O I_O + P_{CCM}}$

Efficiency when system moves into DCM

$D_{DCM} = \left(\frac{2 \times I_O \times L \times f \times V_O}{(V_{IN} - V_O) \times V_{IN}}\right)$

$I_{PK\_DCM} = \frac{(V_{IN} - V_O) \times D_{DCM}}{L \times f}$ (peak current)

$I_{RMS\_TOP\_DCM} = I_{PK\_DCM} \times \sqrt{\frac{D_{DCM}}{3}}$ (RMS current in top FET)

$D'_{DCM} = \frac{2 \times I_O}{I_{PK\_DCM}} - D_{DCM}$ ("diode" duty cycle)

$I_{RMS\_BOT\_DCM} = I_{PK\_DCM} \times \sqrt{\frac{D'_{DCM}}{3}}$

$I_{RMS\_IND\_DCM} = I_{PK\_DCM}\sqrt{\left(\frac{D_{DCM}}{3} + \frac{D'_{DCM}}{3}\right)}$ (RMS in inductor)

$I_{AVG\_TOP\_DCM} = \frac{I_{PK\_DCM}}{2} \times D_{DCM}$ (average current in top FET)

$I_{RMS\_CIN\_DCM} = \sqrt{I_{RMS\_TOP\_DCM}^{\ 2} - I_{AVG\_TOP\_DCM}^{\ 2}}$ (RMS input cap)

$P_{TOP\_DCM} = I_{RMS\_TOP\_DCM}^{\ 2} \times R_{DS\_TOP}$;

$P_{BOT\_DCM} = I_{RMS\_BOT\_DCM}^{\ 2} \times R_{DS\_BOT}$;

$P_{IND\_DCM} = I_{RMS\_IND\_DCM}^{\ 2} \times DCR$;

$P_{CIN\_DCM} = I_{RMS\_CIN\_DCM}^{\ 2} \times ESR_{IN}$

Switching loss (crossover term):

$P_{SW\_DCM} = \frac{V_{IN}I_{PK\_DCM}}{2} \times (f \times t_{CROSS})$

Deadtime Loss:

Assume Schottky across both FETs, so $V_{DEAD} = 0.6$ typ

$P_{DEAD\_DCM} = V_{DEAD} \times I_{PK\_DCM} \times (f \times t_{DEAD})$

Controller IC loss: assume constant current drawn I_{CONT}

$P_{CONT} = V_{IN} \times I_{CONT}$

Total loss in DCM

$P_{DCM} = P_{TOP\_DCM} + P_{BOT\_DCM} + P_{IND\_DCM} + P_{CIN\_DCM} + P_{SW\_DCM} + P_{DEAD\_DCM} + P_{CONT}$

Efficiency in DCM:

$\eta_{DCM} = \frac{V_O I_O}{V_O I_O + P_{DCM}}$

Fig. 9: Equations for CCM/FCCM and DCM for use in "Full Buck Model" spreadsheet