ZL30155

DUAL CHANNEL UNIVERSAL CLOCK TRANSLATOR

The ZL30155 Dual Channel Universal Clock Translator, part of Microsemi's ClockCenter platform of Synchronous Clock devices, delivers industry-leading synchronization performance for high-speed complex applications. The highly integrated and programmable solution provides translation from any input reference frequency to any output clock frequency with jitter performance that can directly drive 10G PHY devices.

The ZL30155 integrates two independent digital PLLs, accepts four input references and generates 12 programmable clock outputs. The highly integrated solution allows designers to replace multiple components with a single chip, simplifying design and reducing component count and power.

Single-Chip Solution for Complex, High-Speed Applications

The industry's highest performance, most integrated timing solution for complex, high-speed applications.

Reduces design complexity and cost

- Operates from a single crystal resonator or clock oscillator
- Single device integrates two independent clock channels

Highest Performance Solution Available

- Programmable synthesizers generate any clock rate from 1 kHz to 720 MHz
- Two precision synthesizers generate clocks with jitter below 0.7 ps RMS for 10G PHYs
- Programmable digital PLLs synchronize to any clock rate from 1 kHz to 720 MHz
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLLs filter jitter from 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Automatic hitless reference switching and digital holdover on reference fail
- Eight LVPECL outputs and four LVCMOS outputs
- Four reference inputs configurable as single ended or differential

Fully Programmable

- Dynamically configurable via simple SPI/I2C interface

ZL30155 Block Diagram
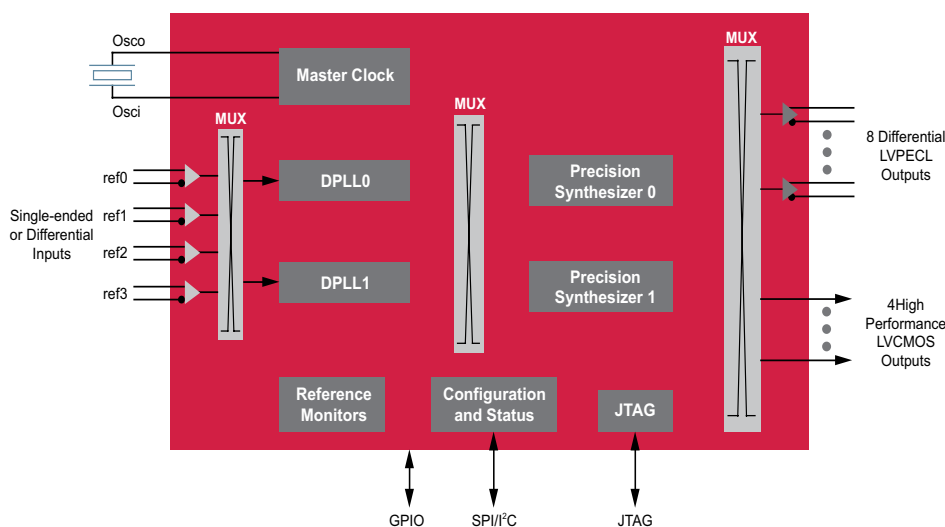
Applications

- 10 Gigabit line cards
- OTN multiplexers and transponders
- Synchronous Ethernet including 10GBASE-R and 10GBASE-W
- SONET/SDH, Fibre Channel, XAUI

Availability and Support

The ZL30155 Dual Channel Universal Clock Translator is in volume production. To learn more about Microsemi's new Clock-Center platform, http://www.zarlink.com/zarlink/hs/timing_ClockCenter.htm. Full information, including complete data sheets and design manuals, is available to registered MyZarlink customers. To register for a MyZarlink account, visit http://www.zarlink.com/zarlink/hs/login.htm.

Microsemi

10G OTN Transponder Application

Delivering a high level of integration coupled with unique frequency translation flexibility and per port programmability, the ZL30155 Dual Channel Universal Clock Translator is the perfect choice for any rate—any port—all the time performance in OTN applications.

The single-chip device provides full duplex timing and clocks that are jitter compliant and programmable by application. Two independent narrow band digital PLLs are integrated into this unique 2 stage architecture to support any rate to any rate frequency translation between four input references and up to 12 programmable output clocks.

The ZL30155 can accept up to four, single-ended or differential, input references of any frequency between 1 kHz and 720 MHz. Two integrated narrowband digital PLLs enable the device to accept low frequency input references and provides improved filtering. Output clock frequencies are independently defined from input references, allowing for generation of any frequency between 1 kHz and 720 MHz. Two high performance synthesizers provide independent output clock programmability on a per port basis. Per port programmability is critical in OTN applications where systems need to be able to support multiple types of traffic and requirements can change dynamically.
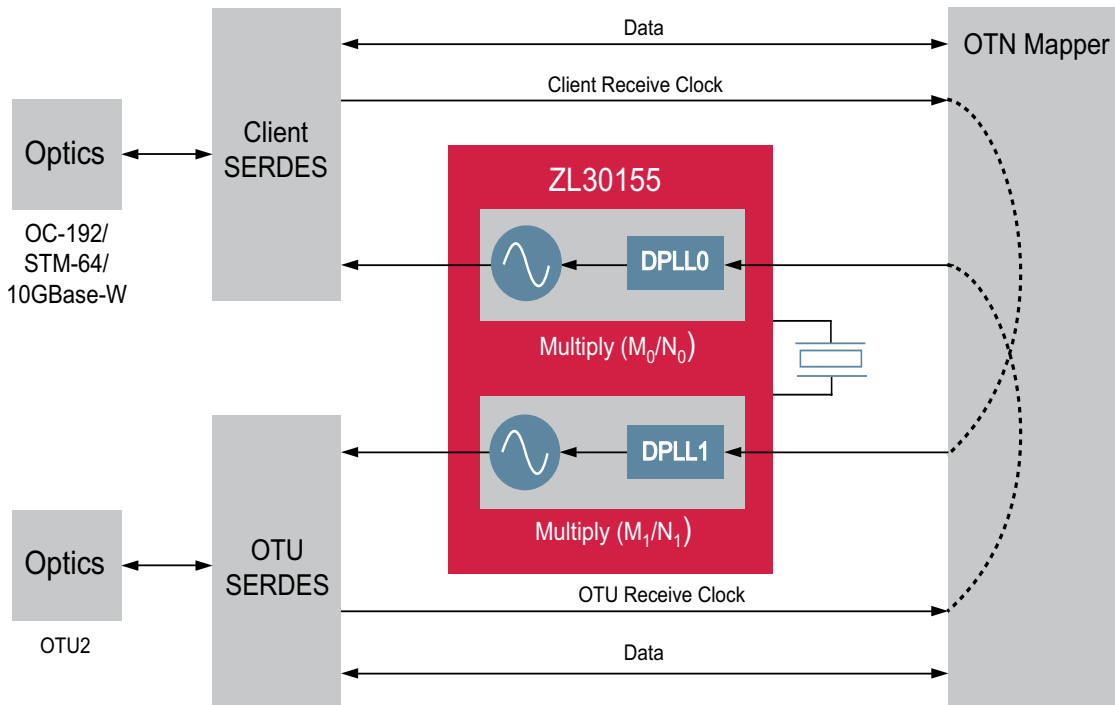
The application diagram below illustrates how the ClockCenter ZL30155 device can be implemented as a single-chip solution in a complex 10G OTN Transponder application. In this application, the ClockCenter ZL30155 is used to support full duplex timing. A standard SONET/SDH clock frequency, such as 622.08 Mhz, comes from a client SERDES through an OTN mapper and into the ZL30155 via one of its four input references. The ZL30155 uses DPLL1 and Synthesizer 1 to perform FEC scaling for transmit as an OTU clock through the OTU SERDES.

At the same time, an OTU receive clock with a frequency such as 669.32 MHz comes in from an OTU SERDES through an OTN mapper and into the ZL30155 as one of its three remaining input references. The ZL30155 uses DPLL0 and Synthesizer 0 to down convert the FEC scaling to 622.08 MHz for transmit as SONET/SDH clock through the client SERDES.

Either port can be independently and dynamically programmed to support any desired frequency and perform any desired scaling enabling full duplex timing from a single ZL30155 device.

Key functions of the ZL30155 enabling full duplex timing in OTN applications include frequency translation from any input clock rate to any output clock rate, per port programmability, jitter filtering, low jitter generation, hitless reference switching, free running capability and integration of multiple independent PLLs and synthesizers in a single chip.