Implementing Auxiliary Power in PoE

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Overview

Many PoE applications employ Auxiliary power sources, typically an AC-powered "wall wart" or a solar panel, connected to the Powered Device (PD). Integrating Auxiliary power can be a challenging design task and the PoE designer must understand the various methods, inherent tradeoffs and pitfalls that exist with each method of implementation. The main issues the designer may need to address are power source priority, smooth transitions between different power sources and inrush currents limiting.

Depending on the connection point there are three basic configurations that are commonly used to add Auxiliary power to PoE systems. Figure 1 shows broad introductory schematics of each option. Note also that we can usually go from a configuration with OR-ing diodes placed on the upper (positive) rail, to a configuration with diodes attached to the lower (return) rail. The underlying logic presented below remains the same for either configuration.

Option A: Connection at the PD's front end (before the pass-FET). Often called the "Front Aux" technique, or "FAUX" option.

Option B: Connection at the input of the PD's switching converter (behind the front end). Often called the "Rear Aux" technique, or "RAUX" option.

Note: In the latter case, there is a sub-option that includes an additional OR-ing diode ("D2", marked "optional" in Figure 1). The resulting behavior gets somewhat changed as discussed later.

Note: Both Option A and Option B (the latter without the extra diode sub-option) share the upper rail. So the schematic difference is really only where the return wire of the adapter is connected: before the pass-FET (Option A) or after the pass-FET(Option B).

Option C: Connection at the PD's DC-DC converter's output voltage. We will call it "direct OR-ed", or "output OR-ed".

Each of the above methods has its pros and cons as discussed below.

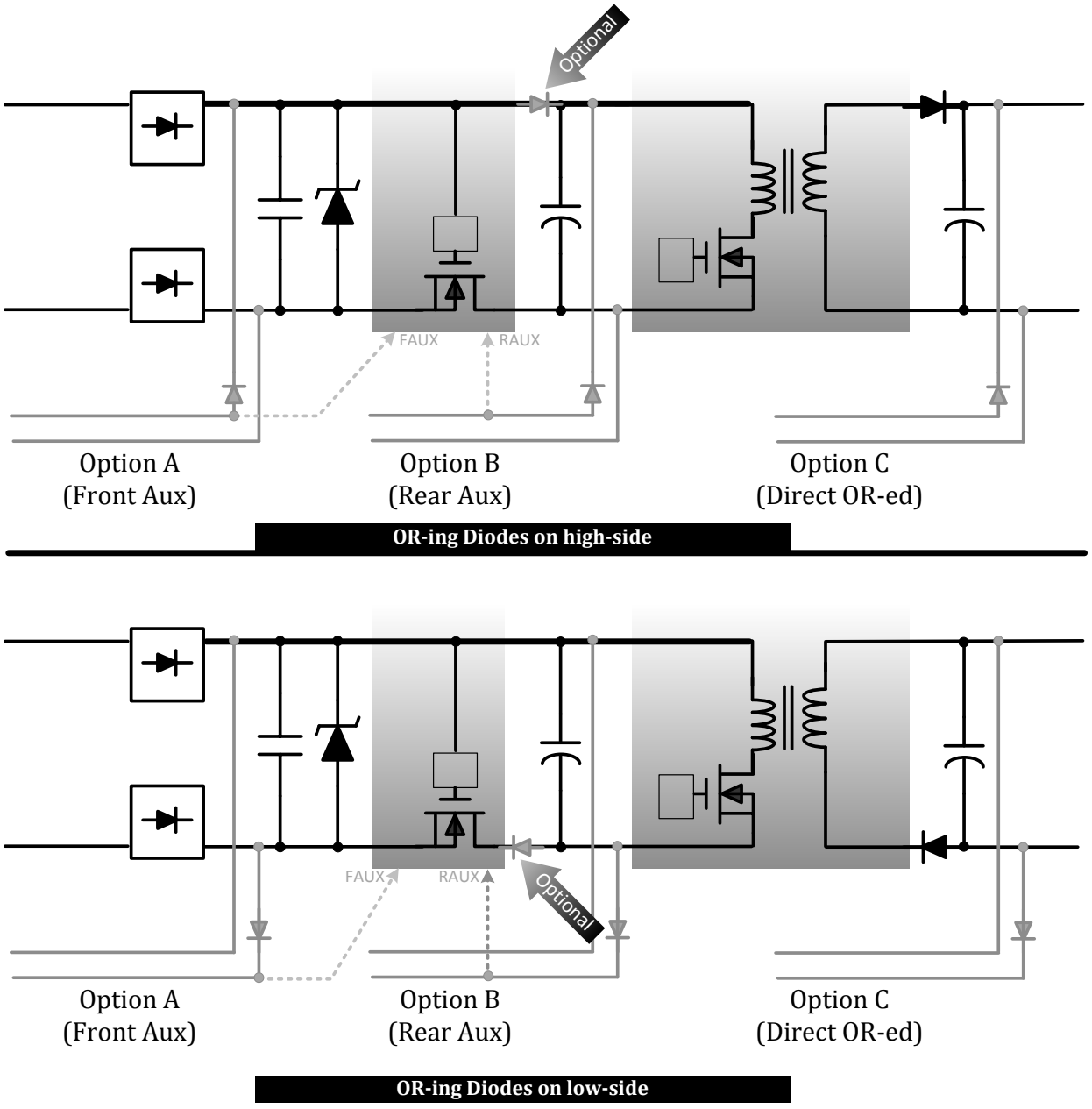

Figure 1: Adding Auxiliary Power

Auxiliary Power Option A (Front Aux or "FAUX" method)

The main drawbacks of this method are:

- First in, first served;
- Not possible to define adapter priority;
- Possible current sharing when PoE and adapter voltages are close;
- PD must support much higher currents.

We will discuss it in details below.

Let's first consider a typical case when V_{AUX} is within PoE Range (see Figure 2).

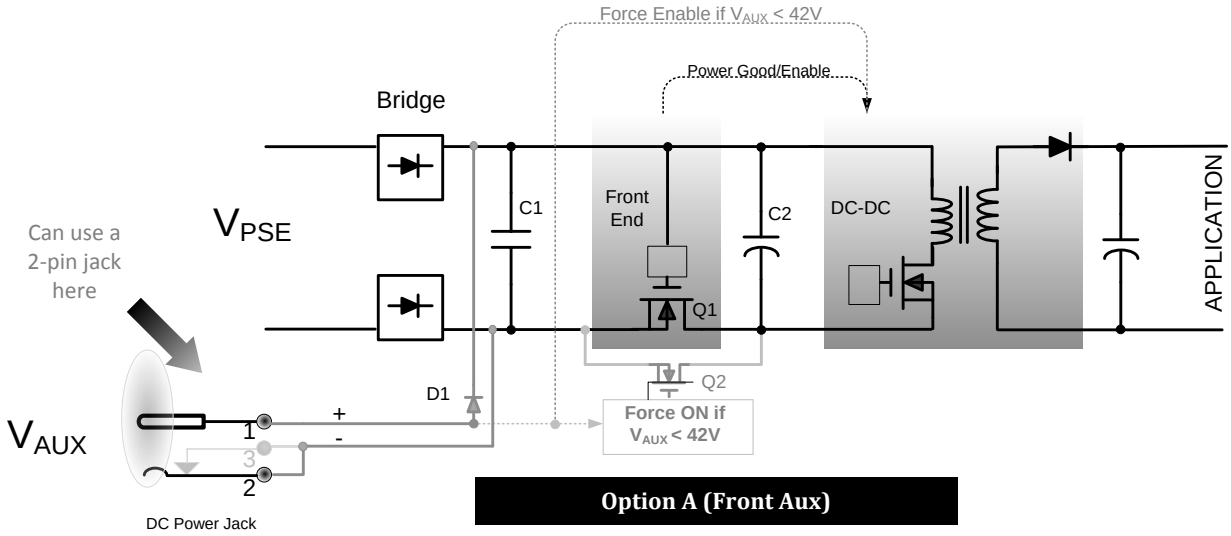

Figure 2: Front Aux Method in more detail

If PoE power is present (i.e. voltage V_{PSE} at PD is between 37Vand 57V), V_{AUX} needs to be greater than V_{PSE} for the OR-ing diode D1 in Figure 2 to conduct. Therefore "wall-adapter priority", something that is usually preferred in applications, is not assured. V_{AUX} will take over only if it is the larger of the two. When that happens, it will cause D1 to conduct. If V_{AUX} isn't larger than V_{PSE}, the application will continue to be powered from the PoE rail.

However, if V_{PSE} is not present initially, or it momentarily drops out for whatever reason, V_{AUX} will then be able to cause D1 to conduct. Since with this configuration V_{PSE} is injected at the input of the Front End, for the application to actually receive power from the AUX rail, the pass-FET (Q1) must conduct. The PD ICs turn ON the pass-FET somewhere between 36V to 42V, since the IEEE standard requires that any PD must activate on a rising voltage waveform before the voltage reaches 42V. In other words, if the AUX rail is higher than 42V, the pass-FET will turn on and the application will then receive power from the AUX rail.

If V_{AUX} is already providing power and PSE tries to turn ON, it will not detect the 25k signature resistor anymore, since V_{AUX} would have charged up the port capacitance in parallel to the 25k. So, FAUX method without additional provisions is a case of "first come, first served". If the PSE is providing power, the AUX rail can take over only if it is greater than PSE rail, otherwise the PSE will continue to provide power indefinitely. If the AUX rail is providing power, the PSE rail can never come. In this case only if the AUX rail drops out, will the PSE rail be able to take over.

Note: If the AUX rail is close to V_{PSE}, it is possible that when D1 conducts, the bridge rectifier may not get *fully* reverse-biased. So the PSE may not turn OFF right away. Depending on the cable resistance, both the wall-adapter and the PSE may continue to deliver power --- in some ratio. On closer examination we will realize that D1 *starts* to conduct when V_{AUX} exceeds the port voltage on the *PD-side*, but for the PSE to stop delivering power completely (bridge rectifier reverse-biased), V_{AUX} must eventually equal or exceed the port voltage at the *PSE-end*. In fact, as per the IEEE standard, the PSE will stop delivering power only when the current it is pushing through, drops below 5mA. And once that happens, it will be unable to come up again unless of course, the adapter is powered down or unplugged.

Summarizing the cases so far (and ignoring diodes forward drops for simplicity):

a) **Larger V_{AUX}:** $42V<V_{PSE}<V_{AUX}$ (example: $V_{AUX}=54V$, $V_{PSE}=50V$). **Wall-adapter priority** (Aux dominance).

   PD application will not get reset if adapter is plugged in. But the PD application will get reset if adapter is unplugged because PSE will be OFF.

b) Smaller V_{AUX} (but in PoE range): $42V<V_{AUX}<V_{PSE}$ (example: $V_{AUX} = 48V$, $V_{PSE}=54V$). **First come, first served.**

   PD application will not get reset if PSE is turned OFF (provided adapter is already plugged in). But the PD application will get reset if the adapter is unplugged.

Controlling Inrush Currents:

One problem to be aware of is that of inrush currents during "hot-swap" (change-over from PSE to AUX and vice versa). In general, we have two voltage sources of unequal voltages. If one suddenly takes over (under any conductive condition), it may find a large bulk capacitor ("C2", at the input of DC-DC stage) charging up almost immediately since pass-FET is ON. The inrush current into C2 can be high. Luckily, OR-ing diodes rarely get damaged when this happens because diodes typically have very high non-repetitive surge current ratings. However, any FET in the path of this inrush, such as pass-FET can get damaged.

The IEEE PoE standard does *not* demand that pass-FET Q1 have any active current limiting if C1+ C2 + C_{PSE} is less than 180µF. But for ensuring a smooth power-up with Front Aux connection, it is actually necessary to have not only an inrush current limit but an additional operational current limit in the PD if you may need to plug an adapter with voltage greater than V_{PSE} while Q1 is fully conducting. For example, Microsemi PD70210 and PD70211 have the operational current limit of about 2.2A. Under normal PoE operation, this default current limit is high enough to remain "transparent", but under hot-swap conditions, it will enter into the picture to limit inrush and to protect FET. Note that some commercial PD chips rely on thermal shutdown under fault conditions, which is undesirable.

We therefore conclude that to support the Front Aux option, the pass-FET of the Front End must always have a well-defined current limit.

V_{AUX} outside PoE Range.

So far we have discussed the case of V_{AUX} within the normal PoE voltage range. If V_{AUX} is less than 42V as mentioned, the PD Front End may not turn ON (i.e. Q1 will not conduct). In theory, this can be overcome by introducing a small boost converter in the adapter line. This will wake up the Front-End, which will then make Q1conduct.

Another option to support low AUX voltages is to bypass the internal pass-FET "Q1" by an additional external FET ("Q2")- see Figure 2. We will then need to force-enable the DC-DC stage (i.e. defeat its IEEE-compliant UVLO). At this, we should take great care to never turn ON the external bypass FET "Q2" while still operating (partially or fully) under PoE power --- because that would defeat the current limiting function present inside Q1. We should wait until only D1 is conducting (zero current through the Bridge rectifier), before we turn Q2 ON.

Also, to control inrush currents, since Q2 typically has no current limiting, to protect it better from the high inrush currents, it is advisable to insert a small current limiting resistor in series with the OR-ing diode D1, or an NTC (negative temperature coefficient) device in series with the OR-ing diode.

Brute-Force Wall-Adapter Priority.

There is another method to ensure "wall-adapter priority" (Aux dominance) under any condition: by simply disconnecting the PSE power whenever the wall adapter is plugged in. In theory, this could be accomplished by using a three-terminal adapter socket. It is also known as a "2-conductor, interrupting DC power jack".

For this method, the jack current rating should be at least 5A, to avoid the contacts from wearing out prematurely and the voltage rating should be well above 60V.

Unfortunately, known commercially available multi-terminal jacks are rated only for up to 48V and are not intended for interrupting power flow. Their manufacturers state that power must be turned off before inserting or removing the mating plug. In addition, with such a configuration, the PSE rail cannot come up until the adapter is not only powered down, but actually *unplugged* from the PD (the male DC plug removed from the jack). Finally, the PD application will very likely get reset whenever the adapter is plugged into the PD, or when it is unplugged. Because of the above problems the method with ground switching jack is not practical.

A relay can be used instead of a multi-terminal socket as shown in Figure 3. With the relay we can use a two terminal jack, and the male plug does not have to be manually plugged in or unplugged. Only when there is voltage present on the AUX rail, will the relay activate, and create adapter priority. But once again, if V_{AUX} is outside the normal PoE operating range, we will need to force Q1 to conduct (or bypass it with Q2) and force-enable the DC-DC converter. But despite that, if we cannot allow more current through Q1 or Q2, the total power will be significantly limited if the AUX rail voltage is too low.

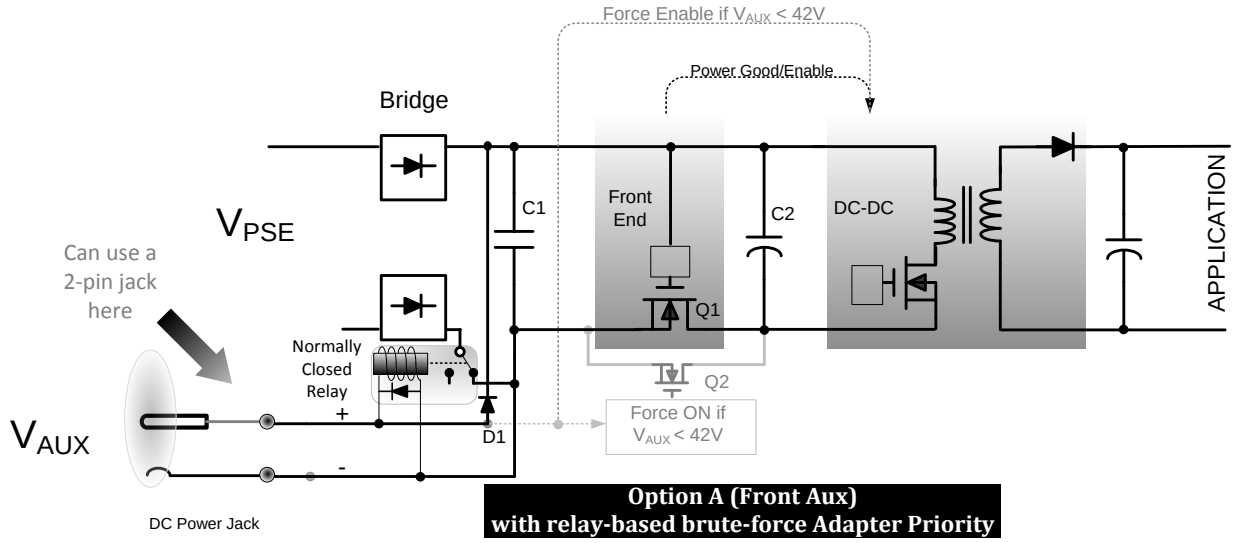

Figure 3: Front Aux Method in more detail (with relay-based brute-force adapter priority)

Despite all the described solutions, usually the Front Aux method is *not* preferred mainly because an implementation of Aux power source priority complicates the circuit and because pass-FET of the Front End ("Q1") has to be ON to deliver power. Instead, a better choice is Rear Aux method which is described below.

Auxiliary Power Option B (Rear Aux or "RAUX" method)

Application of Rear Aux is shown in Figure 6. This method has the following advantage from a heuristic viewpoint: it introduces the ability to cause the PSE to disconnect power if desired, by just turning OFF the pass-FET ("Q1") of the Front End. If the PSE current then falls below 5 mA, the PSE will typically disconnect, though it will likely keep attempting detection.

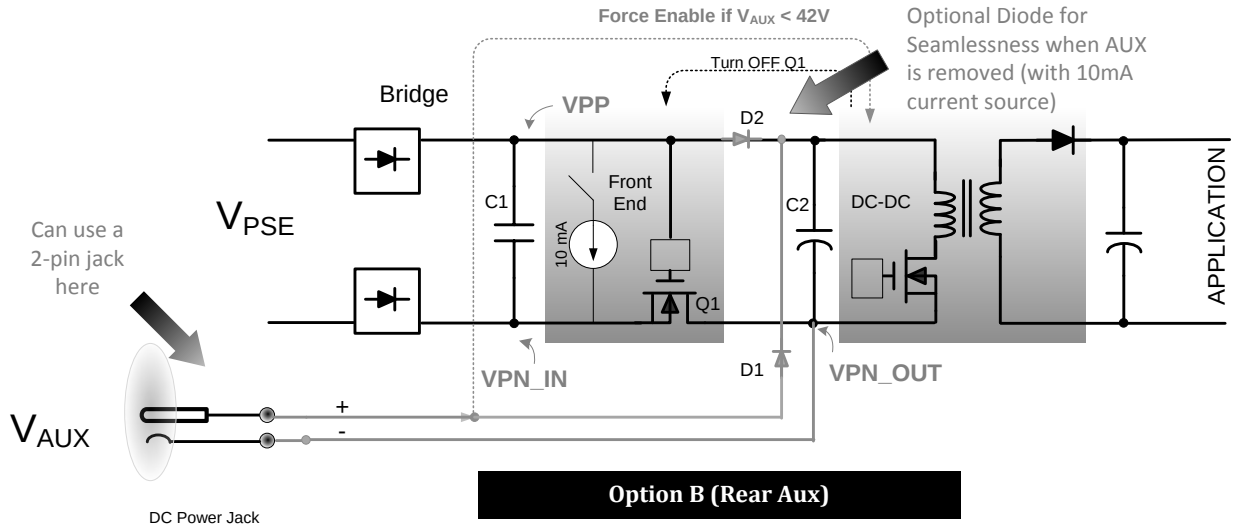

Figure 4: Rear Aux Method in more detail

Rear Aux method has another major **advantage**: when the Aux rail is delivering power, its current does not pass through the PD's pass-FET (Q1) and is not limited by the front end current limit. Therefore, as long as the DC-DC stage can function down to lower voltages, full power to the application can be provided even for lower AUX rails.

As in the Front Aux method, we have two cases when the AUX rail is within the normal PoE range (ignoring diode forward drops for simplicity, and assuming optional diode D2 is not present so far):

a) **Larger V_{AUX}:** $V_{PSE}<V_{AUX}$ (example: V_{AUX}=54V, V_{PSE}=50V). **Wall-adapter priority** (Aux dominance).

PD application will not get reset if adapter is plugged in. But the PD application will get reset if adapter is unplugged.

b) Smaller V_{AUX} (but in PoE range): $42V<V_{AUX}<V_{PSE}$ (example: V_{AUX} = 48V, V_{PSE}=54V). **First come, first served.**

In this case, we do not need the pass-FET of the Front End ("Q1") to be ON to deliver power.

With Rear Aux method we have an ability to forcibly turn OFF the pass-FET of the Front End when adapter power is available, so it is no longer "first come, first served". This option requires a special pin in the Front End controller. For example, Microsemi controllers PD70210A and PD70211 have WA_EN pin which turns OFF internal pass FET when logic High voltage is applied to it. By using this pin we can enforce adapter priority regardless of the relation between PoE and adapter voltages. By sensing the voltage on the remote side of the OR-ing diode D1 as per the dashed line marked "RAUX" in Figure 1, we can detect the presence of the AUX rail. So, even if V_{AUX} is less than V_{PSE}, by using WA_EN pin we can force the Aux rail to dominate for any condition, and at all times, by simply turning off the pass-FET of the Front End (disconnecting the PSE from the application).

When we turn OFF the pass-FET Q1, there are actually two possibilities going forward -- the two "sub-options" within this Rear Aux option as mentioned earlier:

a) **Diode "D2" not present**: The PSE will get disconnected and stay disconnected. Because the AUX voltage will flow back into the port capacitance, in parallel to the 25k signature resistor, and that will prevent the PSE from ever detecting a valid PD and turning ON the PoE rail (keeping it in standby, waiting for AUX rail to be removed).This conserves system power, optimizes power delivery, and allows port power to be allocated by the host elsewhere where required (other ports). But that "green" feature can also be a disadvantage on resumption of PoE power. Because PoE power may not be available immediately if it was meanwhile committed elsewhere. So though asserting adapter priority will be seamless, causing no controller's PD-side reset, when the adapter is either powered down or unplugged, there will be a PD-side reset on resumption of PoE power.

b) Diode "D2" present: With this addition, we can choose an option to "keep alive" the PoE rail as a sort-of "UPS standby" in case the wall adapters is not delivering power. The diode D2 will prevent the negation of the 25k signature by the AUX rail, so the PSE will be able to power up (again). But Q1 is still kept OFF so the PSE rail does not force its way through D2 based on higher voltage. In other words, Q1 is kept OFF. But the PSE is not allowed to disconnect after detecting 25k signature, by keeping the rail alive by drawing a small current to the left of Q1. We therefore need to design the Front End such that when the wall adapter is sensed via the RAUX pin, we force the Front End to draw >10mA from the PSE, preventing MPS disconnect (see Figure 4). This way we can have the advantage that if the Aux rail is removed, the PoE rail can be smoothly (seamlessly) take over power delivery (perhaps with the help of some architectural soft-transitioning features). This will ensure no interruption in power and consequent PD reset.

Summarizing the Rear Aux option:

1) Potentially seamless transitioning from PoE power to Aux power and back is possible with Rear Aux, provided the Front End is designed to support this feature with a dedicated WA_EN pin on the Front End. In addition, we need to provide the diode D2 shown in Figure 4. Otherwise, the AUX voltage will flow back into the port capacitance, in parallel to the 25k signature resistor, and that will prevent the PSE from ever detecting a valid PD.

2) Although wall adapter priority is naturally possible if V_{AUX}>V_{PSE}, with Rear Aux method we can easily ensure unconditional adapter priority with a dedicated WA_EN pin that turns OFF the pass-FET of the Front End. As with Front Aux, in theory we can also assure "brute-force" adapter priority by using a a relay as shown in Figure 5. Unfortunately, all the limitations of the mechanical switch and relay that we discussed in the Front Aux option, are applicable here too. For one, we are likely going to lose seamlessness under hot-swap conditions.

3) Inrush current protection for adapter line is not inherently available with Rear Aux method since adapter is connected after a PD chip. The adapter must protect itself from inrush currents. In addition to this, hot plugging adapter can cause contact arcing in the DC jack. The circuit is Fig.5 provides "slow start" for adapter line that limits its surge current and protects contacts from arcing.

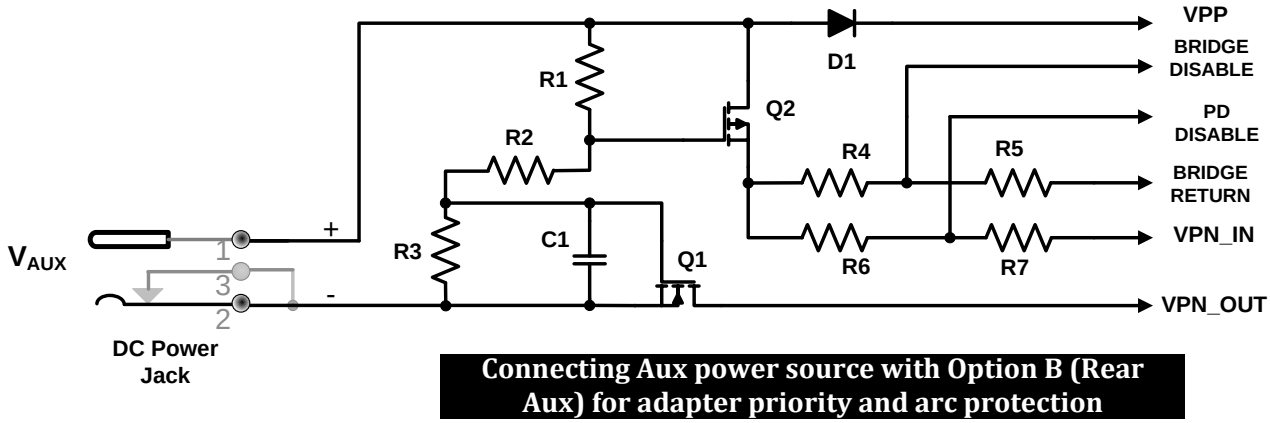

Figure 5: Connecting Auxiliary power source with arc protection and adapter priority

Auxiliary FET Q1 limits initial current from the adapter due to slow raise of its gate voltage. After the initial WA connection, Q1 will be fully "ON" and ensure low losses due to

its low Rds_on. An additional signal FET Q2 will disable active bridge (if used) and PD controller via dividers R4,R5 and R6,R7.
Typical values are: R1=2k, R2=11k, R3=4k, C1=10uF/25V, R4,R6=150k, R5,R7=14.3k, Q1-FDS86242, Q2-ZVP3310FTA.

Auxiliary Power Option C (Direct OR-ed)

The final option is connecting Auxiliary power directly to the output of the PD power supply (see Figure 1). The main advantage of Direct OR-ed method is possibility of seamless transition from adapter power to PoE: since DC-DC converter is continuing operating (at no load) even in the presence of DC adapter, its power consumption is usually sufficient to prevent PSE from turning off. However, this method has a number of disadvantages. In all previous options, the Aux rail could be unregulated and the PWM/DC-DC stage would carry out the required regulation. The Direct OR-ed method requires an Aux power supply designed to deliver fully regulated voltage required by the PD load. In addition, if the DC-DC converter uses synchronous rectifiers, this configuration will also need an additional OR-ing diode or a FET emulating diode in series with DC-DC output. This adds cost and leads to additional constant power loss under regular PoE operation.

CONCLUSION

The preferred method of connecting Auxiliary DC power is Rear Aux method (Option B) used with PD controller that allows turning off internal pass-FET by a logic “adapter present” signal, such as Microsemi PD70210A and PD70211.

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