



N-CHANNEL MOSFET

Qualified per MIL-PRF-19500/555

Qualified Levels:
JAN, JANTX, and
JANTXV

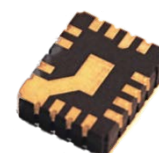
DESCRIPTION

This 2N6790U device is military qualified up to a JANTXV level for high-reliability applications. Microsemi also offers numerous other products to meet higher and lower power voltage regulation applications.

Important: For the latest information, visit our website <http://www.microsemi.com>.

FEATURES

- JEDEC registered 2N6790U.
- JAN, JANTX, and JANTXV qualification per MIL-PRF-19500/555 available.
- RoHS compliant versions available (commercial grade only).



**U-18 LCC
Package**

Also available in:

TO-205AF Package
(leadless)
 [2N6790U](#)

APPLICATIONS / BENEFITS

- High frequency operation.
- Lightweight package.
- ESD to class 1A.

MAXIMUM RATINGS @ $T_C = +25^\circ\text{C}$ unless otherwise noted

Parameters / Test Conditions	Symbol	Value	Unit
Junction & Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	8.93	$^\circ\text{C/W}$
Drain to Gate Voltage	V_{DG}	200	V
Drain – Source Voltage	V_{DS}	200	V
Gate – Source Voltage	V_{GS}	± 20	V
Continuous Drain Current @ $T_C = +25^\circ\text{C}$	I_{D1}	2.8	A
Continuous Drain Current @ $T_C = +100^\circ\text{C}$	I_{D2}	1.8	A
Off-State Power Dissipation ⁽¹⁾	P_{D1}	14	W
Source Current – Drain Diode (Forward Biased V_{SD})	I_S	2.8	A
Off-State Current	I_{DM}	11	A (pk)
Drain to Source On State Resistance ⁽²⁾	$r_{DS(on)}$	0.80	Ω

Notes: 1. Derated linearly by 0.11 W/ $^\circ\text{C}$ for $T_C > +25^\circ\text{C}$.
2. $V_{GS} = 10\text{ V}$, $I_D = 1.8\text{ A}$

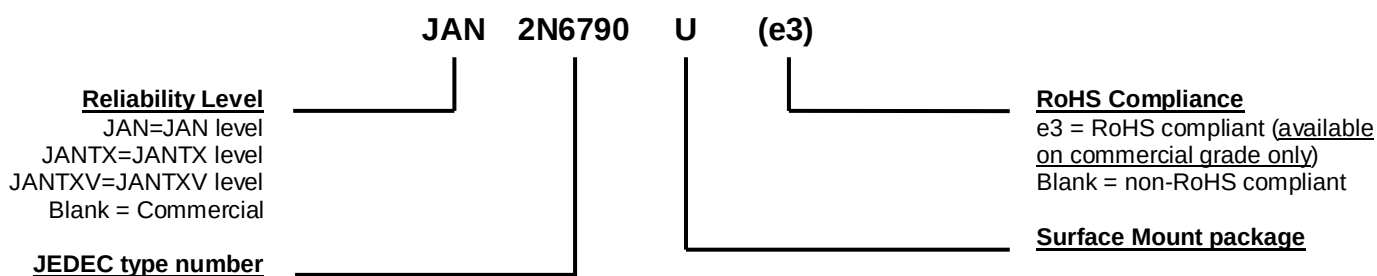
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MECHANICAL and PACKAGING

- CASE: Ceramic LCC-18 with kovar gold plated lid.
- TERMINALS: Gold plating over nickel.
- MARKING: Manufacturer's ID, part number, date code, ESD symbol at Pin 1 location.
- POLARITY: See pad layout.
- TAPE & REEL option: Standard per EIA-481-D. Consult factory for quantities.
- See [Package Dimensions](#) on last page.

PART NOMENCLATURE**SYMBOLS & DEFINITIONS**

Symbol	Definition
I_D	Drain current.
I_F	Forward current.
T_C	Case temperature.
V_{DD}	Drain supply voltage.
V_{DS}	Drain to source voltage.
V_{GS}	Gate to source voltage.

ELECTRICAL CHARACTERISTICS @ $T_A = +25^\circ\text{C}$, unless otherwise noted

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage $V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	$V_{(BR)DSS}$	200		V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}$ $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}, T_j = +125^\circ\text{C}$ $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}, T_j = -55^\circ\text{C}$	$V_{GS(th)1}$ $V_{GS(th)2}$ $V_{GS(th)3}$	2.0 1.0	4.0 5.0	V
Gate Current $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}, T_j = +125^\circ\text{C}$	I_{GSS1} I_{GSS2}		± 100 ± 200	nA

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
ON CHARACTERISTICS				
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = 160\text{ V}$ $V_{GS} = 0\text{ V}, V_{DS} = 160\text{ V}, T_j = +125^\circ\text{C}$	I_{DSS1} I_{DSS2}		25 0.25	μA mA
Static Drain-Source On-State Resistance $V_{GS} = 10\text{ V}, I_D = 1.8\text{ A}$ pulsed $V_{GS} = 10\text{ V}, I_D = 2.8\text{ A}$ pulsed $T_j = +125^\circ\text{C}$ $V_{GS} = 10\text{ V}, I_D = 1.8\text{ A}$ pulsed	$r_{DS(on)1}$ $r_{DS(on)2}$ $r_{DS(on)3}$		0.80 0.85 1.50	Ω Ω Ω
Diode Forward Voltage $V_{GS} = 0\text{ V}, I_D = 2.8\text{ A}$ pulsed	V_{SD}		1.5	V

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Gate Charge: On-State Gate Charge Gate to Source Charge Gate to Drain Charge	$Q_{g(on)}$ Q_{gs} Q_{gd}		14.3 3.0 9.0	nC

SWITCHING CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Switching time tests: Turn-on delay time $I_D = 2.8\text{ A}, V_{GS} = 10\text{ V}$ Rinse time Gate drive impedance = $7.5\ \Omega$, Turn-off delay time $V_{DD} = 74\text{ V}$ Fall time	$t_{d(on)}$ t_r $t_{d(off)}$ t_f		40 50 50 50	ns
Diode Reverse Recovery Time $di/dt = 100\text{ A}/\mu\text{s}, V_{DD} \leq 50\text{ V}$, $I_D = I_{D1} = 2.8\text{ A}$	t_{rr}		400	ns

GRAPHS

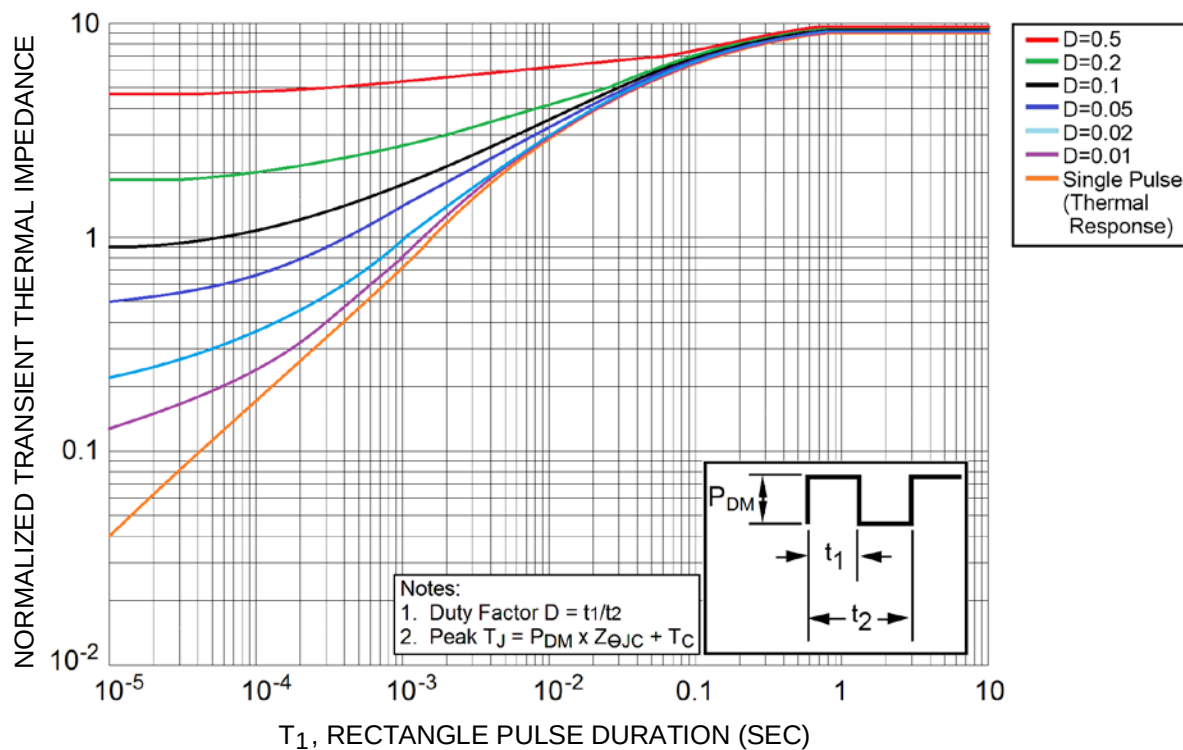


Figure 1
Thermal Impedance Curves

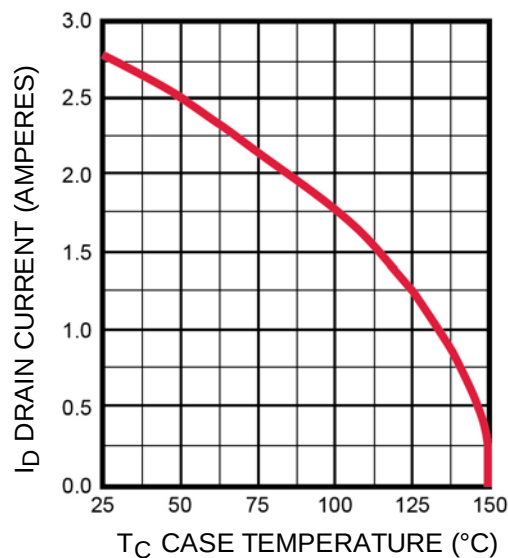


Figure 2
Maximum Drain Current vs. Case Temperature Graph

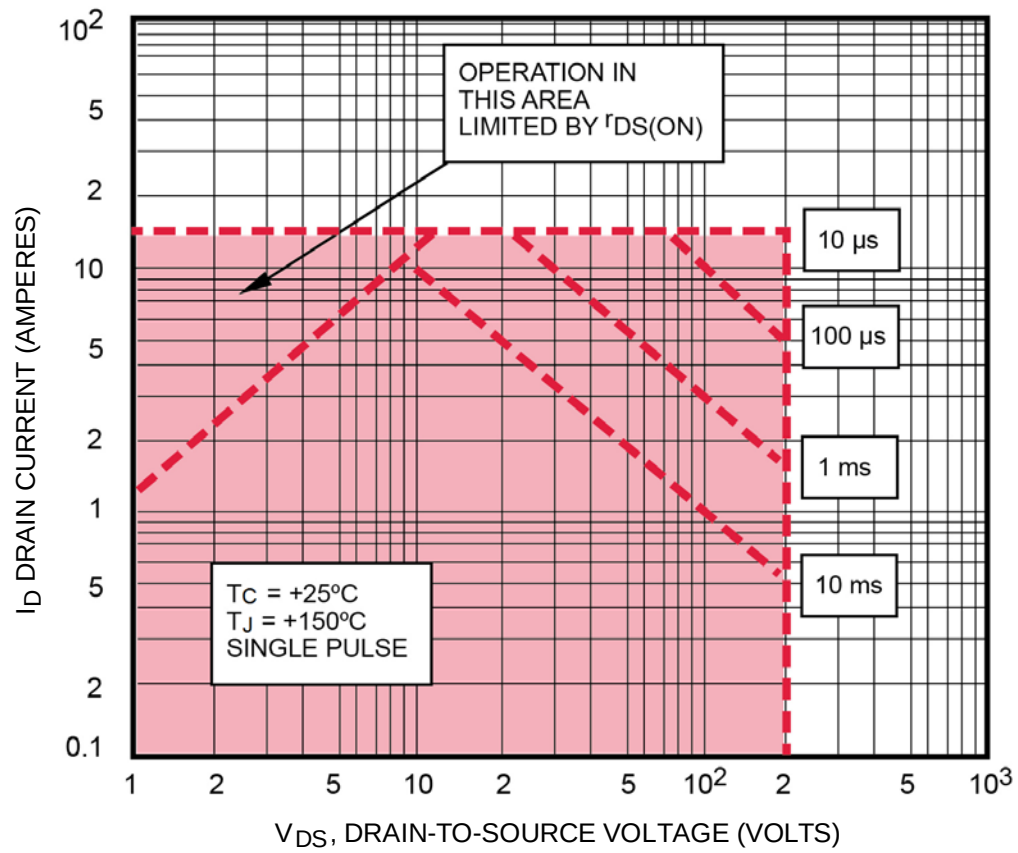
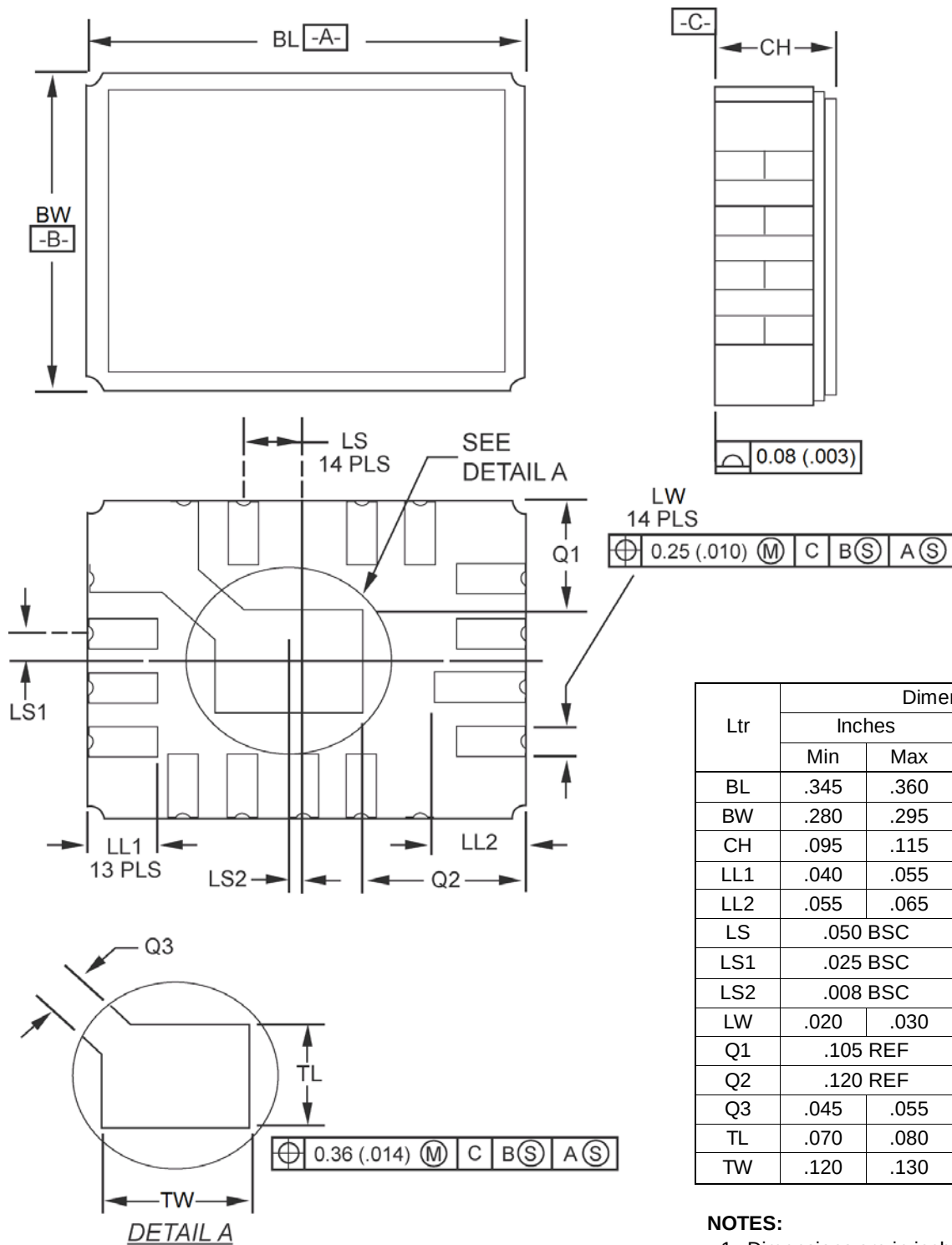
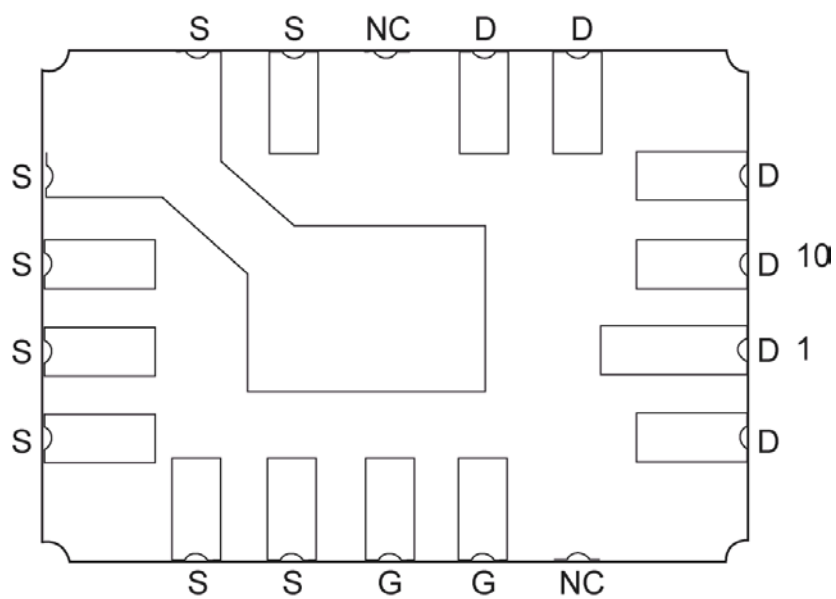
GRAPHS (continued)


Figure 3
Maximum Safe Operating Area

PACKAGE DIMENSIONS

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to Φ x symbology.

PAD LAYOUT

PAD ASSIGNMENTS