INPLUG® Series:IPS315/315H/318

PWM Controller
Integrated Solution

DESCRIPTION

The IN-PLUG® IPS31x PWM controller series is derived from AAI's IPS1x off-line switcher series. It is intended for automotive applications that require DC to DC solutions up to approximately 70W. Controllers operate from as low as 8V DC battery voltage and are tailored for 12V, 24V, 36V and 48V DC applications. This series is optimized for very simple, low component count, low cost buck, boost and SEPIC topologies. They offer isolated and non-isolated solutions with a feedback selection for direct or though optocoupler/ bias winding loop control.

They are designed to satisfy the requirements of high ambient temperature environments and housed in a DIP or SOIC8 package for commercial and automotive temperature ranges respectively 0°C to +70°C and -40°C to +125°C.

The IN-PLUG® IPS31x controllers contain a shunt-regulator, a precision oscillator, a PWM block with its associated comparator and loop compensation components as well as all the necessary biasing and protection circuitry (undervoltage and overcurrent). The controllers only differ by optional features such as built-in overload protection (IPS315H) and/or very low stanby power in "no load" condition (IPS318).

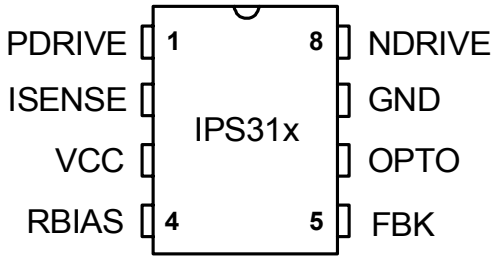
FEATURES

- Operates from 7.5V DC battery voltage
- Tailored for 12V, 24V, 36V and 48V battery operation
- Up to 100% duty cycle operation for low input voltages
- Adjustable frequency up to 400KHz
- Direct feedback, feedback through optocoupler or through bias winding.
- Simple and low component count buck, boost and SEPIC topologies.
- Power shut-down for stand-by modes
- Designed to operate in the harsh environment
- Rated for operation from -40°C to 125°C

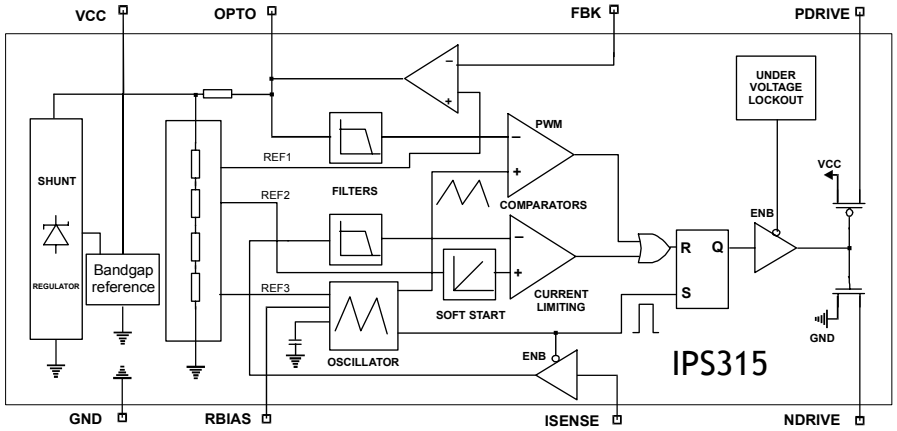
APPLICATIONS

- DC-DC converters
- Car Turn Signals
- Car Taillights
- Car Headlights
- Lamp and LED Control

PIN CONFIGURATION: DIP-8 / SOIC-8



FUNCTIONAL BLOCK DIAGRAM

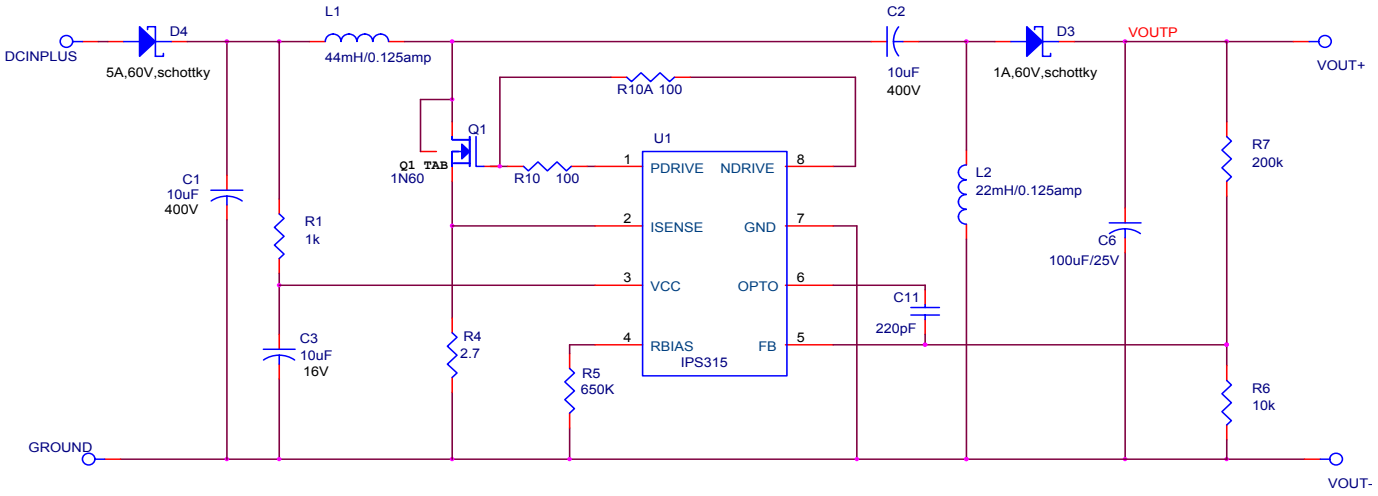


PIN DESCRIPTION

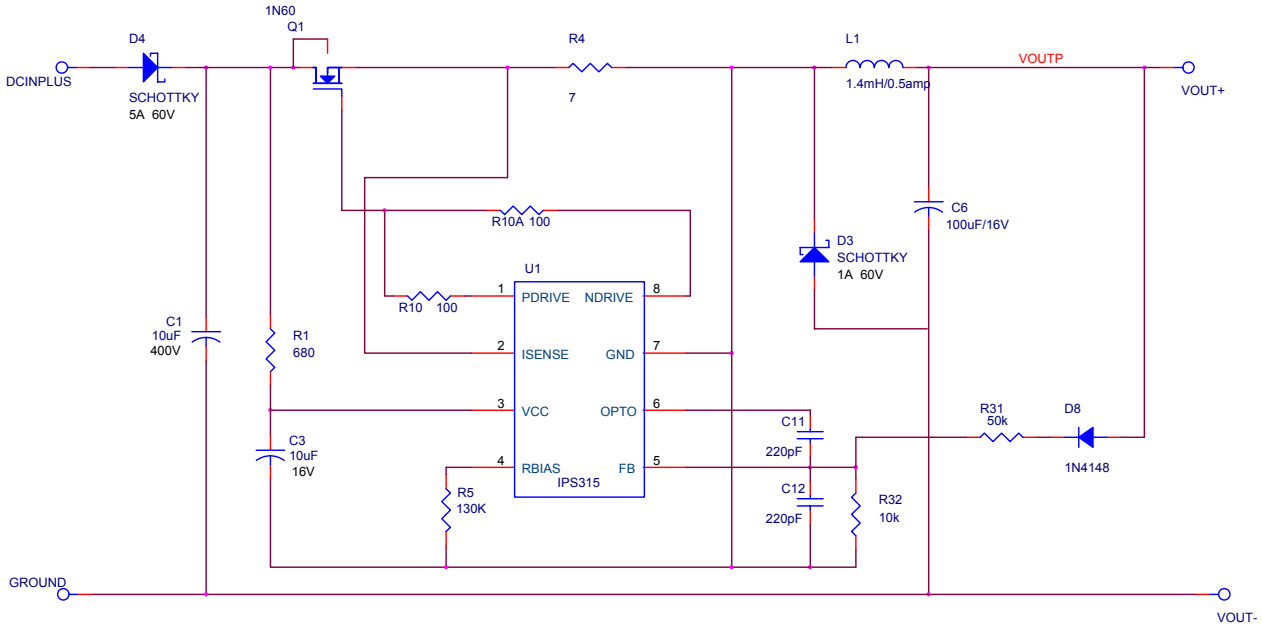
Number	Name	Description
1	PDRIVE	Internal P drive terminal to be connected to the gate of the outside power MOSFET. (The rising edge can be adjusted with an external resistor)
2	I_{SENSE}	MOSFET current sensing. Any voltage over 700 mv @ 25°C on this pin will stop gate pulses.
3	V_{CC}	IC positive supply. The chip behaves like a 7.2 volts zener diode.
4	R_{BIAS}	External R_{BIAS} connection to set the operating frequency.
5	FBK	An input connecting to an internal error amplifier. The amplifier has a 0.925Volt reference connected to it's other input.
6	OPTO	Feedback input for optoisolator to ground, and a connection point for a compensation capacitor/network to the FBK pin
7	GND	Ground
8	NDRIVE	Internal N drive terminal to be connected to the gate of the outside power MOSFET. (The falling edge can be adjusted with an external resistor)

APPLICATION SCHEMATICS

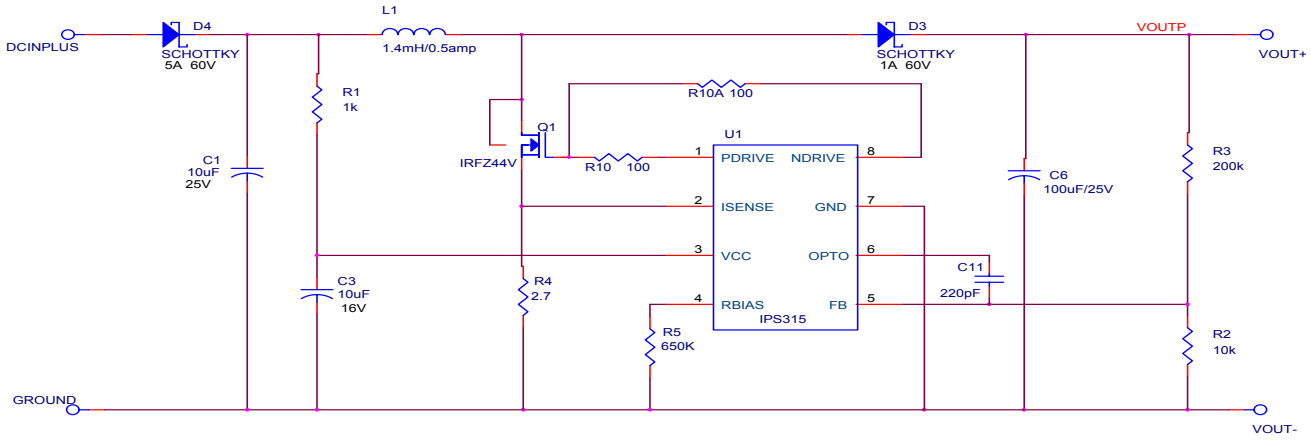
SEPIC Topology: 1 Watt Application, VIN=8VDC to 48V, Output= 21VDC/30mA



BUCK Topology: 1 Watt Application, VIN= 8VDC to 48VDC, Output= 6VDC/100mA

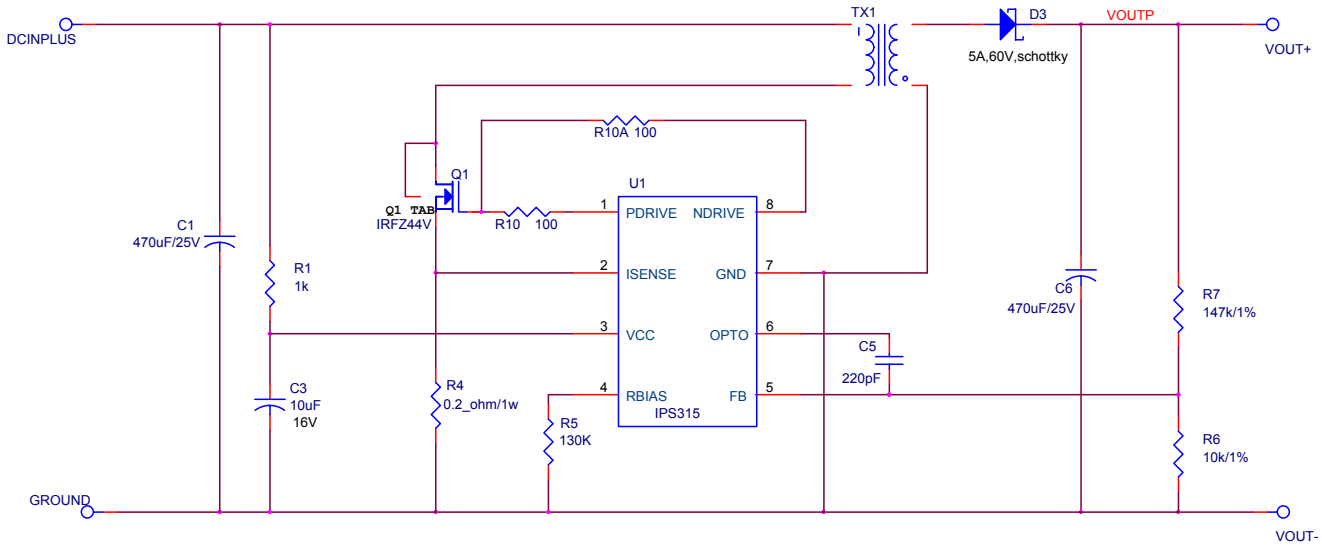


BOOST TOPOLOGY: 1 Watt Application, VIN=8VDC to 48V, Output= 21VDC/30mA



FLYBACK TOPOLOGY: 5 Watt Application, VIN=7.5 VDC to 48 VDC, Output=14VDC/350mA

(100 kHz, 1-to-1 turns ratio)



The buck and boost topologies provide a good solution when the application requires that the input-to-output voltage change is either always an increase (boost) or decrease (buck). For applications that need the output to be both above and below the output, either a SEPIC or one-to-one turns-ratio flyback can be used. There are many similarities between the two topologies (one switch, two windings on one core). The SEPIC has an input-to-output capacitor, which adds an additional component in the power path. The tradeoff is that the flyback switch needs to tolerate an inductive voltage 'kick' from the transformer leakage inductance at turn-off. The SEPIC capacitor takes this energy and transfers it to the output. The flyback has higher rms current in its input and output capacitors compared to the SEPIC, but the flyback input capacitor typically has the same current requirement as the SEPIC transfer capacitor. The flyback windings will have half the inductance of the SEPIC windings, but the size of the required core is nearly the same for the two topologies if core and winding losses are kept identical.

IN-PLUG® IPS31x SERIES FUNCTIONAL DESCRIPTION

The **IPS31x family** are PWM controllers for Switching Power Supplies, tailored for automotive applications. The principal features are:

- Low start Current.
- Shunt regulator to allow the maximum flexibility to power the chip.
- Protection against under-voltage.
- Precise oscillator with externally adjustable frequency up to 400KHz.
- Duty cycle up to 98%
- Direct feeback or feedback through optocoupler.
- On-chip filters for the loop compensation and the over-current sensing.
- Soft start to protect the MOSFET.
- Separate MOSFET P and N drivers to adjust rising and falling edge independently.

The shunt regulator operates like a zener diode, keeping the chip supply voltage around 7.2 volts. At start-up the chip stays in stand-by mode until the voltage of VCC reaches about 7.2 volts. During this phase, the consumption is of the order of 120 μA. When the 7.2 volts are reached, the driver starts providing gate pulses. The chip will go back to the stand-by mode if the supply voltage decreases down to ~6 volts. The overall chip consumption in normal operation is about 600 μA, not counting the current required to drive the MOSFET gate.

Direct Feedback:

At start-up, the zero volt application output voltage is presented to the inverting pin of the error amplifier called FBK. The output of the error amplifier goes high and allows to drive the swiching MOSFET with a maximum power (98% duty cycle), but the duty cycle is controlled by the internal soft start unit which smoothly increases the MOSFET current up to its maximum. When the FBK pin voltage reaches the 0.925V threshold voltage of the internal reference, the pulsewidth on the output starts decreasing.

Feedback through Optocoupler:

The opto pin is pulled to VCC through an internal resistor, allowing a maximal duty cycle of 98 %. During start-up, the duty cycle is controlled by the internal soft start unit which smoothly increases the MOSFET current up to its maximum, corresponding to 700mV developped across the sense resistor.

When the expected output voltage is reached, the optocoupler's led is driven, and the opto pin voltage decreases, reducing the duty cycle to a controlled value. The current limiting protection operates by turning-off the MOSFET when the ISENSE pin voltage exceeds ~700 mv. This ensures a cycle to cycle protection of the MOSFET.

Note: A compensation network between FBK and OPTO pins ensures loop stability

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING		
Characteristics	**Value**	**UNITS**
Shunt regulator max I_{CC} (pin 3) - see Fig 3-	40	mA
All analog inputs (pin 2, 4, 5, 6)	Min= -0.3, Max= +6.3V	V
Peak drive output current (pin1)	Source=100, Sink=170	mA
Junction to case thermal resistance $R_{\theta J-C}$	PDIL = 42, SOIC = 45	°C / W
Junction to PCB thermal resistance $R_{\theta J-A}$	PDIL = 125, SOIC =155	
Power dissipation for T_A <= 70°C	PDIL = 640, SOIC = 500	mW
Operating junction temperature	- 40 to 150	°C
Storage temperature range	- 55 to 150	
Lead temperature (3 mm from case for 5 sec.)	260	

PARAMETER	TEST CONDITIONS	PARAMETERS			UNITS
	@ 25°C unless specified	MIN.	TYP.	MAX.	
Supply, bias & circuit protection					
Shunt regulator voltage	ICC = 1 to 30 mA	6.7	7.2	7.7	V
Shunt regulator dynamic resistance (see Fig. 3)	1 to 30 mA	2	3	5	Ω
Shunt regulator max peak repetitive current		-	30	-	mA
Min I_{CC} to start oscillator		-	-	140	μA
Under voltage lock-out		V_{CC} – 1.4	V_{CC} - 1.1	V_{CC} – 0.8	V
Min I_{CC} to ensure continuous operation	1A, 80V, 5 nC MOSFET	1.1 @ 50KHz	3.2 @ 100KHz	4.9 @ 200KHz	mA
Current limiting sensing voltage		655	700	745	mV
Temperature coefficient of current limiting		-	-	50	μV/°C
Soft/start duration	0 to 700mV	-	20	-	clock cycles
Leading edge blanking		200	-	450	ns
Oscillator & PWM					
Range of operating frequencies		50	100	300	KHz
RBIAS values for above frequencies (see Fig. 1)		560	210	60	KΩ
Oscillator stability with supply & temperature (see Fig. 2 for average)	I_{CC} = 5 mA Temp = 0 to 70°C	-1.5	-	1.5	%
Maximum duty cycle		-	98%	-	%
Minimum duty cycle		-	0	-	%
*Hiccup Detect Time T_{Hdtc}	Freq = 70 kHz (note 2)			7	msec
*Hiccup Off Time T_{Hroff}	Proportional to $R_{start}C_{vcc}$				

ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER	TEST CONDITIONS	PARAMETERS			UNITS
	@ 25°C unless specified	MIN.	TYP.	MAX.	
Error amplifier					
FBK voltage reference		0.916	0.925	0.934	Volts
Sensitivity in mV / % of PWM		-	37	-	mV
Voltage for max duty cycle	OPTO pin	-	4	-	V
Voltage for min duty cycle	OPTO pin	-	0.2	-	V
Input Impedance	OPTO pin	-	50	-	KΩ
**Cycle Skip Threshold	OPTO pin		0.900		Volts
P & N Outputs to MOSFET gate					
P gate driver saturation	10 mA (source)	-	-	1	V
N gate driver saturation	10 mA (sink)	-	-	0.6	V
Gate pull-down resistor	(internal)	280	400	520	KΩ
PDRIVE Rise time (10% to 90%)	240 pF load	-	250	-	ns
NDRIVE Fall time (10% to 90%)	240 pF load	-	100	-	ns

Note 1: Electrical parameters, although guaranteed, are not all 100% tested in production.
Note 2: Proportional to 1/freq. Example: at 50KHz, detect time T_{Hdtc} = 7ms x 70KHz / 50KHz = 10ms
***IPS315H and IPS318 only, **IPS318 only**

FIGURE 1 – FREQUENCY SELECTION vs RBIAS

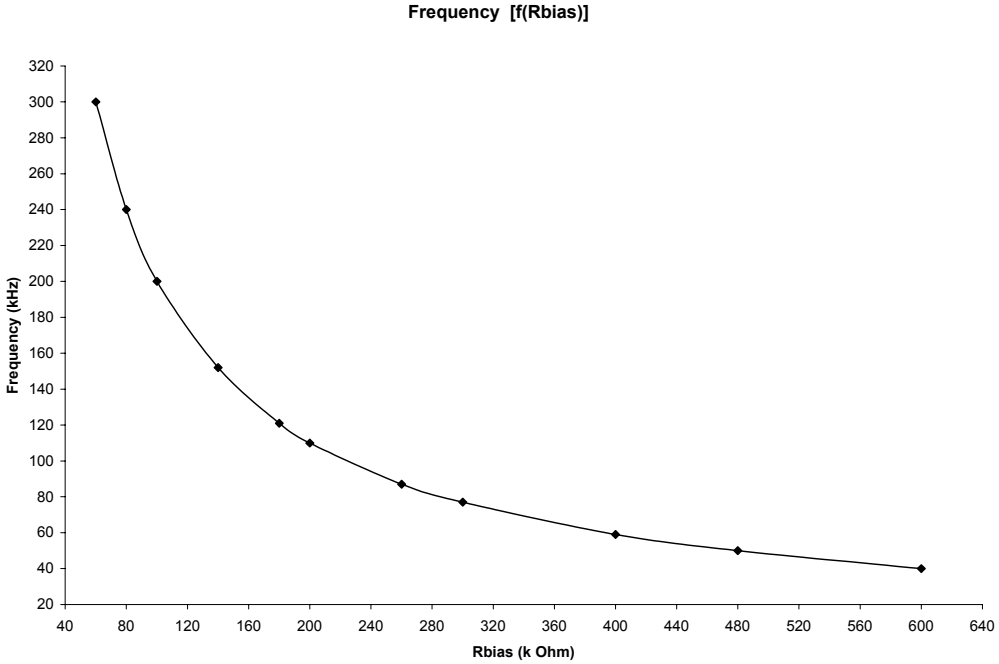


FIGURE 2 – OSCILLATOR FREQUENCY STABILITY WITH TEMPERATURE

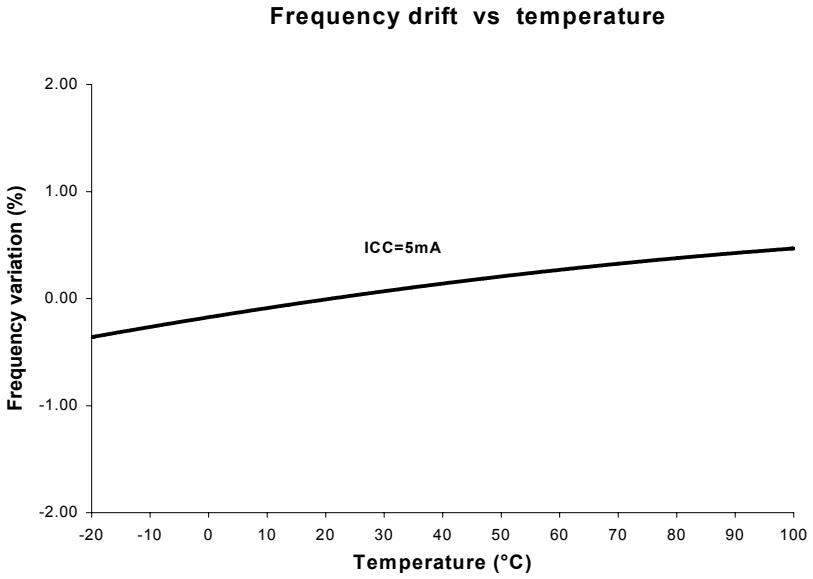


FIGURE 3 – SHUNT REGULATOR I_{CC} vs V_{CC}

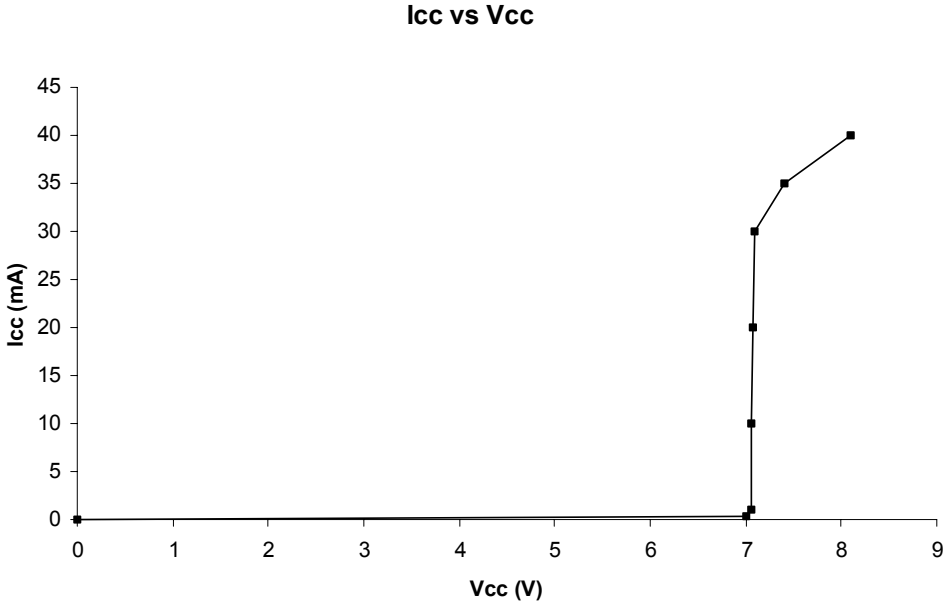
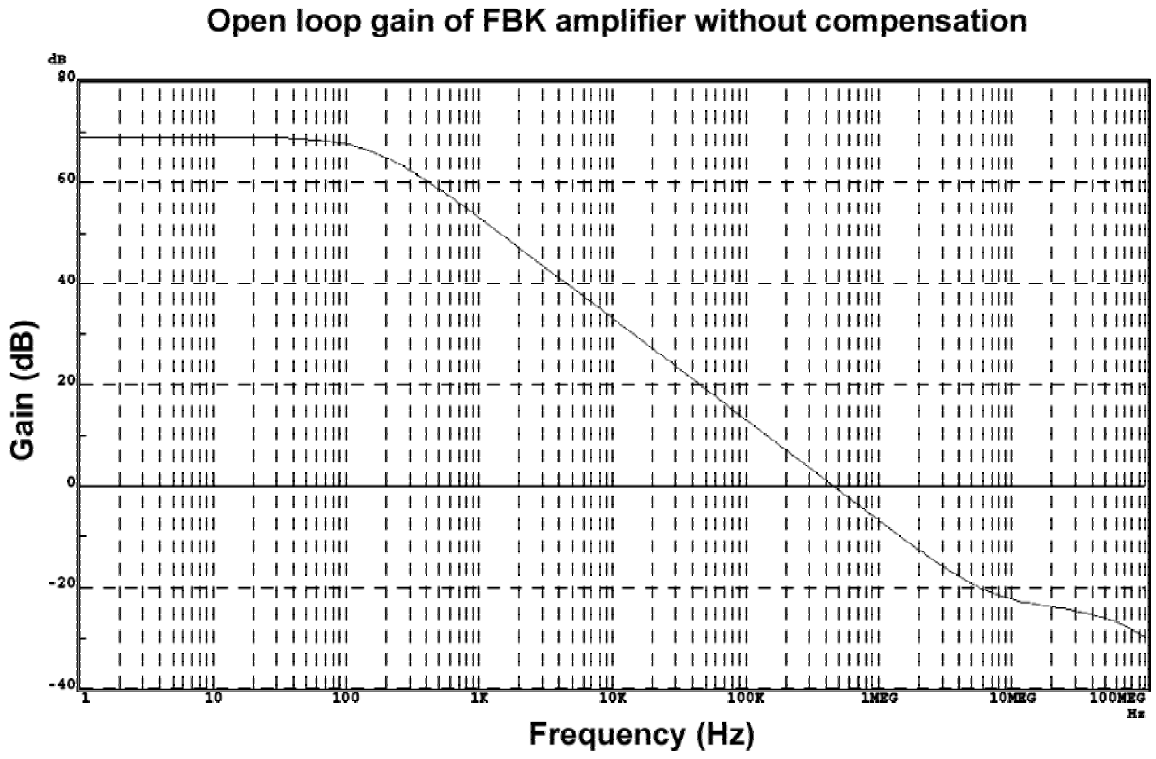


FIGURE 4 – FBK ERROR AMPLIFIER FREQUENCY RESPONSE



ORDERING INFORMATION

Part No. Tube	Part No. Tape & Reel	Package	Temperature Range	
IPS315C-D-G-LF		8-Pin PDIP	0°C to +70°C	Commercial
IPS315A-D-G-LF		8-Pin PDIP	-40°C to +125°C	Automotive
IPS315C-SO-G-LF	IPS315C-SO-G-LF-TR	8-Pin SOIC	0°C to +70°C	Commercial
IPS315A-SO-G-LF	IPS315A-SO-G-LF-TR	8-Pin SOIC	-40°C to +125°C	Automotive
IPS315HC-D-G-LF		8-Pin PDIP	0°C to +70°C	Commercial
IPS315HA-D-G-LF		8-Pin PDIP	-40°C to +125°C	Automotive
IPS315HC-SO-G-LF	IPS315HC-SO-G-LF-TR	8-Pin SOIC	0°C to +70°C	Commercial
IPS315HA-SO-G-LF	IPS315HA-SO-G-LF-TR	8-Pin SOIC	-40°C to +125°C	Automotive
IPS318C-D-G-LF		8-Pin PDIP	0°C to +70°C	Commercial
IPS318A-D-G-LF		8-Pin PDIP	-40°C to +125°C	Automotive
IPS318C-SO-G-LF	IPS318C-SO-G-LF-TR	8-Pin SOIC	0°C to +70°C	Commercial
IPS318A-SO-G-LF	IPS318A-SO-G-LF-TR	8-Pin SOIC	-40°C to +125°C	Automotive

For more information, refer to PACKAGE DIMENSIONS AND MARKING

IPS315H AND IPS318 – HICCUP MODE

The output power that triggers the hiccup mode is monitored by sensing the MOSFET current through the ISENSE resistor (R4 in the above schematics). The hiccup mode doesn't require any specific component on the load-side. This mode called "hiccup" is a special "overload protection" mode where the IPS315H/318 resets itself when an overload condition is detected and which duration exceeds the maximum authorized time T_{Hdtc} as described below. The description here assumes that we are talking about a flyback topology, where there is no overlap in time or electrical connection between the FET being 'on' and the output diode conducting. Various topologies have various operating characteristics that don't necessarily follow that rule, but understanding hiccup operation here will (hopefully) explain what how this feature is implemented.

Approximatly $\mathbf{T_{Hoff}}$ after power-up and when the IPS315H/318 is fully operational, the output power is sensed to check an overload condition present or not ("true" or "false") . If it is "true" and remains "true" all over $\mathbf{T_{Hdtc}}$ then the chip resets. Power supply re-establishes and after $\mathbf{T_{Hoff}}$ time, the chip restarts monotoring the output power through RSENSE and the "hiccup" mode could repeat itself as described.

If the overload condition is "false" or when it is true for less than $\mathbf{T_{Hdtc}}$, the chip simply operates like the IPS315 flyback controller.

Overload Condition:

An overload condition is defined by

$P_{Sout} > P_{Smax}$ → "true";

$P_{Sout} < P_{Smax}$ → "false";

P_{Sout} = SMPS output power (secondary);

P_{Smax} = maximum authorized output power delivered by the SMPS secondary.

Hiccup detect time T_{Hdtc} and off time T_{Hoff}:

$\mathbf{T_{Hoff}}$ = time from start-up to P_{SOUT} sensing;

T_{Hdtc} = maximum detect time of overload condition to trigger chip reset;

$(T_{Hoff} + T_{Hdtc})/ T_{Hoff.}$ = hiccup duty cycle.

Note: Conditions of adjacent figure were altered to better show the "hiccup" operation mode. Actual duty cycle will be much less as indicated in formula below.

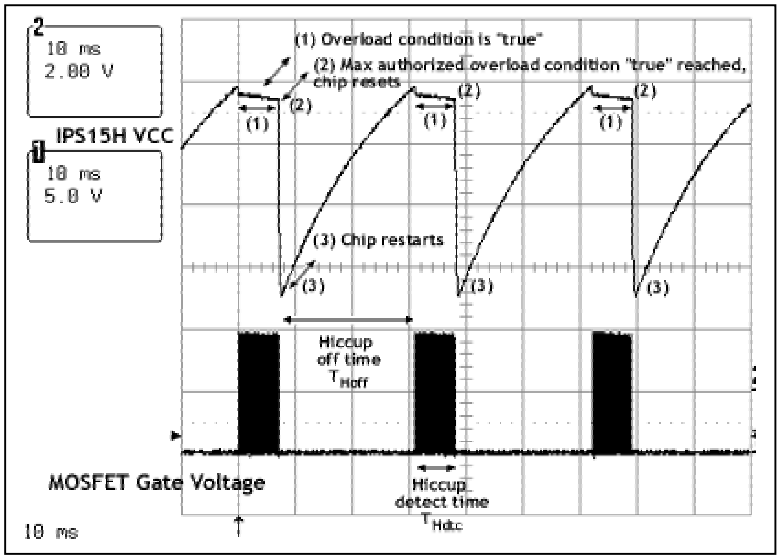


Figure 5: "Hiccup" mode in constant overload

Calculation of the output power "P_{Smax}" that triggers the hiccup mode:

As explained above, when $P_{Sout} > P_{Smax}$ for more than T_{Hdtc} time, hiccup mode starts. The previous formula could also be seen from the primary as $P_{Sout} = (P_{Pout}$ - losses$) > P_{Smax}$ where losses correspond to the overall losses (schottky, transformer, MOSFET, snubber etc..). As a first approximation the losses could be estimated to 25% and consequently 75% of primary power P_{Pmax} could be used.

$P_{Pout} > (P_{Smax}$ + losses$) = ½ L_p Ipeak^2 F$ → Ipeak = 0.7V/RSENSE (0.7V = max ISENSE pin voltage, Ipeak = peak MOSFET current).

$P_{Smax}/0.75 = ½ L_p Ipeak^2 F = ½ L_p (0.7V/RSENSE)^2 F$

This relation will help the SMPS designer to determine the 3 suitable parameters for their application: Lp = primary inductance of TX transformer, RSENSE = ISENSE resistor, F = frequency of operation.

For a specific example, with R4 = 2.2Ohm, L_p=1.5mH and F= 70KHz → Pout = 4W – losses ~ 3W. At 5V, the overload condition is set "true" when Ipeak reaches approximatly 600mA.

Calculation of hiccup detect time (T_{Hdtc}) and off time (T_{Hoff})

T_{Hdtc} is proportional to 1/F and typically is 7ms for F_{nom}=70KHz. To calculate T_{Hdtc} at any other frequency, apply 7ms x F_{nom}/F1. Example: F1= 50KHz, T_{dtc} = 7ms x 70KHz/50KHz ~ 10ms

$T_{Hoff} \sim \frac{6 \times (Rstart) \times Vcc}{Vin\ RMS}$. With R = 1.5M, C = 10uF, with Vin =90V, $T_{Hoff} \sim \frac{6 \times 1.5M\Omega \times 10\mu F}{90V} \sim 1s$

Calculation of the max value of the output capacitor :

During the power-up phase, the output capacitor needs to be fully charged within the hiccup detect time T_{Hdtc} otherwise the IPS chip would detect an overload condition which doesn't exist and will enter hiccup mode. Please calculate the maximum capacitor value suitable for your application by applying:

$C6\ max \leq \frac{Lp \times 385 \times (Ipeak)^2}{Vout^2}$ Where Lp = primary inductance of TX transformer
Ipeak = maximum peak current in the MOSFET
Vout = output DC voltage of the SMPS

Using example component values from before, the calculation shows an absolute max value of ~ 2300µF.

HICCUP PROTECTION AGAINST FEEDBACK FAILURE USING A LOW-POWER ZENER

When adding a zener diode with a voltage slightly above the maximum output DC operating voltage, the SMPS will automatically enter hiccup mode if the feedback (optocoupler in an isolated application) fails open. Thanks to entering hiccup mode, the average power dissipation in the diode will be limited to a small fraction of what the SMPS could deliver when the feedback loop is opened. This is why a low-power zener is sufficient for full protection. Therefore the combination of the hiccup capability with a simple low-power low-cost ouput diode brings a very affordable protection against optocoupler failure, avoiding destruction of the load and the SMPS itself. A simple replacement of the failed components then will bring the SMPS back to normal operation.

As already described previously, in hiccup mode the average current drops to a low value. A very low-power rated zener can be therefore selected according to the intrinsic voltage required by the application. This will allow the SMPS to remain overloaded indefinitely without any reliability or safety concerns.

IPS318 – CYCLE SKIPPING MODE

The IPS318 not only protects against overload conditions, but also keeps the power consumption to a minimum in "light load" conditions by entering a cycle skipping mode. The OPTO pin is pulled to the internal 5V rail through an on-chip resistor which value is 50kΩ nominal. A "light load" condition threshold has been internally set to 900mV on the OPTO pin, meaning that the "cycle skipping" mode is active when $0 \leq Vopto \leq 900mV$. In this mode, the power consumption will be kept to a minimum in order to comply with the tightest green requirements. When the OPTO pin voltage is > 900mV, the chip resumes normal operation. This cycle skipping feature keeps the minimum duty cycle to a small, non-zero amount, interspersed by gaps with no pulses, thereby lowering the power consumption by reducing the amount of power wasted in charging/discharging FET/transformer parasitic capacitances.

PIN DESCRIPTION AND APPLICATIONS INFORMATION

The IPS315 is intended as a PWM controller for a switching power supply (either AC-to-DC or DC-to-DC) operating in voltage mode.

VCC (Pin 3) and GND (Pin 7)

The VCC pin acts like a 7.2 volt zener. The GND pin is the lowest voltage the pin sees. The GND pin is also the negative voltage reference for the VCC zener, the ISENSE voltage comparator, the OPTO input voltage, and the FBK input voltage, the RBIAS oscillator resistor, and the NDRIVE gate drive. The

intended design implementation for powering the chip is to have a resistor from VCC to the input voltage for startup, with potentially an additional source of current for normal chip operation. This resistor should be sized such that at minimum input voltage (and subtracting 7.2 volts for the VCC voltage), there is enough current to operate the chip, plus supply the FET gate drive, and OPTO transistor. A separate supply could also provide chip power in more complex applications. It is recommended as good engineering practice to have a decoupling capacitor from VCC to GND of at least 10uF. No input voltage to the chip should be greater than VCC or less than GND.
Note: The VCC pin can be pulled low with switch such as a transistor FET or a relay to turn-off the chip.

Tips for lab experiments
The chip can be damaged with pin voltages greater than 13 volts. When testing power supply designs, it is typical to perform debug with a laboratory current limited external power supply connected to the VCC pin and GND. The external supply in this case should be set for about 10 volts and 10 milliamps. It is possible to damage the chip if the external supply is set for (say) 15 volts and 10 milliamps, the lab supply is turned on, and then the supply is connected to the chip pins because the voltage will be 15 volts (in this example) until the VCC pin starts conducting current and discharges any output capacitance in the lab supply.

PDRIVE (Pin 1) and NDRIVE (Pin 8)
These two pins are intended to each have a resistor connected to them, with the resistors connected together on their opposite sides to provide the gate drive for an external power FET. It is a good design practice to keep the resistors value above 100Ohm to minimize kickback current into the chip. The PDRIVE pin puts current into the FET gate capacitance for FET turn-on, while the NDRIVE pin drains current output of the FET gate capacitance for FET turn-off. The gate resistors should not be greater than about 5k ohms, otherwise the turn-on and turn-off of the FET will be slow enough to cause high power dissipation in the FET because of the amount of time spent in the 'linear region' during the on-off and off-on transitions. Lower resistance provides faster transitions, which means lower losses in the FET, but this also means larger amounts of EMI will be generated. When driving large FETs (high current) or operating at high frequencies, the PDRIVE and NDRIVE pins may not be able to provide sufficient drive performance. This difficulty can be overcome by adding an external pair of low-power transistors (one NPN, one PNP). If you are interested in getting an example schematic showing this, please contact AAI Marketing. Note that the current from the PDRIVE pin to the FET gate comes through the VCC pin, which is why a high value startup resistor on VCC may not be able to provide enough current to the chip to sustain normal operation, thus requiring an additional source of VCC chip power (via the patented snubber or a transformer bias winding). Also note that compared to the IPS1x family, the gate drive voltage will be less with the IPS315 because of the lower VCC voltage. This means that FETs for IPS315 applications must be checked or chosen to ensure good operation at a gate voltage 7.2 volts.

ISENSE (Pin 2)
This pin provides a cycle-by-cycle shutdown function. It connects to an internal voltage comparator which has a 0.7 volt reference on its other input. The intention is that this pin is connected to a current sense resistor connected to the source of the power FET. Current into the FET gate and other noise can appear across a current sense resistor. This means that in some applications it may be necessary to add a small RC filter to the ISENSE pin for good performance. In many applications, the ISENSE pin provides an 'overcurrent/overpower' protection function for the power supply. Due to the signal propagation delays internal and intrinsic in the chip, the overcurrent/overpower threshold can vary with input voltage. Adding two resistors to the power supply can help reduce this variation. If you are interested in getting an example schematic showing this and an explanation of the details, please contact AAI Marketing.

RBIAS (Pin 4)
This pin sets the oscillator frequency with a resistor to ground. Refer to the attached graph for choosing the resistor value. A small capacitor (100-200pF) can be put in parallel with the frequency setting resistor to avoid jitter induced by board noise

FBK (Pin 5)
This pin provides an inverted polarity feedback compared to the OPTO pin. It is a high impedance input connected to a feedback amplifier. The amplifier has a 0.925 volt reference connected to its other input internally. The output of the amplifier goes to the OPTO pin. The error amplifier has excessive gain and bandwidth which preclude its use without a compensation network. For compensation, it is intended that a capacitor (68nF is a typical value) be connected between this pin and the OPTO pin. This capacitor combined with voltage divide resistors will set the 0dB gain frequency. If this pin is not being used, it should be tied to ground to allow the OPTO pin to be used.

OPTO (Pin 6)
This pin is intended to provide a connection for the collector of the phototransistor (with emitter to ground) of an optoisolator for feedback from an isolated secondary. Electrically, this pin looks like a 50kOhm resistance pulled up to 5 volts. It is intended to be a current source of a maximum of 100 microamps. A high voltage (4V) causes a high pulsewidth on the output, while a low voltage (0V) causes a low pulsewidth on the output. When using the FDBK pin as the feedback to the chip, this pin is the output of the FDBK error amplifier, and is one side of the connection for the compensation network. When using the OPTO pin to provide the feedback signal, an external feedback amplifier and compensation network are needed.

PACKAGE DIMENSIONS AND MARKING

The IPS31x is available in plastic 8-pin DIP and SOIC packages. Refer to the latest version of specification AAPS001 (ASIC Advantage's "Package Numbering, Marking, and Outline Standard", available at www.asicadvantage.com) for specific information concerning the package dimensions and package marking.

The following is a brief overview of certain terms and conditions of sale of product. For a full and complete copy of all the General Terms and Conditions of Sale, visit our webpage http://www.asicadvantage.com/terms.htm.

LIMITED WARRANTY

The product is warranted that it will conform to the applicable specifications and be free of defects for one year. Buyer is responsible for selection of, use of and results obtained from use of the product. Buyer indemnifies and holds ASIC Advantage, Inc. harmless for claims arising out of the application of ASIC Advantage, Inc.'s products to Buyer's designs. Applications described herein or in any catalogs, advertisements or other documents are for illustrative purposes only.

CRITICAL APPLICATIONS

Products are not authorized for use in critical applications including aerospace and life support applications. Use of products in these applications is fully at the risk of the Buyer. Critical applications include any system or device whose failure to perform can result in significant injury to the user.

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- IN-PLUG® is a registered trademark of ASIC Advantage, Inc.
- AAI's modified snubber network is patented under the US Patent # 6,233,165. IN-PLUG® Customers are granted a royalty-free licence for its utilization, provision the parts are purchased factory direct or from an authorized agent.

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When AAI accepts to design and manufacture IN-PLUG® products to Buyer's designs or specifications, buyer has certain obligations to provide defense in a suit or proceeding claiming infringement of a patent, copyright or trademark or for misappropriation of use of any trade secrets or for unfair competition.

COMPLIANCE WITH LAWS

Buyer agrees that at all times it will comply with all applicable federal, state, municipal, and local laws, orders and regulations. Buyer agrees to comply with all applicable restrictions on exports and re-exports including obtaining any required U.S. Government license, authorization, or approval. Buyer shall pay any duties, levies, taxes, brokerage fees, or customs fees imposed on the products.

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All shipments of goods shall be delivered ExWorks, Sunnyvale, CA, U.S.A. Title in the goods shall not pass to Buyer until ASIC Advantage, Inc. has received in full all amounts owed by Buyer.

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