IN-PLUG® series: IPS18
Off-line Switcher With Hiccup & Cycle skipping, Ultra Green, Low Cost, High Efficiency. Fail-Safe Protection from Feedback Loop Failure When Combined with Low Power Zener.

- REVISION 10 -

INTRODUCTION

DESCRIPTION

The IN-PLUG® IPS18 is an enhanced off-line switcher version of the IPS15H "hiccup" flyback controller that includes the same basic features plus has been optimized for stand-by applications where the SMPS has to deliver a small amount of power while being required to comply with the tightest "green" regulations.

The original functions of the IPS15 have been retained. They include soft start, line over-voltage protection, shunt-regulator, precision oscillator, PWM with its associated comparator and loop compensation components as well as all the necessary biasing and protection circuitry (thermal shutdown, under-voltage, over-voltage and over-current).

As with the IPS15H, the IPS18 "hiccup" circuitry involves a counter and some other digital blocks. This feature has been added to avoid delivering a high current to the load in an overload condition, which may result in damages to the SMPS, the load or both.

The overload condition is sensed from the line-side by monitoring the MOSFET current. The MOSFET must be allowed to operate at maximum current for the SMPS to properly start and respond to transient conditions. If the operation at maximum current is too long, then it is in an overload condition and the circuit enters "Hiccup Mode". The peak current in the load is still high in order to be able to return to normal mode, but the duty cycle is so low that the average current drops below 100mA therefore allowing the SMPS to remain overloaded indefinitely without any reliability or safety concerns.

The IPS18 not only protects against overload conditions and increases the overall SMPS efficiency by up to 10% but keeps the power consumption to a minimum in "light load" conditions by entering a cycle skipping mode.

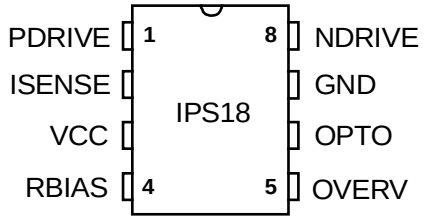
FEATURES

- "Hiccup" function for overload protection.
- "Cycle skipping" in "light load" conditions for ultra green low power requirements
- Max output power controlled from line-side to avoid load-side current sensing circuitry and associated 10% losses.
- Fail-safe protection from optocoupler failure when combined with low-cost low-power zener.
- Lower quiescent current (max. 50% of the IPS15)
- Can drive a large variety of power MOSFETs
- Simple, less critical, lower cost transformer.
- Wide range PWM for stable operation at any load and line voltage.
- Operates with optocoupler or bias winding for constant voltage applications: zeners, adjustable shunt regulator like TL431.
- EMI reduction in critical applications thanks to:
  - Adjustable operating frequency.
  - Separate MOSFET N & P drives
- Power shut-down for stand-by modes.
- Cycle to cycle over-current protection
- Under-voltage lock-out
- Line over-voltage protection.
- External component savings: MOV, X-cap, Y-cap (Application permitting)

APPLICATIONS

- Standby power supplies for TV, VCR and IR remotely-controlled appliances.
- Cordless and feature phones.
- Cellular phone chargers.
- Power tools fast chargers with trickle and on/off.
- Laptops and personal digital assistants.
- Utility meters.
- Replacements for bulky plug-in transformers.

PIN CONFIGURATION: DIP-8 / SOIC-8

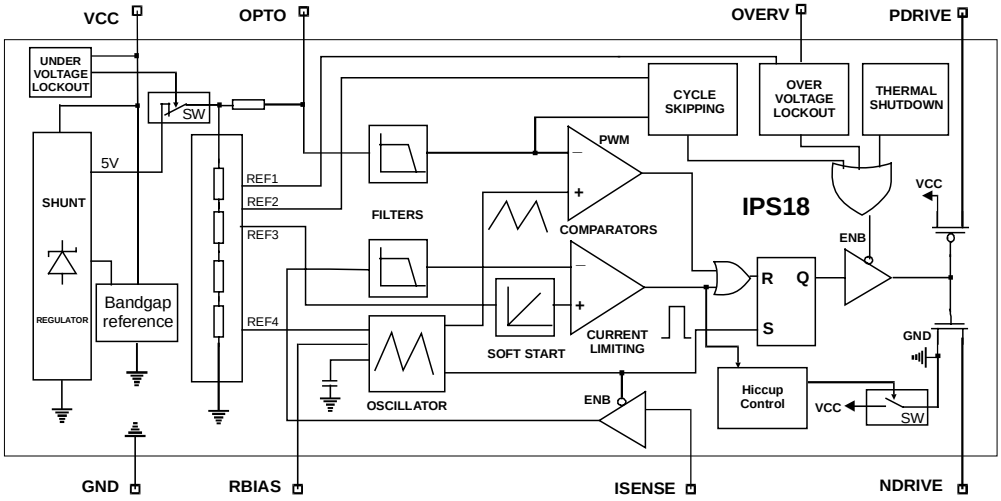


ORDERING INFORMATION

Part No.	ROHS / Pb-Free	Package	Temperature Range	
IPS18C-D	-G-LF	8-Pin PDIP	0°C to +70°C	Commercial
IPS18I-D	-G-LF	8-Pin PDIP	-40°C to +85°C	Industrial
IPS18C-SO	-G-LF	8-Pin SOIC	0°C to +70°C	Commercial
IPS18I-SO	-G-LF	8-Pin SOIC	-40°C to +85°C	Industrial

For detailed ordering information, see page 15

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION SCHEMATIC: AC in 90-265V, DC out 5V, Imax 600mA

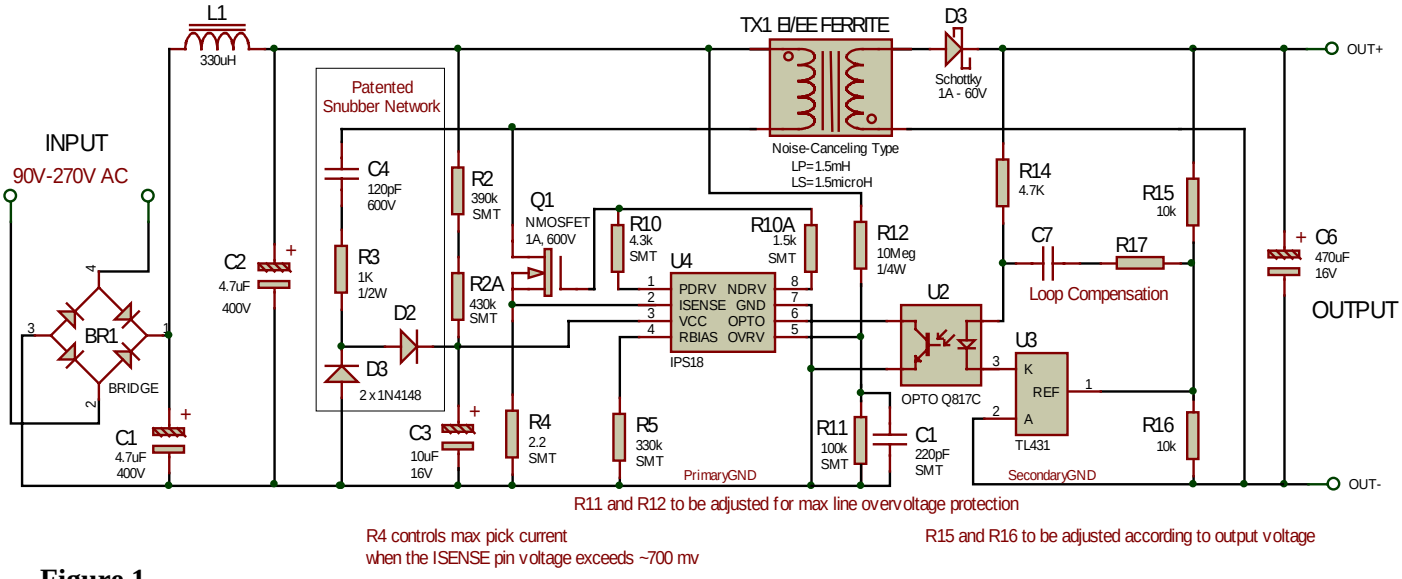


Figure 1

Note: Original R2 has been split into R2 and R2A to double the voltage rating.

Hiccup mode:

The output power that triggers the hiccup mode is monitored from the line-side by sensing the MOSFET current through the ISENSE resistor (R4 in the example of Fig.1). The hiccup mode doesn't require any specific component on the load-side. This mode called "hiccup" is a special "overload protection" mode where the IPS18 resets itself when an overload condition is detected and which duration exceeds the maximum authorized time T_{Hdtc} as described below:

Approximatly $\mathbf{T_{Hoff}}$ after power-up and when the IPS18 is fully operational, the output power is sensed to check an overload condition present or not ("true" or "false") . If it is "true" and remains "true" all over $\mathbf{T_{Hdtc}}$ then the IPS18 resets. Power supply re-establishes and after $\mathbf{T_{Hoff}}$ time, the chip restarts monotoring the output power through RSENSE and the "hiccup" mode could repeat itself as described.

If the overload condition is "false" or when it is true for less than $\mathbf{T_{Hdtc}}$, the IPS18 simply operates like the original IPS10 / IPS15 flyback controllers.

Overload Condition:

An overload condition is defined by

$P_{Sout} > P_{Smax}$ → "true";

$P_{Sout} < P_{Smax}$ → "false";

P_{Sout} = SMPS output power (secondary);

P_{Smax} = maximum authorized output power delivered by the SMPS secondary.

Hiccup detect time T_{Hdtc} and off time T_{Hoff}:

$\mathbf{T_{Hoff}}$ = time from start-up to P_{SOUT} sensing;

T_{Hdtc} = maximum detect time of overload condition to trigger chip reset;

$(T_{Hoff} + T_{Hdtc}) / T_{Hoff.}$ = hiccup duty cycle.

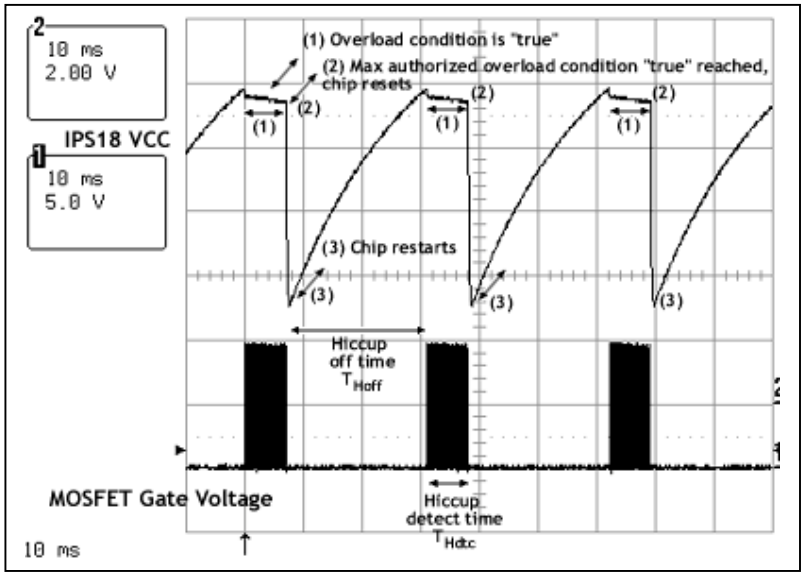


Figure 2: "Hiccup" mode in constant overload condition.

Note: Conditions of figure 2 were altered to better show the "hiccup" operation mode. Actual duty cycle will be much less as indicated in formula below.

Calculation of the output power "P_{Smax}" that triggers the hiccup mode:

As explained above, when $P_{Sout} > P_{Smax}$ for more than T_{Hdtc} time, hiccup mode starts. The previous formula could also be seen from the primary as $P_{Sout} = (P_{Pout}$ - losses$) > P_{Smax}$ where losses correspond to the overall losses (schottky, transformer, MOSFET, snubber etc..). As a first approximation the losses could be estimated to 25% and consequently 75% of primary power P_{Pmax} could be used.

$P_{Pout} > (P_{Smax}$ + losses$) = ½\ L_p Ipeak^2 F$ → Ipeak = 0.7V/RSENSE (0.7V = max ISENSE pin voltage, Ipeak = peak MOSFET current).

$P_{Smax}/0.75 = ½\ L_p Ipeak^2 F = ½\ L_p (0.7V/RSENSE)^2 F$

This relation will help the SMPS designer to determine the 3 suitable parameters for their application: Lp = primary inductance of TX transformer, RSENSE = ISENSE resistor, F = frequency of operation.

As in our example of Fig.1 with R4 = 2.2Ohm, L_p=1.5mH and F= 70KHz → Pout = 4W – losses ~ 3W. At 5V, the overload condition is set "true" when Ipeak reaches approximatly 600mA.

Calculation of hiccup detect time (T_{Hdtc}) and off time (T_{Hoff})

$\mathbf{T_{Hdtc}}$ is proportional to 1/F and typically is 7ms for F_{nom}=70KHz. To calculate $\mathbf{T_{Hdtc}}$ at any other frequency, apply 7ms x F_{nom}/F1. Example: F1= 50KHz, $\mathbf{T_{dtc}}$ = 7ms x 70KHz/50KHz ~ 10ms

$\mathbf{T_{Hoff}} \sim \frac{6 \times (R2 + R2A) \times C3}{\text{Vin RMS}}$. In the example of figure 1, with Vin =90V, $\mathbf{T_{Hoff}} \sim \frac{6 \times 1.5M\Omega \times 10\mu F}{90V} \sim 1s$

Calculation of the max value of the output capacitor C6 (see Fig.1):

During the power-up phase, the output capacitor C6 needs to be fully charged within the hiccup detect time T_{Hdtc} otherwise the IPS18 would detect an overload condition which doesn't exist and will enter hiccup mode. Please calculate the maximum capacitor value suitable for your application by applying:

$$C6\ max \leq \frac{Lp \times 385 \times (Ipeak)^2}{Vout^2}$$

Where Lp = primary inductance of TX transformer
Ipeak = maximum peak current in the MOSFET
Vout = output DC voltage of the SMPs

In the schematic above, the calculation of C6 max shows an absolute max value of ~ 2300µF.

PROTECTION AGAINST OPTOCOUPLER FAILURE USING A SIMPLE LOW-COST, LOW-POWER ZENER

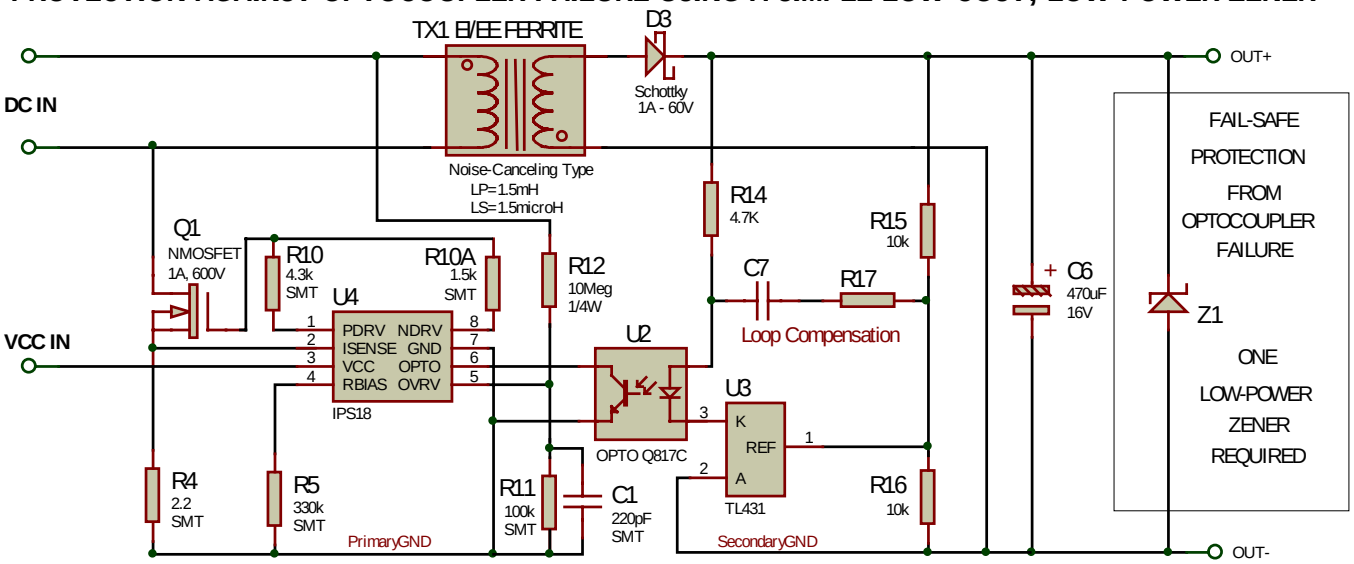


Figure 3

When adding a zener diode with a voltage slightly above the maximum output DC operating voltage, the SMPS will automatically enter hiccup mode if the optocoupler fails open.
Thanks to entering hiccup mode, the average power dissipation in the diode will be limited to a small fraction of what the SMPS could deliver when the feedback loop is opened. This is why a low-power zener is sufficient for full protection.
Therefore the combination of the IPS18 hiccup capability with a simple low-power low-cost ouput diode brings a very affordable protection against optocoupler failure, avoiding destruction of the load and the SMPS itself. A simple replacement of the optocoupler then will bring the SMPS back to normal operation.

As already described in the front page, in hiccup mode the average current drops well below 100mA. A very low-power rated zener can be therefore selected according to the intrinsic voltage required by the application. This will allow the SMPS to remain overloaded indefinitely without any reliability or safety concerns.

PIN DESCRIPTION

Number	Name	Description
1	PDRIVE	Internal P drive terminal to be connected to the gate of the outside power MOSFET. (The rising edge can be adjusted with an external resistor)
2	I_{SENSE}	MOSFET current sensing. Any voltage over 700 mv @ 25°C on this pin for an internally defined number of clock cycles, will trigger "hiccup" mode.
3	V_{CC}	IC positive supply. The chip behaves like a 9.7 volts zener diode.
4	R_{BIAS}	External R_{BIAS} connection to set the operating frequency.
5	OVERV	Line over-voltage lock-out pin. @ 25°C a voltage over 4V on this pin will pull the MOSFET gate to GND.
6	OPTO	Feedback input
7	GND	Ground
8	NDRIVE	Internal N drive terminal to be connected to the gate of the outside power MOSFET. (The falling edge can be adjusted with an external resistor)

IN-PLUG® IPS18 FUNCTIONAL DESCRIPTION

As the IPS15, the IN-PLUG® **IPS18** is a PWM controller for flyback switching power supply applications. This version has been designed to protect SMPSs from overload conditions with a minimum circuitry and minimum load side losses and to comply with the ultra green requirements in keeping the power consumption to a minimum in "light load" conditions. This is achieved by entering a cycle skipping mode.

The principal features are:

- "Hiccup" function for overload protection;
- "Cycle skipping" in "light load" conditions for ultra green low power requirements;
- Low quiescent Current (half of IPS15);
- Max output power (overload) controlled from line-side;
- Shunt regulator to allow the maximum flexibility to power the chip;
- Protections against overheating, and line over-voltage;
- Under-voltage lockout;
- Precise oscillator with externally adjustable frequency;
- On-chip filters for the loop compensation and the over-current sensing;
- Soft start and over-voltage shut-down to protect the MOSFET;
- Separate MOSFET P and N drivers to adjust rising and falling edge independently.

The shunt regulator operates like a zener diode, keeping the chip supply voltage around 9.7 volts. At start-up the chip stays in stand-by mode until the voltage of VCC reaches about 9.7 volts. During this phase, the consumption is of the order of 60 µA and the IC being partially disabled can only handle a maximum of 1mA of supply current. When the 9.7 volts are reached, the driver starts providing gate pulses. The chip will go back to the stand-by mode if the supply voltage decreases down to ~8 volts. The overall chip consumption in normal operation is about 350 µA, not counting the current required to drive the MOSFET gate.

For domestic application, the chip can be supplied from the rectified line voltage through a resistor. In such case, the resistor has to be sized to drive enough current to the chip.

For international applications, the IC gets the start current from a resistor connected to the rectified line voltage (~70 µA) then, after the first gate pulse, the patented modified snubber network (*) provides the additional current to keep the chip running.

The opto pin is pulled to the internal 5V rail through an on-chip resistor which value is 60KΩ nominal, in order to allow a maximal duty cycle of 66 % at ~ 4V. A "light load" condition threshold has been internally set to 900mV, meaning that the "cycle skipping" mode is active when $0 \leq Vopto \leq 900mV$. In this mode, the power consumption will be kept to a minimum in order to comply with the tightest green requirements. When the OPTO pin voltage is > 900mV, the chip resumes normal operation.

During start-up, the duty cycle is controlled by the internal soft start unit which smoothly increases the MOSFET current up to its maximum, corresponding to 700mV developped across the sense resistor.

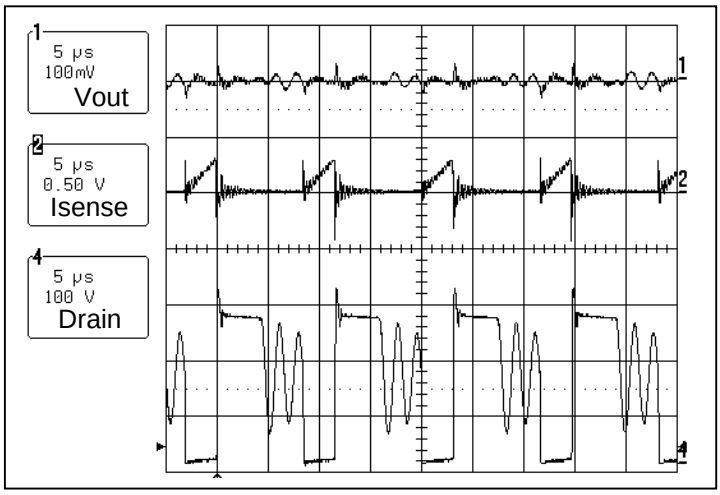
When the expected output voltage is reached, the optocoupler's led is driven, and the opto pin voltage decreases, reducing the duty cycle to a controlled value. The initial current limiting protection of the original IPS15 that was simply turning-off the MOSFET when the ISENSE pin voltage exceeds ~700 mv, is now used to trigger the "hiccup mode" when the condition is present for a maximum time defined by an internal IPS18 digital counter.

This overload condition is sensed from the line-side by monitoring the MOSFET current. The MOSFET must be allowed to operate at maximum current for the SMPS to properly start and respond to transient conditions. When the "time of operation at maximum current" counter overflows, it is in an overload condition and the circuit enters "Hiccup Mode". The peak current in the load is still high in order to be able to return to normal mode, but the duty cycle is so low that the average current drops below 100mA therefore allowing the SMPS to remain overloaded indefinitely without any reliability or safety concerns.

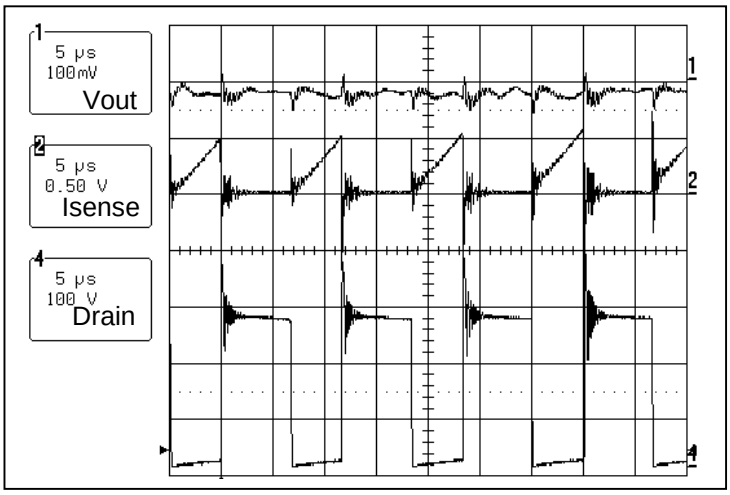
The line-side voltage limiting protection operates by turning-off the MOSFET when the OVERV pin voltage exceeds ~4V.

(*) *US Patent # 6,233,165* - ***Royalty free licence for IN-PLUG® Customers.***

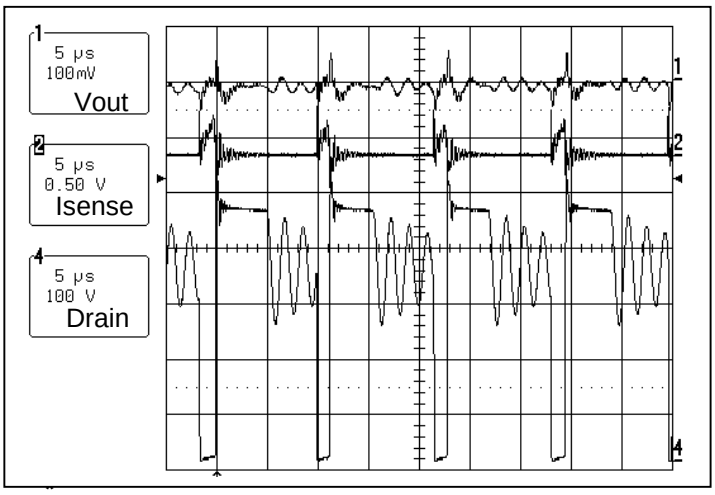
AC 110V - IPS18 normal operation at 5W*



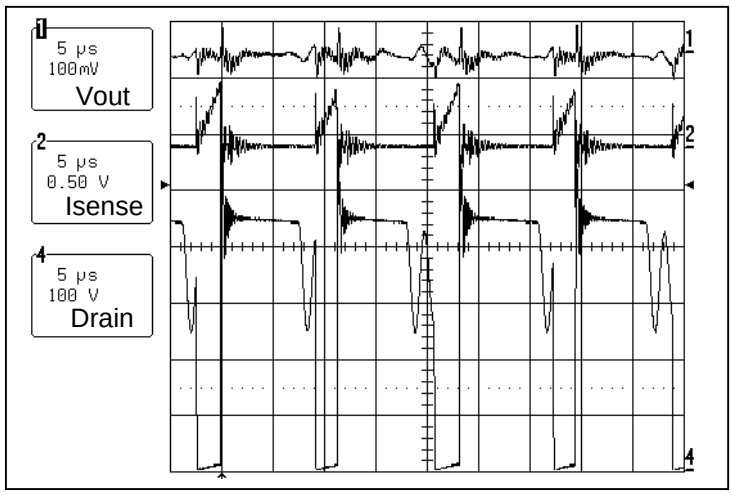
IPS18 normal operation at 15W*



AC 250V - IPS18 normal operation at 5W*



IPS18 normal operation at 15W*



***** Together with a 1A, 600V MOSFET.

OUTPUT POWER CAPABILITY			
Part Number	**Package**	**230V AC or 115V AC w/ Doubler**	**85 – 285V AC**
IPS18	**DIP-8 / SOIC-8**	**Up to 70W (1)**	**Up to 30W (1)**

Note (1): Governed by size and package of external MOSFET

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING		
Characteristics	**Value**	**UNITS**
Shunt regulator max I_{CC} in normal operation (pin 3) - see fig 6-	**50**	**mA**
Shunt regulator max I_{CC} at start-up	**1**	**mA**
All analog inputs (pin 2, 4, 5, 6)	**Min= -0.3, Max= +6.3V**	**V**
Peak drive output current (pin1)	**Source=100, Sink=170**	**mA**
Junction to case thermal resistance $R_{\theta J-C}$	**PDIL = 42, SOIC = 45**	**°C / W**
Junction to PCB thermal resistance $R_{\theta J-A}$	**PDIL = 125, SOIC =155**	
Power dissipation for T_A <= 70°C	**PDIL = 640, SOIC = 500**	**mW**
Operating junction temperature	**- 40 to 150**	**°C**
Storage temperature range	**- 55 to 150**	
Lead temperature (3 mm from case for 5 sec.)	**260**	

PARAMETER	TEST CONDITIONS	PARAMETERS			UNITS
	@ 25°C unless specified	MIN.	TYP.	MAX.	
Supply, bias & circuit protection					
Shunt regulator voltage	**ICC = 1 to 30 mA**	**9.2**	**9.7**	**10.5**	**V**
Shunt regulator dynamic resistance	**1 to 30 mA**	**2**	**3**	**5**	**Ω**
Shunt regulator max peak repetitive current		**-**	**35**	**-**	**mA**
Min I_{CC} to start oscillator		**-**	**-**	**80**	µA
Under voltage lock-out		**V_{CC} – 2.2**	**V_{CC} - 1.5**	**V_{CC} - 1.4**	V
Min I_{CC} to ensure continuous operation	**1A, 600V, 5 nC MOSFET**	**1.1 @ 20KHz**	**3.2 @ 80KHz**	**4.9 @ 150KHz**	**mA**
Current limiting sensing voltage		**655**	**700**	**745**	**mV**
Temperature coefficient of current limiting		**-**	**30**	**-**	**µV/°C**
Overvoltage sensing voltage		**3.85**	**4**	**4.15**	**V**
Soft/start duration	**0 to 700mV**	**-**	**30**	**-**	**clock cycles**
Leading edge blanking		**-**	**900**	**-**	**ns**
Thermal shutdown trip temperature		**-**	**140**	**-**	**°C**

ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETER	PARAMETER	PARAMETERS			UNITS
	@ 25°C unless specified	MIN.	TYP.	MAX.	
Oscillator & PWM					
Range of operating frequencies		30	80	150	KHz
RBIAS values for above frequencies (see figure 4)		550	170	80	KΩ
Oscillator stability with supply & temperature (see figure 5 for average)	I_{CC} = 5 mA Temp = 0 to 70°C	-1.5	-	1.5	%
Maximum duty cycle		-	66	-	%
Minimum duty cycle		-	0	-	%
Hiccup detect time T_{Hdtc}	F = 70 KHz* - see Note2	-	7	-	ms
Hiccup off time T_{Hroff}	Proportional to R2 x C3 See explanation page 3				
Error amplifier					
Sensitivity in mV / % of PWM		-	54	95	mV
Voltage for max duty cycle	OPTO pin	-	4	-	V
Threshold voltage for entering cycle skipping mode	OPTO pin	-	0.9	-	V
Input impedance	OPTO pin	40	60	80	KΩ
P & N Outputs to MOSFET gate					
P gate driver saturation	10 mA (source)	-	-	1	V
N gate driver saturation	10 mA (sink)	-	-	0.6	V
Gate pull-down resistor	(internal)	280	400	520	KΩ
PDRIVE Rise time (10% to 90%)	240 pF load	-	150	-	ns
NDRIVE Fall time (10% to 90%)	240 pF load	-	75	-	ns
Max recommended total external MOSFET charge	@ 20 KHz	-	-	100	nC
"	@ 80 KHz	-	-	50	nC
"	@ 150 KHz	-	-	15	nC

Note1: Electrical parameters, although guaranteed, are not all 100% tested in production.

*** Note2: Detect time T_{Hdtc} is proportional to 1/F. For example at 50KHz, detect time T_{Hdtc} = 7ms x 70KHz / 50KHz = 10ms (full explanation page 3)**

Figure 4: Frequency vs Rbias

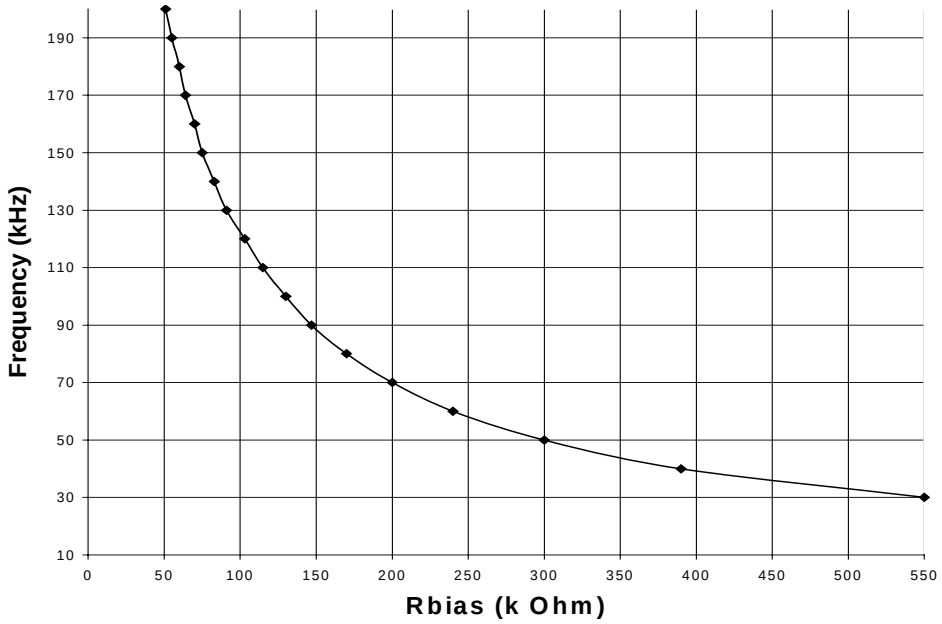


Figure 5 Frequency drift vs temperature

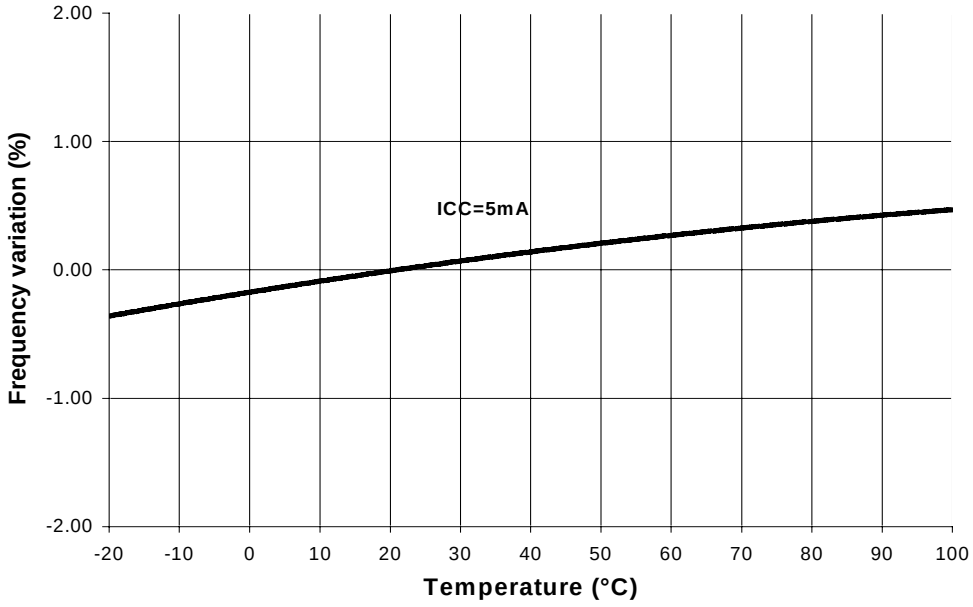
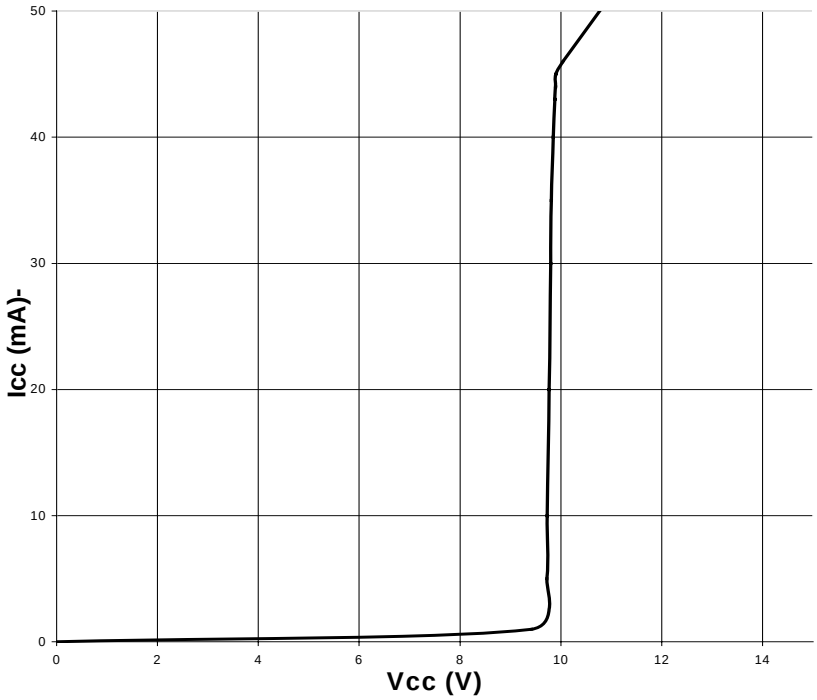


Figure 6: Shunt regulator V/I characteristics*



*** Note: Do not attempt to force more than 1mA into Vcc pin during start-up.**

GOOD DESIGN PRACTICES

IPS18 and loop stability:

The IPS18 is intrinsically very fast and doesn't participate to the loop stability. It only involves a comparator that doesn't bring any gain and exhibits a negligible phase shift.
It has been designed on purpose to allow its utilization in a large range of applications:
(a) Operating at frequencies up to 200 kHz and even above,
(b) Involving very different types of loop stability from "cycle skipping" where the loop is not compensated at all, to good stability achieved through the utilization of a TL431 and finally superior transient response when using half of the IPS25 feedback controller.
The loop compensation is entirely achieved on the load side and the feedback is performed by an optocoupler which gain and dynamic response play an important role in the loop stability.

Precaution in selecting the optocoupler:

The optocoupler must be **using a Phototransistor** and **NOT** a Photodarlington. Most optocouplers of this type are offered in a wide range of coupling efficiency, also called transfer ratio. Even the cheapest ones have a guaranteed transfer ratio of the order of 100% meaning that 1mA of current in the IR LED creates approximately 1mA of current in the receiving phototransistor. The user should be able to design the loop to be stable even though the actual transfer ratio differs by more than a factor of 3 (example from 100% to 300% or 50% to 150%).
Unfortunately optocouplers were not designed for low-current applications and this results in very bad speed and saturation characteristics for the phototransistor which could become incredibly slow and create severe loop stability problems should it be allowed to saturate hard in the application (the optocoupler could cause the IPS18 to skip cycles due to the long time required by the opto transistor to go out of saturation).

In the example of figure 1, the output voltage is 10 volts as defined by R15 and R16 and 2.5V at the Pin #1 of the TL431. The cathode of the TL431 can go to a voltage as low as 2 Volts. The IR LED requires approximately 1 Volt which means that the voltage drop across R14 could be up to 6 volts resulting in a maximum current of 700uA. This value is plentiful for the utilization of a broad range of optocouplers and yet small enough to avoid hard saturation.

Loop stability with the TL431:

The TL431 has an enormous DC gain and will not ensure stability unless specific loop-compensation components such as a RC network are added as indicated below.

The RC network should have a cut-off frequency at 100Hz to roll-off the gain at low frequencies but **reach a plateau around 100Hz** and have enough AC gain at twice the line frequency and achieve a good line ripple rejection.

This is achieved by the loop compensation network **C7, R17** of figure1. The gain rolls off until the impedance of C7 reaches the value of R7. At much higher frequencies, the gain continue to roll-off due to the natural frequency response of the TL431.

The goal is to reach a very low gain at the switching frequency.

If the addition of C7 & R17 with values as shown results in gain is too low, the values of R15 & R16 should be reduced in proportion to lower the impedance at Pin #1 of TL 431. Alternately, if the gain is too high the values of R17 should be reduced and C7 re-adjusted accordingly to maintain the required cut-off frequency.

Criteria to calculate the network :

1) R17 must be much higher than the input resistance of TL431 constituted by R16//R15=5K → 68Kohm OK.

2) F=100Hz=1/(2 x 3.14 x R17 x C7) gives approximately 22,000 pF for C7.

Discontinuous operation:

Check discontinuous mode of operation of the transformer (see application note AN-IPS02 page 2 for details) to ensure that the Flyback SMPS is indeed operating in discontinuous mode in the entire range of Input Voltages and Output Current. The response of the SMPS drastically changes in continuous mode, it gets considerably slower which requires a totally different loop compensation technique. Remember that it is very difficult to ensure loop stability with a simple schematic when the SMPS is allowed to transition between Discontinuous and Continuous modes.

MOSFET driver protection:

The MOSFET driver has been sized to be capable of driving power MOSFETs featuring a total gate charge up to 100nC.

The MOSFET should be turned-on relatively slowly and turned-off much faster. These 2 parameters can be independently adjusted through the external resistors R10 (pin1) and R10A (pin8).

The minimum value of these resistors should be 50Ω in order to reduce EMI and minimize the noise injection which could result from Miller-capacitance kick-back during transient conditions.

See application note AN-IPS-02 for EMI reduction techniques.

ADDITIONAL RECOMMENDATIONS:

For best results in low power off-line SMPSs with the **IPS18**, the following MOSFET features are recommended:

- Low gate charge (max 50 nC).
- 400 V breakdown voltage for domestic use (USA / Japan).
- 600V breakdown voltage for European use (800V when transformer leakage inductance is very small).
- 1, 2 or 3A depending on the maximum output power.

Examples of suitable MOSFETS:

- **IXYS PolarHT™ and Polar HV™** MOSFET series: IXTY1R4N60P, IXTY2N60P, IXTY3N60P
- **Fairchild** MOSFET series: FQPF1N60, FQPF 2N60, FQPF 3N60.
- **Infineon COOLMOS™** series: SPD01N60S5, SPD02N60S5, SPD03N60S5.
- **Motorola** MOSFET series: MTP1N60, MTP2N60, MTP3N60.
- **SGS-Thomson** MOSFET series: STD1NB60, STD2NB60, STD3NB60.
- **Etc…**

Notes:

- Due to the rapid evolution of MOSFET technologies, please check for current models when designing a new SMPS.
- **PolarHT™ and Polar HV™** are trademarks of IXYS corporation
- **COOLMOS™** is a trademark of Infineon.

TRANSFORMER CHARACTERISTICS:

(a) Transformer design:

E-core with suitable gap to prevent saturation or distributed-gap toroid. Primary inductance of 1.5 mH is very typical in 5 -10W applications with 5V output DC:
Turn ratio = 9 for 220V input or universal 85V – 265V.
Turn ratio = 7 for 100-120V AC input (Japan and USA)

(b) Transformer phasing:

Check the phase indicated in figure 1. Also refer to applications notes AN-IPS-01 and AN-IPS-02.

SNUBBER NETWORK:

With reference to figure 1, R2 + R2A provide the start-up current for the chip. C3 is being charged through R2+R2A. Once the chip supply voltage is high enough, the gate drive starts and the chip is then powered by the modified snubber network presently being patented by our company.
The snubber values may have to be optimized for different specific operating conditions:

- R3 could be reduced to 100 ohms and sometimes eliminated.
- C4 could be increased to 200pF and sometimes more.

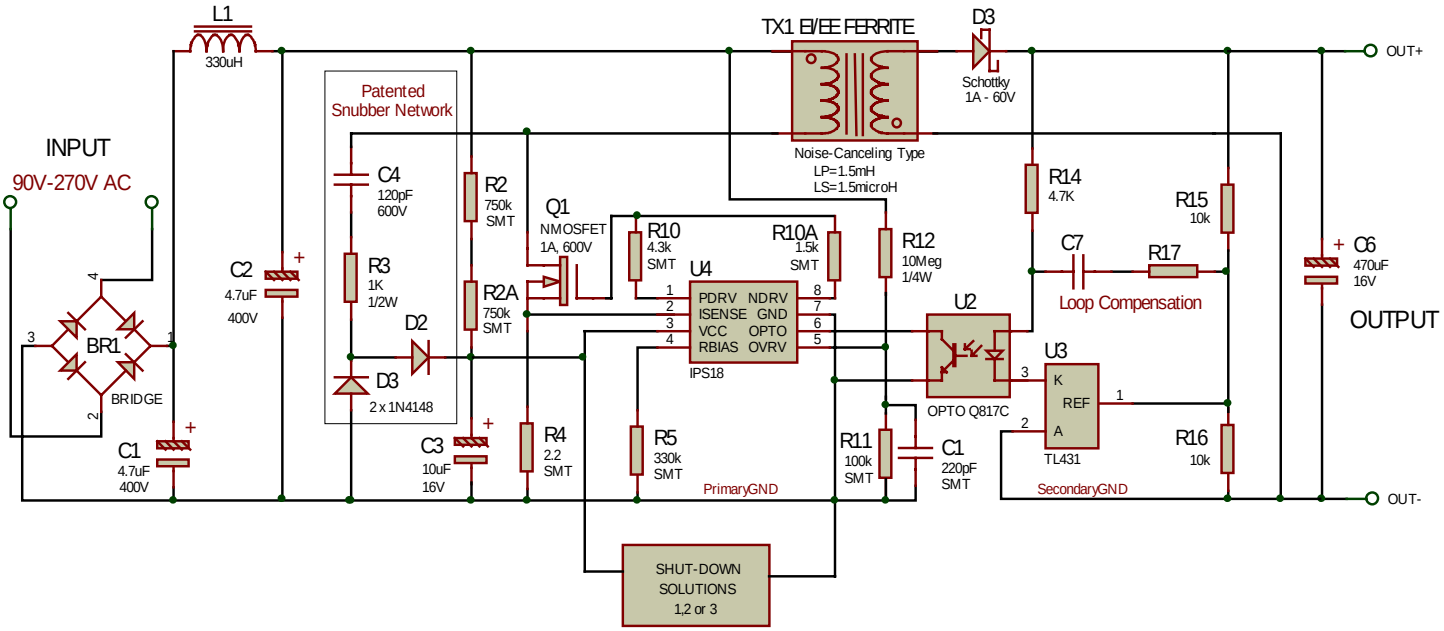
Depending on the characteristics of the transformer, essentially leakage inductance and distributed capacitance, the snubber network shown in figure 1, may not be efficient enough to reduce the voltage spikes when operating at 20W or above. Please refer to applications notes AN-IPS-01 and AN-IPS-02 design tips or EMI reduction techniques, or feel free to contact our technical support for assistance.

POWER SHUT-DOWN SOLUTIONS for STAND-BY REQUIREMENTS:

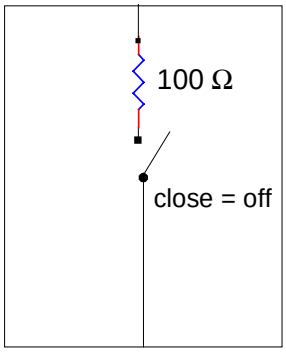
For low-power stand-by requirements, the primary circuitry can be shut-down by pulling the IPS18 VCC pin "LOW" through a 100Ω resistor.
This can be easily done using a:

- Simple switch
- PNP transistor
- NPN transistor

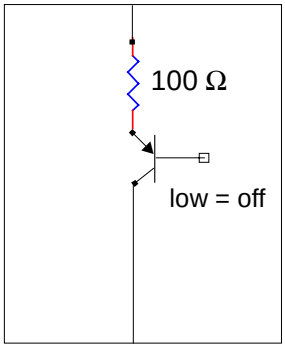
SHUT-DOWN SOLUTIONS (cont'd):



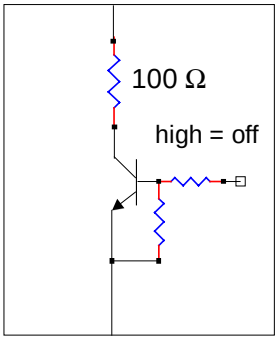
Solution 1:
simple switch, close = off
100Ω resistor
mandatory



Solution 2:
PNP transistor, low = off
(low = less than 4V)
100Ω resistor
optional



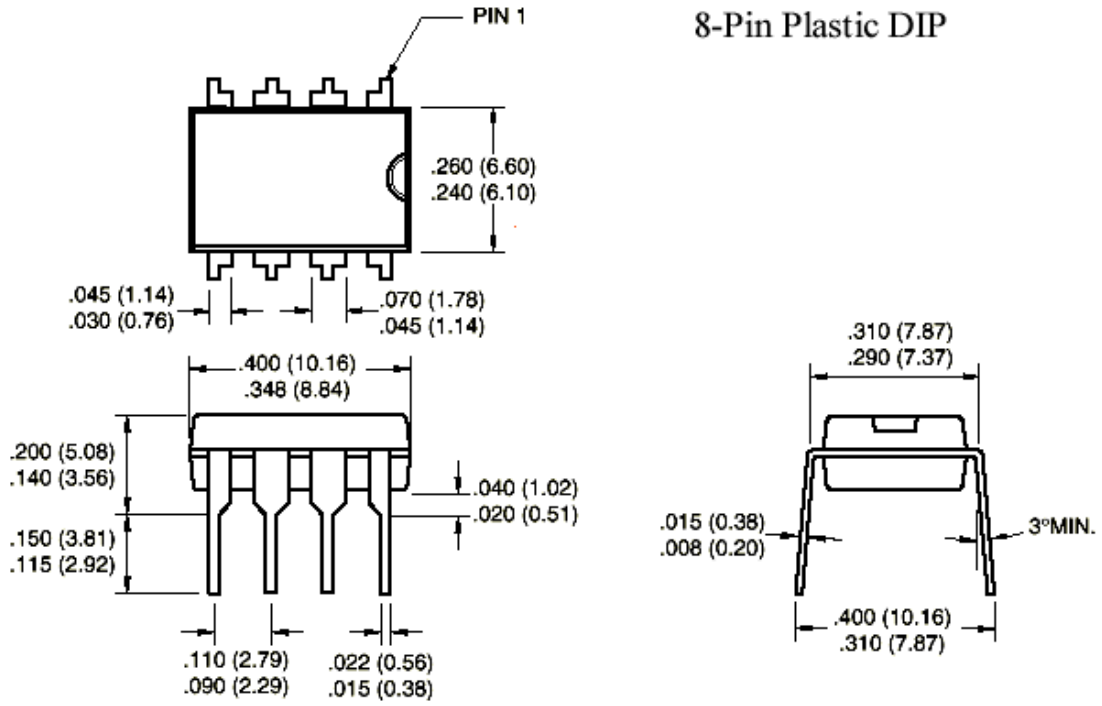
Solution 3:
NPN transistor, high = off
100Ω resistor
optional



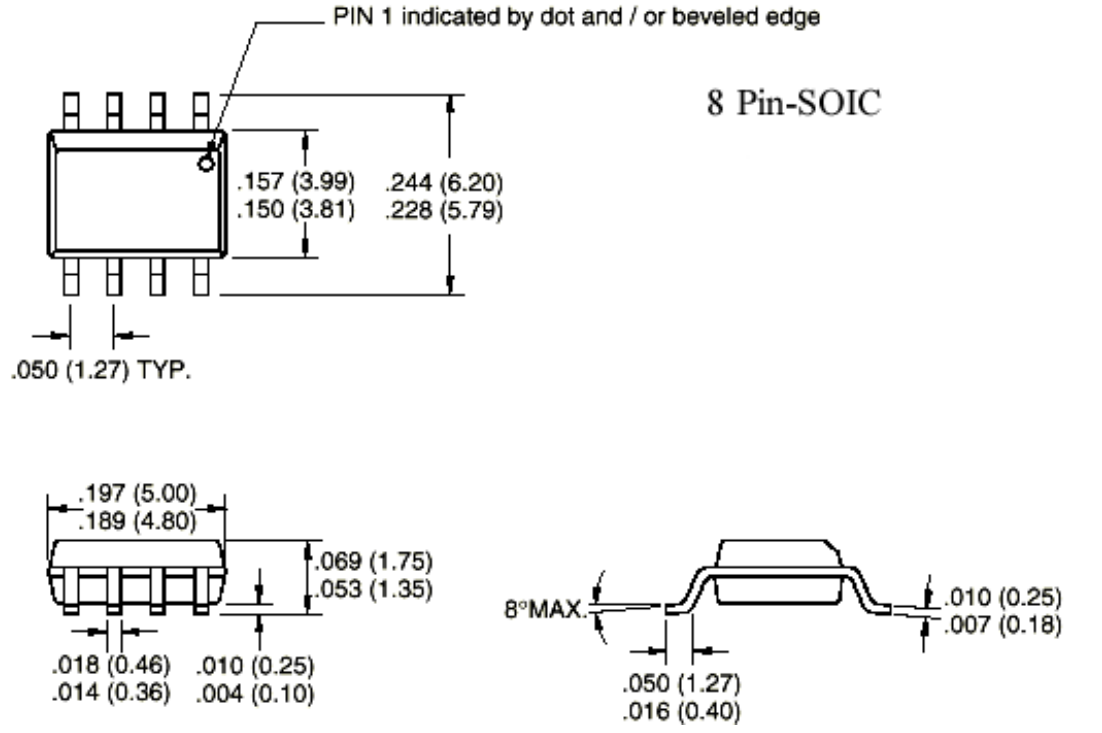
When the "LOW" state is released, the VCC is naturally re-established, re-activating the IPS18.

PACKAGE DIMENSIONS

PLASTIC DIP-8



PLASTIC SOIC-8



ORDERING INFORMATION

Part-Number

IPS XXXH C – YY – G-LF - TR

IN-PLUG® Controller Series

Flyback
Feedback
PFC
Push-Pull
LED Driver

Controller Type

Flyback: 10 series
Feedback: 20 series
PFC: 100 series
Push-Pull: 200 series
Automotive: 300 series
LED Driver: 400 series
"H" with hiccup overload protection

Temperature Range

C : Commercial (0, +70°C)
I : Industrial (-40°C. +85°C)
A: Automotive (-40°C. +125°C)
Note : Default or not specified is <commercial>

Package Type

D : DIP8
SO : SOIC8
(For production with a new date code, since January 2006, the package type does not appear anymore on package marking)

ROHS + Pb-Free

Tape and Reel

TR : Tape & Reel
TU : Tube
Note1 : Default or not specified is « tube ».
Note2 : Does not appear on package marking.

Example of Marking

Non-Green Package

Green ROHS + Pb-Free Package

(Note : For production with a new date code, since January 2006, the package type does not appear anymore on package marking)

This ordering information is for commercial and industrial standard IN-PLUG® controllers ONLY. For custom controllers or for military temperature range, call AAI's sales representative.

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- IN-PLUG® is a registered trademark of ASIC Advantage, Inc.
- AAI's modified snubber network is patented under the US Patent # 6,233,165. IN-PLUG® Customers are granted a royalty-free licence for its utilization, provision the parts are purchased factory direct or from an authorized agent.

PROTECTION FOR CUSTOM IN-PLUG® SOLUTIONS

When AAI accepts to design and manufacture IN-PLUG® products to Buyer's designs or specifications, buyer has certain obligations to provide defense in a suit or proceeding claiming infringement of a patent, copyright or trademark or for misappropriation of use of any trade secrets or for unfair competition.

COMPLIANCE WITH LAWS

Buyer agrees that at all times it will comply with all applicable federal, state, municipal, and local laws, orders and regulations. Buyer agrees to comply with all applicable restrictions on exports and re-exports including obtaining any required U.S. Government license, authorization, or approval. Buyer shall pay any duties, levies, taxes, brokerage fees, or customs fees imposed on the products.

TITLE AND DELIVERY

All shipments of goods shall be delivered ExWorks, Sunnyvale, CA, U.S.A. Title in the goods shall not pass to Buyer until ASIC Advantage, Inc. has received in full all amounts owed by Buyer.

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