Introduction

The following document provides guidelines for designing a PoE system Powered Device (PD) compliant with IEEE 802.3af (IEEE802.3at Type 1) or 802.3at (Type 2) standards by using Microsemi's PD70100 or PD70200 Front-End ICs. PD70100 Front-End IC provides all necessary detection, classification, and operating current levels compliant with IEEE 802.3af PoE standard. PD70200 Front-End IC provides the necessary detection, classification, 2-event mark for "AT" flag, and operating current levels compliant with IEEE 802.3at Type 2 standard.

This document includes a brief overview of PoE functionality with respect to the applicable standards; however it is not to be considered a substitute for IEEE standards. Applicable standard should always be consulted when making decisions affecting the design of the circuit.

PD70100 and PD70200 device family consists of PD70101A and PD70201 which are devices comprising both PD front end functionality and a PWM controller.

PD70101A and PD70201 are targeted for applications where the PD application needs compact and cost effective solution in a single package.

PD70100 and PD70200 device family also consists of PD70210/A which supports PD power levels of up to 95W in a single device.

Applicable Documents

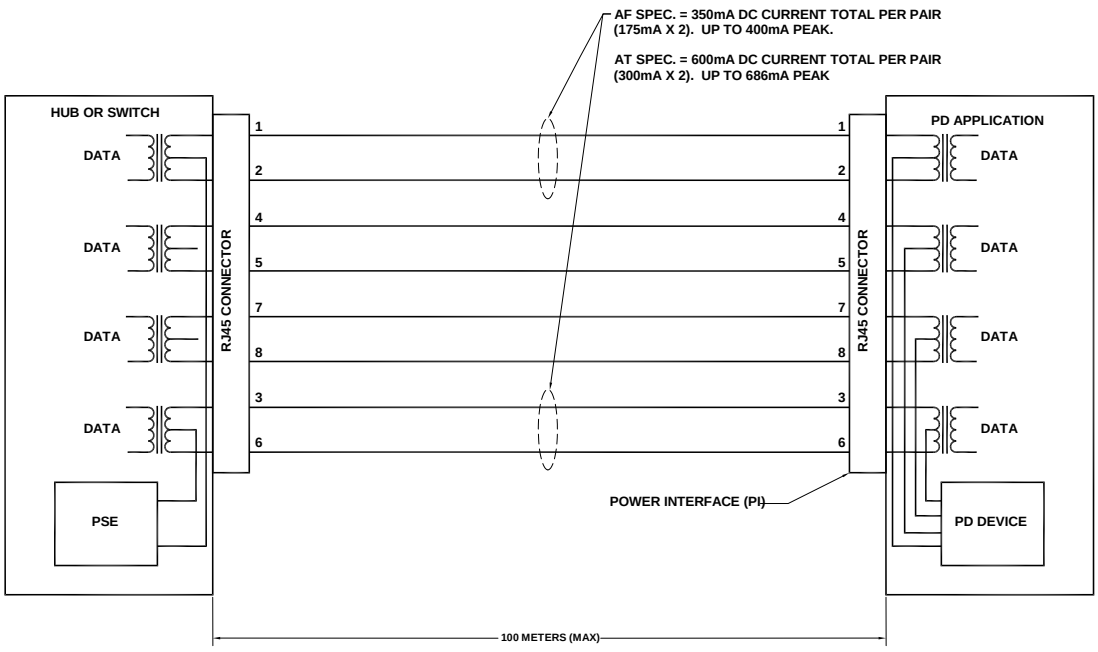
- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD70100/PD70200 datasheet, catalog number DS_PD70100_70200

POE Overview

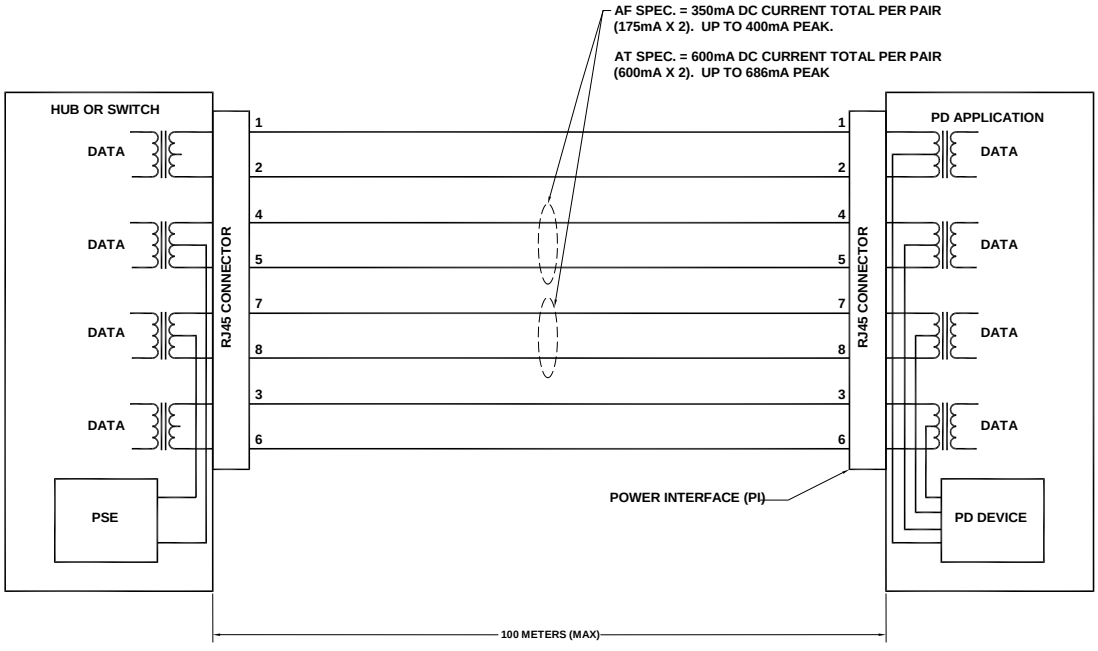
In its simplest form, PoE consists of a power source, referred to as Power Source Equipment (PSE), an Ethernet cable (typically contained in an infrastructure) with maximum length of 100 meters, and a Powered Device (PD) which accepts both data and power from the Power Interface (PI) of the Ethernet cable. PI is typically an eight pin RJ45 type connector. A diagram of this arrangement is shown in Figure 1.

IEEE 802.3af or IEEE 802.3at type 1 PSEs are designed to operate with Ethernet cabling which may include CAT3 (per TIA/EIA 568). As such they may contain a 26AWG wire. A cable of this type may impose a 20Ω maximum power loop resistance to a PSE operating into the maximum specified 100 meter cable length. IEEE 802.3at type 2 PSEs are designed to operate at higher output power levels with CAT 5 or higher (per TIA/EIA 568) Ethernet cabling. These cables contain 24AWG wire (or better) and may impose a maximum 12.5Ω power loop resistance to a PSE operating into the maximum specified 100 meter cable length. The voltage drop and internal temperature rise created in a 100 meter Ethernet cable affect the voltage and current available to the PD. A brief comparison between the AF and AT standards for the PSE and the PD are presented in Table 1 and Table 2, respectively.

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308



Alternative A



Alternative B

Figure 1: Basic PoE Configuration for IEEE 802.3at Standard

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

Comparison of IEEE 802.3af and IEEE 802.3at Standards for PSE		
PSE Requirements	**IEEE 802.3af or IEEE 802.3at type 1**	**IEEE 802.3at type 2**
Guaranteed Power at PSE Output	15.4W	30W
PSE Output Voltage	44V to 57V	50V to 57V
Guaranteed Current at PSE Output	350mA DC with up to 400mA peaks	600mA DC with up to 686mA peaks
Maximum Cable Resistance	20Ω	12.5Ω
Physical Layer Classification	Optional	Mandatory
Supported Physical Layer Classification Classes	Class 0 to Class 4	Class 4 - mandatory
Data Link Classification	Optional	Optional
2-Events Classification	Not required	Mandatory
4 pairs power feeding	Not allowed	Allowed with 2 collocated PSEs
Communication Supported	10/100 BASE-T (Midspans) 10/100/1000 BASE-T (switches)	10/100/1000 BASE-T Including Midspans (Both type1 and type2)

Table 1: IEEE 802.3af and 802.3at Standards for PSE

Comparison of IEEE 802.3af and IEEE 802.3at Standards for PD		
PD Requirements	**IEEE 802.3af or IEEE 802.3at type 1**	**IEEE 802.3at type 2**
Guaranteed Power at PD Input	12.95W	25.50W
PD Input Voltage	37V to 57V	42.5V to 57V
Guaranteed Current at PD Input	350mA DC with up to 400mA peaks	600mA DC with up to 686mA peaks
Maximum Cable Resistance	20Ω	12.5Ω
Physical Layer Classification	Mandatory (no class = Class 0)	Mandatory
Supported Physical Layer Classification Classes	Class0 to Class4	Class 4 – mandatory
Data Link Classification	Optional	Optional
2-Events Classification	Not required	Mandatory
4 pairs power receiving	Allowed	Allowed
Communication Supported	10/100 BASE-T (Midspans) 10/100/1000 BASE-T (switches)	10/100/1000 BASE-T Including Midspans (both type1 and type2)

Table 2: IEEE 802.3af and 802.3at Standards for PD

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

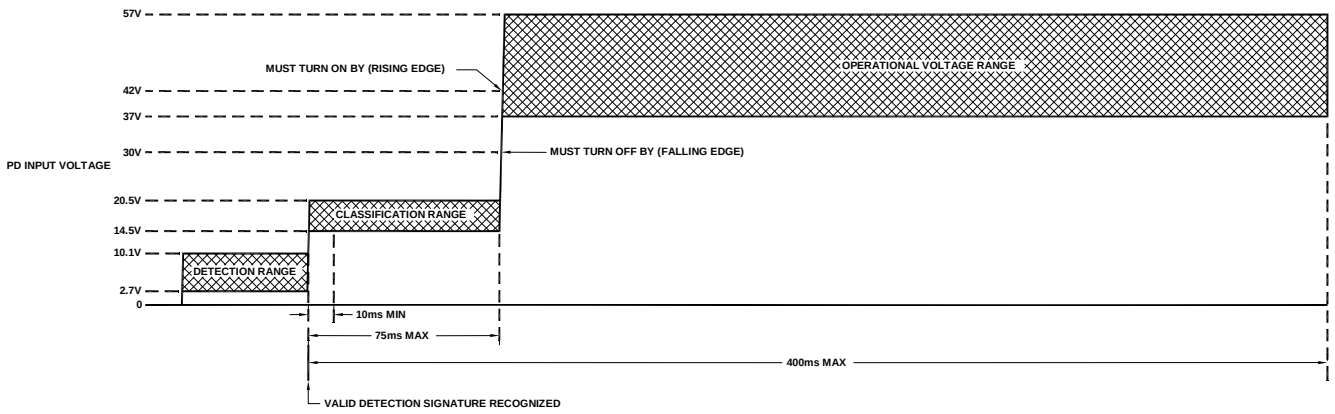
PSEs can supply power on the RJ45 PI through either the RX and TX wire pairs (pins 1-2 and 3-6, respectively for 10/100 Base-T), or the spare pairs (pins 4-5 and 7-8). For 1000 Base-T connections, power can be present on the same pin combination. However the spare pair terminology is eliminated as data is transmitted on all pairs. Power through wire pairs can be of either polarity. To accommodate all possible combinations of PoE power available at the PI, a use of dual diode bridges on the PD side is required.

IEEE standards define a method of determining whether a cable is disconnected, connected to a non-PoE device, or connected to a PoE-compliant PD. IEEE standards further define a method of determining power requirements of the connected PoE-compliant PD, and a method by which the PD may determine whether PSE is compliant with IEEE 802.3at type 2 power levels. These determining methods are accomplished in three phases: Detection phase, Classification Phase, and 2 Event Classification (recognized by PD70200 only). The determining events are triggered at different voltage levels, all of which occur before the PSE applies the nominal PoE voltage levels specified in Table 2. nominal operating voltage is not applied if a valid signature is not present during the Detection phase. A diagram of the Detection, Classification, and Power-up sequences is shown in Figure 2.

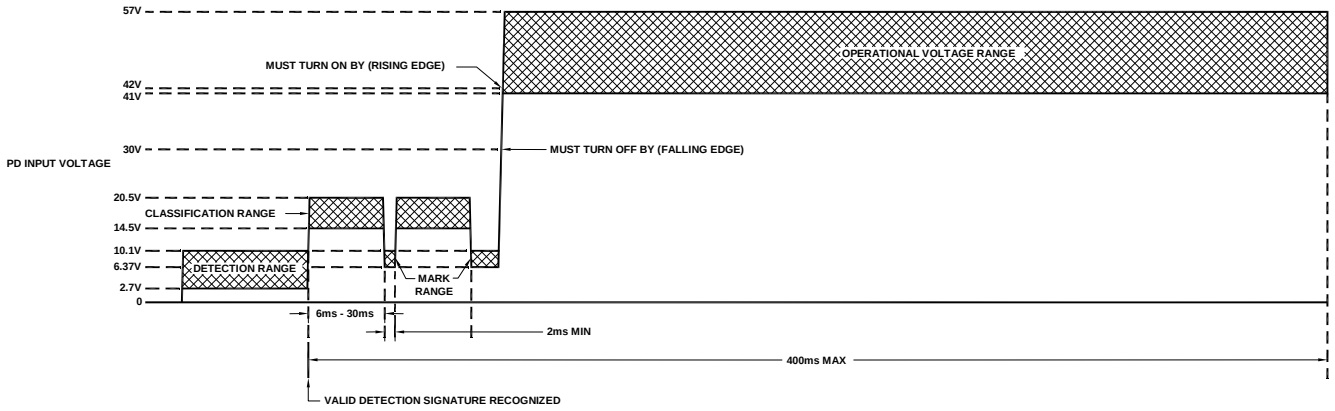
PSE initially operates in an idle state, in which PI is unpowered, with an exception of a periodic detection signal “looking” for a valid detection signature. Signal levels presented at the PI during Detection phase are of sufficiently low levels for not causing damage to non-PoE devices. During Detection phase, a PoE-compliant PD will provide a valid detection signature using two components, each located on the output side of the diode bridges. A capacitor of 50nF to 120nF connected directly across the diode bridge output terminals, and a 25kΩ resistor, switched across the diode bridge output terminals, and present only during Detection phase.

After a valid signature is detected, PSE may start Classification phase. Classification phase is optional for 802.3af and 802.3at type 1 PSEs and PDs; however it is mandatory for 802.3at type 2 PSEs and PDs. Classification signature is achieved by means of a programmed current draw, set by the PD corresponding to one of 5 classes. The programmed current draw is required to be at a valid level within 5ms from beginning of Classification phase, and must remain constant throughout Classification period (after Classification period the programmed current draw is disabled). Class levels and their corresponding currents are outlined in Table 3.

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308



802.3af AND 802.3at TYPE 1 PD INPUT REQUIREMENTS



802.3at TYPE 2 PD INPUT REQUIREMENTS

Figure 2: Basic PoE Detection, Classification, and Power-Up Sequences

Classification Current Definitions Note: PD Input Voltage During Classification Phase = 14.5V to 20.5V					
Class	**Usage**	**Maximum PD Power**	**PD Current Draw During Classification**		
			Min	**Average**	**Max**
0	Default	0.44W to 12.95W	0		4mA
1	Optional	0.44W to 3.84W	9mA	10.5mA	12mA
2	Optional	3.84W to 6.49W	17mA	18.5mA	20mA
3	Optional	6.49W to 12.95W	26mA	28mA	30mA
4	Reserved for Future Use (AF compliant PD) Classify AT (AT compliant PD)	Treat as Class 0 (AF compliant PD) Treat as Class 4 (AT compliant PD)	36mA	40mA	44mA

Table 3: Classification Current Definitions

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

In addition to hardware-generated (physical layer) classification outlined above, IEEE standards define a Data Link Layer (DLL) classification, established through Ethernet data link after PD power-up occurs. DLL classification may be used by 802.3af or 802.3at type 1 PDs optionally, but *shall* be used by 802.3at type 2 PDs. IEEE standard requires 802.3at type 2 compliant PDs that must use both hardware generated and DLL generated classifications.

A final Classification phase is required only for IEEE 802.3at type 2 compliant PSEs and PDs. Classification phase serves in informing the PD whether PSE is 802.3at type 2 compliant or not. An AT type 2 compliant PSE will provide a "2-Events Classification" signature during Classification phase. The 2-Events Classification signature toggles the input voltage between standard classification voltage range (14.5V to 20.5V) and a voltage "mark" level, specified between 6.37V and 10V. PSE voltage is toggled twice between these two voltage ranges to indicate PSE is 802.3at type 2 compliant. AT type 2 compliant PD is required to recognize the 2-event classification, and provide to internal circuits a flag signal that indicates PD is connected to an AT type 2 compliant PSE.

Should the port voltage present at the PI drops below 2.8V, AT type 2 compliant PD must reset the AT flag

Once Detection and Classification phases are complete, PSE will provide IEEE with a specified operating voltage at a maximum current level determined by the PSE itself. IEEE standard requires normal operation voltage that will be established by the PSE within 400ms of a valid detection signature.

During normal operation, PD must provide a signature to inform the PSE it is still present and requires power. This signature is referred to as "Maintain Power Signature" (MPS). MPS is defined as a minimum current draw by the PD, lasting a minimum period of 60ms, and occurring at least once every 400ms. If a valid MPS is not detected by the PSE, it will disconnect the power from the PI, return to an idle state, and start Detection phase. A diagram of the Maintain Power Signature is shown in Figure 3.

All compliant PDs contain an isolating switch that disconnects the return side of the PD from the PI during Detection and Classification phases, or during power loss. PD is required to turn on the isolating switch at PI voltage levels of 42V or higher, and turn off the isolating switch at PI voltage levels of 30V or lower. In case PD circuit output is connected to a bulk capacitor of 180µF or more, PD must actively limit the current during start-up to 350mA or less. A block diagram illustrating a basic PD circuit is shown in Figure 4.

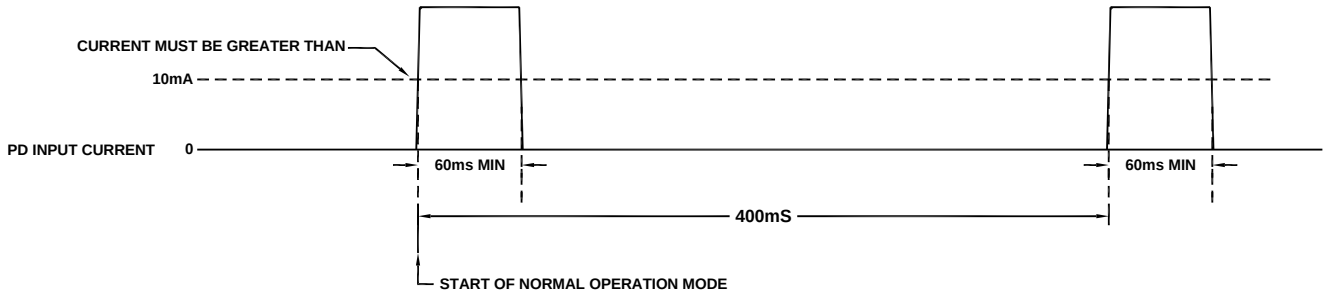


Figure 3: PoE Maintain Power Signature (MPS) Requirements

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

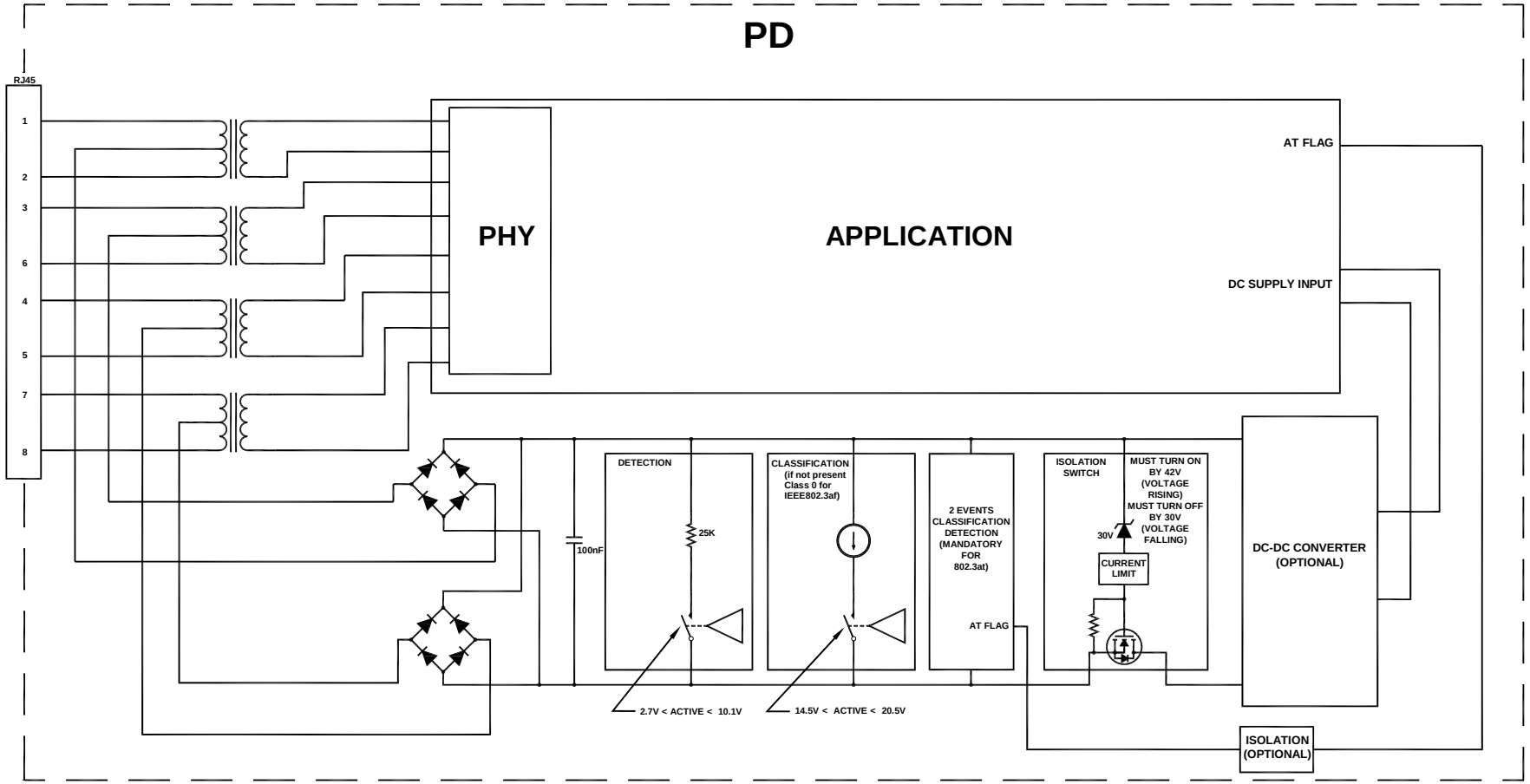


Figure 4: Basic PD Block Diagram

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

PD70100/PD70200 Features_

- IEEE 802.3af (IEEE802.3at Type 1) Compliant (PD70100)
- IEEE802.3at Type 2 Compliant (PD70200)
- Supports up to 47.7W 4 pair systems with a single PD70200
- Provides PD Detection Signature
- Programmable PD Classification Signature
- Supports 2 Event Classification Flag (PD70200)
- Active Low, Open Drain Power Good Signal
- Integrated Isolation Switch
- 24.9KΩ signature resistor disconnection when power is on, for power saving
- Inrush Current Limit (Soft Start)
- Integrated 12V Start-up Supply Output for DC-DC Converters
- Short Circuit Protection
- Internal Discharge Circuitry for DC-DC Bulk Capacitor
- Wide Temperature Operating Range -40°C to +85°C
- On-Chip Thermal Protection

Using PD70100/PD70200 Front-End IC_____

PD70100 Front-End IC provides the necessary Detection, Classification, and Isolation Switch control functions for a PoE-powered device conforming to IEEE 802.3af or 802.3at type 1 standards. PD70200 Front-End IC provides the same functions as PD70100, with an additional higher Isolation Switch current capability, additional 2-Events- Classification detection and AT Flag generation conforming to IEEE 802.3at type 2 standard. Both chips are designed for minimal external components.

PD70100/PD70200 IC may be configured as a two or four pair system (see Figure 5). In the first option one PD70100/PD70200 IC is driven from both diode bridges (output terminals connected in parallel). In the second option PD70100/PD70200 IC is configured as a four pair system (see Figure 6) in which each of two PD70100/PD70200 ICs is driven individually by one of the two diode bridges. In the four-pair, two-IC system, the isolation switch output terminals of the two PD70100/PD70200 ICs are connected in parallel. This configuration, as opposed to the two pair system, allows available output power to double affectively.

In a two pair/four pair single IC system, a single PD70100/PD70200 IC is placed in a PD design between the two input diode bridges and the input filter/bulk capacitor for the DC/DC converter (DC/DC requirements are based on application; however a typical application may use an isolated DC/DC converter topology). A paralleled output terminal from the two diode bridges is externally connected to the PD70100/PD70200 IC at V_{PP} (positive connection, pin 12), and VPN_{IN} (negative connection, pin 4,5). PD70100/PD70200 output connections to the DC/DC converter/application are made at V_{PP} (positive connection, pin 12), and VPN_{OUT} (negative connection). VPN_{OUT} is the application ground connection to the integrated isolation switch of the PD70100/PD70200 IC.

In addition to the basic input/output connections, the following components are required for a typical application:

- **Input capacitor:** Between V_{PP} pin, and VPN_{IN} pin is recommended to use a 100V 100nF X7R capacitor. This capacitor can be between 50nF to 120nF. This capacitor should be located as close as possible to PD device
- **Input TVS:** Between V_{PP} pin, and VPN_{IN} pin is recommended to use a 58V TVS similar to 1SMA58AT3G.
- **Detection Resistor:** Connect a 24.9kΩ ±1% resistor between V_{PP} and R_{DET} (Pin 1). This resistor is used to satisfy the Detection signature. A low wattage type may be used as there is less than a 7mW stress on this resistor while Detection phase is active, and the resistor is disconnected after power is on.
- **Reference Resistor:** Connect a 240kΩ ±1% resistor between R_{REF} (pin 2) and VPN_{IN} (pins 4, 5). This resistor should be located as close as practical to the PD70100/PD70200 IC. A low wattage type may be used (there is less than 1mW stress on this resistor).
- **Classification Current Resistor:** The value of this resistor determines the PD current draw during Classification Phase. Values corresponding to IEEE compliant classification levels are shown in Table 4. Connect this resistor between R_{CLASS} (pin 3) and VPN_{IN} (pins 4, 5).
- **Power Good Pull-up:** Power Good signal is available at P_{GOOD} (pin 10). After startup, a P_{GOOD} flag is generated low voltage to optionally inform the application DC/DC converter that the power rails are ready. This is an open drain pin which requires a resistor pull-up to be functional. Pull-up voltage on this pin cannot exceed 74V and is recommended to be pulled up to a voltage no higher than V_{PP}. This pin is output low, rated at 0.4V and 5mA. It is recommended to connect a 50kΩ or higher resistor between this pin and V_{PP}.
- **AT Flag Pull-up (PD70200 only):** AT Flag signal is available at AT_FLAG (pin 9). This is an open

drain pin which requires a resistor pull-up to be functional. Pull-up voltage on this pin cannot exceed 74V and is recommended to be pulled up to a voltage no higher than V_{PP}. This pin is output low rated at 0.4V and 5mA. It is recommended to connect a 50kΩ or higher resistor between this pin and V_{PP}.

- **V_{AUX} Output Capacitor:** V_{AUX} is a low power regulated output available for use as a start-up supply for an external DC/DC converter controller. This supply is low duty, and intended to be used on a supply rail bootstrapped to a DC/DC converter output. V_{AUX} output requires ceramic capacitor of minimum 4.7µF, to be connected directly between V_{AUX} (pin 11) and VPN_{OUT}.

Programmed Classification Signature R_{CLASS} Resistance Values				
Class	**R_{CLASS} Resistor Value**	**PD70100/PD70200 Current Draw During Classification**		
		Min.	**Average**	**Max.**
0	Open	0		3mA
1	113Ω ±1%	9.5mA	10.5mA	11.5mA
2	64.9Ω ±1%	17.5mA	18.5mA	19.5mA
3	42.2Ω ±1%	26.5mA	28mA	29.5mA
4	30.9Ω ±1%	38mA	40mA	42mA

Table 4: RCLASS Resistance Values

A single PD70100/PD70200 IC may be operated with 4 pairs for extended power capability up to 16.65W (PD70100) or 47.7W (PD70200). PD70100/PD70200 component requirements are the same as applications operating with 2 pairs. A typical 2 pairs/4pairs single IC configuration is outlined in Figure 6.

An additional circuit may be optionally added to sense if input POE power is provided on 2 pairs or 4 pairs. This circuit is shown in the application example of **Error! Reference source not found.**.

Refer to the optional circuit of **Error! Reference source not found.**, for detecting the presence of the 4 pairs.

D8 is 18V Zener diode; it causes the circuit to be active only above the Class phase of the PSE. This way during the detection and the classification phases there is no unwanted leakage on PSE output. R11 and R12 provides pull up current so that the presence of the individual 2 pairs input may be sensed and combined into a logical OR function via diodes D10 through D11.

The output of the 4 pair detection circuit is then used to drive the switch circuit of U3, R10, R13, and Q2. The signal present at the drain of Q2 will be low if only 2 pairs are present and high if all 4 pairs are providing power. Be aware that the output of this 4 pair's detection circuit is at POE voltage levels, and should not directly interface to low-level logic. In the described circuit, the Drain of Q2 interfaces directly to an Optoisolator and the output of it will be an isolated inverted indication.

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

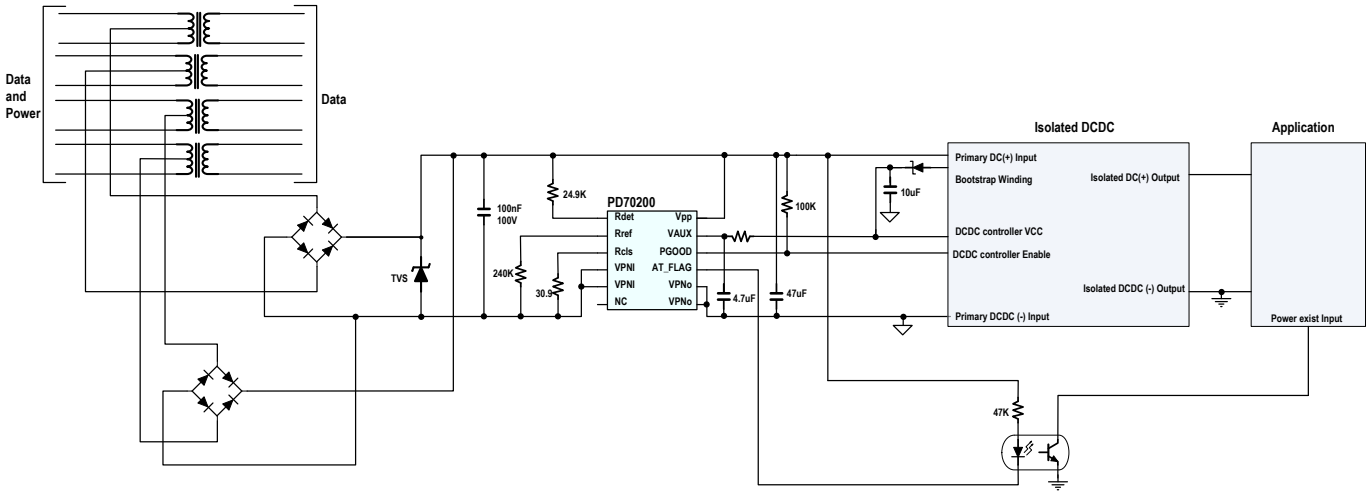


Figure 5: Typical 2 or 4 Pair Configuration with a Single PD70100/PD70200 IC

In a four pairs system, dual PD70100/PD70200 ICs are placed in a PD design, each driven by a separate diode bridge. Positive voltage at V_{PP} and Isolation Switch output at VPN_{OUT} are combined in parallel for each PD70100/PD70200 IC. The parallel output terminals drive the input filter/bulk capacitor for the DC/DC converter. This affectively doubles the total input power capability to the DC/DC converter.

External components requirements for the four pairs system are same as for the two pairs configuration. Under certain conditions, power available at the PI may be on two pairs only. If the AT flag should be used for by the application for its operation, it should be ORed using a common cathode diode. Providing DC/DC start-up under all possible power input configurations.

In the case of 4 pair configuration, V_{AUX} regulator output will not be used. A simple linear regulator should be used. The regulator is comprised of a zener diode of 14V, N channel FET, and a 24.9K resistor. A high power diode should be connected between VPNo pins of each device and DCDC.

A two PD70200 configuration for supporting 4 pairs PSE that has two independent AT channels (Not synchronized), is outlined in Figure 6.

Note:

A single PD70210/A device should be used for supporting a 4 pairs PSE that has two synchronized ports.

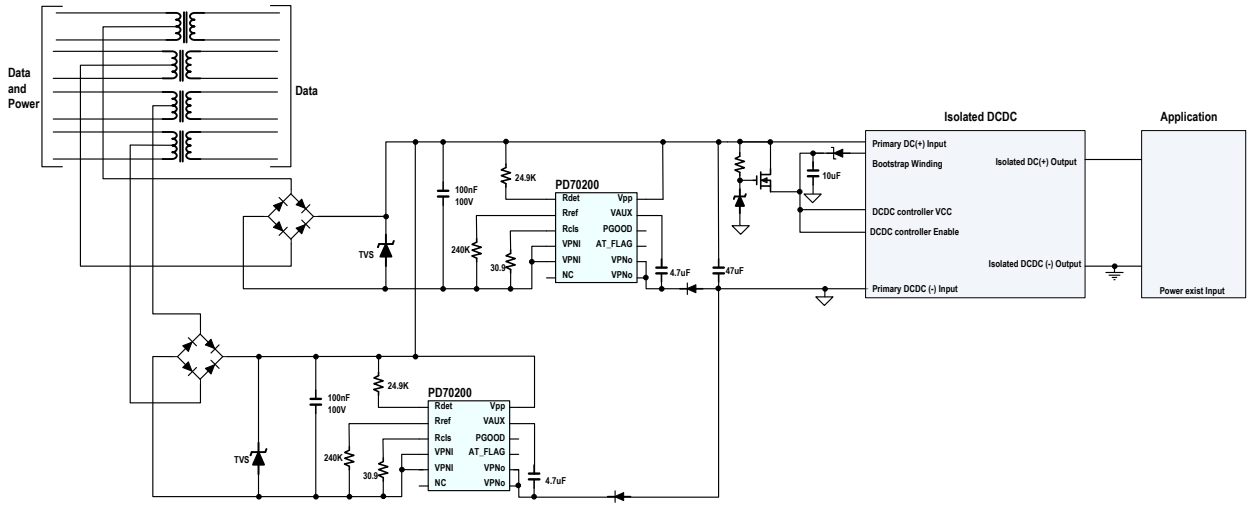


Figure 6: dual PD70200 configuration for supporting non sync detection 4P PSE

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

Operation with an External (non POE) DC Source

PD applications utilizing PD70100/PD70200 IC may be operated with an external power source (DC wall adaptor). There are three methods of providing power with an external source:

1) External source connected directly to PD70100/PD70200 Input (VPP to VPN_{IN}). Requires external source output voltage to be 40V minimum under all load conditions. Adaptor must be isolated from VPP or VPN_{IN} either through a switched connection or a diode.

2) External source connected directly to PD70100/PD70200 output connection to the application. External source output voltage will be dependent on application input requirements. External source must be isolated from VPP or VPN_{OUT} either through a switched connection or a diode pair. If the application involves driving the input of a DC-DC converter controller whose VCC supply rail is bootstrapped to the converter output, a low power external linear regulator circuit must be supplied. That's because PD70100/PD70200 V_{AUX} supply will not function while powering the application with an external source in this configuration. This statement is also true for PD70100/PD70200 P_{GOOD} function. Any application use of P_{GOOD} function will need to be accounted for, as P_{GOOD} output will not function while powering the application with an external source in this configuration. If required, the additional linear regulator circuit and P_{GOOD} circuit will depend on application requirements.

3) External source connected directly to application's low voltage supply rails (output side of an isolated or non-isolated power supply). External source must be isolated from application power supply's output either through a switched connection, a diode pair, or a separate regulator that sources current only (does not sink current).

PD70100/PD70200 configured with an external wall adaptor is diagrammed in Figure 7 to Figure 9.

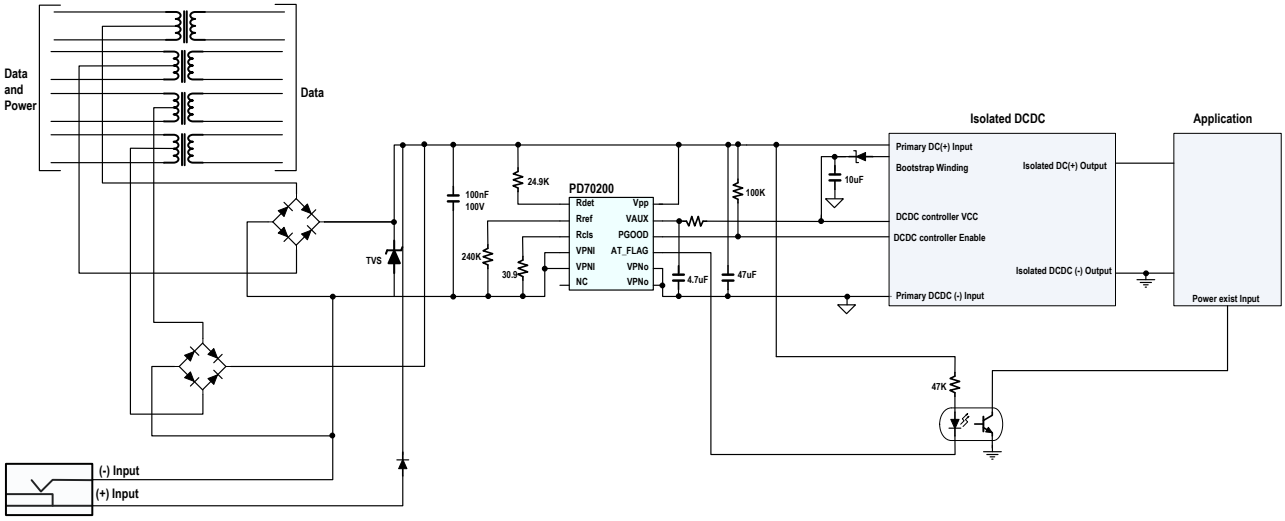


Figure 7: External Power Input connected to PD70200 Input- Power OR using series Diode

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

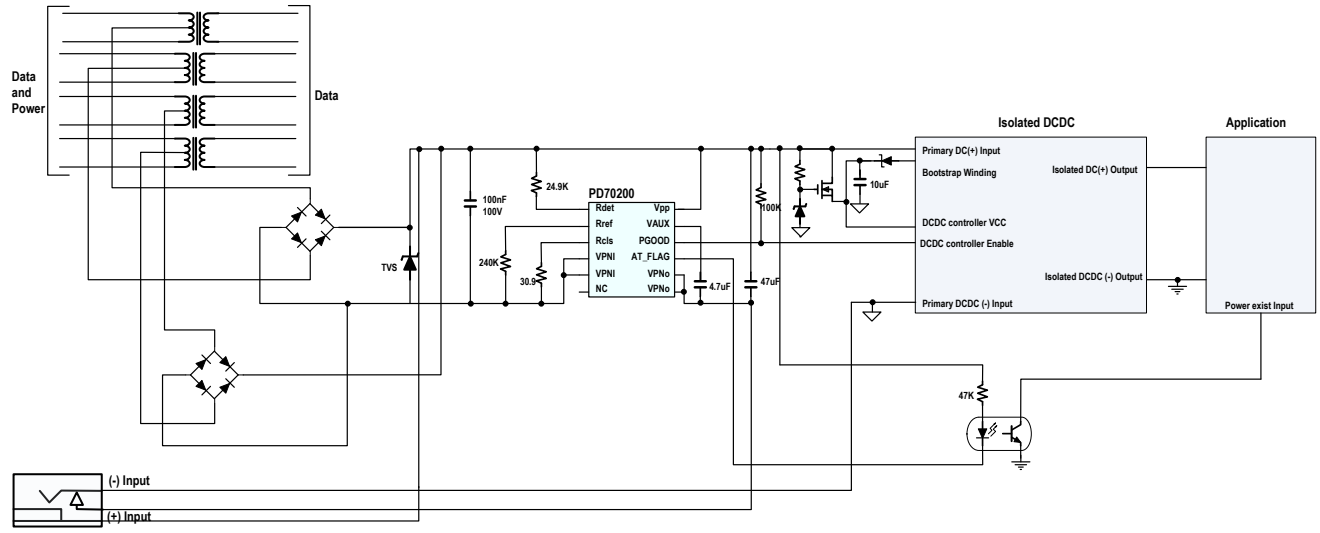


Figure 8: External Power Input connected to PD70200 Output – Switched Connection

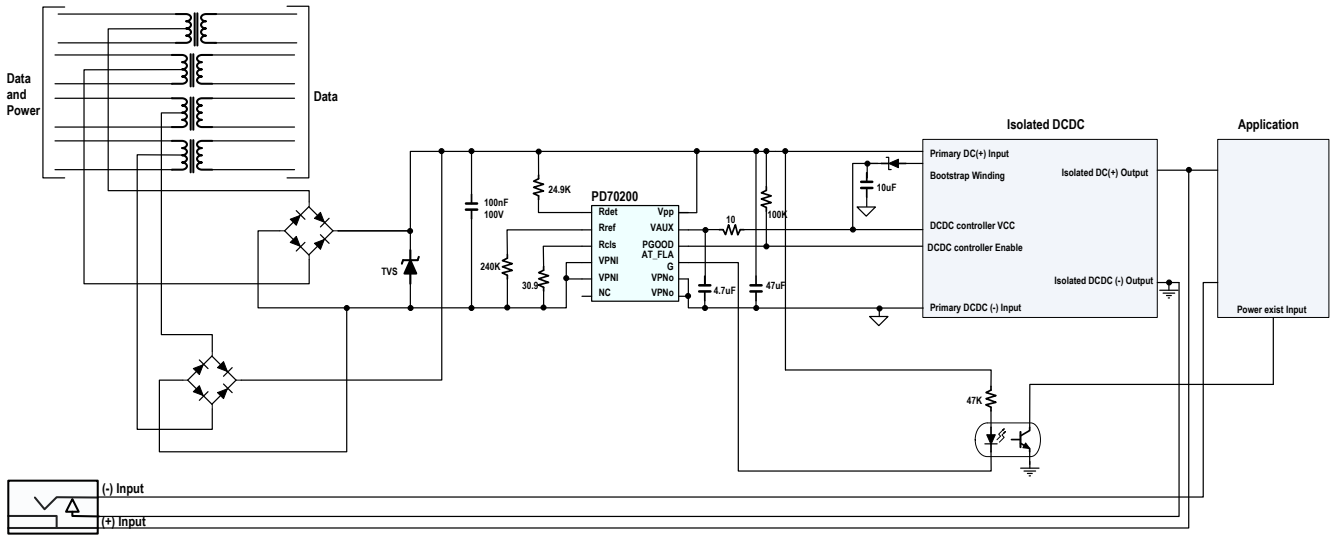


Figure 9: External Power Input connected to Application supply Rails – Switched Connection

General Circuit Description

Event Thresholds

PD70100/PD70200 IC switches between states based on voltage level differences between V_{PP} and VPN_{IN}.

Threshold levels between V_{PP} and VPN_{IN} are defined as follows:

- **V_{PP} - VPN_{IN} = 1.1V to 10.0V (Rising Voltage):** Detection resistor R_{DET} is connected between V_{PP} and VPN_{IN}.
- **V_{PP} - VPN_{IN} = 10.1V to 12.8V (Rising Voltage):** Detection Resistor R_{DET} is disconnected from VPN_{IN}.
- **V_{PP} - VPN_{IN} = 11.1V to 13.5V (Rising Voltage):** Classification current source is connected between V_{PP} and VPN_{IN}. This threshold establishes the programmed current draw set by R_{CLASS}. Current magnitude sets class level per IEEE 802.3af or IEEE 802.3at. This function is optional for IEEE 802.3af compliant PDs and mandatory for IEEE 802.3at compliant PDs. There is a minimum 1V hysteresis between Enable and Disable thresholds of classification current source. Classification current source remains connected during VPP rising voltage up to 20.9V.
- **V_{PP} - VPN_{IN} = 20.9V to 23.9V (Rising Voltage):** Classification current source is disconnected from VPN_{IN}.

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

- **V_{PP} - VPN_{IN} = 4.9V to 10.1V (Falling Voltage):** This is the Mark voltage range. IC will recognize V_{PP} - VPN_{IN} voltage falling from Classification current source connect threshold (11.1V to 13.5V) to Mark threshold as one event of the 2 Events Classification Signature. Two events will cause PD70200 IC to set AT_FLAG pin to its active low state. This function is available on PD70200 only.
- **V_{PP} - VPN_{IN} = 36V to 42V (Rising Voltage):** Isolation switch is switched from Off to Low Current Soft Start mode. In Soft Start mode the isolation switch limits the DC current to 240mA (typical). The current limit circuitry during Soft Start mode monitors the voltage difference across the isolation switch (VPN_{OUT} - VPN_{IN}) and maintains Soft Start current while (VPN_{OUT} - VPN_{IN}) > 0.7V. When VPN_{OUT} - VPN_{IN} drops to 0.7V or below, isolation switch Soft Start current limit is disabled, V_{AUX} is enabled, P_{GOOD} and AT_FLAG are asserted, and the isolation switch is fully turned on with 2A (max) overcurrent protection.
- **V_{PP} - VPN_{IN} = 31V to 34V (Falling Voltage):** Isolation switch is switched off at this threshold, establishing high impedance between VPN_{IN} and VPN_{OUT}. Bulk capacitor discharge function is enabled, and stays enabled as long as difference between voltages V_{PP} and VPN_{OUT} remains between 1.5V and 32V.
- **V_{PP} - VPN_{IN} = 2.45V to 4.85V (Falling Voltage):** Detection resistor R_{DET} is reconnected at this threshold (falling V_{PP} voltage only). R_{DET} is disconnected when V_{PP} - VPN_{IN} voltage drops below 1.1V.

Soft Start Current Limit

PD70100/PD70200 IC provides Soft Start current limiting. A rising voltage of 36V to 42V between V_{PP} and VPN_{IN} will enable isolation switch in Soft Start Current Limit mode. During this time, the current through isolation switch is limited to 240mA (typical). PD70100/PD70200 IC continuously monitors the voltage drop across isolation switch (VPN_{OUT} to VPN_{IN}) during Soft Start mode. When difference between voltages VPN_{OUT} and VPN_{IN} drops below 0.7V, PD70100 /PD70200 IC will switch to normal operating mode, in which isolation switch is fully on, with over-current protection circuitry active.

Soft Start current limit is necessary for limiting the inrush current created by initial charge-up of input capacitors upon system start-up. Large inrush currents can create large voltage sags at PI, which in turn can cause system functions tied to event thresholds (such as AT_FLAG) to reset to their initial states. Soft Start current limit will significantly reduce voltage sag upon start-up.

PD70100/PD70200 IC Soft Start function limits current to a maximum of 320mA (240mA typical). Start-up into a fully discharged bulk capacitor will result in large power dissipation in the isolation switch for a period of time dependent on the size of the bulk capacitance. This occurs due to the initial voltage drop across the isolation switch. Maximum initial voltage drop across isolation switch can be of 42V. In other words, initial power dissipation of the isolation switch can be no higher than 13.4W (42V x 320mA). Maximum power dissipated by the isolation switch will decrease as the bulk capacitor charges, eventually decreasing to a maximum normal operating power dissipation of 74mW (PD70100) or 311mW (PD70200). The period of time required to switch from Soft Start mode to normal operation mode can be calculated using the following formula:

$$T = \frac{(\Delta V - 0.7) \times C}{I}$$

Whereas:

I = PD70100/PD70200 IC's current during soft start

C = Total input bulk capacitance

ΔV = Initial VPN_{OUT} - VPN_{IN} voltage at start of soft start ($\Delta Vmax = V_{PP}$)

PD70100/PD70200 IC can safely operate with a total bulk capacitance of 220µF.

Bulk Capacitor Discharge

PD70100/PD70200 IC provides discharge of the application bulk capacitor when V_{PP} - VPN_{IN} falling voltage drops below the isolation switch turn-off threshold (31V to 34V). This feature insures that the application bulk capacitance does not discharge through the detection resistor, which can cause detection signature to fail and prevent PSE from starting the PD. While enabled, discharge function provides a minimum controlled discharge current of 22.8mA, which flows through VPP pin, internally through isolation MOSFET's body diode, and out through VPN_{OUT} pin. Discharge circuitry monitors voltage difference between V_{PP} - VPN_{OUT}, and remains active while difference voltage is 1.5V ≤ (V_{PP} - VPN_{OUT}) ≤ 32V. Maximum time to discharge can be calculated by:

$$T = \frac{(\Delta V - 1.5V) \times C}{0.0228}$$

Whereas:

C = Total Input Bulk Capacitance

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

ΔV = Initial V_{PP} - VPN_{OUT} Voltage at Isolation Switch Turn-off

Example: Assuming an initial capacitor voltage of 32V, it will take 294ms for a 220µF capacitor to discharge to a 1.5V level.

PD70100/PD70200 discharge circuitry can be safely operated with a bulk capacitance of up to 220µF.

Auxiliary Voltage – V_{AUX}

PD70100/PD70200 IC has an available regulated voltage output, V_{AUX}, to be used primarily as a start-up supply for an external DC/DC controller. V_{AUX} is a low current, low duty cycle output, providing current momentarily until an external bootstrap supply can take over.

V_{AUX} output is regulated at nominal 10.5V, and will supply a peak current of 10mA for 10ms. Continuous current is 2mA. Typically V_{AUX} output is connected to a bootstrapped supply of higher voltage (such as a rectified auxiliary output from an isolated DC/DC converter transformer). V_{AUX} output does not sink current. Once bootstrapped voltage exceeds V_{AUX} output voltage level, V_{AUX} output will no longer provide current and will be transparent to the operation of the DC/DC converter. It is recommended to design the rectified bootstrapped output under all operating conditions for a minimum output voltage of $12V_{DC}$.

During Soft Start mode or at isolation switch turn-off, V_{AUX} output is disabled due to falling V_{PP}. V_{AUX} regulated output is enabled only when isolation switch is in normal operation mode. This insures DC/DC controller does not start prematurely.

P_{GOOD} Output

PD70100 and PD70200 IC provide an open drain output indicating power good status. This output is in a high impedance state until V_{PP} - VPN_{IN} voltage exceeds isolation switch turn-on threshold, and isolation switch moves from Soft Start current limit mode to normal operation mode. Upon assertion, P_{GOOD} output switches to ground with a current sink capability of 5mA. When V_{PP} - VPN_{IN} voltage falls below the isolation switch turn-off threshold, P_{GOOD} output reasserts back to high impedance state.

This output may be used as an enable/disable control for a DC/DC converter to detect when PI voltage has fallen below IEEE 802.3af/at specified operating threshold. Alternatively, it can be used to guarantee Soft Start function is finished before DC/DC is allowed to start.

AT_FLAG Output (PD70200 only)

PD70200 IC provides an open drain output indicating a 2 Events Classification was detected. This output is in a high impedance state until the V_{PP} - VPN_{IN} voltage exceeds isolation switch turn-on threshold and isolation switch moves from Soft Start Current Limit mode to normal operation mode. It will then assert to low, but only if a 2 Events Classification Signature was recognized during Classification phase described earlier. Upon assertion, AT_FLAG output switches to ground with a current sink capability of 5mA. AT_FLAG output re-asserts back to high impedance state when V_{PP} - VPN_{IN} voltage falls below isolation switch turn-off threshold.

AT_FLAG signal is synchronized with P_{GOOD} signal. For example, P_{GOOD} can be asserted without asserting AT_FLAG, but AT_FLAG cannot be asserted without asserting P_{GOOD}.

AT_FLAG signal is typically used for indicating the PD application that PSE is capable of supplying AT power levels. PD application is often electrically isolated. AT_FLAG is referenced to the primary ground. As such, it requires an optoisolator to provide an isolation barrier between primary ground and application ground for electrically isolated applications.

Thermal Protection

PD70100/PD70200 IC provides thermal protection. Integrated thermal sensors monitor the internal temperatures of the isolation switch and classification current source. If the overtemperature threshold of either sensor is exceeded, that sensor's respective circuit will disable.

To insure trouble free operation, it's important to make sure PD70100/PD70200 IC's exposed pad is mounted to a copper area on the PCB that provides an adequate heatsink.

PCB Layout Guidelines

IEEE 802.3af/at standards specify certain isolation requirements which must be met by all POE equipment. Isolation is specified at 1500Vrms minimum between incoming Data and Power lines, and any signal, power or chassis connection that can come into contact by the end user outside the application. On a typical FR4 PCB, this requirement is generally satisfied by creating an isolation barrier of a minimum 0.08 inch (2mm) between adjacent traces requiring IEEE 802.3 1500Vrms isolation. For multilayer PCBs, 1500Vrms isolation requirement can be met between adjacent PCB layers by providing a minimum isolation thickness of 0.015 inch (0.4mm).

Any adjacent traces containing POE voltage potentials should be considered for proper creepage and clearance per IEC 60950.

Give PD70100/PD70200 PCB design special attention to provide adequate heatsinking of the exposed pad (VPN_{OUT}). PD70100/PD70200 IC's 12 pin DFN package utilizes the exposed pad to provide

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

thermal cooling of the package, and as such requires PCB design to include sufficient copper area attached to the exposed pad. For multilayer boards, conductive vias to an adjacent plane layer may be used. However, keep in mind that exposed pad is electrically connected to VPN_{OUT} and must be electrically isolated from VPN_{IN}, as well as secondary and chassis grounds per IEEE 802.3 specifications.

When using vias to provide thermal conductivity between a plane layer and exposed pad, barrels should be 12mils in diameter and (where possible) placed in a grid pattern with 47mils (1.2mm) center to center spacing. Barrel holes should be plugged or tented for proper solder paste release. When tented holes are used, solder mask inclusion area should be 4mils (0.1mm) larger than via barrel.

A recommended footprint for PD70100/PD70200 and via placement example is diagrammed in Figure 10 and Figure 11.

For single or dual layer boards you should use large copper fills in direct contact with the exposed pad. Copper thickness of 2Oz will improve thermal performance. If using copper traces of less than 2Oz, it is recommended to increase overall trace thickness by adding excess solder to trace areas where appropriate.

PCB design should provide wide, heavy copper traces for high current power lines. A 4 pair, extended power PD can have maximum trace currents of ~1.2A for the VPP and VSS input terminals. Traces carrying current for VPP, VPN_{IN}, and VPN_{OUT} should be sized to provide the lowest temperature rise practical at the maximum current. For example, a minimum of 15 mils wide 2Oz copper will accommodate up to 1.6A current with a maximum 10°C temperature rise. If using copper traces of less than 2Oz, increase the minimum width to accommodate maximum current with lowest temperature rise.

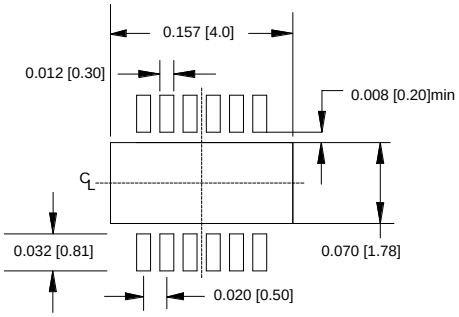


Figure 10: Recommended Footprint for PD70100/PD70200 (Dimensions in [] = mm)

POE signals contain voltages up to 57Vdc. Component working voltage must be considered, and components sized accordingly. Surface mount resistors are a good example: 0402 and 0603 resistors have typical maximum working voltage specifications of 50V, whereas 0805 resistors are typically specified at 150V. For PD70100/PD70200 ICs, pull-up resistors connected to AT_FLAG and P_{GOOD} are the only resistors which are subjected to full POE voltage levels. These resistors must be sized to accommodate 57V; it is recommended to size these components for 150V.

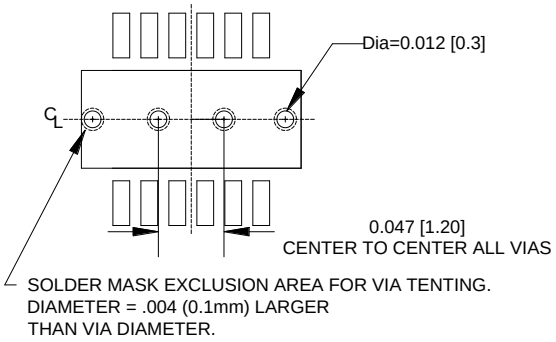


Figure 11: Recommended Thermal Via Placement (Dimensions in [] = mm)

When used with PD70100/PD70200 IC, detection resistor R_{DET} is only connected at POE voltages up to 12.8V, and is disconnected otherwise. 24.9K R_{DET} resistor may be a low voltage type when used with PD70100/PD70200 IC's R_{DET} pin. For applications which have an unswitched detection resistor, detection resistor must be sized for 57V or greater.

Application Examples

Reference designs for both 4 pair and 2 pair applications can be found on the following pages.

The examples shows a single PD70200 configuration and dual PD70200 configuration.

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

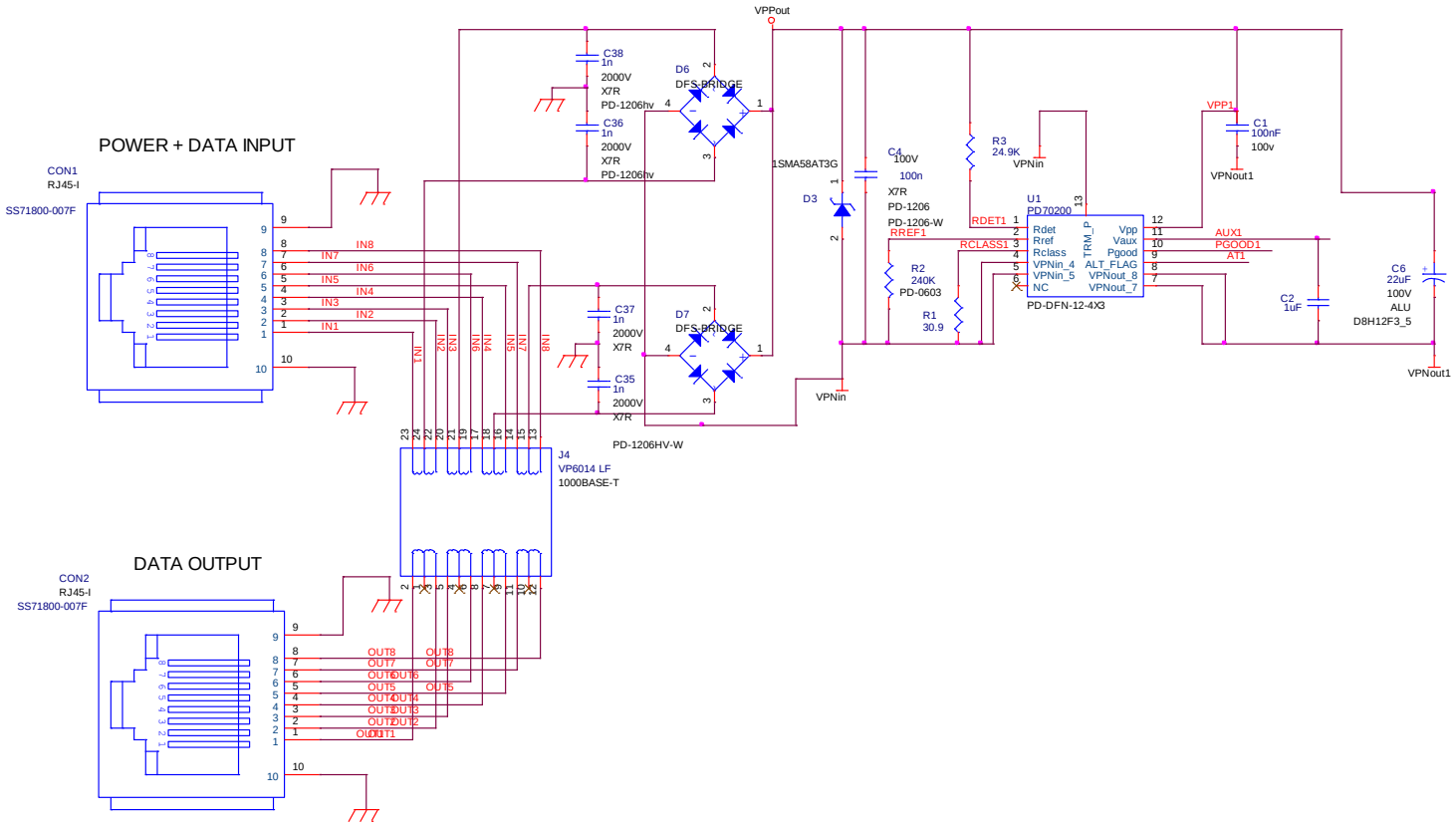


Figure 12: Schematic – PD70200 front end for Type 2 IEEE 802.3at Design

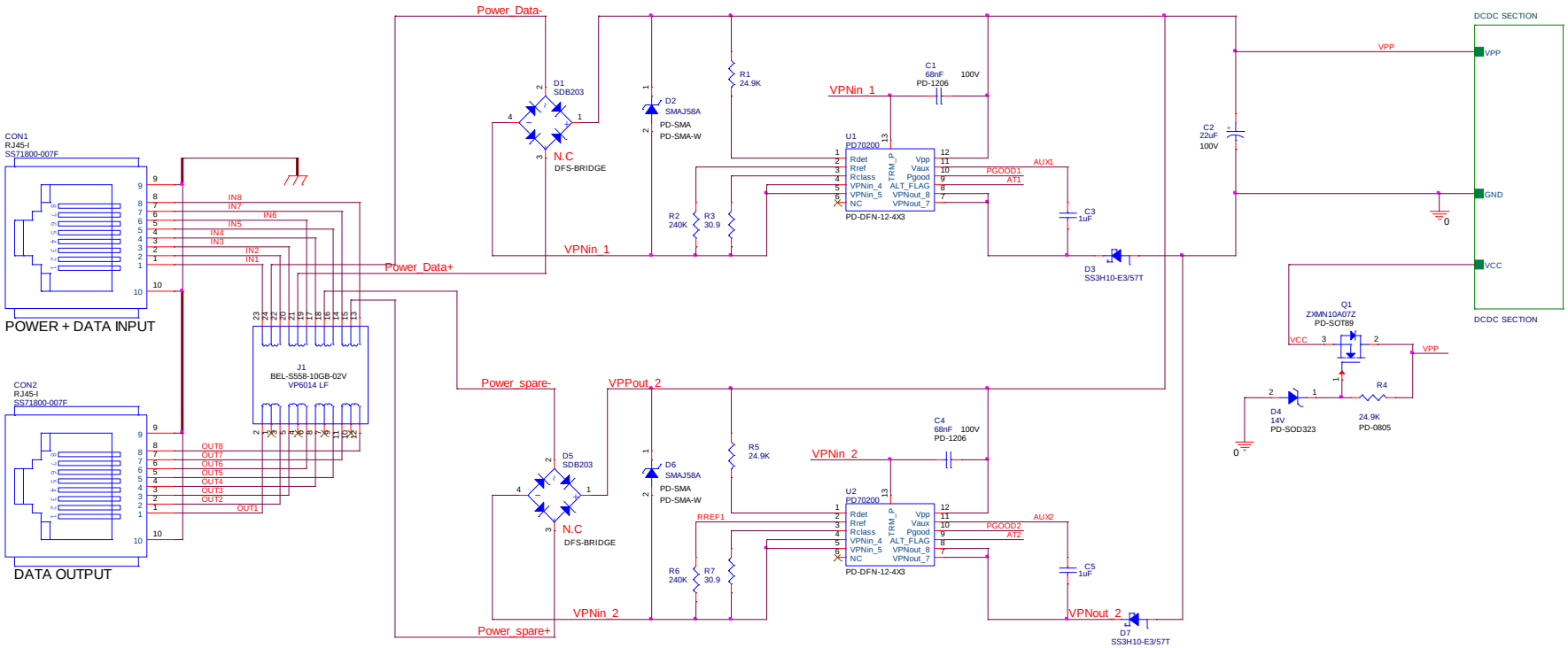


Figure 13: Schematic - 4 Pair Front End Design using dual PD70200 supporting PSE having two independent ports

Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Phone (USA): (800) 713-4113, (ROW): (949) 221-7100 Fax: (949) 756-0308

Revision History

Revision Level / Date	Para. Affected	Description
0.1/ 11/4/10		Originate
0.2 2/2/11	All	All Figures & Pin numbers
1.0 2/9/12	All	update
1.1 7/10/14	two PD70200 configuration. Design example.	Update description. Remove 23W schematic design example.
1.2 10/02/2015	Figure 5-9	Figure fix, Change IC PN from PD70100A to PD70100

For support contact: sales_AMSG@microsemi.com

Visit our web site at: www.microsemi.com **Catalog Number**: 06-0129-080