Total Ionizing Dose Test Report

No. 22T-RT4G150-CQ352- K7HWA

January 25, 2022

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I. SUMMARY TABLE

Table. 1. Summary

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO_2)
2. Power Supply Current	Passed 125 krad(SiO_2)
3. Input Threshold (VIL/VIH)	Passed 125 krad(SiO_2)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO_2)
5. Propagation Delay	Passed 125 krad(SiO_2) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the Automatic Test Equipment (ATE) program. The report summarizes sample pins.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters.

Table. 2. DUT and Irradiation Parameters

Part Number	RT4G150
Package	CQ352
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	K7HWA
Quantity Tested	6
Serial Number (Dose)	07249 (125 krad), 07276 (125 krad), 07287 (125 krad), 07304 (125 krad), 07315 (125 krad), 07318 (125 krad)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

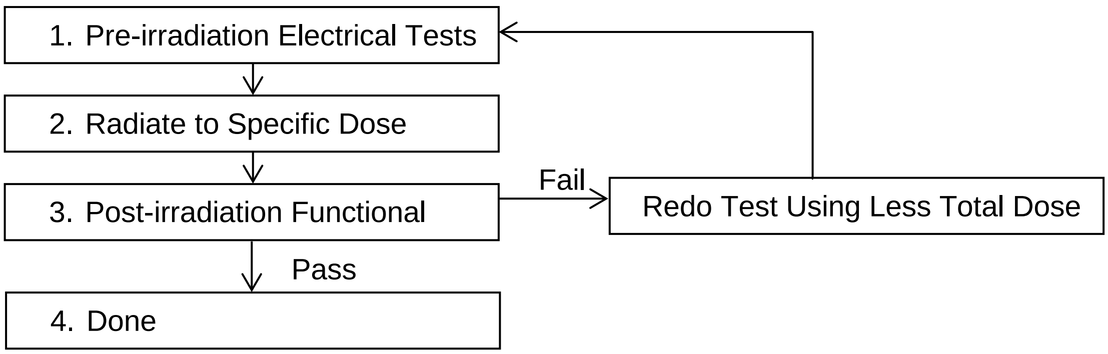

Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 3. Fabric Functional Coverage

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump and PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design. LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents are reported.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-25 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL.

Table. 4. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
07249	125 krad	0.2762	0.2927	5.97
07276	125 krad	0.2768	0.3022	9.18
07287	125 krad	0.2392	0.2635	10.16
07304	125 krad	0.2781	0.3073	10.50
07315	125 krad	0.2718	0.3079	13.28
07318	125 krad	0.2948	0.3403	15.43

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI\_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
07249	125 krad	0.0053	0.0058	9.43
07276	125 krad	0.0053	0.0058	9.43
07287	125 krad	0.0053	0.0056	5.66
07304	125 krad	0.0053	0.0058	9.43
07315	125 krad	0.0053	0.0058	9.43
07318	125 krad	0.0056	0.0060	7.14

Table. 6. Pre-irradiation and Post-irradiation $I_{DDI\_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
07249	125 krad	0.0204	0.0230	12.75
07276	125 krad	0.0201	0.0220	9.45
07287	125 krad	0.0202	0.0255	26.24
07304	125 krad	0.0201	0.0236	17.41
07315	125 krad	0.0202	0.0250	23.76
07318	125 krad	0.0206	0.0240	16.50

Table. 7. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
07249	125 krad	0.0031	0.0034	9.68
07276	125 krad	0.0031	0.0032	3.23
07287	125 krad	0.0031	0.0041	32.26
07304	125 krad	0.0031	0.0034	9.68
07315	125 krad	0.0030	0.0032	6.67
07318	125 krad	0.0032	0.0031	-3.13

The following figures (2-25) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

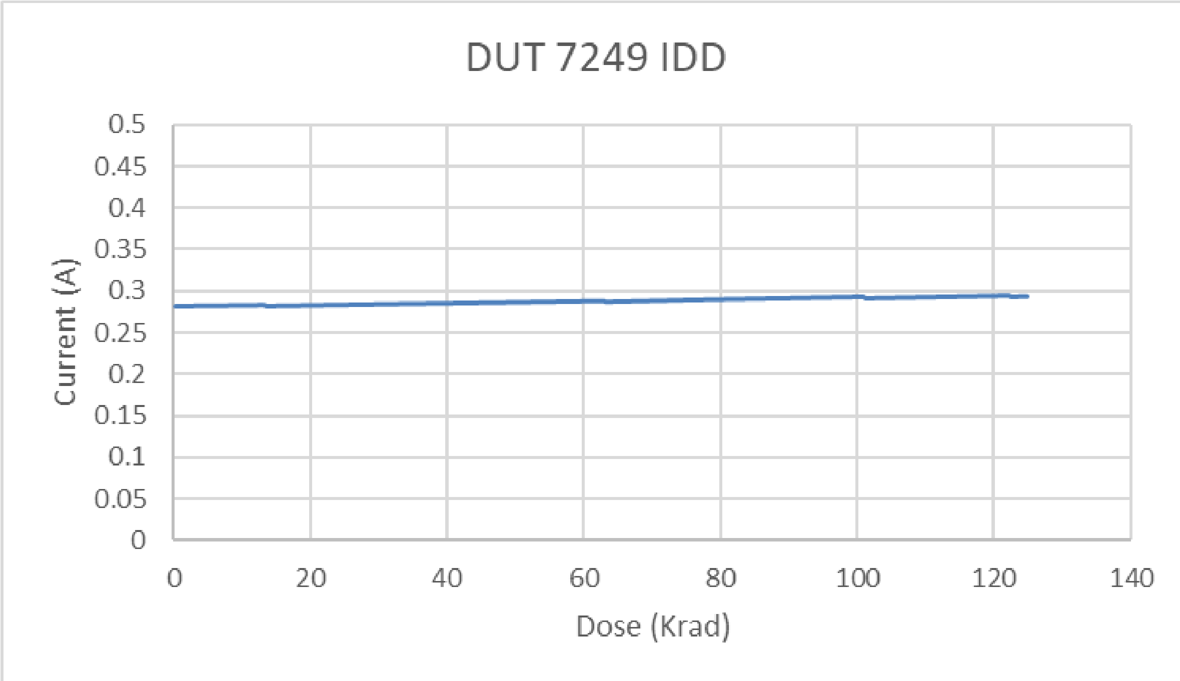

Fig. 2. DUT 07249 core power supply current (I_{DD}) versus TID

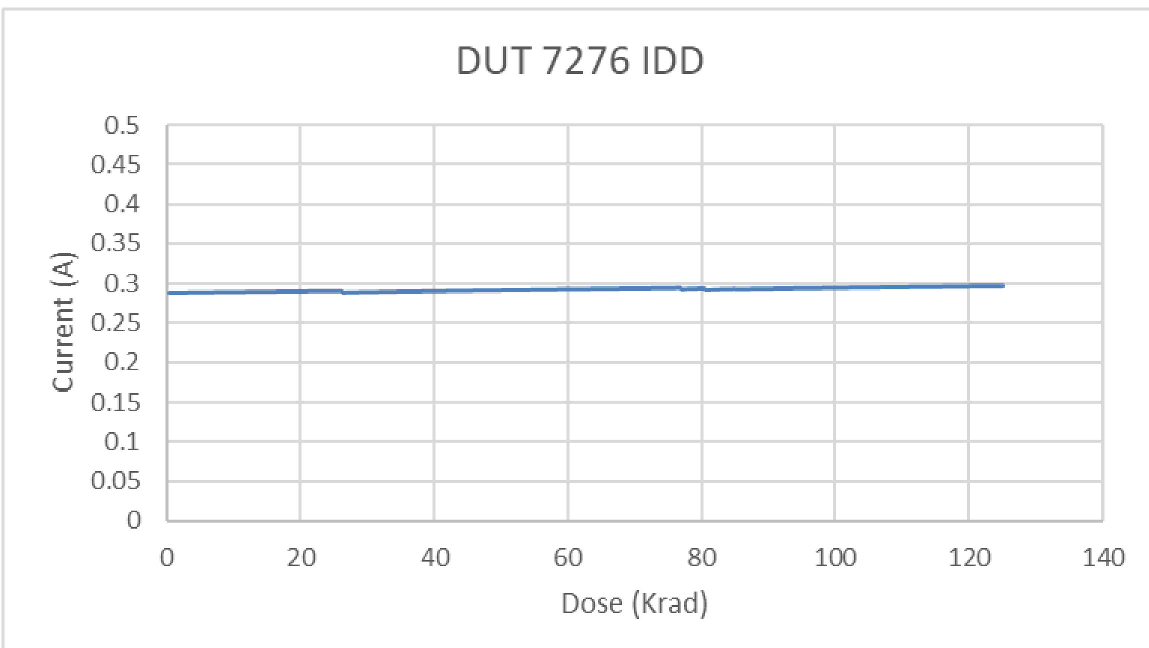

Fig. 3. DUT 07276 core power supply current (I_{DD}) versus TID

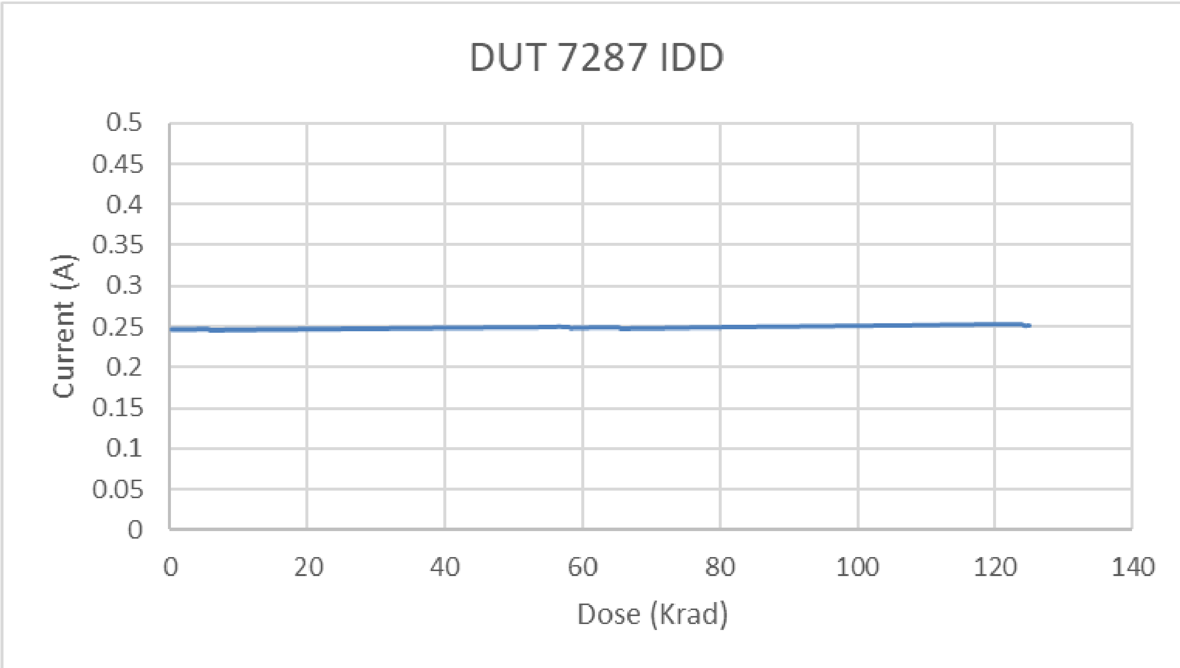

Fig. 4. DUT 07287 core power supply current (I_{DD}) versus TID

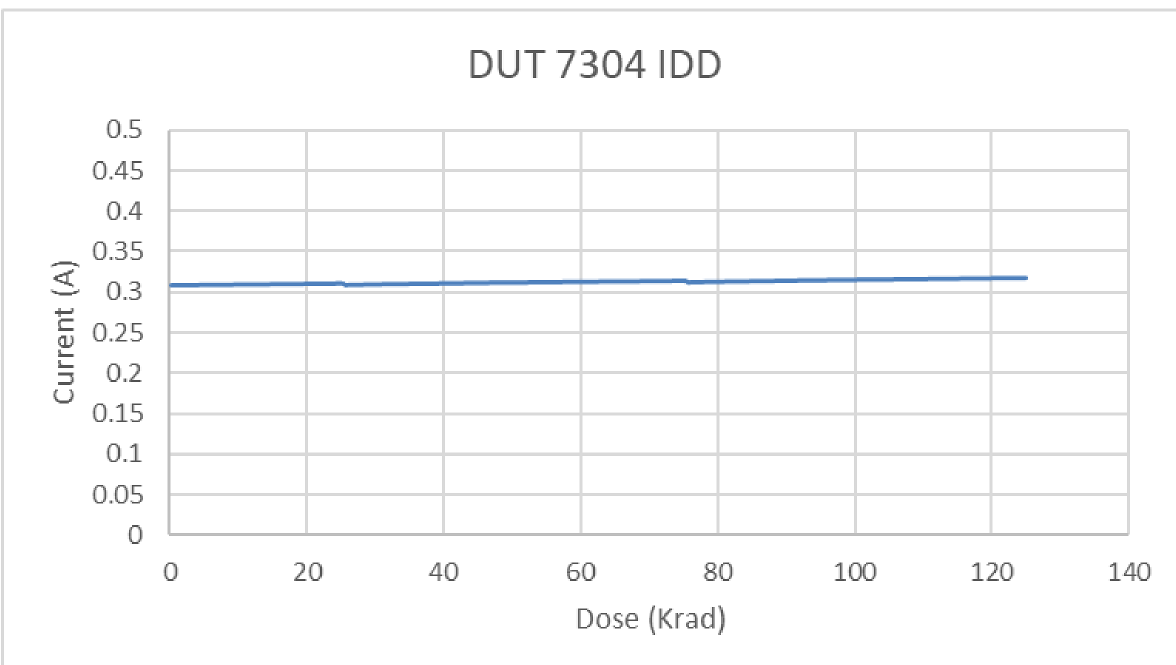

Fig. 5. DUT 07304 core power supply current (I_{DD}) versus TID

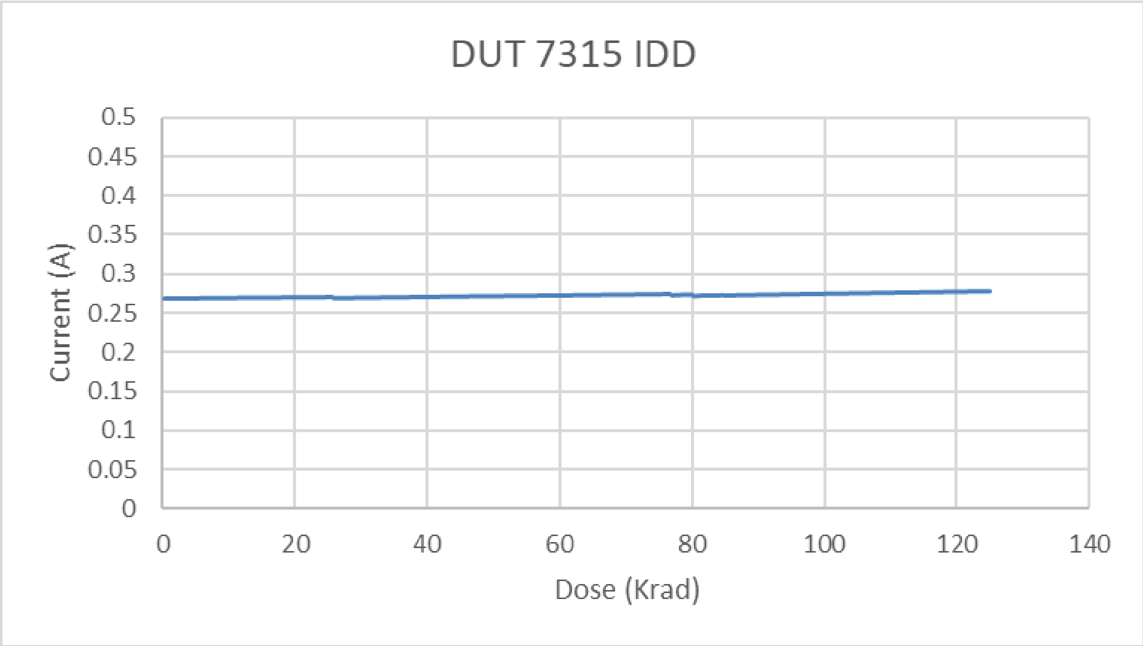

Fig. 6. DUT 07315 core power supply current (I_{DD}) versus TID

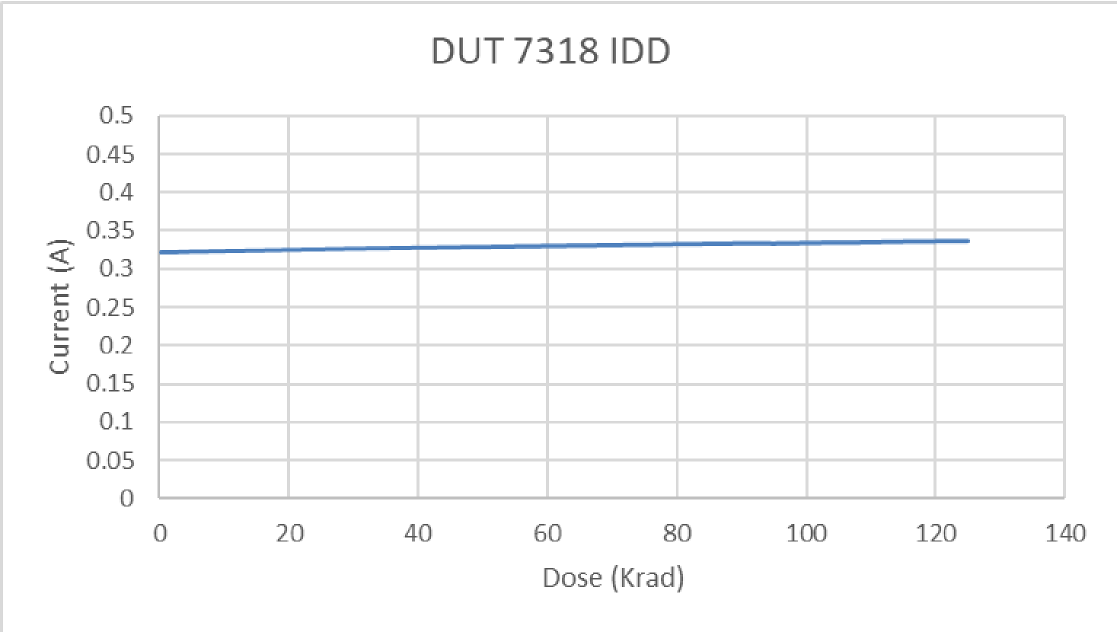

Fig. 7. DUT 07318 core power supply current (I_{DD}) versus TID

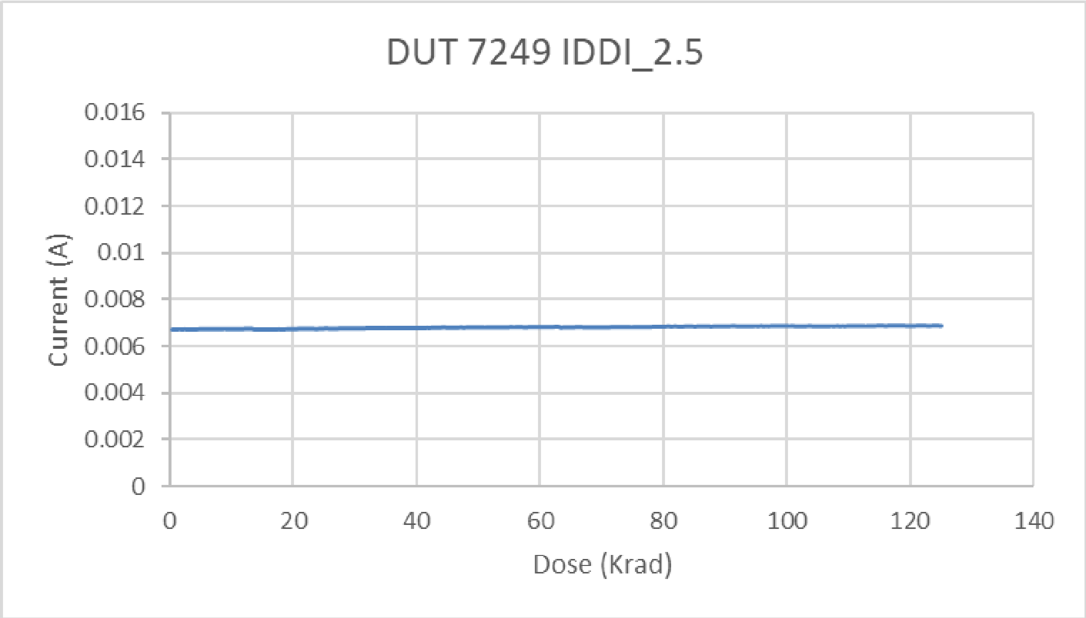

Fig. 8. DUT 07249 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

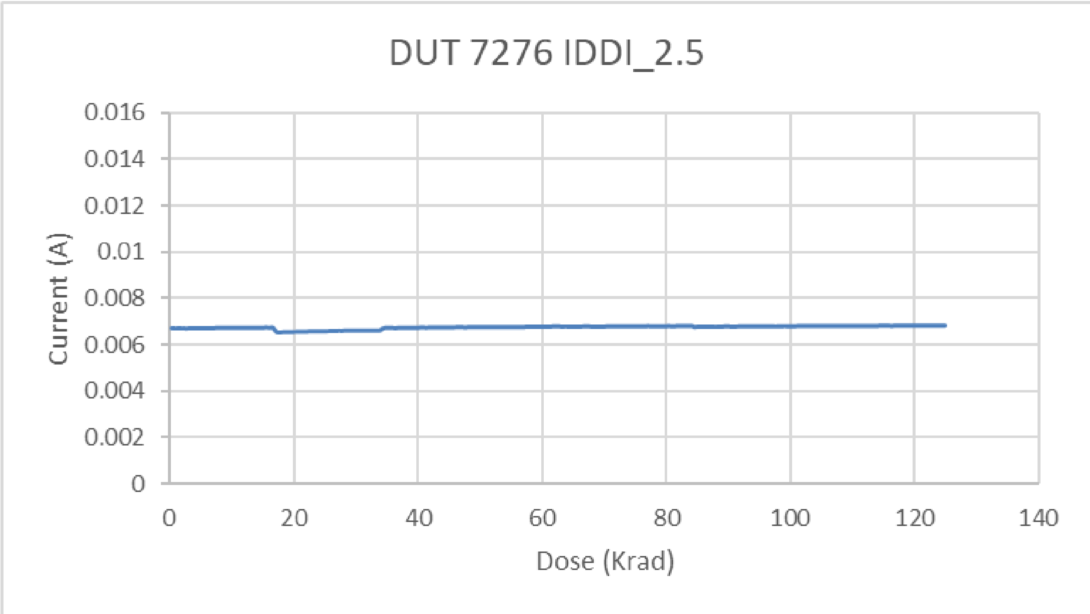

Fig. 9. DUT 07276 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

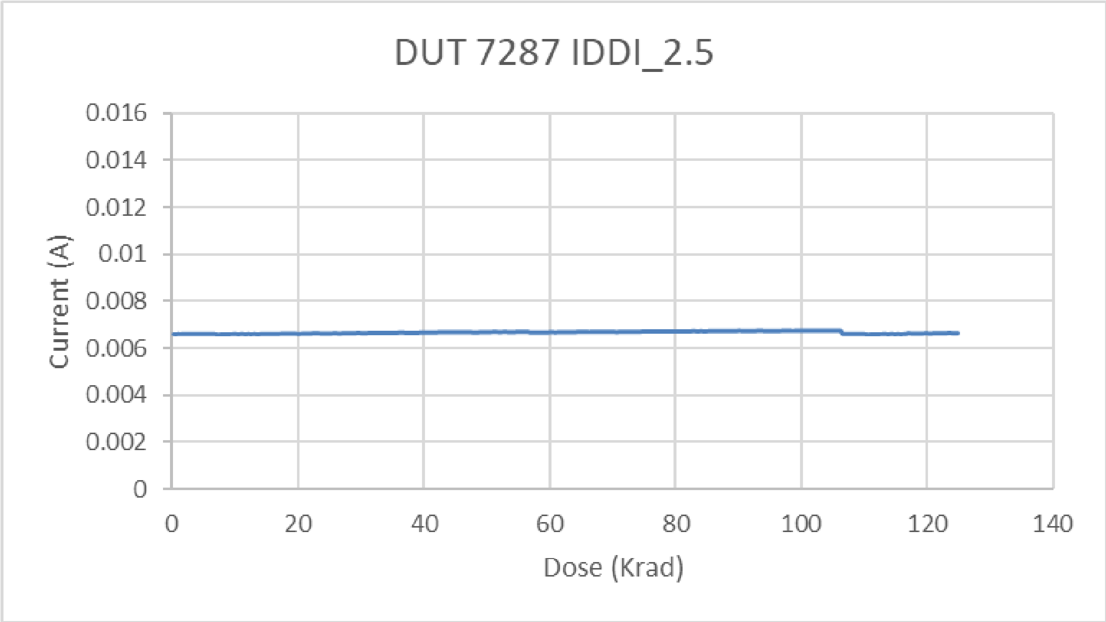

Fig. 10. DUT 07287 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

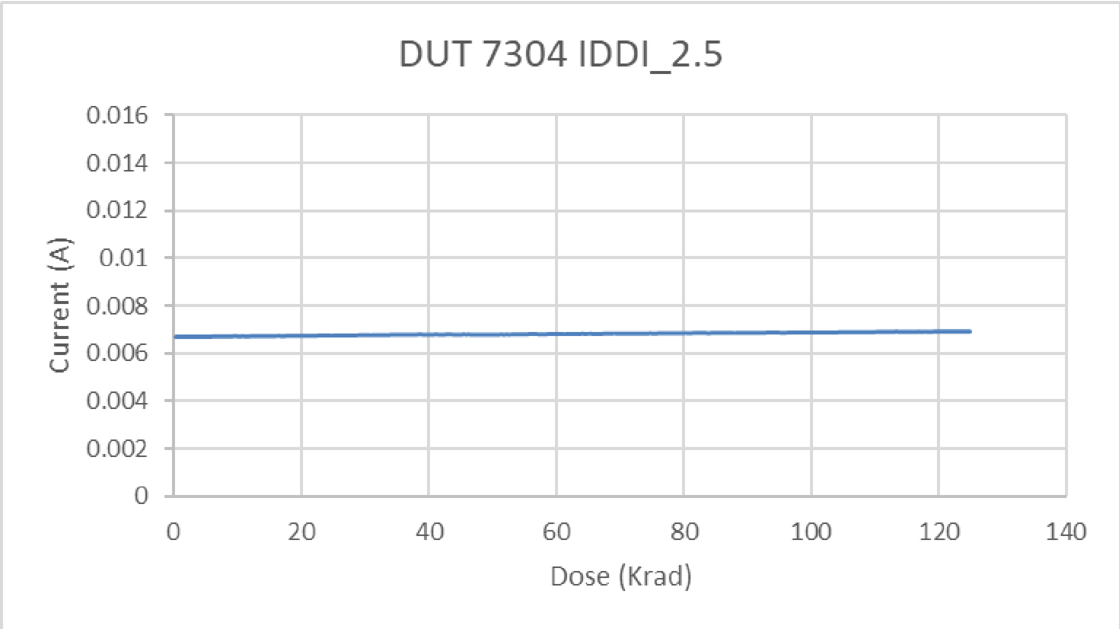

Fig. 11. DUT 07304 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

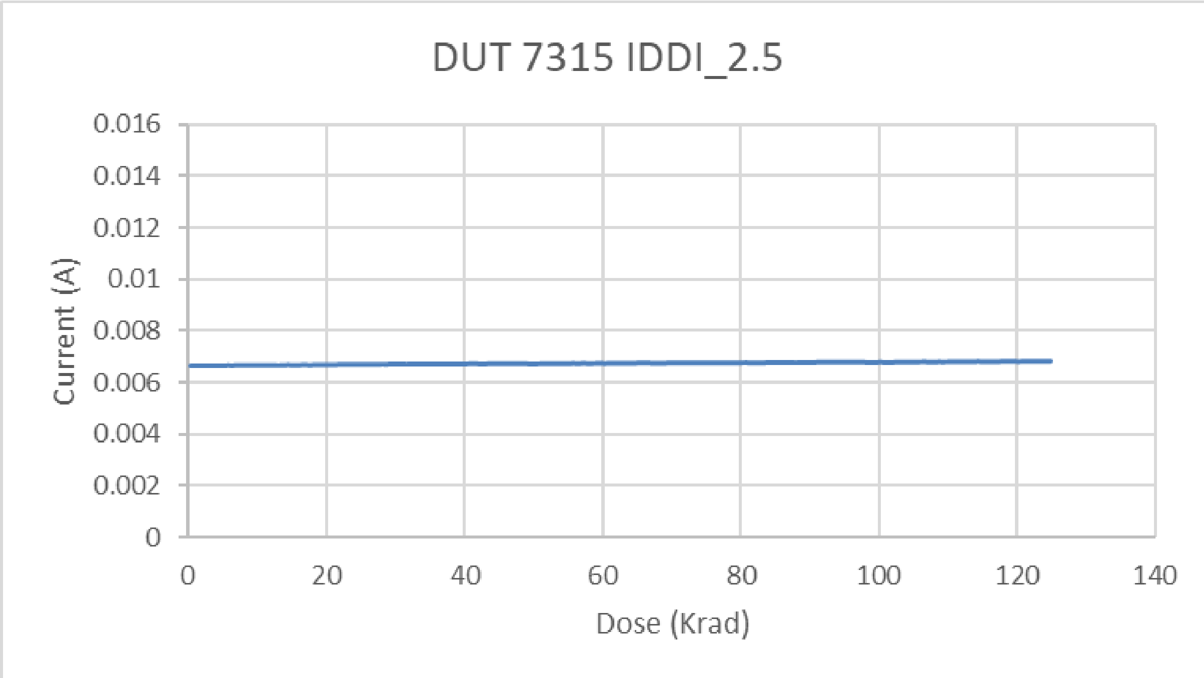

Fig. 12. DUT 07315 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

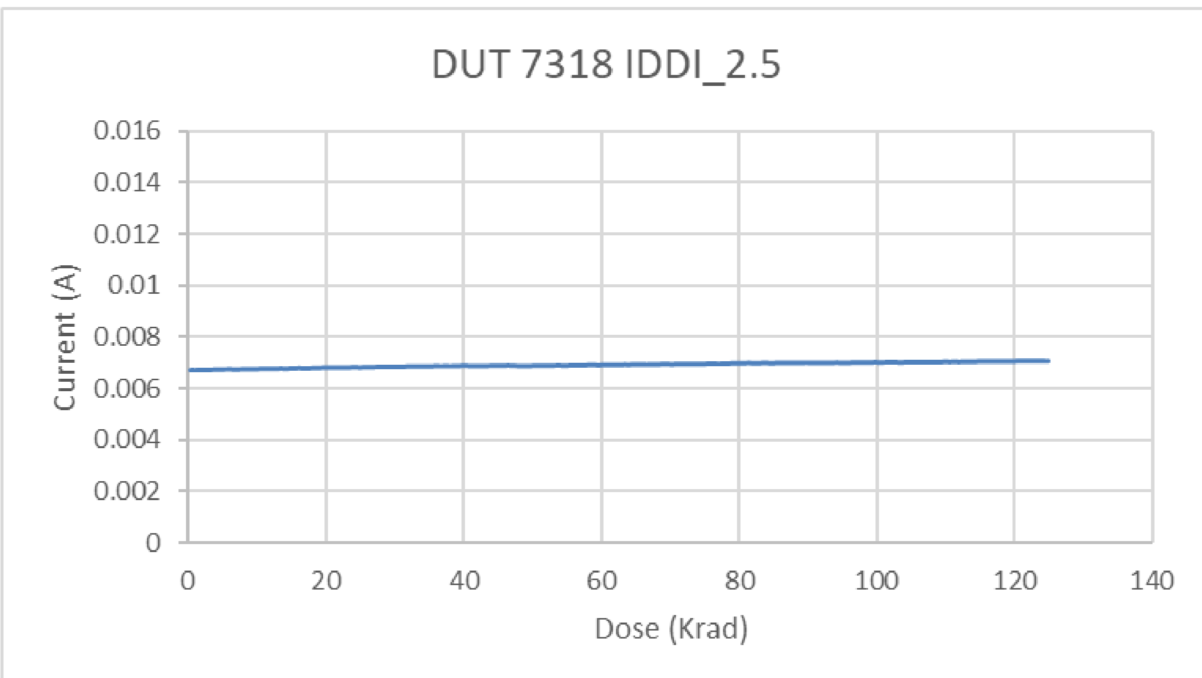

Fig. 13. DUT 07318 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

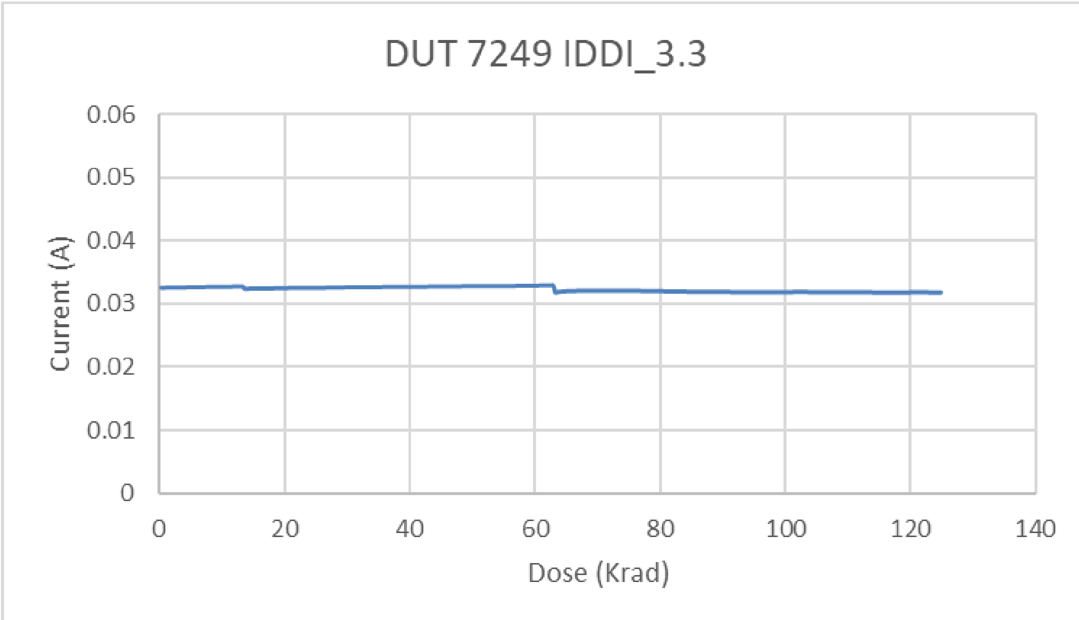

Fig. 14. DUT 07249 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

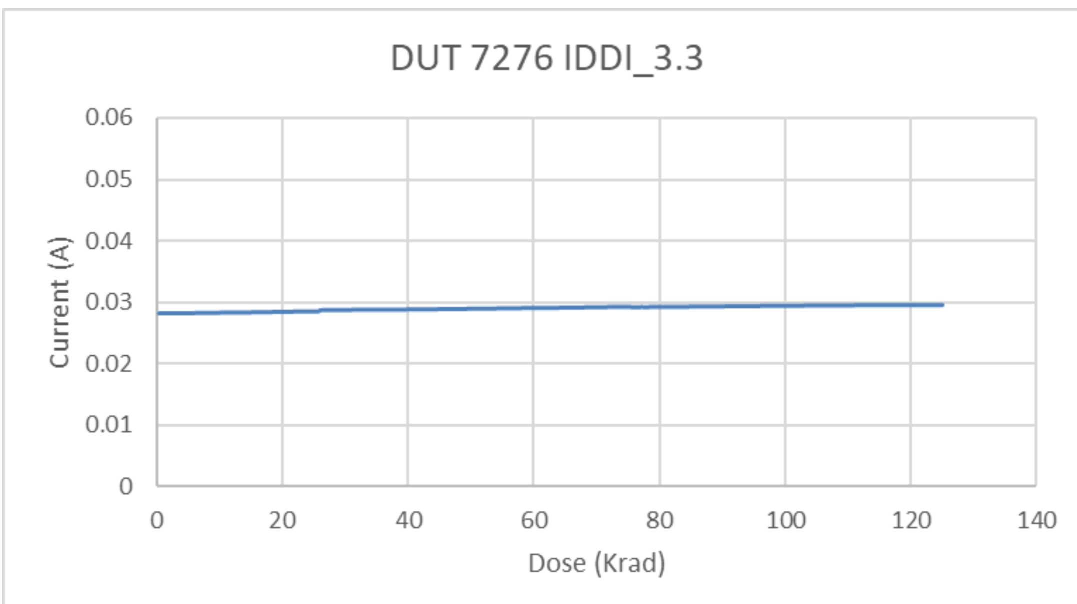

Fig. 15. DUT 07276 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

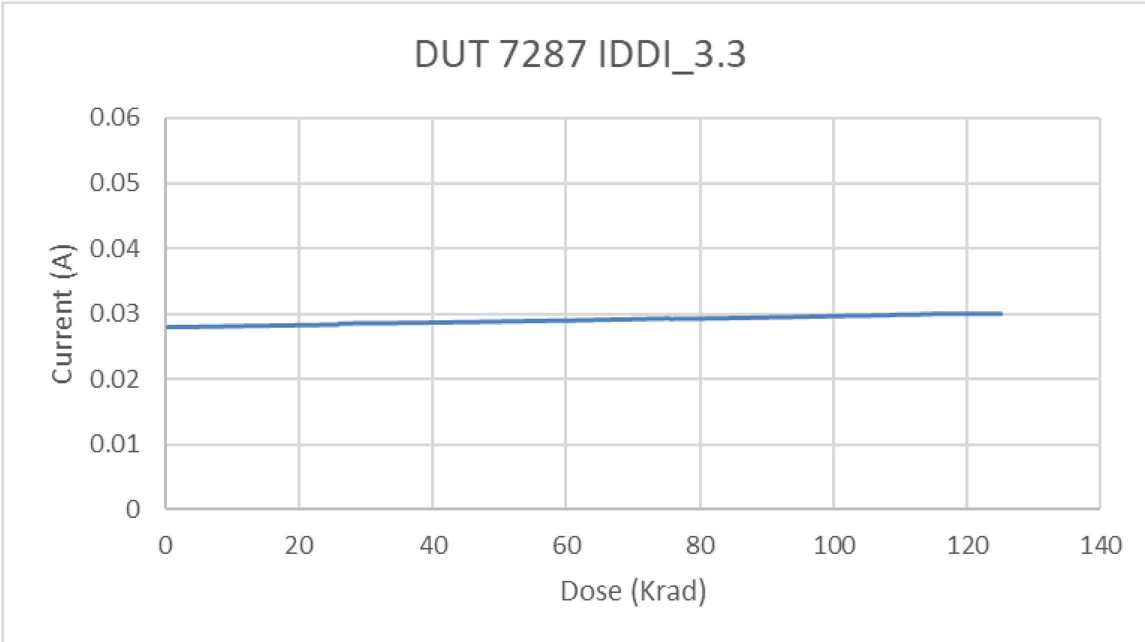

Fig. 16. DUT 07287 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

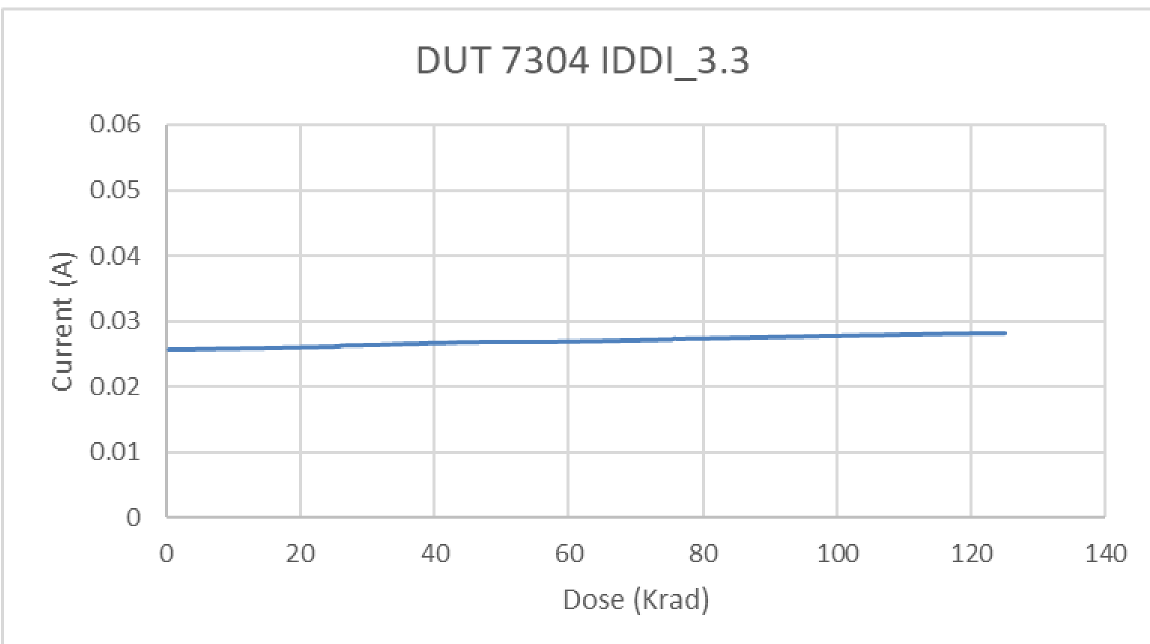

Fig. 17. DUT 07304 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

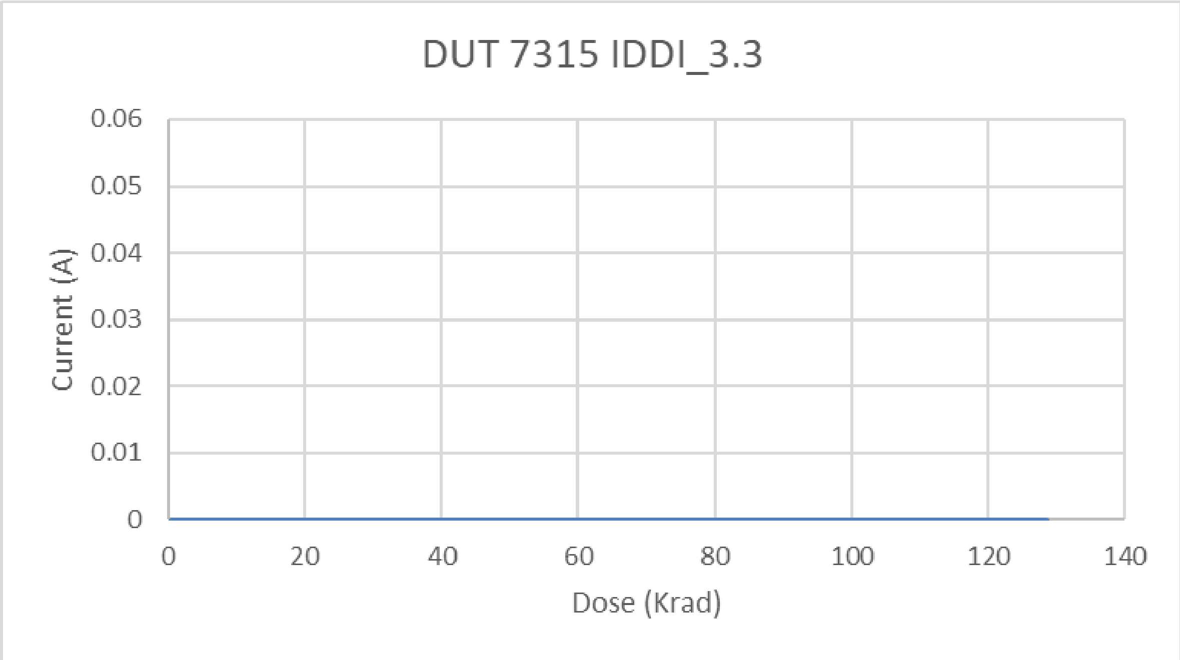

Fig. 18. DUT 07315 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

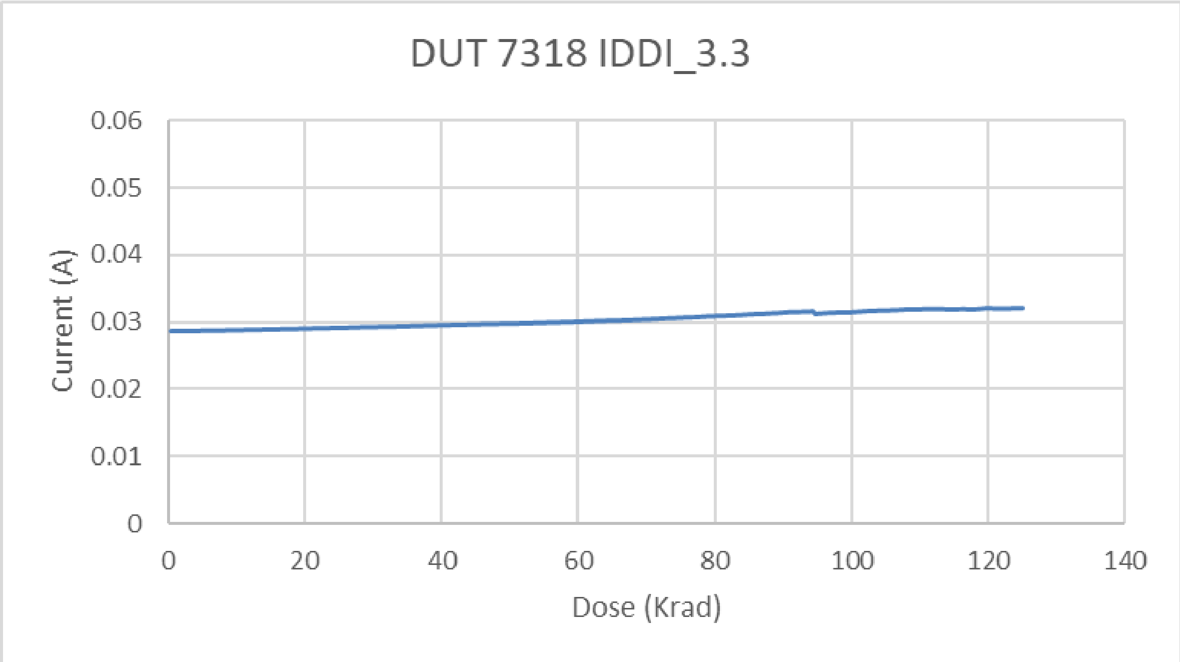

Fig. 19. DUT 07318 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

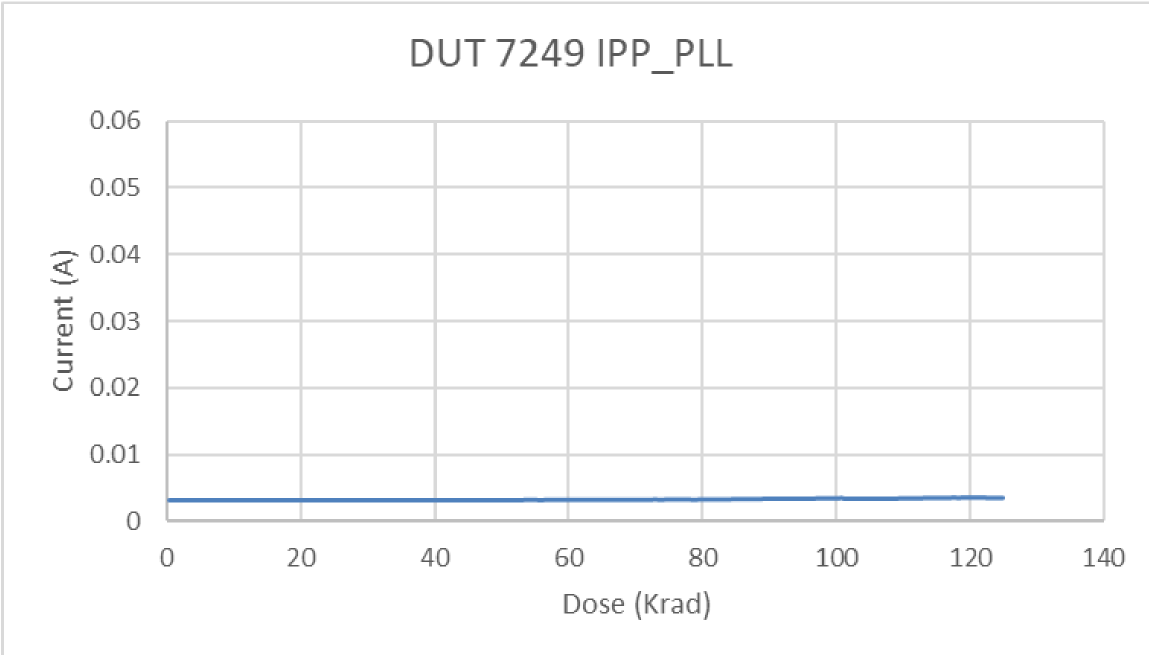

Fig. 20. DUT 07249 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

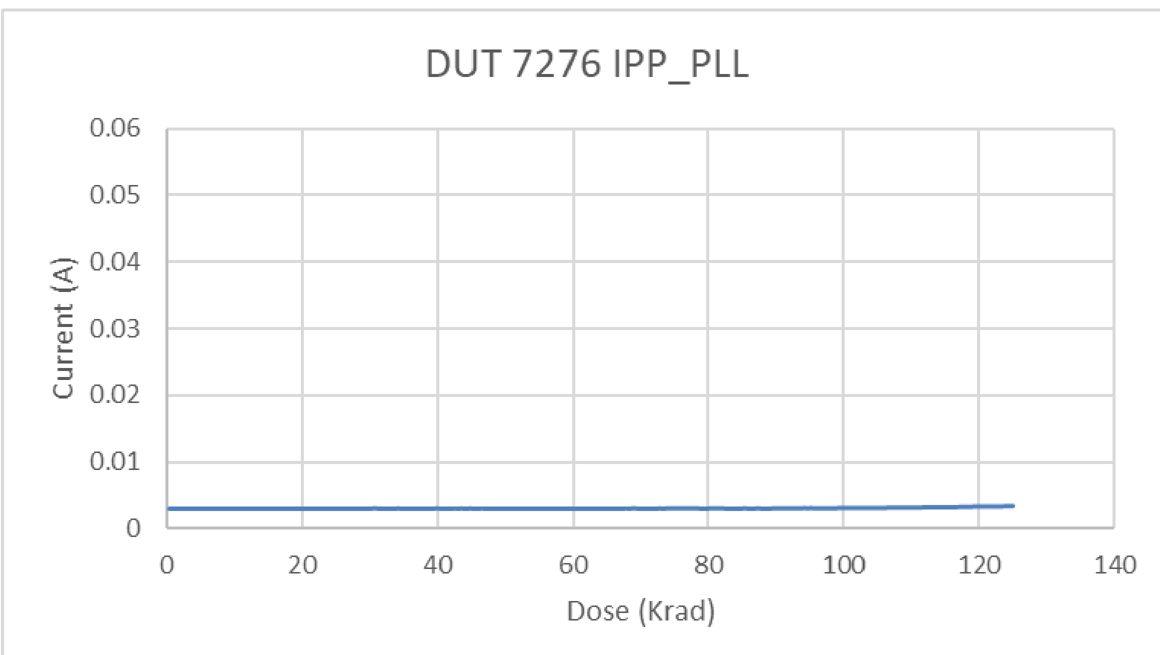

Fig. 21. DUT 07276 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

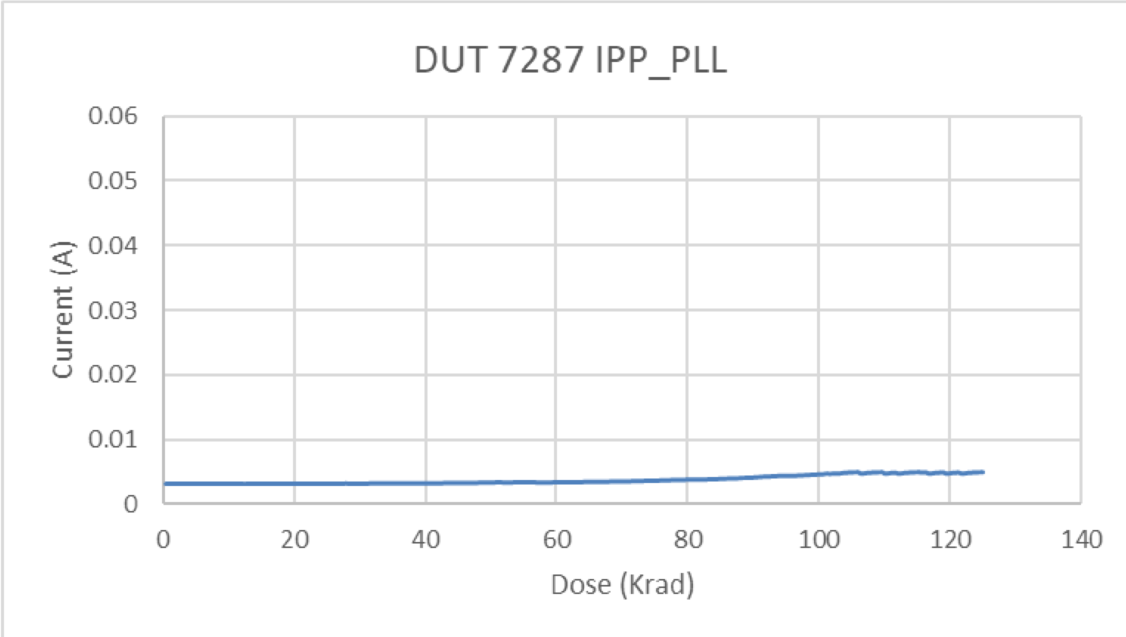

Fig. 22. DUT 07287 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

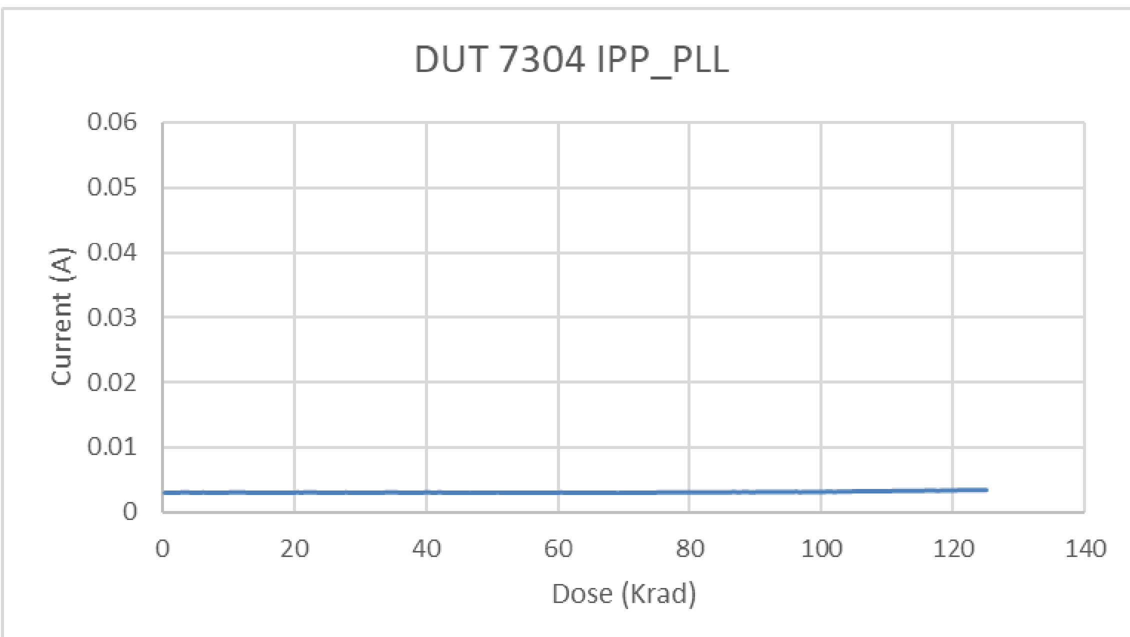

Fig. 23. DUT 07304 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

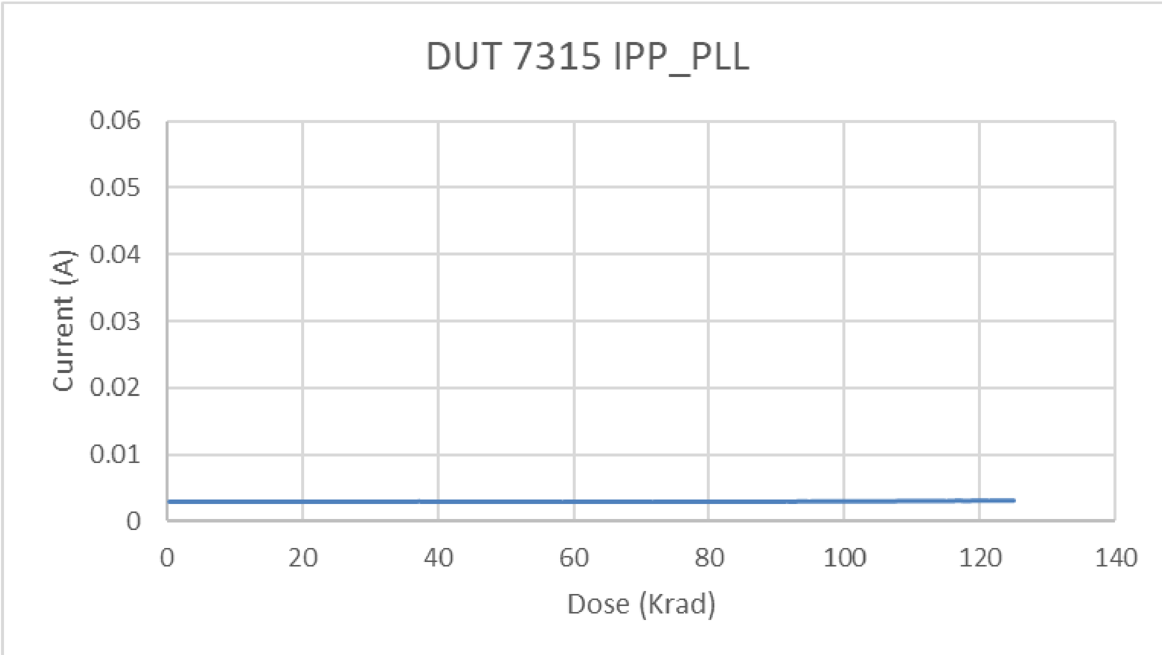

Fig. 24. DUT 07315 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

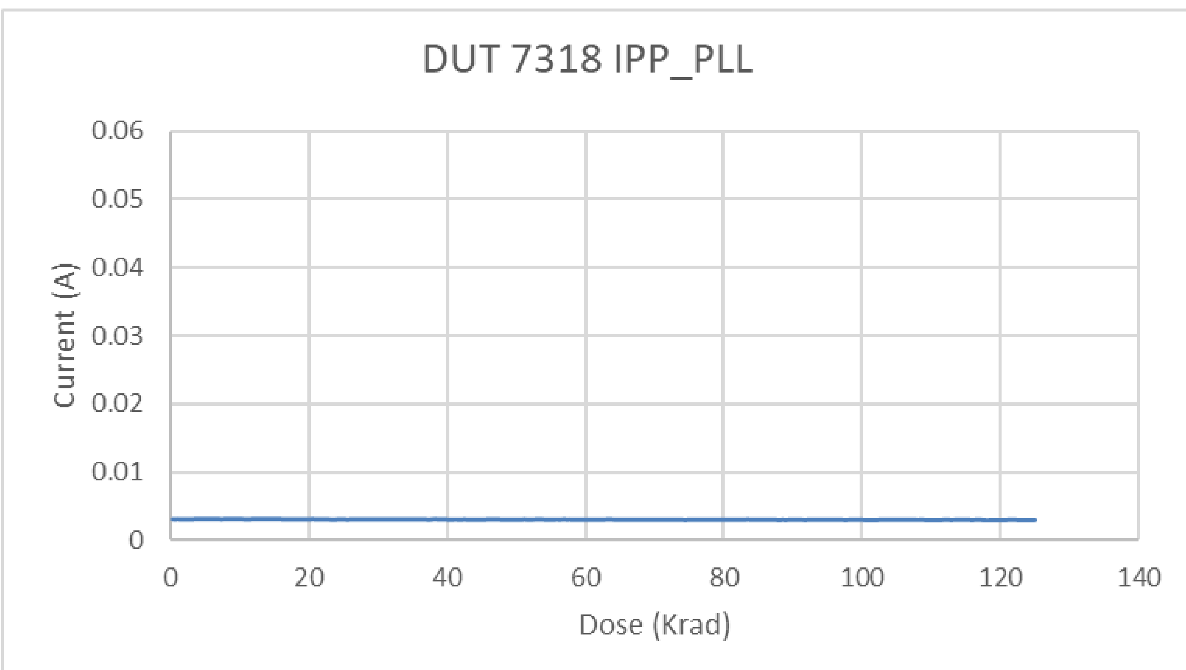

Fig. 25. DUT 07318 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 8. VIH Summary

DUT	Pre-irradiation	Post-irradiation
07249	Passed	Passed
07276	Passed	Passed
07287	Passed	Passed
07304	Passed	Passed
07315	Passed	Passed
07318	Passed	Passed

Table. 9. VIL Summary

DUT	Pre-irradiation	Post-irradiation
07249	Passed	Passed
07276	Passed	Passed
07287	Passed	Passed
07304	Passed	Passed
07315	Passed	Passed
07318	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 10 through 33 are sampled on several pins used in the burn in design.

Table. 10. LVCMOS 25 VOH – DUT 07249

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.131	2.131	2.204	2.205	2.177	2.178	2.159	2.159	2.131	2.132	2.120	2.120
PLL_MON	81	2.128	2.127	2.199	2.199	2.170	2.170	2.148	2.149	2.116	2.117	2.103	2.103
TID_BUF_OUT	92	2.127	2.127	2.197	2.198	2.167	2.167	2.145	2.145	2.110	2.110	2.096	2.097
TOGGLE_MON	97	2.128	2.128	2.200	2.200	2.171	2.172	2.150	2.150	2.118	2.119	2.105	2.106
MONITOR	104	2.127	2.128	2.199	2.199	2.170	2.169	2.149	2.148	2.116	2.117	2.102	2.103

Table. 11. LVCMOS 25 VOH – DUT 07276

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.134	2.133	2.206	2.205	2.179	2.178	2.159	2.159	2.131	2.131	2.120	2.119
PLL_MON	81	2.129	2.129	2.199	2.199	2.168	2.168	2.147	2.146	2.112	2.112	2.097	2.097
TID_BUF_OUT	92	2.129	2.129	2.198	2.198	2.167	2.167	2.145	2.145	2.110	2.110	2.095	2.095
TOGGLE_MON	97	2.130	2.130	2.201	2.201	2.172	2.172	2.150	2.151	2.118	2.118	2.104	2.104
MONITOR	104	2.130	2.129	2.198	2.198	2.168	2.168	2.146	2.146	2.111	2.111	2.096	2.096

Table. 12. LVCMOS 25 VOH – DUT 07287

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.130	2.130	2.204	2.204	2.178	2.177	2.158	2.158	2.131	2.131	2.120	2.119
PLL_MON	81	2.127	2.126	2.198	2.199	2.169	2.169	2.147	2.147	2.115	2.115	2.102	2.101
TID_BUF_OUT	92	2.126	2.126	2.197	2.196	2.167	2.166	2.145	2.143	2.110	2.110	2.096	2.096
TOGGLE_MON	97	2.127	2.127	2.199	2.199	2.170	2.170	2.150	2.150	2.118	2.117	2.104	2.104
MONITOR	104	2.127	2.126	2.198	2.198	2.169	2.169	2.148	2.148	2.115	2.115	2.101	2.101

Table. 13. LVCMOS 25 VOH – DUT 07304

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.132	2.131	2.204	2.204	2.178	2.178	2.159	2.159	2.132	2.132	2.120	2.120
PLL_MON	81	2.127	2.127	2.199	2.199	2.170	2.170	2.149	2.148	2.116	2.116	2.103	2.102
TID_BUF_OUT	92	2.127	2.127	2.197	2.197	2.167	2.167	2.145	2.144	2.111	2.111	2.097	2.096
TOGGLE_MON	97	2.128	2.128	2.200	2.200	2.171	2.171	2.150	2.150	2.119	2.119	2.106	2.105
MONITOR	104	2.127	2.127	2.199	2.199	2.170	2.170	2.148	2.149	2.116	2.115	2.102	2.102

Table. 14. LVCMOS 25 VOH – DUT 07315

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.131	2.131	2.204	2.204	2.177	2.177	2.158	2.159	2.131	2.131	2.119	2.120
PLL_MON	81	2.127	2.127	2.198	2.199	2.168	2.169	2.147	2.147	2.114	2.115	2.101	2.100
TID_BUF_OUT	92	2.126	2.127	2.197	2.197	2.167	2.167	2.145	2.145	2.110	2.111	2.096	2.096
TOGGLE_MON	97	2.127	2.128	2.199	2.200	2.171	2.171	2.150	2.150	2.118	2.118	2.104	2.105
MONITOR	104	2.127	2.127	2.198	2.198	2.169	2.169	2.147	2.147	2.114	2.114	2.100	2.100

Table. 15. LVCMOS 25 VOH – DUT 07318

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.118	2.131	2.192	2.204	2.166	2.178	2.146	2.159	2.119	2.131	2.108	2.120
PLL_MON	81	2.115	2.128	2.186	2.199	2.157	2.170	2.135	2.148	2.103	2.116	2.088	2.102
TID_BUF_OUT	92	2.115	2.127	2.185	2.198	2.155	2.167	2.132	2.145	2.098	2.111	2.083	2.096
TOGGLE_MON	97	2.116	2.129	2.187	2.200	2.158	2.171	2.137	2.150	2.106	2.119	2.092	2.105
MONITOR	104	2.115	2.128	2.187	2.199	2.157	2.170	2.136	2.148	2.103	2.115	2.089	2.102

Table. 16. LVCMOS 25 VOL – DUT 07249

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	239.7	239.3	167.2	166.8	193.0	192.7	211.3	211.1	238.2	237.8	249.3	248.6
PLL_MON	81	243.1	242.3	172.5	172.2	200.9	200.4	221.6	220.6	253.0	251.9	266.3	265.4
TID_BUF_OUT	92	242.6	241.7	173.8	173.6	203.1	202.6	224.8	224.3	258.3	257.7	273.0	272.2
TOGGLE_MON	97	240.9	240.4	171.0	170.7	199.1	198.8	219.7	219.0	250.6	249.9	264.1	263.0
MONITOR	104	241.4	240.8	171.8	171.3	200.4	199.8	221.1	220.5	252.9	252.1	266.6	265.8

Table. 17. LVCMOS 25 VOL – DUT 07276

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	236.8	237.0	165.9	165.9	192.0	192.1	210.8	210.5	238.2	238.2	249.6	249.6
PLL_MON	81	240.5	240.1	172.6	172.3	201.8	201.2	223.5	222.9	256.8	256.4	271.5	270.7
TID_BUF_OUT	92	240.3	240.1	172.8	172.6	202.3	202.2	224.4	224.5	258.8	258.6	273.6	273.7
TOGGLE_MON	97	238.3	237.9	169.8	169.4	198.2	197.8	218.7	218.2	250.8	250.4	264.3	263.7
MONITOR	104	239.3	239.1	172.1	171.9	201.6	201.6	223.7	223.6	257.8	257.6	272.7	272.2

Table. 18. LVCMOS 25 VOL – DUT 07287

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	239.7	240.1	166.9	167.2	193.1	193.0	211.2	211.5	237.9	238.0	248.9	249.2
PLL_MON	81	242.8	242.7	172.4	172.0	200.9	200.7	221.9	221.3	253.2	252.8	266.7	266.3
TID_BUF_OUT	92	242.9	243.0	173.8	173.8	203.0	203.3	224.5	224.6	258.0	257.7	272.2	271.9
TOGGLE_MON	97	241.2	241.0	170.9	171.1	198.9	199.0	219.6	219.1	250.5	250.2	263.7	263.2
MONITOR	104	242.3	242.0	172.0	172.2	200.7	200.6	221.3	221.3	253.4	253.1	266.7	266.4

Table. 19. LVCMOS 25 VOL – DUT 07304

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	238.7	239.0	166.4	166.5	192.4	192.2	210.6	210.9	237.4	237.4	248.2	248.3
PLL_MON	81	241.9	241.9	172.0	171.8	200.3	200.1	221.1	220.7	252.6	252.1	266.0	265.5
TID_BUF_OUT	92	242.4	242.4	173.1	173.2	202.5	202.4	224.1	224.1	257.3	257.1	271.6	271.6
TOGGLE_MON	97	240.5	240.4	170.7	170.6	198.6	198.4	218.9	218.8	249.7	249.3	262.9	262.4
MONITOR	104	241.3	241.2	171.5	171.6	200.3	200.0	220.7	220.7	252.8	252.7	266.3	266.2

Table. 20. LVCMOS 25 VOL – DUT 07315

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	240.0	240.0	167.1	166.7	193.3	192.6	211.8	211.1	238.6	238.1	249.8	249.1
PLL_MON	81	243.1	242.0	173.1	172.5	201.9	200.9	222.9	221.8	254.8	253.4	268.6	267.2
TID_BUF_OUT	92	243.6	242.8	174.1	173.5	203.5	202.7	225.2	224.4	258.6	257.7	273.0	272.2
TOGGLE_MON	97	241.4	240.5	171.2	170.5	199.6	198.5	219.9	219.2	251.3	250.3	264.5	263.3
MONITOR	104	242.5	241.8	172.9	172.5	201.7	200.9	222.7	221.8	255.2	254.3	269.1	268.0

Table. 21. LVCMOS 25 VOL – DUT 07318

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	239.9	239.2	167.2	166.8	193.0	192.4	211.4	211.0	238.2	237.0	249.3	248.0
PLL_MON	81	242.8	241.6	172.5	172.0	201.3	200.2	222.2	221.0	254.0	253.0	267.7	266.4
TID_BUF_OUT	92	242.9	241.7	173.9	173.3	203.2	202.5	224.8	224.1	258.6	257.6	272.9	271.9
TOGGLE_MON	97	240.6	239.3	170.9	170.3	199.1	198.3	219.7	218.5	250.7	249.3	264.1	262.6
MONITOR	104	241.9	240.8	172.3	171.6	201.1	200.0	221.8	221.1	254.0	252.9	267.7	266.8

Table. 22. LVTTL VOH – DUT 07249

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.918	2.918	2.912	2.912	2.898	2.897	2.884	2.884	2.870	2.871
PLL_MON	81	2.915	2.916	2.906	2.906	2.887	2.888	2.869	2.870	2.850	2.851
TID_BUF_OUT	92	2.914	2.915	2.904	2.905	2.884	2.884	2.863	2.863	2.843	2.843
TOGGLE_MON	97	2.916	2.916	2.907	2.907	2.889	2.889	2.871	2.872	2.853	2.854
MONITOR	104	2.916	2.916	2.906	2.906	2.888	2.888	2.869	2.869	2.850	2.850

Table. 23. LVTTL VOH – DUT 07276

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.921	2.921	2.913	2.913	2.898	2.898	2.884	2.884	2.868	2.869
PLL_MON	81	2.917	2.917	2.907	2.906	2.886	2.886	2.865	2.865	2.844	2.844
TID_BUF_OUT	92	2.916	2.916	2.905	2.906	2.884	2.884	2.863	2.863	2.841	2.841
TOGGLE_MON	97	2.917	2.918	2.908	2.908	2.890	2.890	2.871	2.871	2.852	2.852
MONITOR	104	2.917	2.917	2.906	2.906	2.885	2.885	2.864	2.864	2.843	2.842

Table. 24. LVTTL VOH – DUT 07287

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.918	2.918	2.911	2.910	2.897	2.897	2.883	2.883	2.870	2.870
PLL_MON	81	2.915	2.914	2.905	2.905	2.887	2.886	2.868	2.868	2.849	2.850
TID_BUF_OUT	92	2.914	2.914	2.904	2.903	2.883	2.883	2.863	2.863	2.843	2.843
TOGGLE_MON	97	2.915	2.915	2.906	2.906	2.889	2.888	2.871	2.870	2.853	2.853
MONITOR	104	2.915	2.914	2.905	2.905	2.886	2.887	2.868	2.868	2.849	2.849

Table. 25. LVTTL VOH – DUT 07304

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.919	2.918	2.912	2.911	2.898	2.898	2.884	2.885	2.871	2.871
PLL_MON	81	2.915	2.915	2.906	2.906	2.888	2.887	2.869	2.869	2.851	2.850
TID_BUF_OUT	92	2.915	2.914	2.905	2.904	2.884	2.884	2.865	2.864	2.844	2.843
TOGGLE_MON	97	2.916	2.916	2.907	2.907	2.890	2.889	2.872	2.872	2.854	2.854
MONITOR	104	2.915	2.914	2.906	2.905	2.887	2.887	2.869	2.869	2.850	2.850

Table. 26. LVTTL VOH – DUT 07315

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.918	2.918	2.911	2.912	2.897	2.897	2.883	2.884	2.870	2.870
PLL_MON	81	2.915	2.915	2.905	2.905	2.886	2.886	2.867	2.868	2.848	2.849
TID_BUF_OUT	92	2.914	2.914	2.904	2.904	2.884	2.883	2.863	2.863	2.843	2.844
TOGGLE_MON	97	2.916	2.916	2.906	2.907	2.888	2.889	2.870	2.871	2.853	2.853
MONITOR	104	2.914	2.914	2.905	2.905	2.886	2.886	2.866	2.867	2.847	2.848

Table. 27. LVTTL VOH – DUT 07318

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.904	2.919	2.897	2.912	2.882	2.898	2.869	2.885	2.856	2.871
PLL_MON	81	2.901	2.916	2.891	2.907	2.872	2.888	2.853	2.868	2.834	2.850
TID_BUF_OUT	92	2.900	2.915	2.890	2.905	2.869	2.884	2.848	2.864	2.828	2.844
TOGGLE_MON	97	2.901	2.917	2.892	2.908	2.874	2.890	2.856	2.872	2.838	2.854
MONITOR	104	2.900	2.916	2.891	2.906	2.872	2.888	2.853	2.869	2.834	2.850

Table. 28. LVTTL VOL – DUT 07249

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	219.0	218.7	225.4	224.8	238.6	237.7	251.7	251.3	265.2	264.4
PLL_MON	81	222.3	221.7	230.8	230.1	248.7	247.9	266.4	265.5	285.0	283.6
TID_BUF_OUT	92	222.4	221.7	232.0	231.4	251.9	251.3	271.9	271.5	292.4	291.6
TOGGLE_MON	97	220.7	220.2	229.2	228.6	246.7	245.8	264.3	263.3	282.2	281.3
MONITOR	104	221.5	220.8	229.8	229.4	248.1	247.4	266.3	265.4	285.0	284.3

Table. 29. LVTTL VOL – DUT 07276

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	216.8	217.1	223.7	223.5	237.7	237.2	251.9	251.9	266.5	266.4
PLL_MON	81	220.4	220.3	230.3	230.0	250.3	249.7	270.7	270.2	291.5	290.4
TID_BUF_OUT	92	220.4	220.4	230.5	230.3	251.4	251.4	272.6	272.5	294.2	293.6
TOGGLE_MON	97	218.9	218.4	227.6	227.0	245.6	245.2	264.2	263.8	283.1	282.5
MONITOR	104	219.7	219.3	229.6	229.4	250.5	250.1	271.5	271.2	292.8	292.7

Table. 30. LVTTL VOL – DUT 07287

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	219.4	219.7	225.4	225.4	238.0	238.4	251.4	251.5	264.9	265.1
PLL_MON	81	222.1	221.9	230.9	230.5	248.8	248.3	267.0	266.4	285.6	284.8
TID_BUF_OUT	92	222.4	222.3	232.3	232.1	251.8	251.6	271.5	271.2	291.5	291.5
TOGGLE_MON	97	220.9	220.6	229.3	229.1	246.6	246.1	264.0	263.8	281.8	281.5
MONITOR	104	221.8	221.8	230.5	230.4	248.5	248.4	266.7	266.6	285.5	285.4

Table. 31. LVTTL VOL – DUT 07304

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	218.8	218.8	224.6	224.6	237.8	237.8	251.1	250.8	264.3	264.4
PLL_MON	81	221.8	221.8	230.1	230.0	248.2	248.0	266.3	265.6	284.8	284.2
TID_BUF_OUT	92	222.2	222.2	231.8	231.3	251.2	251.1	271.2	271.1	291.3	290.9
TOGGLE_MON	97	220.3	220.1	228.6	228.5	246.1	245.8	263.6	263.1	281.1	280.8
MONITOR	104	221.2	221.1	229.9	229.6	248.0	247.7	266.5	266.3	285.2	285.0

Table. 32. LVTTL VOL – DUT 07315

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	219.7	219.6	225.8	225.1	238.9	238.2	252.3	251.6	265.9	265.3
PLL_MON	81	222.7	221.8	231.5	231.1	250.2	249.0	268.7	267.6	287.6	286.2
TID_BUF_OUT	92	223.3	222.8	232.8	232.1	252.4	251.6	272.5	271.3	292.6	291.6
TOGGLE_MON	97	221.2	220.5	229.5	228.6	247.1	246.0	264.9	263.6	282.9	281.6
MONITOR	104	222.3	221.6	231.2	230.3	250.1	249.3	268.9	268.1	288.0	287.1

Table. 33. LVTTL VOL – DUT 07318

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	219.1	218.3	225.1	224.3	238.0	237.4	251.4	250.6	264.8	264.0
PLL_MON	81	221.7	221.0	230.5	229.6	248.7	247.8	267.3	266.1	286.0	284.5
TID_BUF_OUT	92	222.1	221.1	231.6	230.8	251.8	250.9	271.8	270.6	292.2	290.9
TOGGLE_MON	97	220.1	219.1	228.5	227.1	246.2	245.2	263.9	262.7	282.0	280.6
MONITOR	104	221.3	220.3	230.0	229.2	248.4	247.3	267.2	266.3	285.9	284.9

E. Propagation Delay

Table 34 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 34. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (µs)	Post-irradiation (µs)	Change Degradation (%)
07249	125 krad	0.438	0.442	0.91
07276	125 krad	0.428	0.442	3.27
07287	125 krad	0.45	0.459	2.00
07304	125 krad	0.449	0.459	2.23
07315	125 krad	0.437	0.446	2.06
07318	125 krad	0.448	0.455	1.56

F. Transition Time

The figures below show the pre-irradiation and post-irradiation transitions edges. In each case the radiation induced transition degradation is not observable.

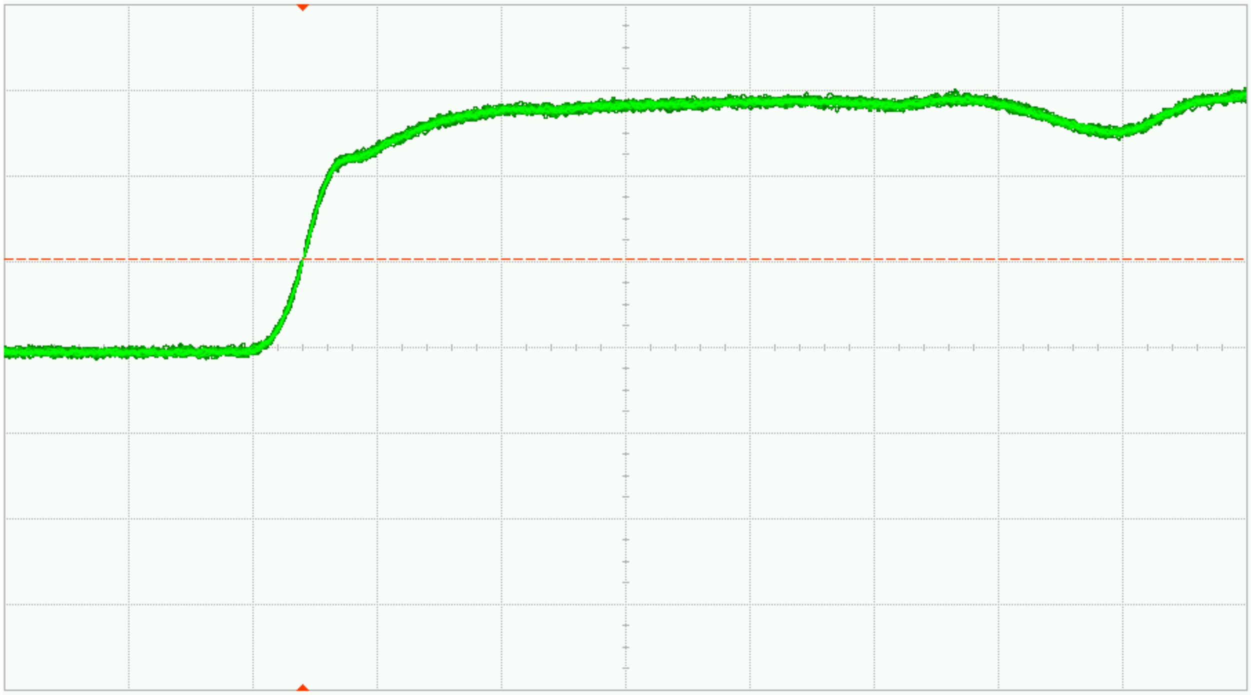

Fig. 26 (a). DUT 07249 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

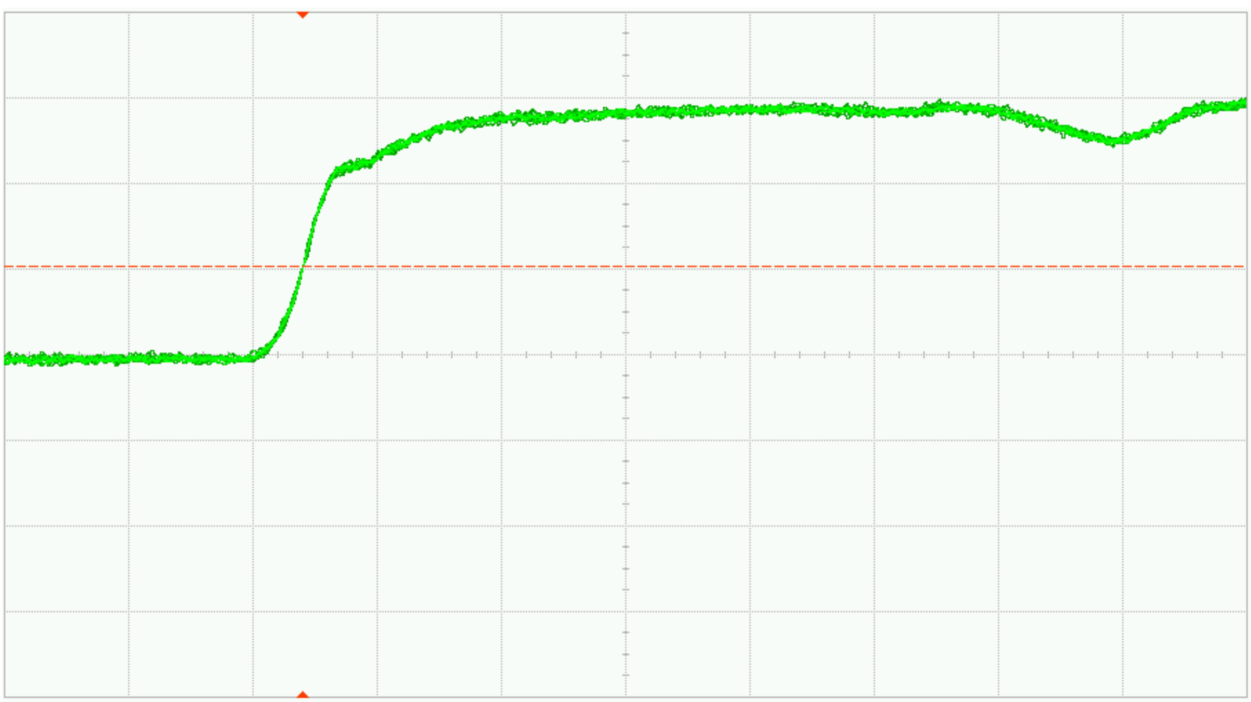

Fig. 26 (b). DUT 07249 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

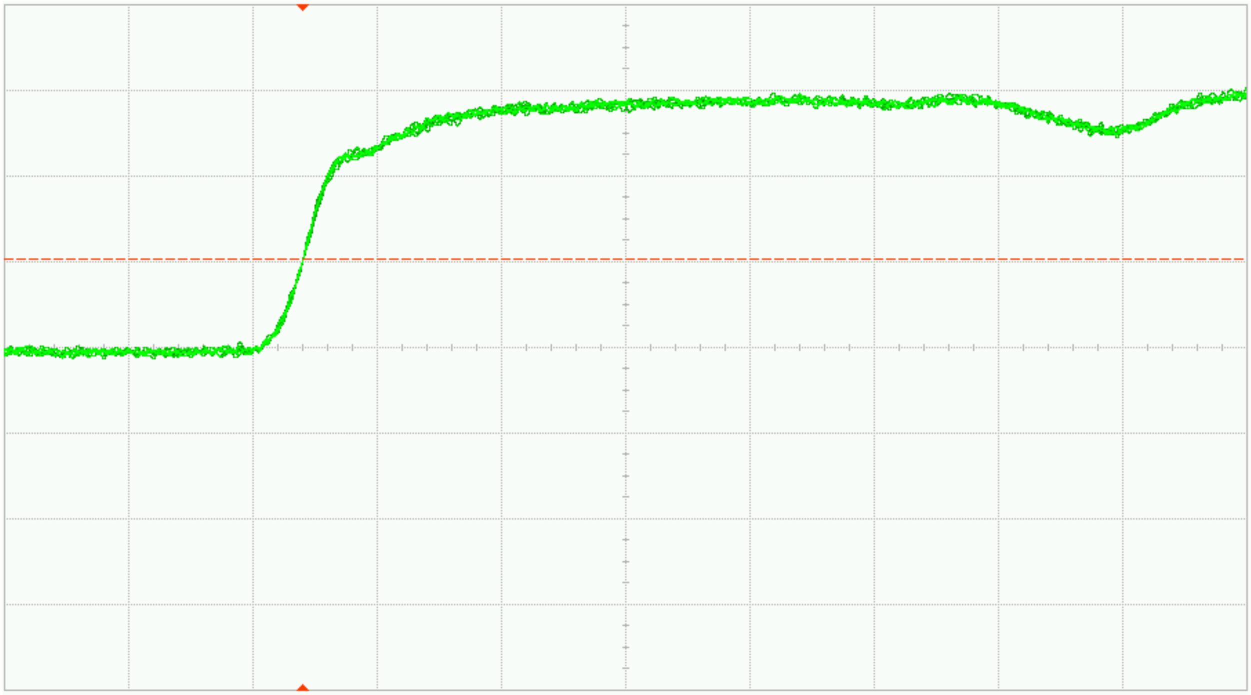

Fig. 27 (a). DUT 07276 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

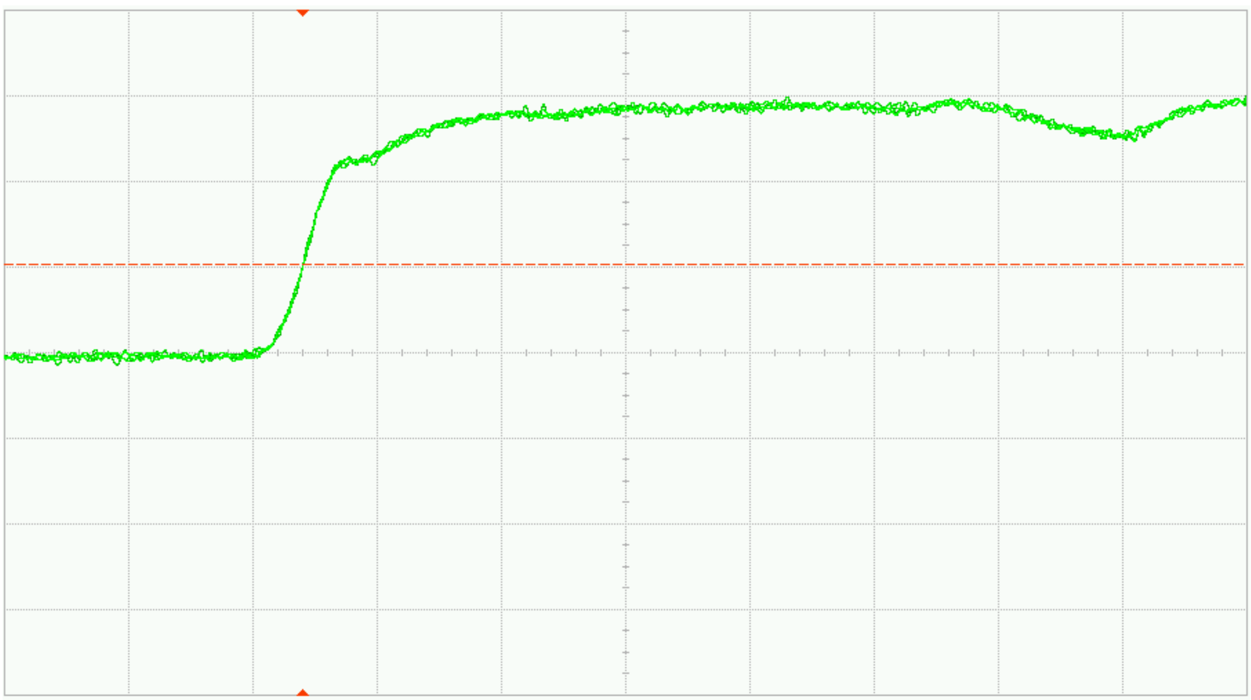

Fig. 27 (b). DUT 07276 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

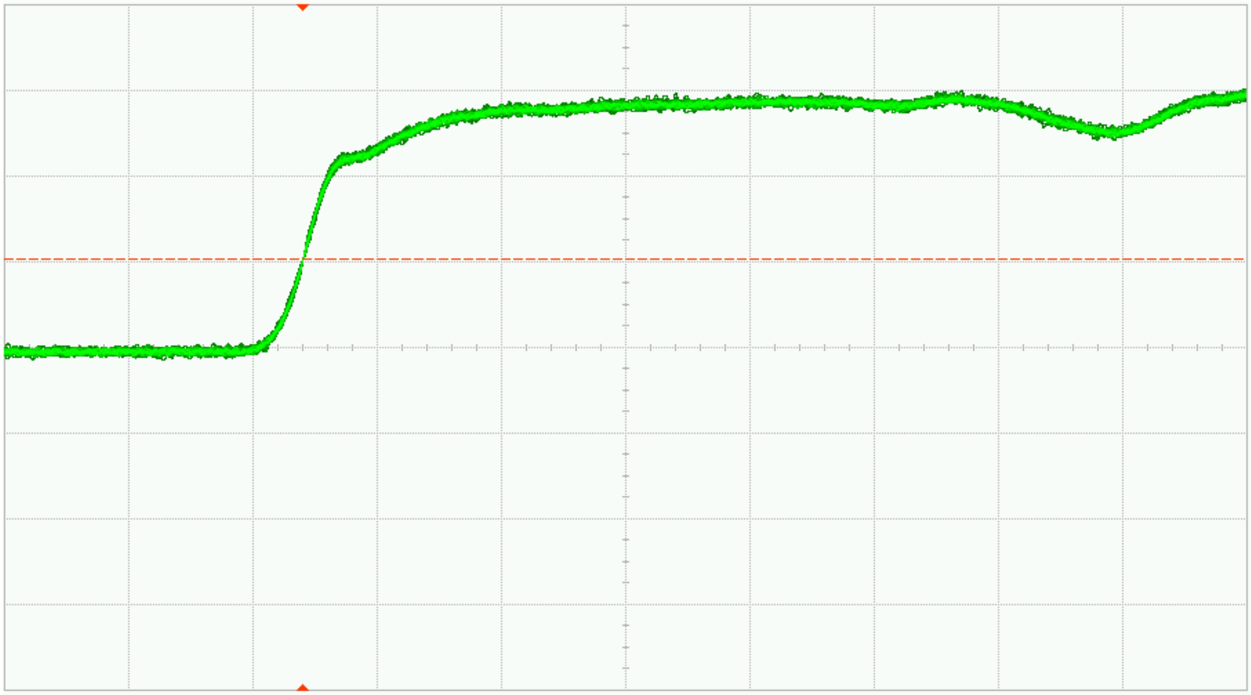

Fig. 28 (a). DUT 07287 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

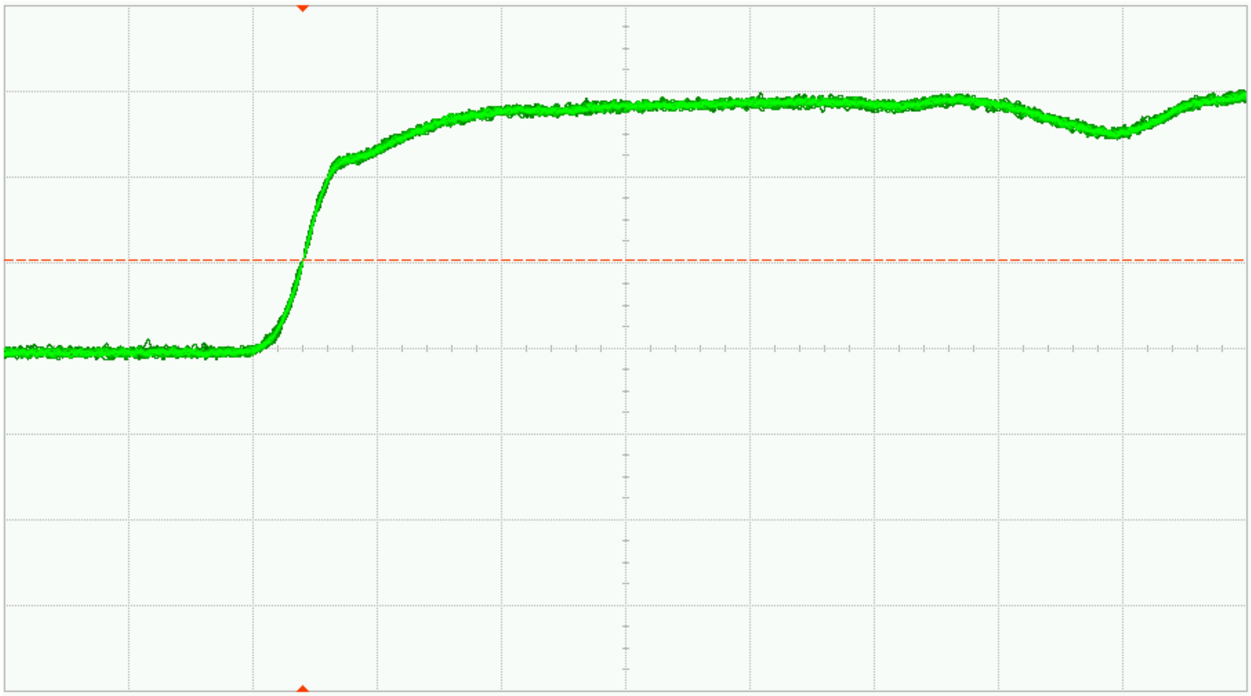

Fig. 28 (b). DUT 07287 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

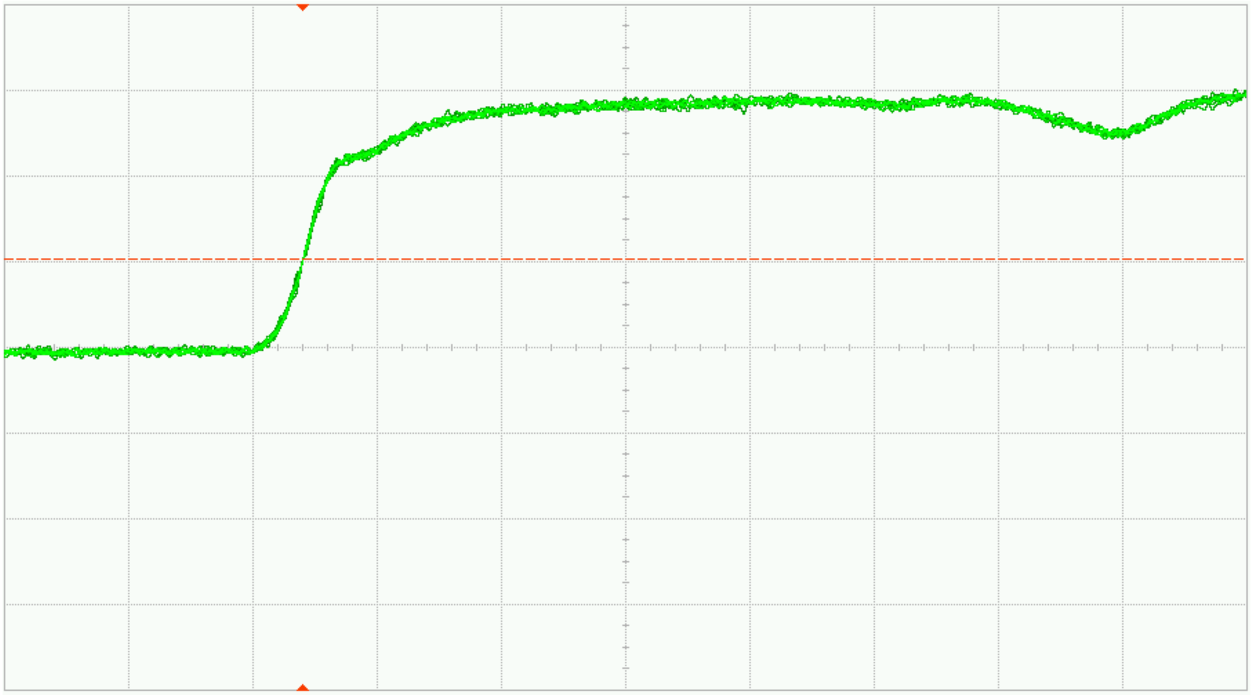

Fig. 29 (a). DUT 07304 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

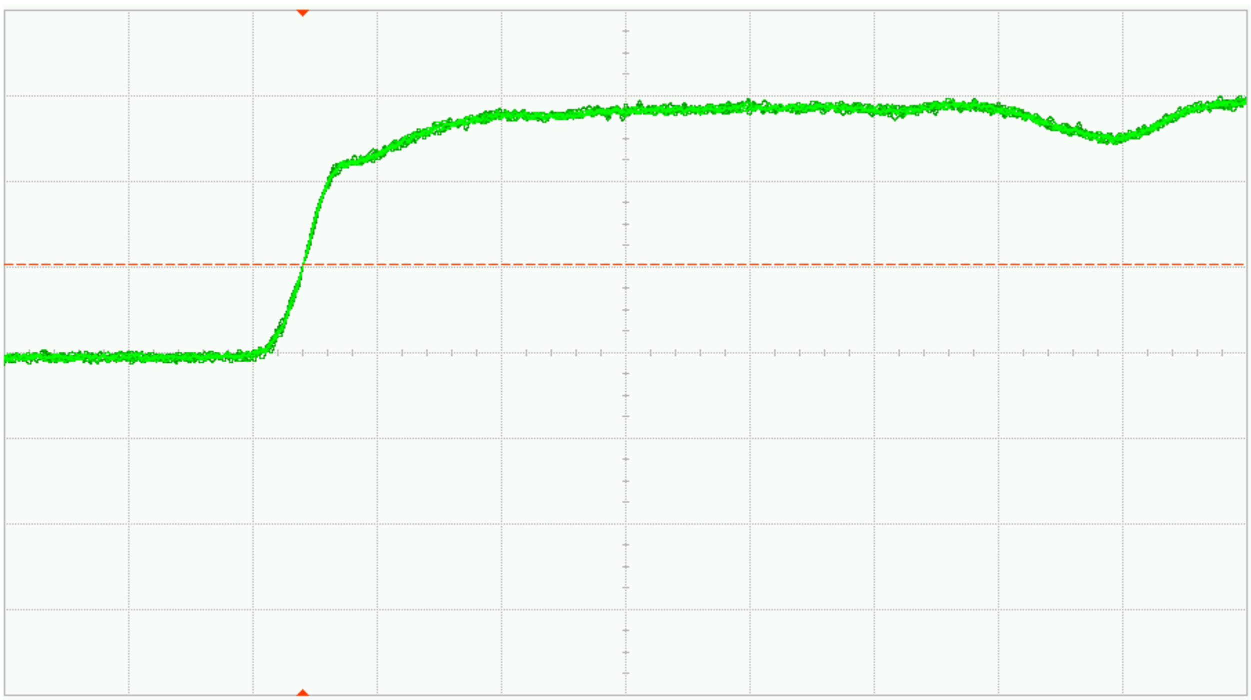

Fig. 29 (b). DUT 07304 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

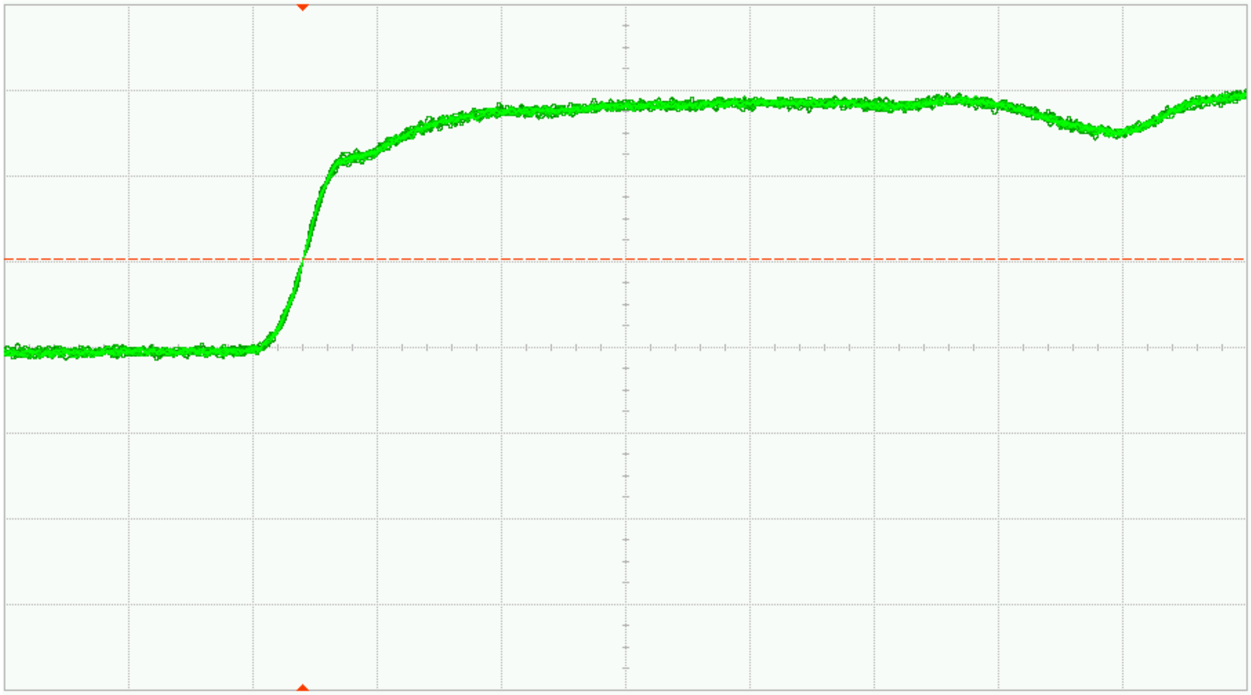

Fig. 30 (a). DUT 07315 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

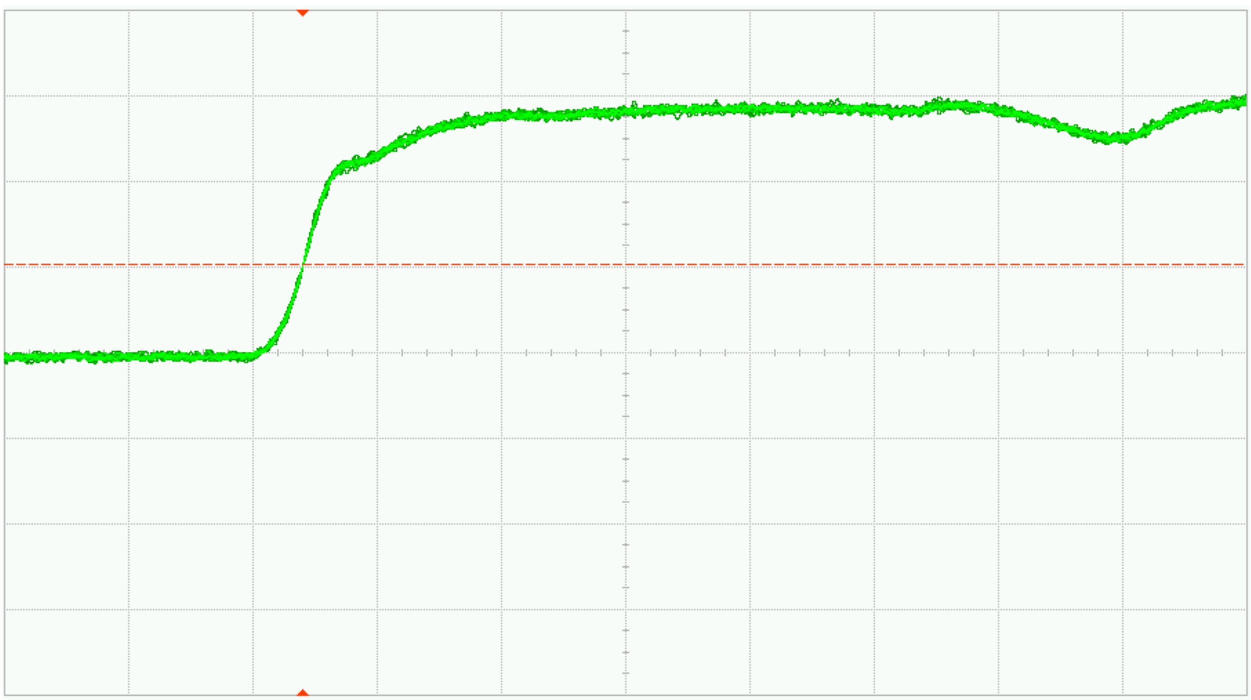

Fig. 30 (b). DUT 07315 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

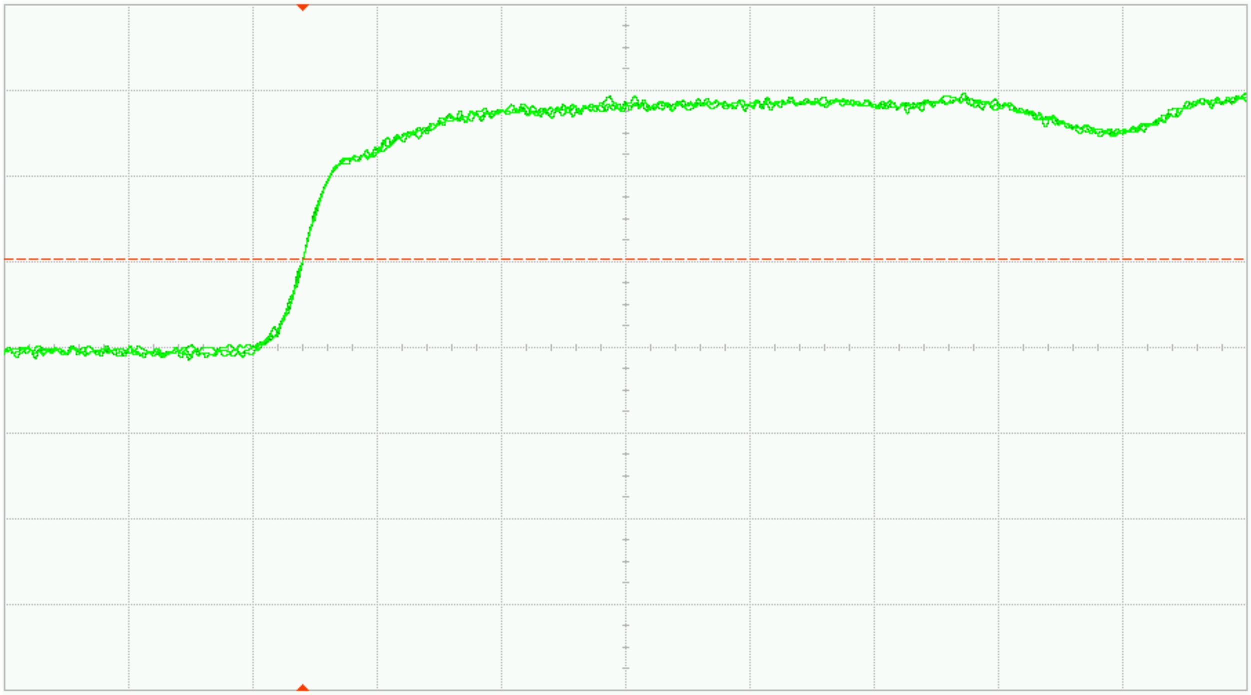

Fig. 31 (a). DUT 07318 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

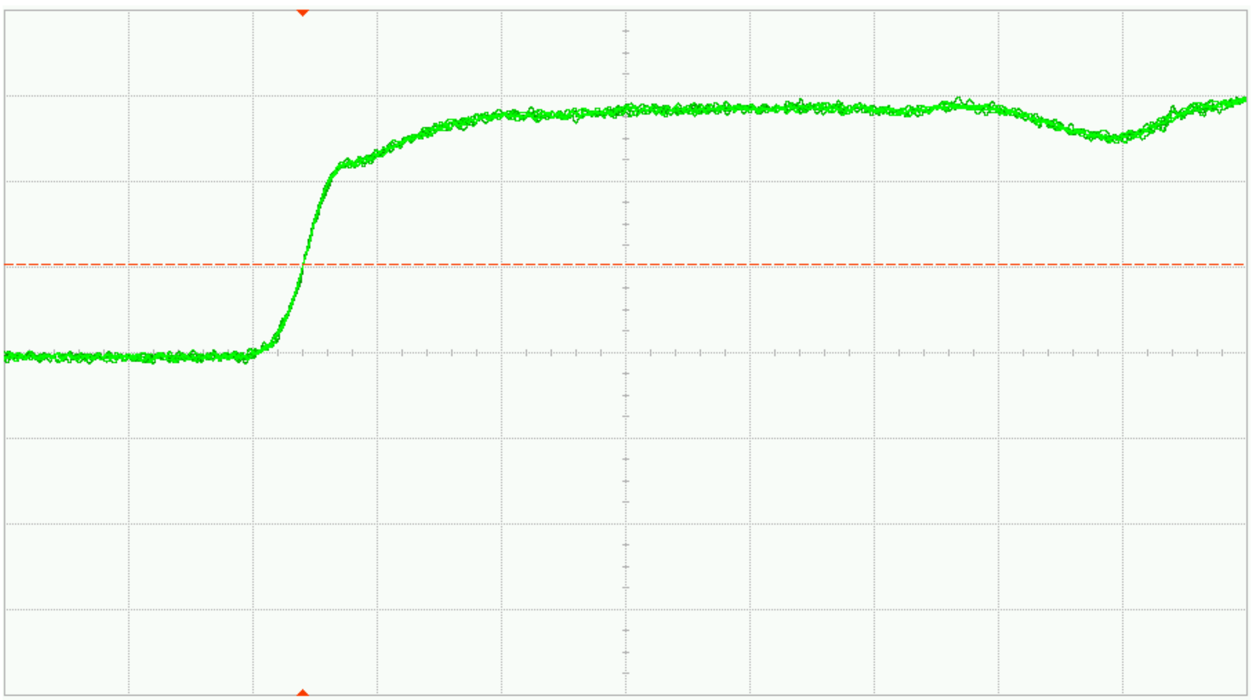

Fig. 31 (b). DUT 07318 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

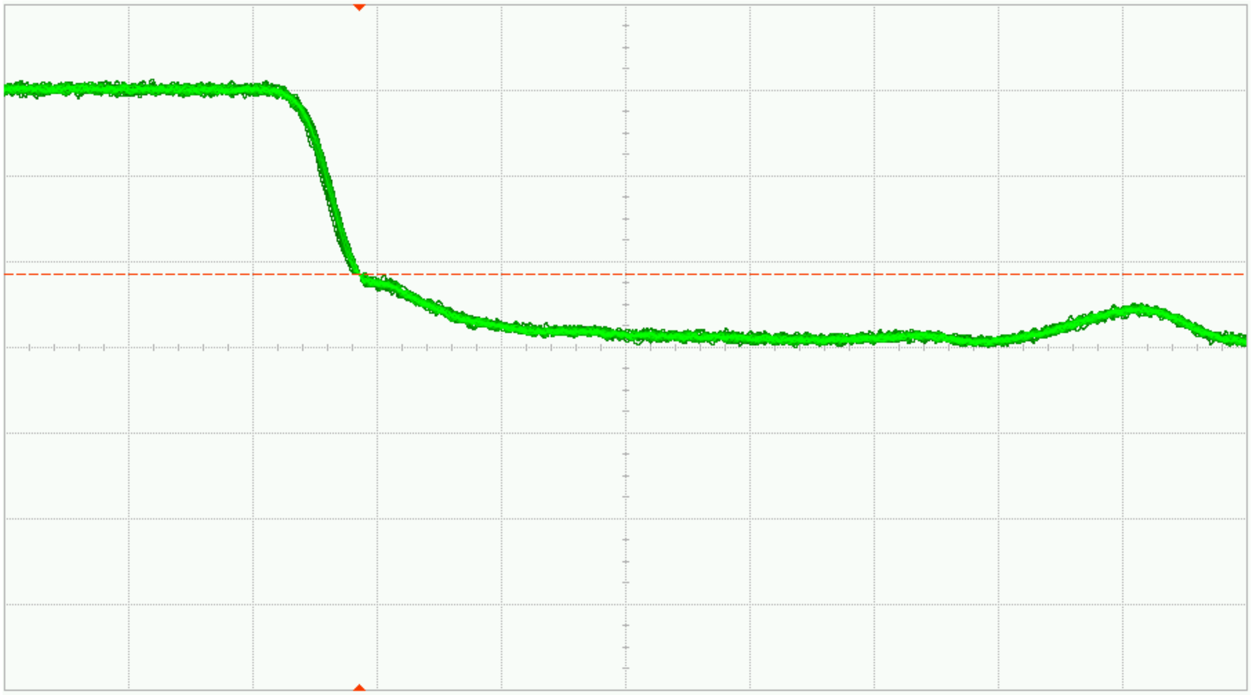

Fig. 32 (a). DUT 07249 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

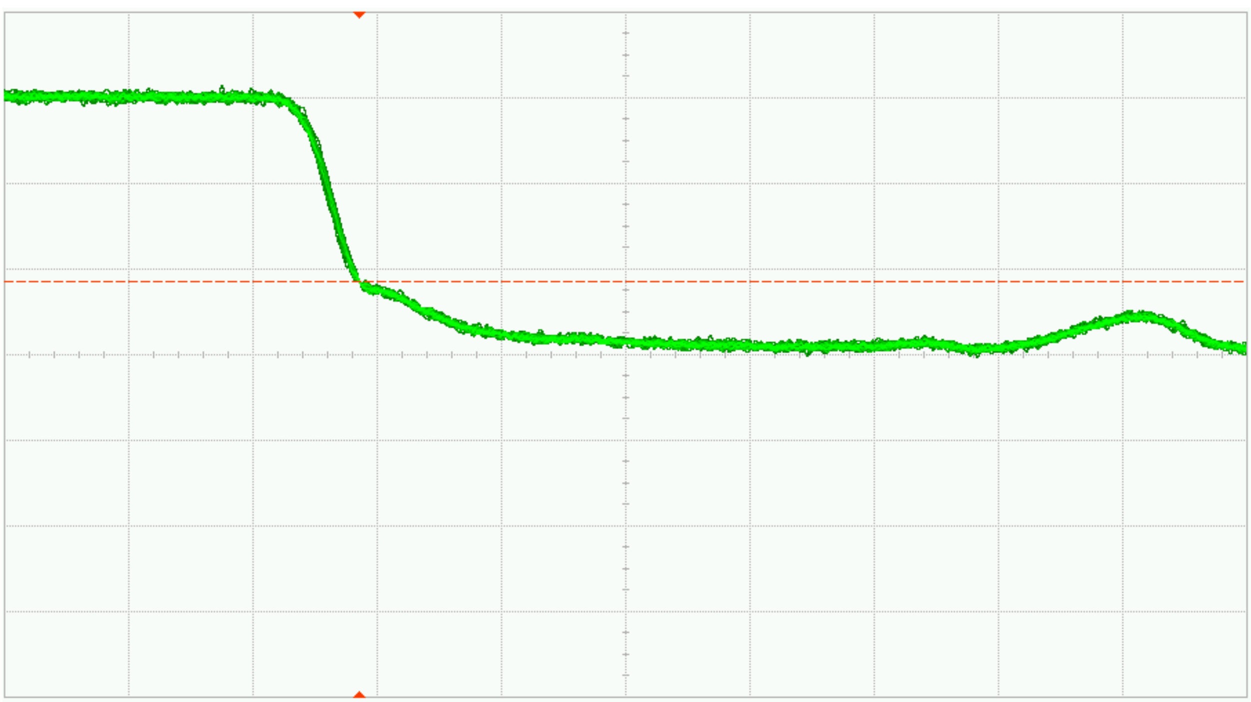

Fig. 32 (b). DUT 07249 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

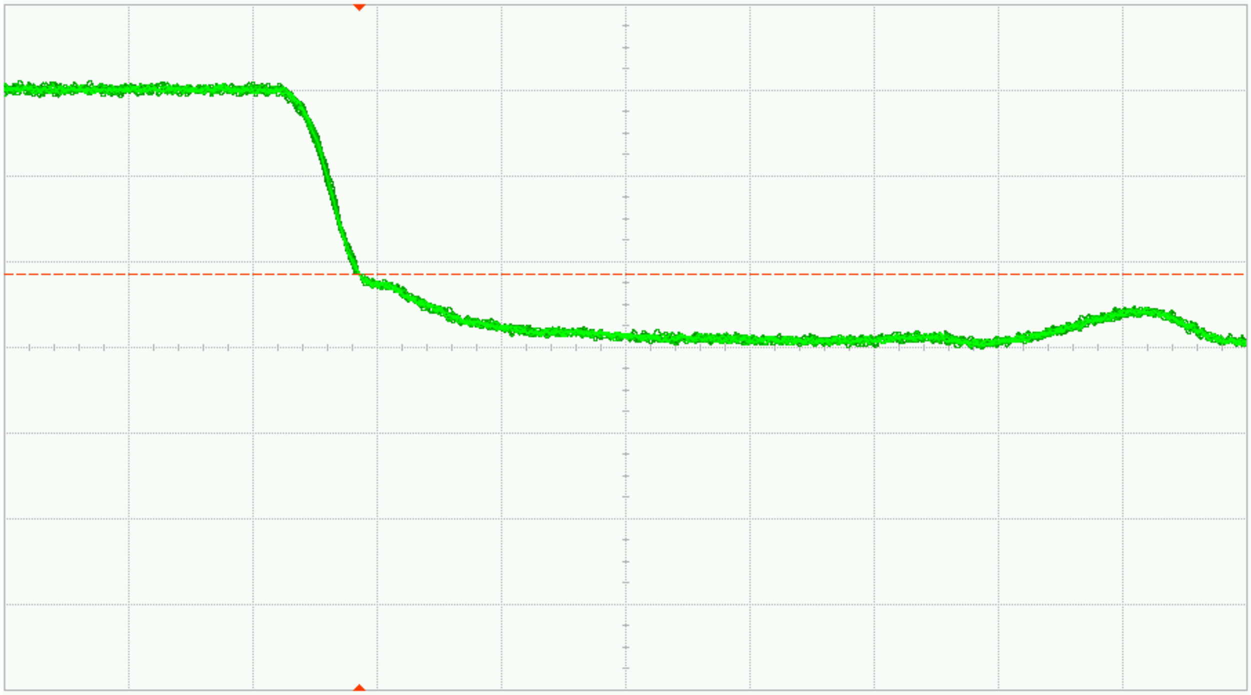

Fig. 33 (a). DUT 07276 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

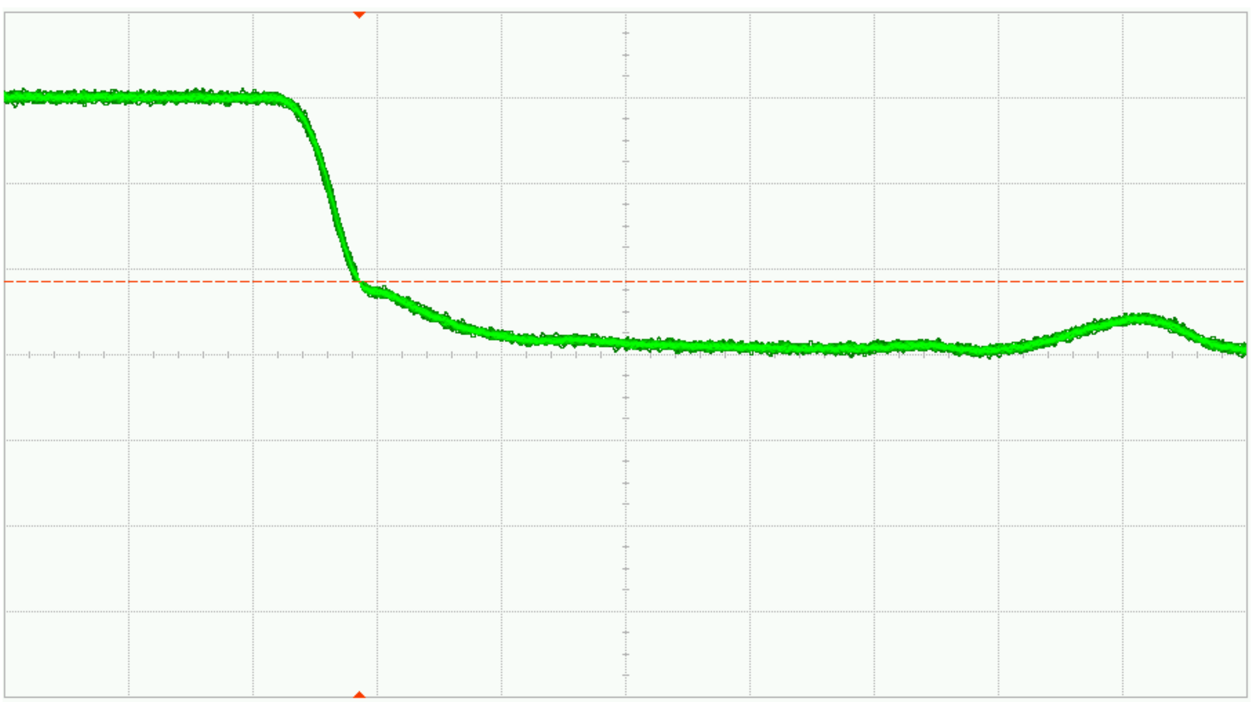

Fig. 33 (b). DUT 07276 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

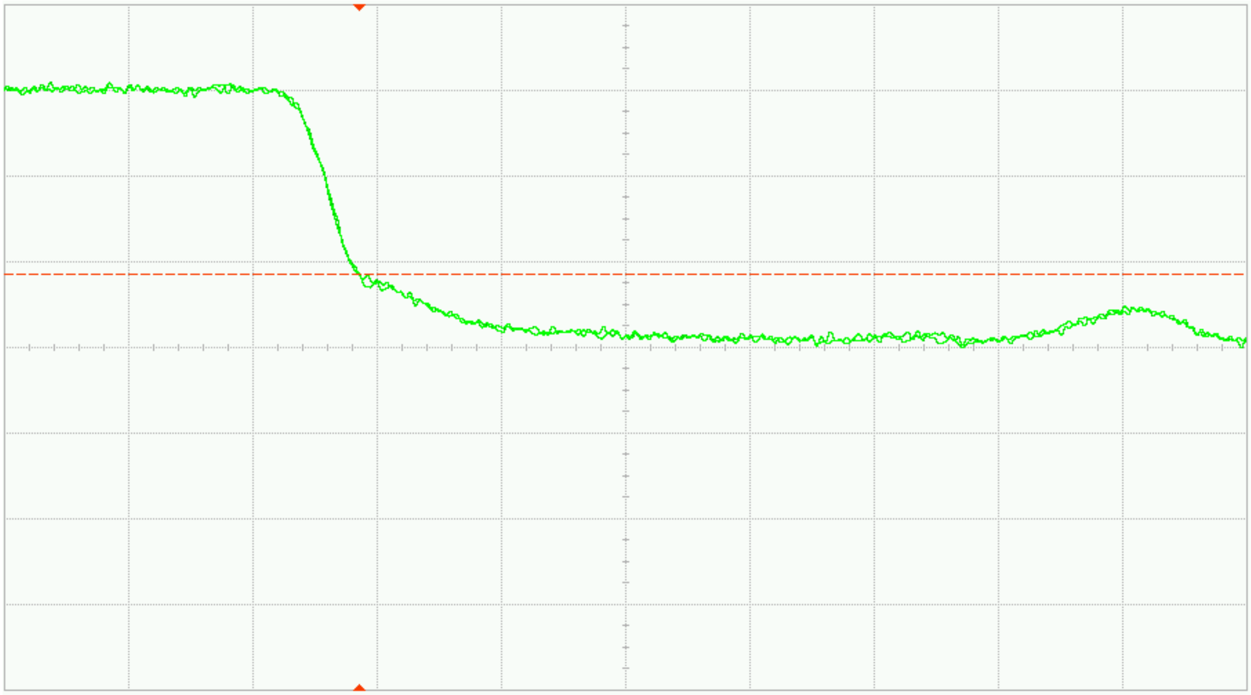

Fig. 34 (a). DUT 07287 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

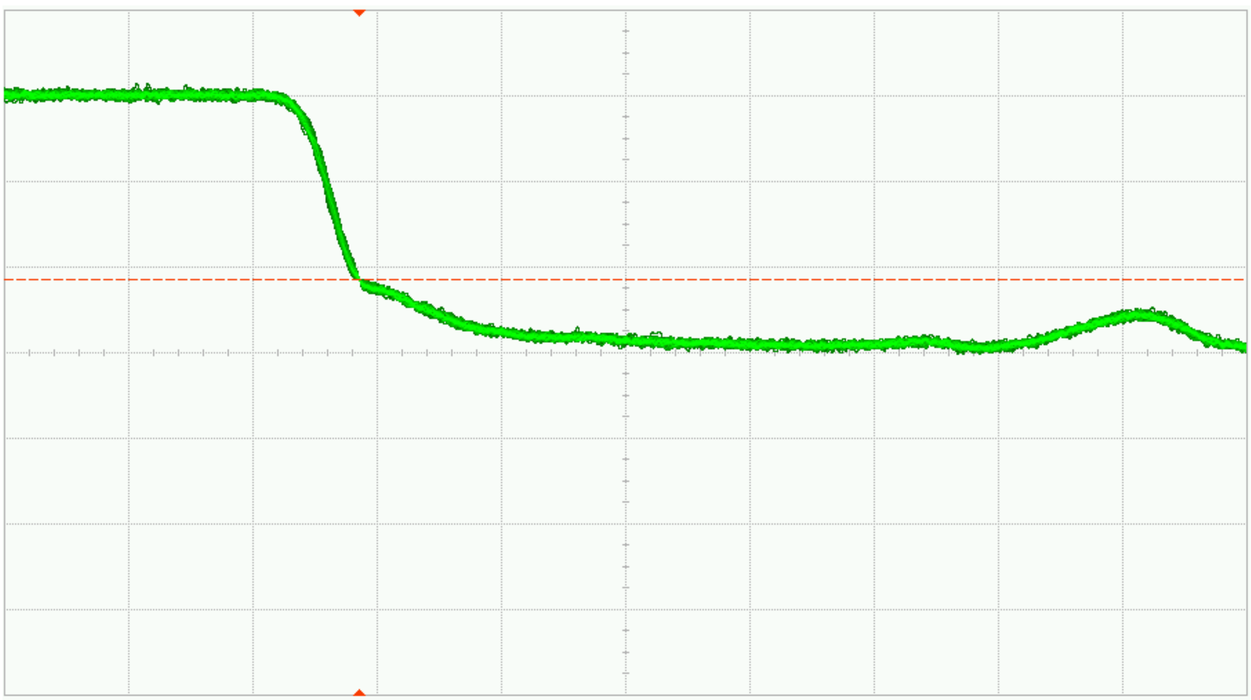

Fig. 34 (b). DUT 07287 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

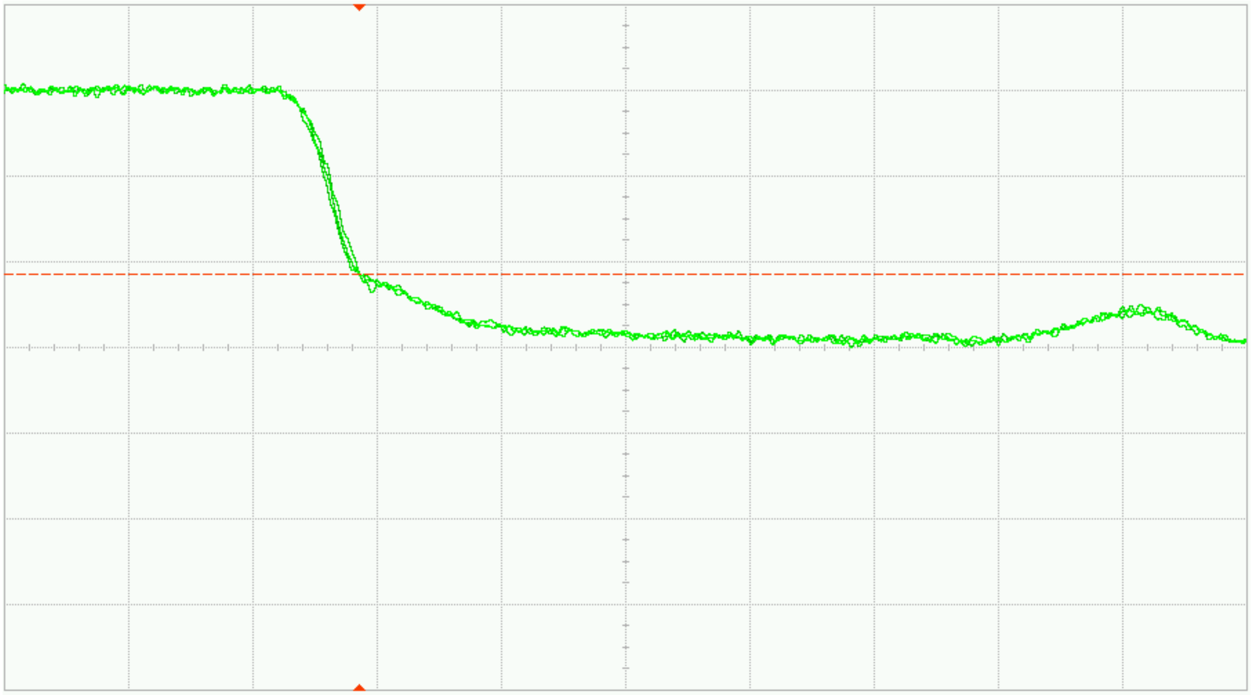

Fig. 35 (a). DUT 07304 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

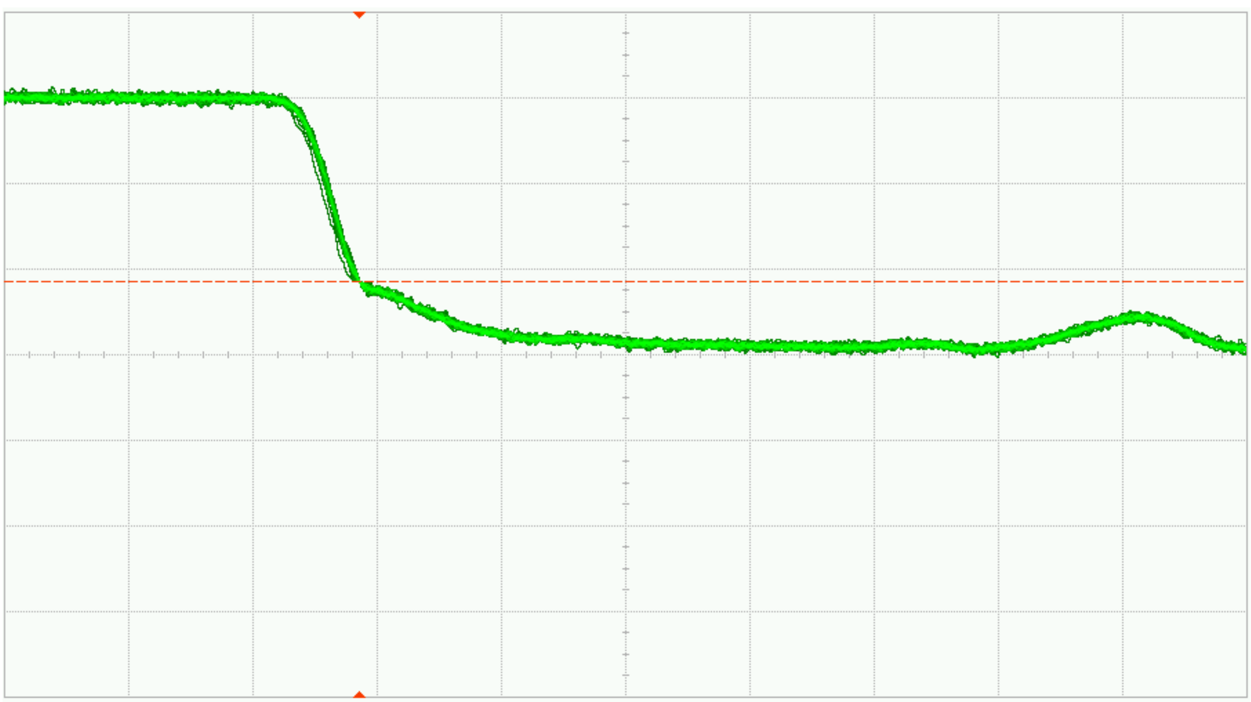

Fig. 35 (b). DUT 07304 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

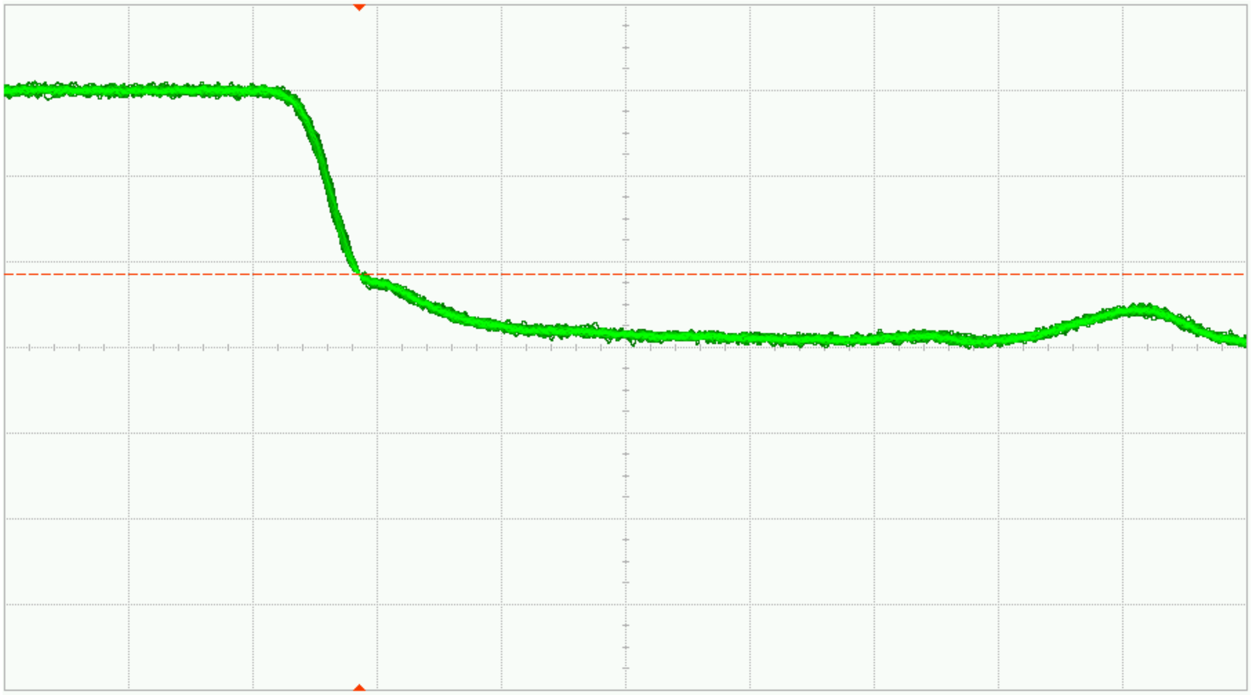

Fig. 36 (a). DUT 07315 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

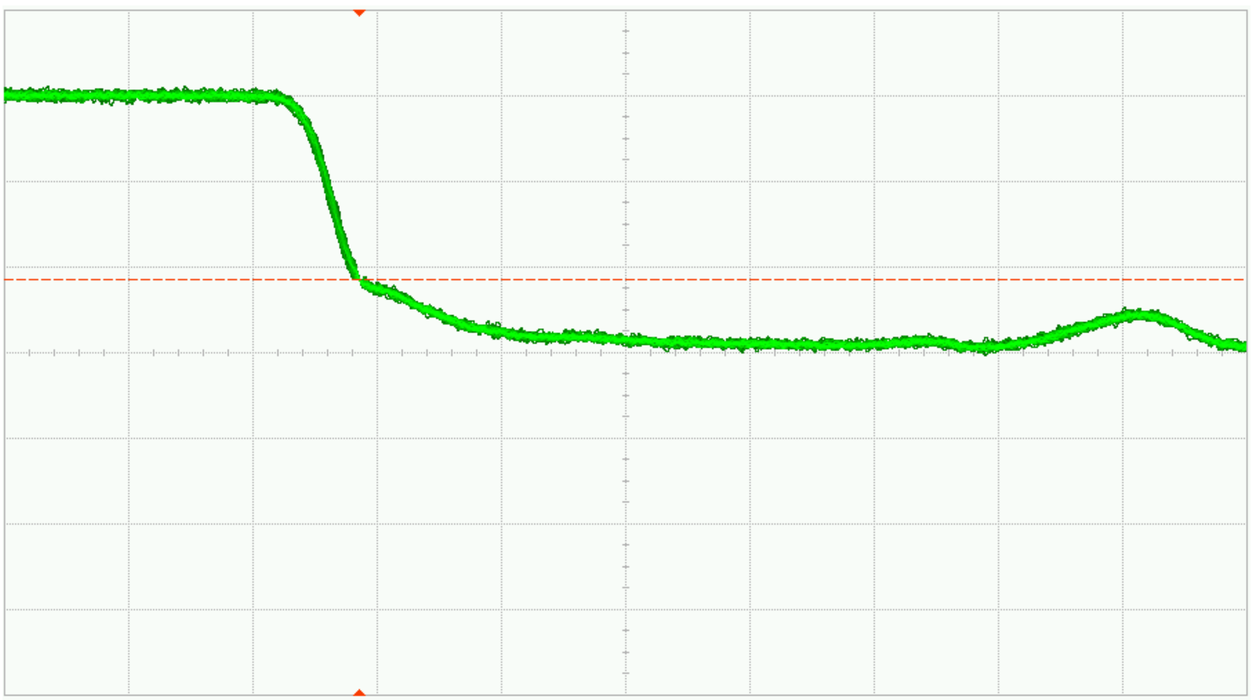

Fig. 36 (b). DUT 07315 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

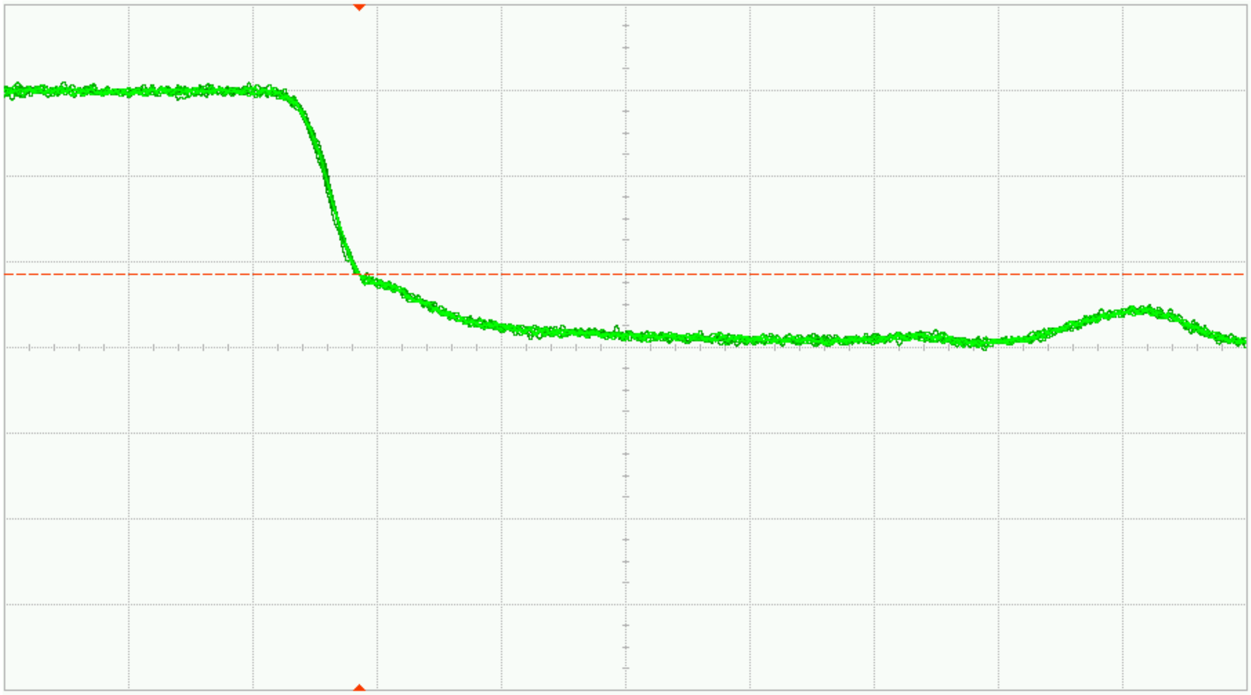

Fig. 37 (a). DUT 07318 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

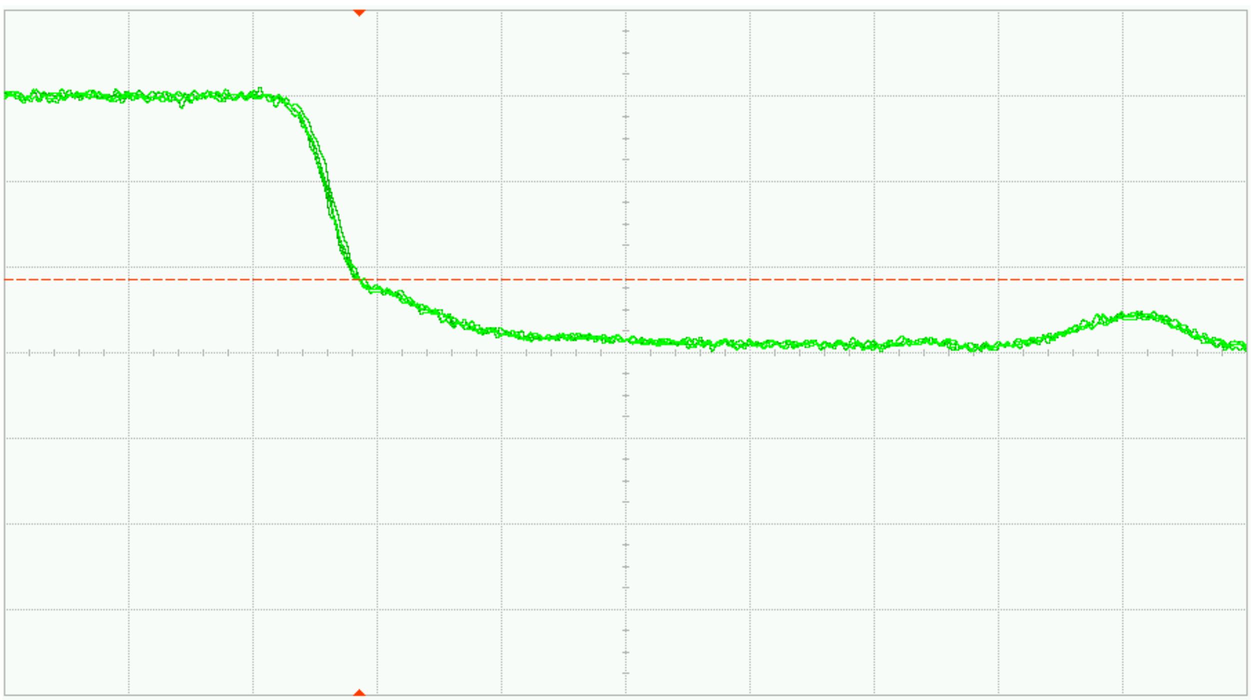

Fig. 37 (b). DUT 07318 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 35. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

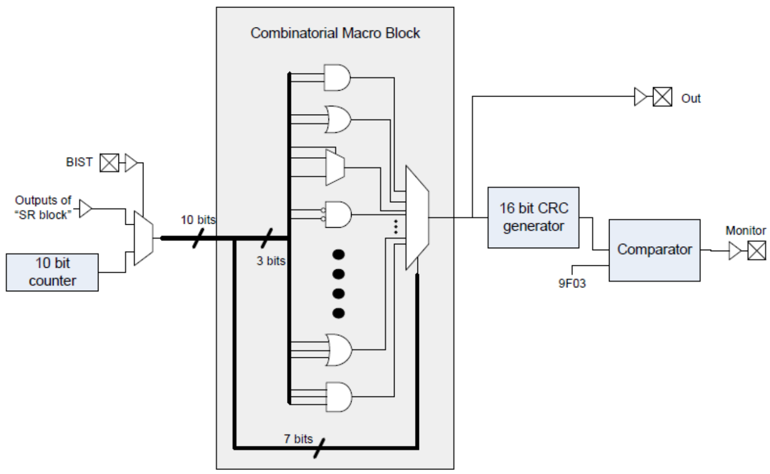

Fig. 38. Combo Block

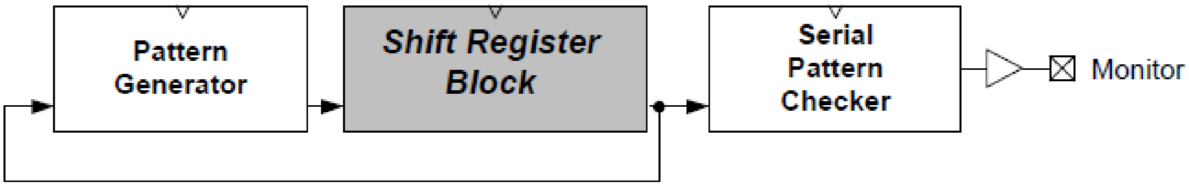

Fig. 39. Shift Register Block

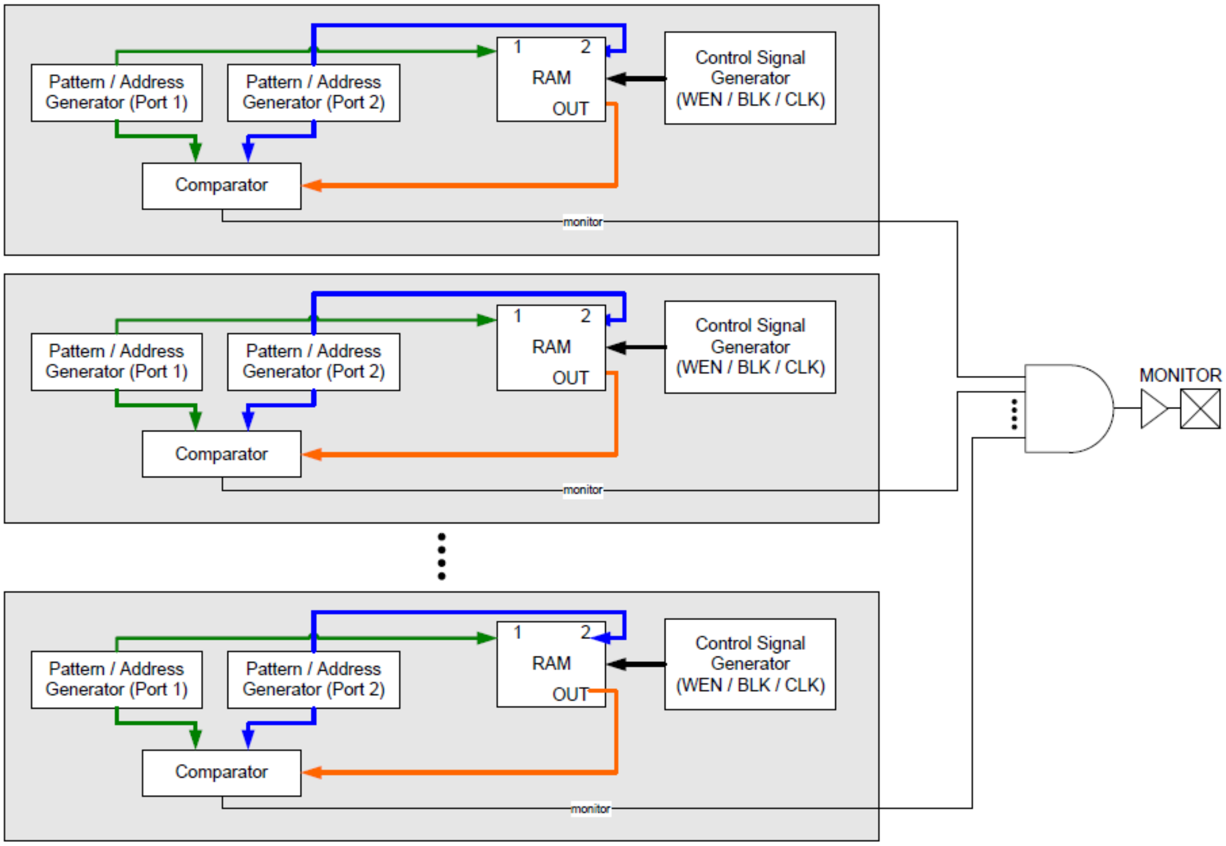

Fig. 40. Embedded Ram Blocks

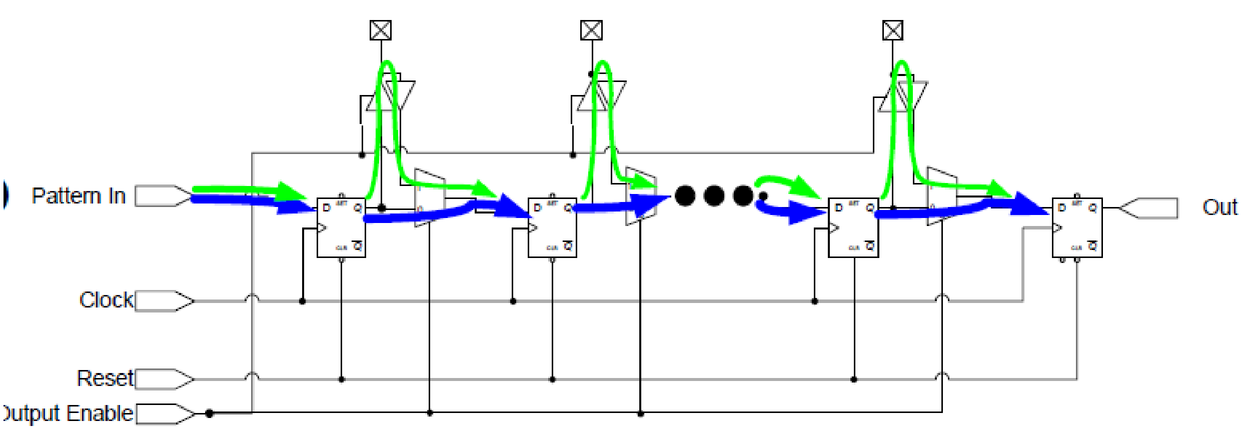

Fig. 41. IO Block

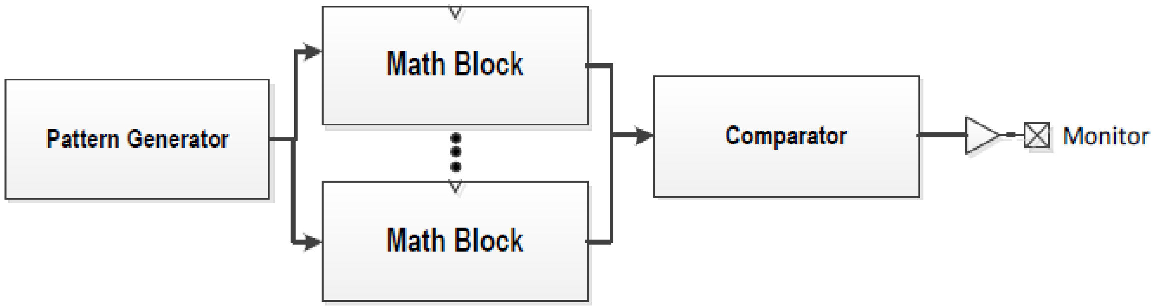

Fig. 42. Math Block

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