
RT PolarFire® FPGA DDR3 Native Interface

Introduction

This application note describes how to perform Write and Read Burst operations to DDR3 memory using Native Interface for different patterns by selecting dip switch ON/OFF (when 00 - increment pattern, when 01 - walking one's pattern, when 10 - walking zero's pattern, and when 11 - decrement pattern) and verify the Write and Read data using SmartDebug tool.

Design Requirements

The following table lists the hardware and software requirements for building a Mi-V processor subsystem.

Design Requirements	Description
Hardware Requirements	
RT PolarFire Evaluation Kit (RTPF500TS-1CG1509M) – 12V/5A AC power adapter and cord – USB 2.0 A to mini-B cable – External FlashPro programmer	Rev 0.1 (Pre-release version)
Software Requirements	
Libero® SoC	See the <code>readme.txt</code> file provided in the design files for all software version needed to create this reference design.

Note: Libero SmartDesign and configuration screenshots provided in this application note are for illustration purpose only. See the provided Libero design to see the latest updates.

Prerequisites

Before you begin:

1. Download and install Libero SoC from the following link: <https://www.microsemi.com/product-directory/design-resources/1750-libero-soc#downloads>
2. Download the reference design files from www.microchip.com/en-us/application-notes/AN4424

Table of Contents

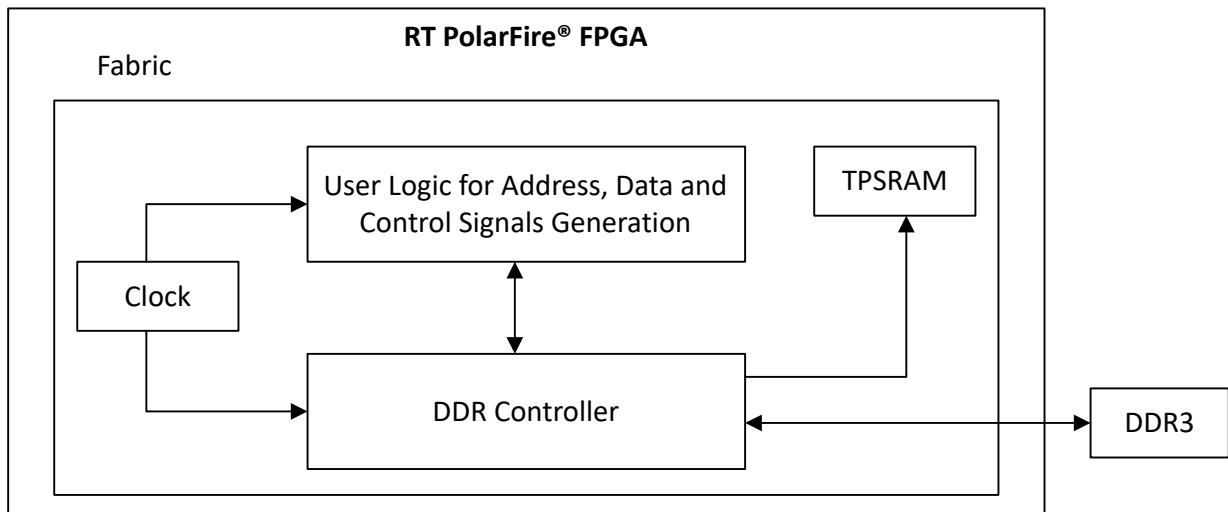
Introduction.....	1
1. Design Requirements.....	1
2. Prerequisites.....	1
1. Design Description.....	3
1.1. Clocking Structure.....	4
1.2. Reset Structure.....	4
2. Design Implementation.....	5
2.1. PF_INIT_MONITOR.....	5
2.2. PF_CCC_0 Configuration.....	5
2.3. DDR3 Configuration.....	6
2.4. TPSRAM Configuration.....	7
2.5. User Logic	8
3. Running the Demo.....	9
3.1. Programming the Device using Libero SoC.....	9
3.2. Running the Design.....	9
4. Appendix: Programming the Device using FlashPro Express.....	12
5. Appendix: Running the TCL Script.....	13
6. Revision History.....	14
Microchip FPGA Support.....	15
The Microchip Website.....	15
Product Change Notification Service.....	15
Customer Support.....	15
Microchip Devices Code Protection Feature.....	15
Legal Notice.....	16
Trademarks.....	16
Quality Management System.....	17
Worldwide Sales and Service.....	18

1. Design Description

This application note describes how to access DDR3 memory by configuring DDR3 controller using Native Interface mode. By writing control logic (Verilog), DDR3 Native Interface is accessed for 16-bit or 32-bit data widths. 32-bit data width is used in this application note. In the design, user logic generates burst transfer size, start address, and data along with proper control signals—Write request, Read request, Busy, and Read valid. When Write request is 1, the input data is written based on the selected pattern. Start address of the burst transfer is required for the controller to generate address based on data width and burst transfer size. When Read valid is 1, controller reads the output data from DDR memory. The start address of the burst transfer is required. The data written at particular address matches with the data output of same read address during Read operation. To verify the DDR output data, connect DDR read valid signal to LSRAM write enable and DDR output data to LSRAM Write data input. Use SmartDebug tool and monitor the LSRAM data based on incremental, decremental, walking one or walking zeros pattern to verify the DDR3 output data. The DDR3 part number used for this application is MT8KTF51264AZ-1G9 (4 GB).

The following figure shows the top-level block diagram of the design.

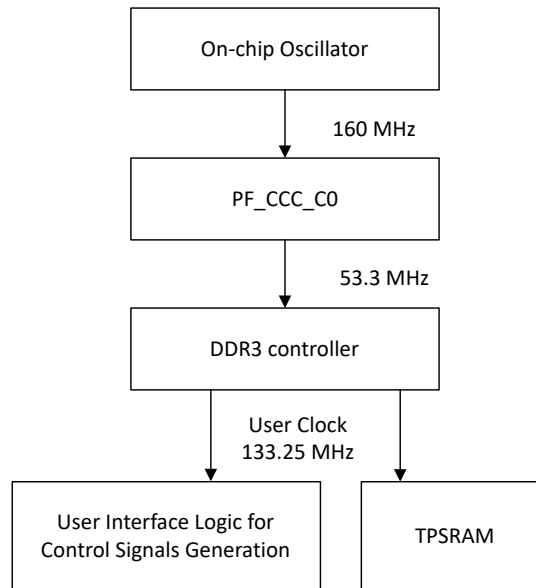
Figure 1-1. Top-level Block Diagram



1.1 Clocking Structure

The 160 MHz on-chip oscillator is connected to the PF_CCC block, which generates 53.3 MHz system clock to DDR3 controller. The 133.25 MHz user clock drives the user interface logic and TPSRAM from DDR3 controller. The following figure shows the clocking structure.

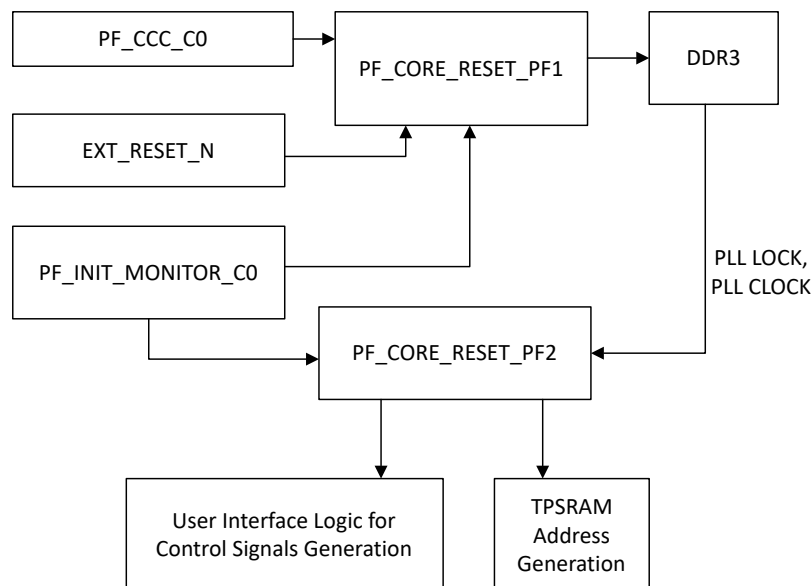
Figure 1-2. Clocking Structure



1.2 Reset Structure

In this reference design, PF_CORE_RESET_PF1 generates the reset signal to DDR3 controller and PF_CORE_RESET_PF2 generates the reset signal to the user logic and TPSRAM. The following figure shows the reset structure.

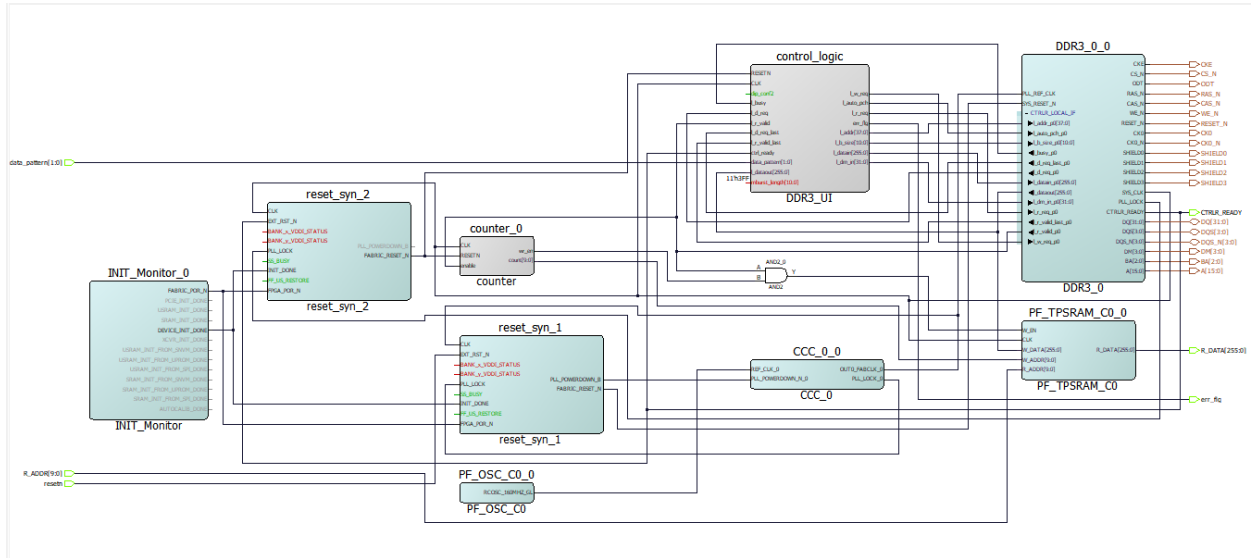
Figure 1-3. Reset Structure



2. Design Implementation

This section shows the Libero design implementation, describes IPs used and their configurations. The following figure shows the design implementation in Libero.

Figure 2-1. DDR3 Native Interface SmartDesign



The following IPs are used in this SmartDesign. The IP cores that are not described in the following section keep the default configuration.

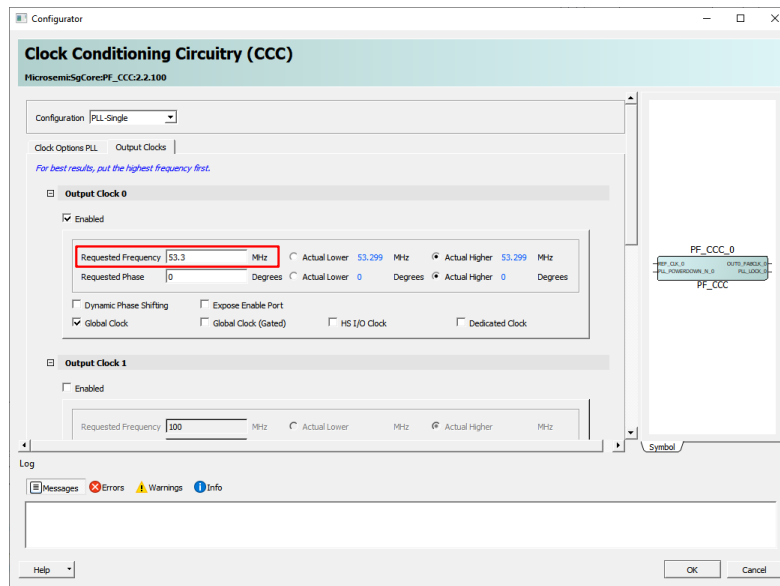
2.1 PF_INIT_MONITOR

The PolarFire Initialization Monitor indicates the status of device initialization.

2.2 PF_CCC_0 Configuration

The PolarFire Clock Conditioning Circuitry (CCC) block receives an input clock of 160 MHz from the on-chip oscillator and generates a 53.3 MHz Fabric clock to DDR controller and user logic. Set **53.3 MHz** as the output frequency as highlighted in the following figure.

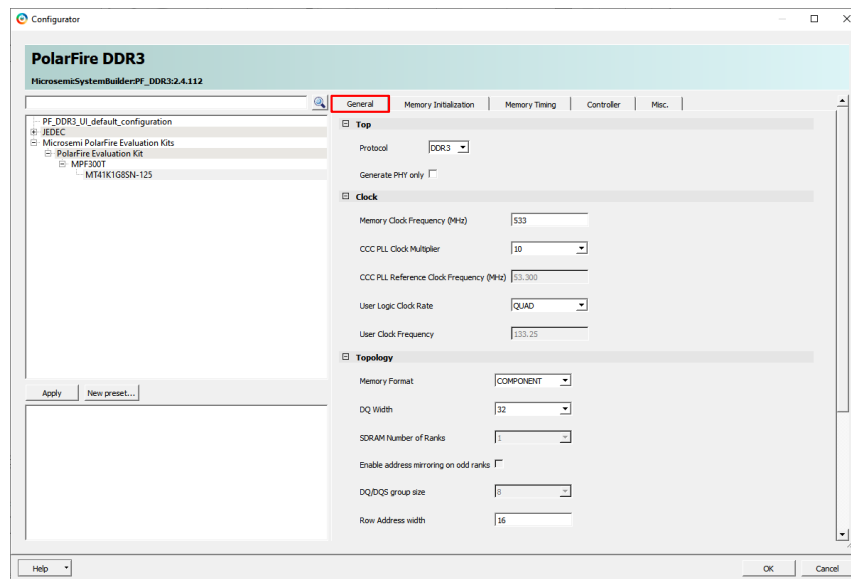
Figure 2-2. CCC Configurator



2.3 DDR3 Configuration

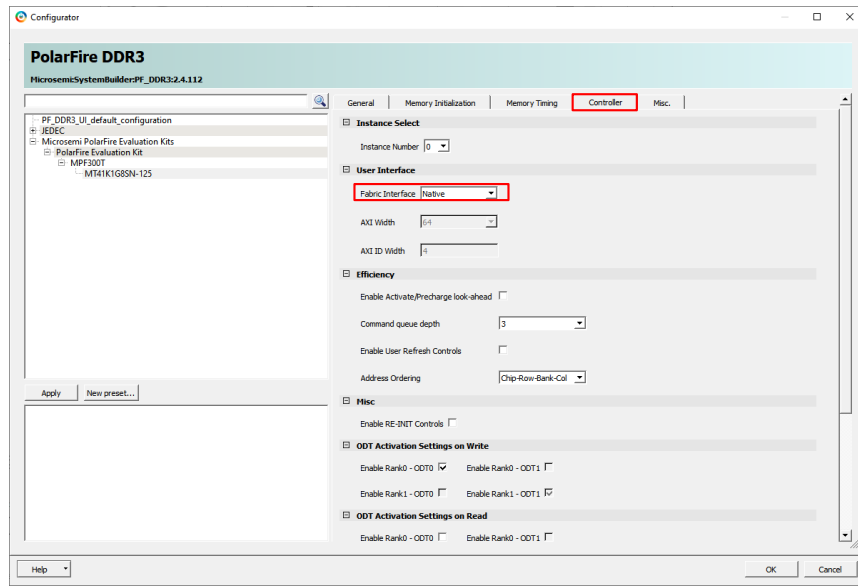
DDR3 controller is configured in Native Interface mode with a data rate of 1066 Mbps, **32-bit** as **DQ Width** (data width), and **DDR Memory Clock Frequency** set to **533 MHz** (Maximum data rate supported is 1066 for standard device). The following figure shows the **General** tab of the PolarFire DDR3 configurator.

Figure 2-3. DDR3 Configurator—General Tab



In the **Controller** tab, select **Native** as **Fabric Interface** under User Interface as highlighted in the following figure.

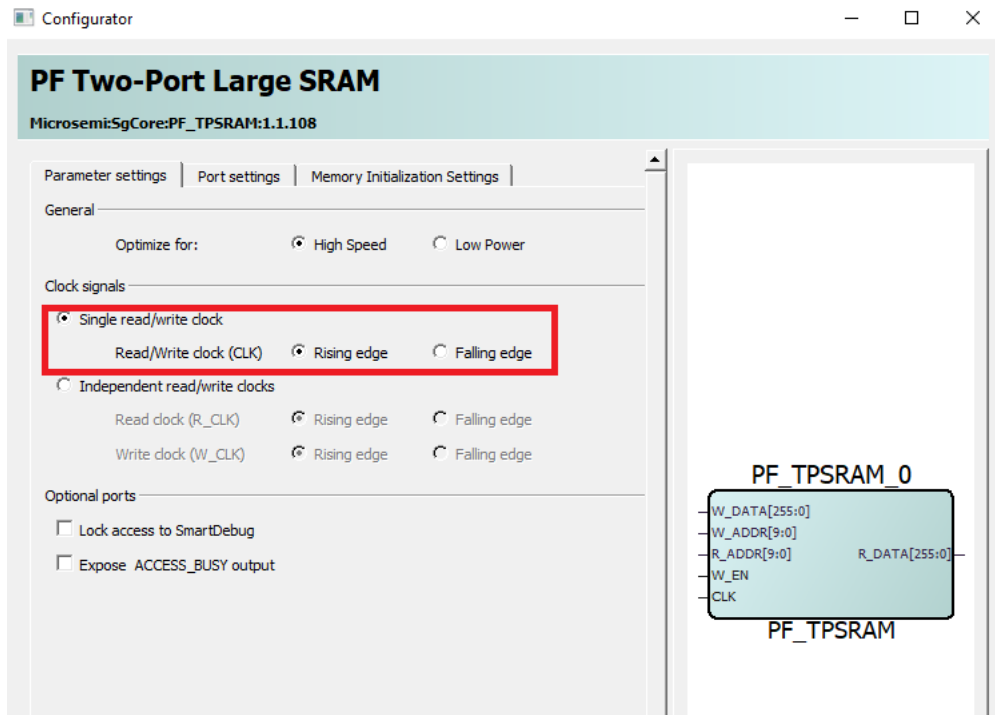
Figure 2-4. DDR3 Configurator—Controller Tab



2.4 TPSRAM Configuration

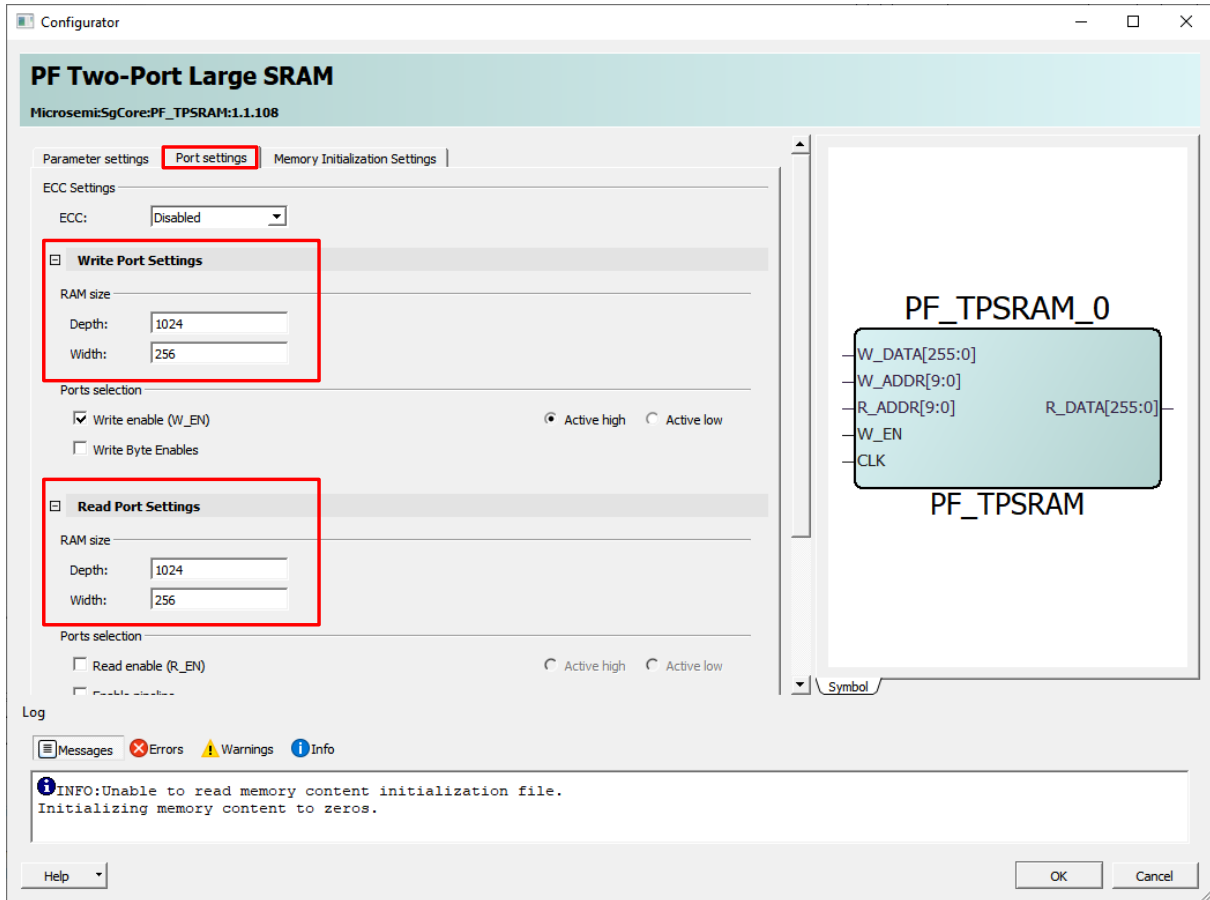
TPSRAM is used to store DDR read data. DDR read data is used as write data input. DDR read valid is used as write enable of TPSRAM. Monitor TPSRAM data in SmartDebug tool to verify the different data patterns such as incremental, decremental, walking ones, and walking zeros that are written in DDR by using native interface logic. In the **Parameter settings** tab, select **Single read/write clock** and **Rising edge** as highlighted in the following figure.

Figure 2-5. TPSRAM Configurator—Parameter Settings Tab



In the **Port Settings** tab, set **1024** as **Depth** and **256** as **Width** for both Read and Write as highlighted in the following figure.

Figure 2-6. TPSRAM Configurator—Port Settings Tab



2.5 User Logic

User logic performs the following:

1. The I_w_req signal is asserted along with the I_addr signal for write operation. In case of multi burst transfer, I_addr is the start address of burst, and the controller increments the address for every clock cycle till it reaches burst size, based on data width.
2. The I_w_req signal is de-asserted, indicating no other write requests are required.
3. As a result of the write request, the subsystem asserts the row address (A), bank address (BA), and chip select (CS_N) to open the bank at the requested row.
4. I_d_req transitions a clock cycle after which subsystem issues the write command with a column address corresponding to the request.
5. The subsystem issues the next write command with the corresponding column address.
6. Controller sends I_d_req data request and then user logic sends I_data_in (input data) to the controller.
7. The written data begins to appear on the SDRAM bus DQ lines.
8. I_r_req is asserted along with the I_addr signal for read operation. In case of multi burst transfer, I_addr is the start address of burst, and the controller increments the address for every clock cycle till it reaches burst size.
9. Controller sends I_r_valid along with output data $I_dataout$ till the address reaches last burst address after I_r_req is asserted.
10. The next write or read operation follows the same sequence from step 1.

3. Running the Demo

This chapter describes steps to program the RT PolarFire device with the 32 KB DDR3 native interface design and detailed procedure for reading and verifying DDR output data through SmartDebug tool.

Before programming the RT PolarFire device, ensure the following settings on the RT PolarFire Evaluation kit:

- Ensure the jumper settings on the board is same as the default jumper settings specified in *RT PolarFire Evaluation Kit User Guide*.
- Connect the host PC to the **J3** connector using the USB cable.
- Connect the power supply to the **J19** connector and switch ON the power supply switch, **SW7**.

3.1 Programming the Device using Libero SoC

To program the device, follow these steps:

1. Open the design in Libero SoC. The Libero **Design Flow** window appears.
2. Double-click **Run PROGRAM Action**. After programming the device successfully, a green tick appears on **Run PROGRAM Action**.

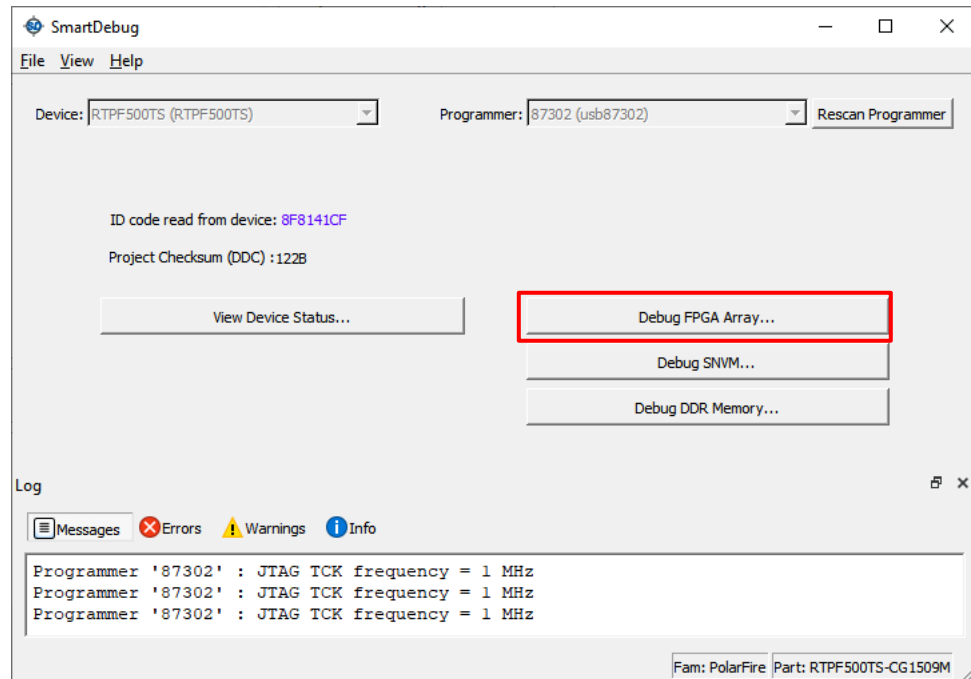
Note: To program the device using FlashPro Express, see [4. Appendix: Programming the Device using FlashPro Express](#).

3.2 Running the Design

Follow these steps to verify the DDR read data using Debug FPGA Array in SmartDebug tool built in the Libero SoC software.

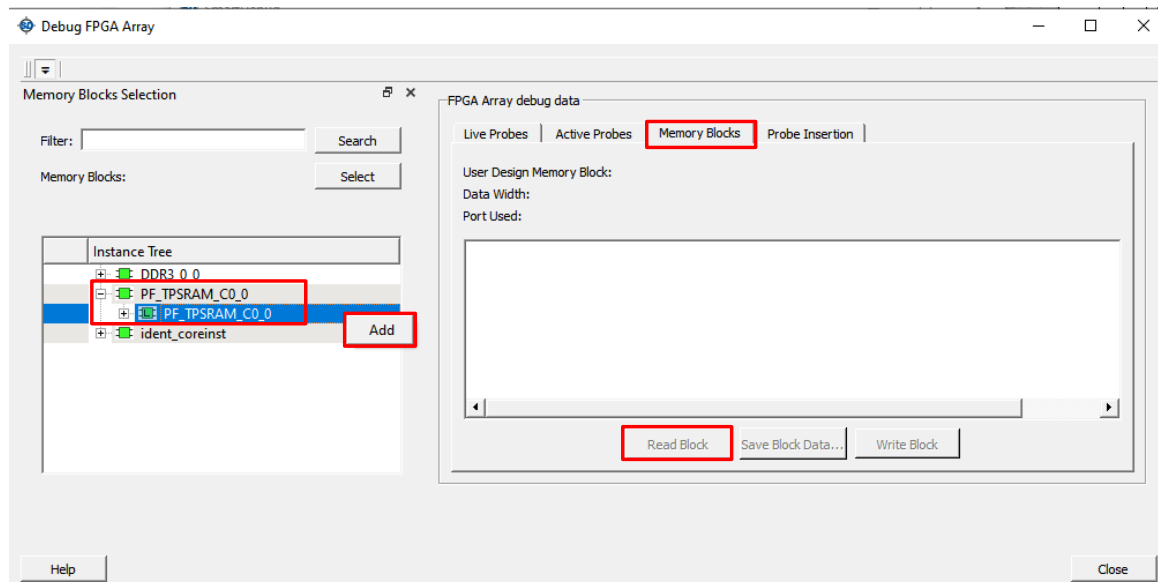
1. In the **Design Flow** tab, double-click **Generate SmartDebug FPGA Array Data**. A green tick appears after successful execution.
2. Double-click **SmartDebug Design**. The SmartDebug window appears.
3. Click **Debug FPGA Array** in the **SmartDebug** window as shown in the following figure. The Debug FPGA Array window appears.

Figure 3-1. SmartDebug Window



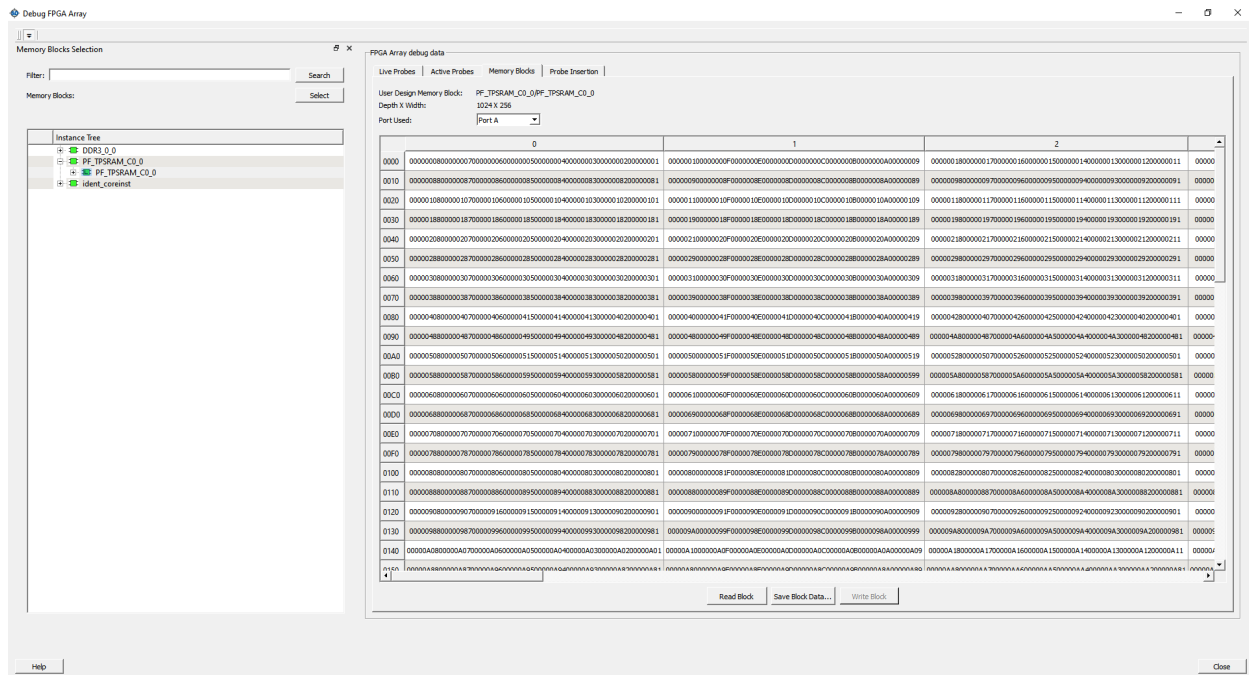
4. In the **Memory Blocks** tab, select **PF_TPSRAM_C0_0** > **Add** and then click **Read Block** as shown in following figure.

Figure 3-2. Debug FPGA Array Window



The DDR read data appears on TPSRAM based pattern selected from the DIP switches. When the DIP switch value is selected as 00 (DIP1 set to 0 and DIP2 set to 0), the incremental data appears in the SmartDebug as shown in the following figure.

Figure 3-3. TPSRAM Data



This concludes the demo.

4. Appendix: Programming the Device using FlashPro Express

This section describes how to program the RT PolarFire device with the .job programming file using FlashPro Express. The .job file is available at the following design files folder location: <download_folder>\Programming_Job

To program the device, complete the following steps:

1. On the host PC, launch the **FlashPro Express** software.
2. Click **New** or select **New Job Project from Project** menu to create a new job project.
3. Enter the following in the **Create New Job Project** dialog box:
 - **Programming job file:** Click **Browse** and navigate to the location where the .job file is located and select the file. The default location is: <download_folder>\Programming_Job
 - **FlashPro Express job project location:** Click **Browse** and navigate to the location where you want to save the project.
4. Click **OK**. The required programming file is selected and ready to be programmed in the device.
5. The **FlashPro Express** window appears. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.
6. Click **RUN** to program the device. When the device is programmed successfully, a **PROGRAMMER(S) PASSED** status is displayed.
7. Close **FlashPro Express**, **Project > Exit**.

See [Running the Demo](#) section to run the demo.

5. Appendix: Running the TCL Script

TCL scripts are provided in the design files folder under directory **TCL_Scripts**. If required, the design flow can be reproduced from Design Implementation before the job file is generated.

To run the TCL, follow these steps:

1. Launch the Libero SoC software.
2. Select **Project > Execute Script...**
3. Click **Browse** and select **script.tcl** from the downloaded TCL_Scripts directory.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within **TCL_Scripts** directory.

For more information about TCL scripts, see **<design_name>/TCL_Scripts/readme.txt**. See [Libero® SoC TCL Command Reference Guide](#) for more details on TCL commands. Contact Technical Support for any queries encountered when running the TCL script.

6. Revision History

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	02/2022	The first publication of the document.

Microchip FPGA Support

Microchip FPGA products group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. Customers are suggested to visit Microchip online resources prior to contacting support as it is very likely that their queries have been already answered.

Contact Technical Support Center through the website at www.microchip.com/support. Mention the FPGA Device Part number, select appropriate case category, and upload design files while creating a technical support case.

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.

- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet- Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, maxCrypto, maxView, memBrain, Mendi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, NVMe Express, NVMe, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQL, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY,

ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, Symmcom, and Trusted Time are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2022, Microchip Technology Incorporated and its subsidiaries. All Rights Reserved.

ISBN: 978-1-5224-9723-3

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com	Australia - Sydney Tel: 61-2-9868-6733 China - Beijing Tel: 86-10-8569-7000 China - Chengdu Tel: 86-28-8665-5511 China - Chongqing Tel: 86-23-8980-9588 China - Dongguan Tel: 86-769-8702-9880 China - Guangzhou Tel: 86-20-8755-8029 China - Hangzhou Tel: 86-571-8792-8115 China - Hong Kong SAR Tel: 852-2943-5100 China - Nanjing Tel: 86-25-8473-2460 China - Qingdao Tel: 86-532-8502-7355 China - Shanghai Tel: 86-21-3326-8000 China - Shenyang Tel: 86-24-2334-2829 China - Shenzhen Tel: 86-755-8864-2200 China - Suzhou Tel: 86-186-6233-1526 China - Wuhan Tel: 86-27-5980-5300 China - Xian Tel: 86-29-8833-7252 China - Xiamen Tel: 86-592-2388138 China - Zhuhai Tel: 86-756-3210040	India - Bangalore Tel: 91-80-3090-4444 India - New Delhi Tel: 91-11-4160-8631 India - Pune Tel: 91-20-4121-0141 Japan - Osaka Tel: 81-6-6152-7160 Japan - Tokyo Tel: 81-3-6880-3770 Korea - Daegu Tel: 82-53-744-4301 Korea - Seoul Tel: 82-2-554-7200 Malaysia - Kuala Lumpur Tel: 60-3-7651-7906 Malaysia - Penang Tel: 60-4-227-8870 Philippines - Manila Tel: 63-2-634-9065 Singapore Tel: 65-6334-8870 Taiwan - Hsin Chu Tel: 886-3-577-8366 Taiwan - Kaohsiung Tel: 886-7-213-7830 Taiwan - Taipei Tel: 886-2-2508-8600 Thailand - Bangkok Tel: 66-2-694-1351 Vietnam - Ho Chi Minh Tel: 84-28-5448-2100	Austria - Wels Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 Denmark - Copenhagen Tel: 45-4485-5910 Fax: 45-4485-2829 Finland - Espoo Tel: 358-9-4520-820 France - Paris Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 Germany - Garching Tel: 49-8931-9700 Germany - Haan Tel: 49-2129-3766400 Germany - Heilbronn Tel: 49-7131-72400 Germany - Karlsruhe Tel: 49-721-625370 Germany - Munich Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 Germany - Rosenheim Tel: 49-8031-354-560 Israel - Ra'anana Tel: 972-9-744-7705 Italy - Milan Tel: 39-0331-742611 Fax: 39-0331-466781 Italy - Padova Tel: 39-049-7625286 Netherlands - Drunen Tel: 31-416-690399 Fax: 31-416-690340 Norway - Trondheim Tel: 47-72884388 Poland - Warsaw Tel: 48-22-3325737 Romania - Bucharest Tel: 40-21-407-87-50 Spain - Madrid Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 Sweden - Gothenberg Tel: 46-31-704-60-40 Sweden - Stockholm Tel: 46-8-5090-4654 UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820