AN4424

RT PolarFire® FPGA DDR3 Native Interface

Introduction

This application note describes how to perform Write and Read Burst operations to DDR3 memory using Native Interface for different patterns by selecting dip switch ON/OFF (when 00 - increment pattern, when 01- walking one's pattern, when 10 -walking zero's pattern, and when 11 - decrement pattern) and verify the Write and Read data using SmartDebug tool.

Design Requirements

The following table lists the hardware and software requirements for building a Mi-V processor subsystem.

Design Requirements	Description
Hardware Requirements	
RT PolarFire Evaluation Kit (RTPF500TS-1CG1509M) – 12V/5A AC power adapter and cord – USB 2.0 A to mini-B cable – External FlashPro programmer	Rev 0.1 (Pre-release version)
Software Requirements	
Libero® SoC	See the `readme.txt` file provided in the design files for all software version needed to create this reference design.

Note: Libero SmartDesign and configuration screenshots provided in this application note are for illustration purpose only. See the provided Libero design to see the latest updates.

Prerequisites

Before you begin:

1. Download and install Libero SoC from the following link: https://www.microsemi.com/product-directory/design-resources/1750-libero-soc#downloads
2. Download the reference design files from www.microchip.com/en-us/application-notes/AN4424

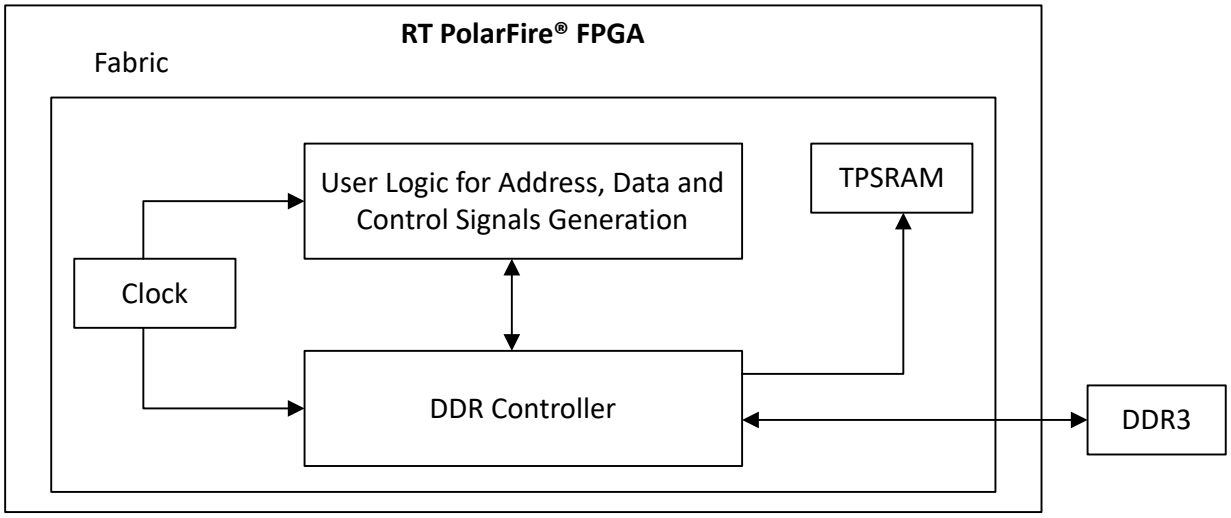
Table of Contents

1. Design Description

This application note describes how to access DDR3 memory by configuring DDR3 controller using Native Interface mode. By writing control logic (Verilog), DDR3 Native Interface is accessed for 16-bit or 32-bit data widths. 32-bit data width is used in this application note. In the design, user logic generates burst transfer size, start address, and data along with proper control signals—Write request, Read request, Busy, and Read valid. When Write request is 1, the input data is written based on the selected pattern. Start address of the burst transfer is required for the controller to generate address based on data width and burst transfer size. When Read valid is 1, controller reads the output data from DDR memory. The start address of the burst transfer is required. The data written at particular address matches with the data output of same read address during Read operation. To verify the DDR output data, connect DDR read valid signal to LSRAM write enable and DDR output data to LSRAM Write data input. Use SmartDebug tool and monitor the LSRAM data based on incremental, decremental, walking one or walking zeros pattern to verify the DDR3 output data. The DDR3 part number used for this application is MT8KTF51264AZ-1G9 (4 GB).

The following figure shows the top-level block diagram of the design.

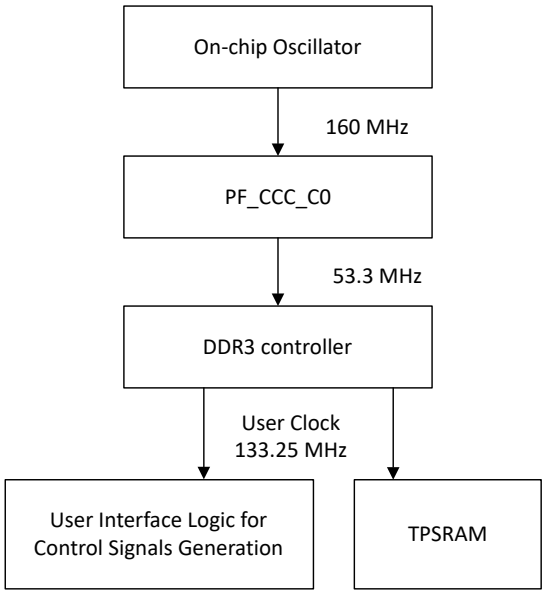
Figure 1-1. Top-level Block Diagram



1.1 Clocking Structure

The 160 MHz on-chip oscillator is connected to the PF_CCC block, which generates 53.3 MHz system clock to DDR3 controller. The 133.25 MHz user clock drives the user interface logic and TPSRAM from DDR3 controller. The following figure shows the clocking structure.

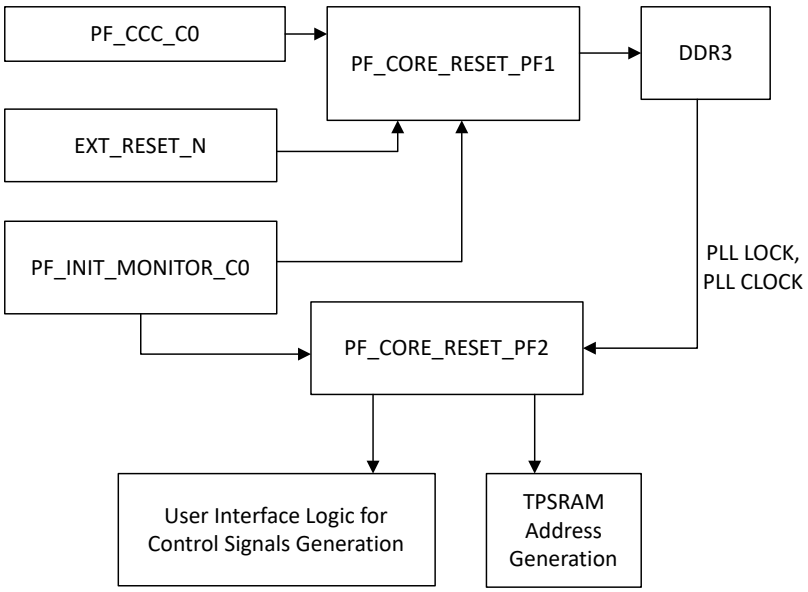
Figure 1-2. Clocking Structure



1.2 Reset Structure

In this reference design, PF_CORE_RESET_PF1 generates the reset signal to DDR3 controller and PF_CORE_RESET_PF2 generates the reset signal to the user logic and TPSRAM. The following figure shows the reset structure.

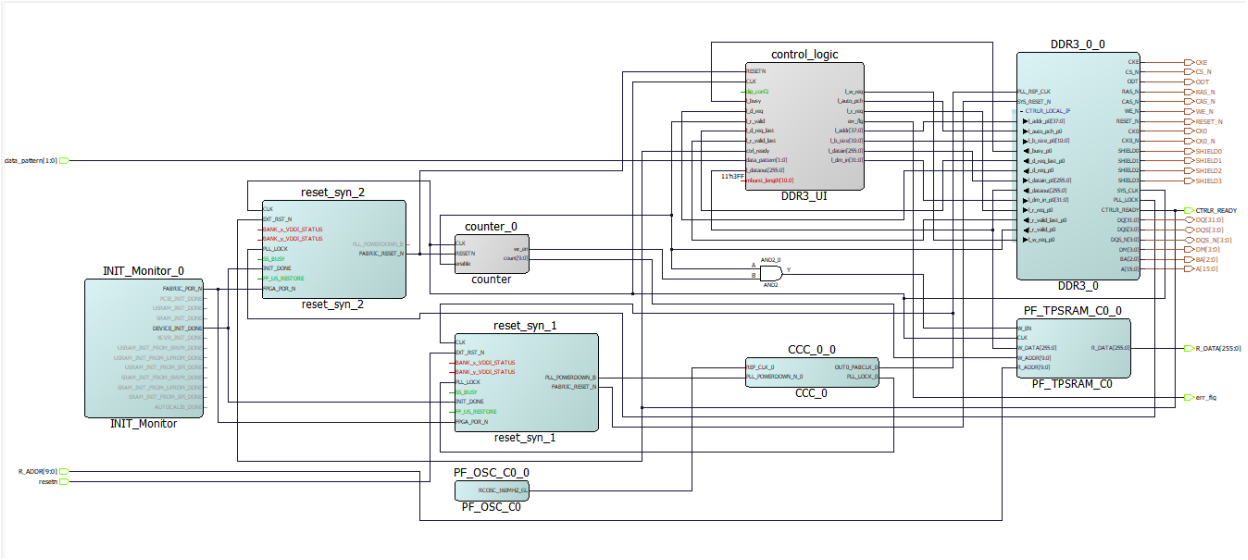
Figure 1-3. Reset Structure



2. Design Implementation

This section shows the Libero design implementation, describes IPs used and their configurations. The following figure shows the design implementation in Libero.

Figure 2-1. DDR3 Native Interface SmartDesign



The following IPs are used in this SmartDesign. The IP cores that are not described in the following section keep the default configuration.

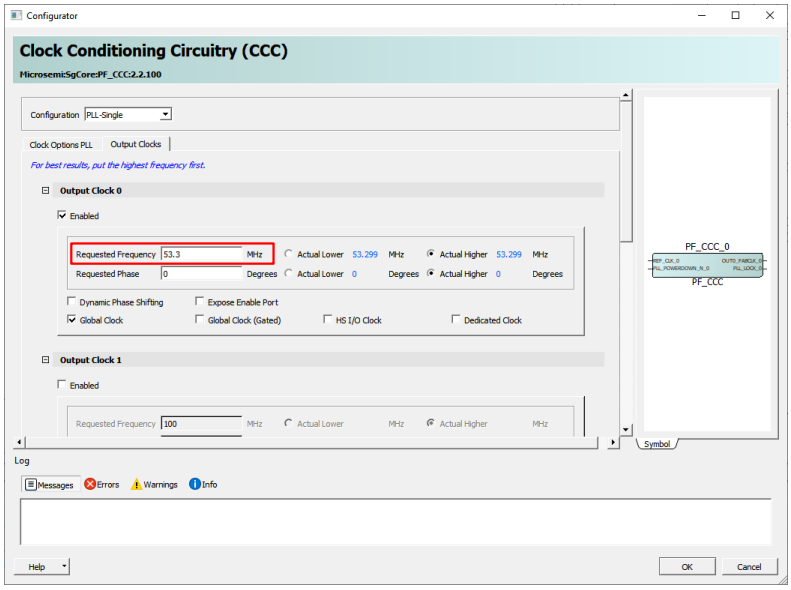
2.1 PF_INIT_MONITOR

The PolarFire Initialization Monitor indicates the status of device initialization.

2.2 PF_CCC_0 Configuration

The PolarFire Clock Conditioning Circuitry (CCC) block receives an input clock of 160 MHz from the on-chip oscillator and generates a 53.3 MHz Fabric clock to DDR controller and user logic. Set **53.3** MHz as the output frequency as highlighted in the following figure.

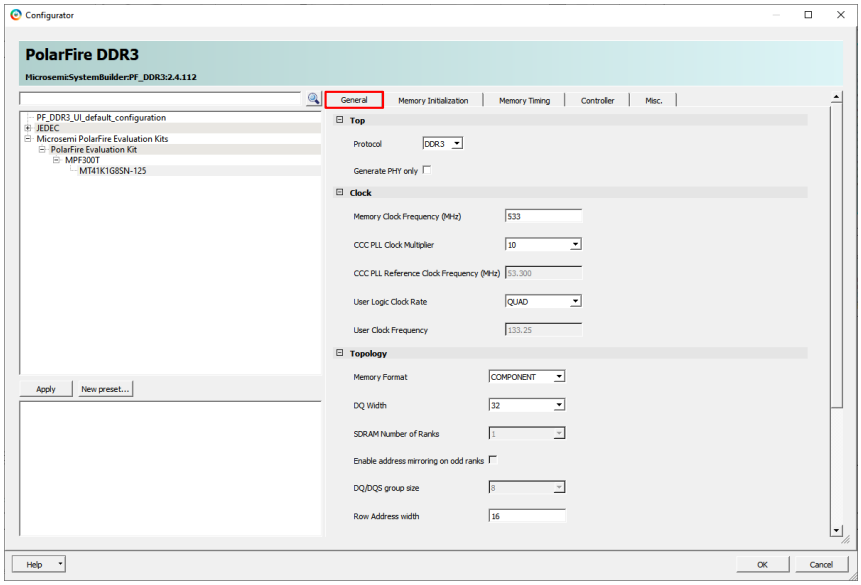
Figure 2-2. CCC Configurator



2.3 DDR3 Configuration

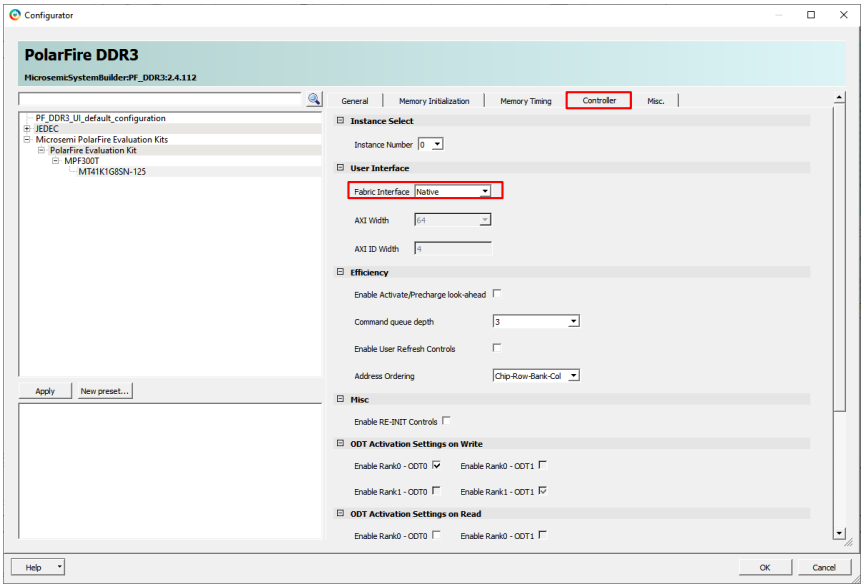
DDR3 controller is configured in Native Interface mode with a data rate of 1066 Mbps, **32-bit** as **DQ Width** (data width), and DDR **Memory Clock Frequency** set to **533** MHz (Maximum data rate supported is 1066 for standard device).The following figure shows the **General** tab of the PolarFire DDR3 configurator.

Figure 2-3. DDR3 Configurator—General Tab



In the **Controller** tab, select **Native** as **Fabric Interface** under User Interface as highlighted in the following figure.

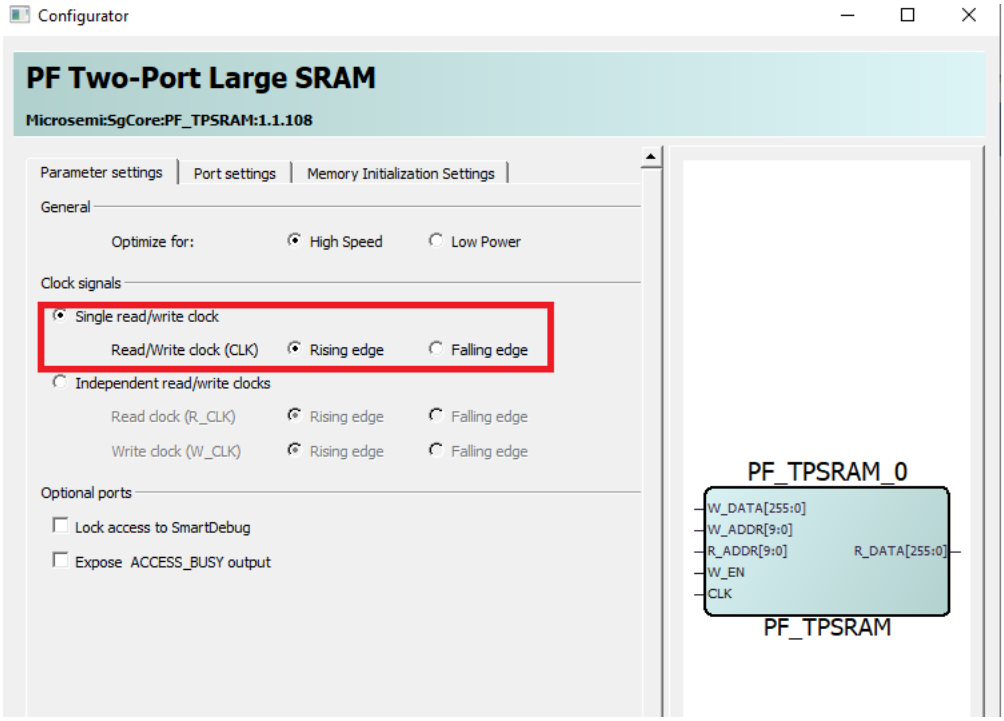
Figure 2-4. DDR3 Configurator—Controller Tab



2.4 TPSRAM Configuration

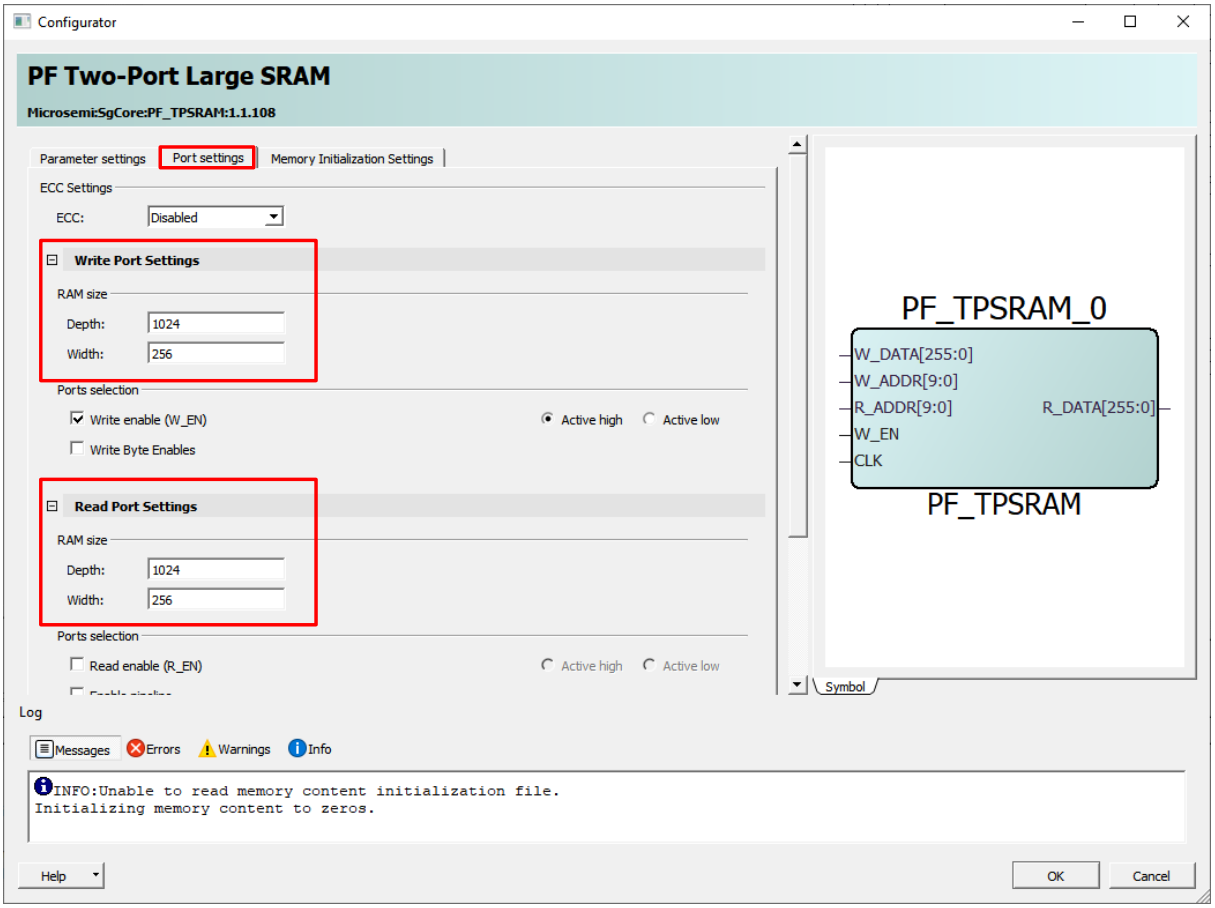
TPSRAM is used to store DDR read data. DDR read data is used as write data input. DDR read valid is used as write enable of TPSRAM. Monitor TPSRAM data in SmartDebug tool to verify the different data patterns such as incremental, decremental, walking ones, and walking zeros that are written in DDR by using native interface logic. In the **Parameter settings** tab, select **Single read/write clock** and **Rising edge** as highlighted in the following figure.

Figure 2-5. TPSRAM Configurator—Parameter Settings Tab



In the **Port Settings** tab, set **1024** as **Depth** and **256** as **Width** for both Read and Write as highlighted in the following figure.

Figure 2-6. TPSRAM Configurator—Port Settings Tab



2.5 User Logic

User logic performs the following:

1. The l_w_req signal is asserted along with the l_addr signal for write operation. In case of multi burst transfer, l_addr is the start address of burst, and the controller increments the address for every clock cycle till it reaches burst size, based on data width.
2. The l_w_req signal is de-asserted, indicating no other write requests are required.
3. As a result of the write request, the subsystem asserts the row address (A), bank address (BA), and chip select (CS_N) to open the bank at the requested row.
4. l_d_req transitions a clock cycle after which subsystem issues the write command with a column address corresponding to the request.
5. The subsystem issues the next write command with the corresponding column address.
6. Controller sends l_d_req data request and then user logic sends l_data_in (input data) to the controller.
7. The written data begins to appear on the SDRAM bus DQ lines.
8. l_r_req is asserted along with the l_addr signal for read operation. In case of multi burst transfer, l_addr is the start address of burst, and the controller increments the address for every clock cycle till it reaches burst size.
9. Controller sends l_r_valid along with output data l_dataout till the address reaches last burst address after l_r_req is asserted.
10. The next write or read operation follows the same sequence from step 1.

3. Running the Demo

This chapter describes steps to program the RT PolarFire device with the 32 KB DDR3 native interface design and detailed procedure for reading and verifying DDR output data through SmartDebug tool.

Before programming the RT PolarFire device, ensure the following settings on the RT PolarFire Evaluation kit:

- Ensure the jumper settings on the board is same as the default jumper settings specified in *RT PolarFire Evaluation Kit User Guide*.
- Connect the host PC to the **J3** connector using the USB cable.
- Connect the power supply to the **J19** connector and switch ON the power supply switch, **SW7**.

3.1 Programming the Device using Libero SoC

To program the device, follow these steps:

1. Open the design in Libero SoC. The Libero **Design Flow** window appears.
2. Double-click **Run PROGRAM Action**. After programming the device successfully, a green tick appears on **Run PROGRAM Action**.

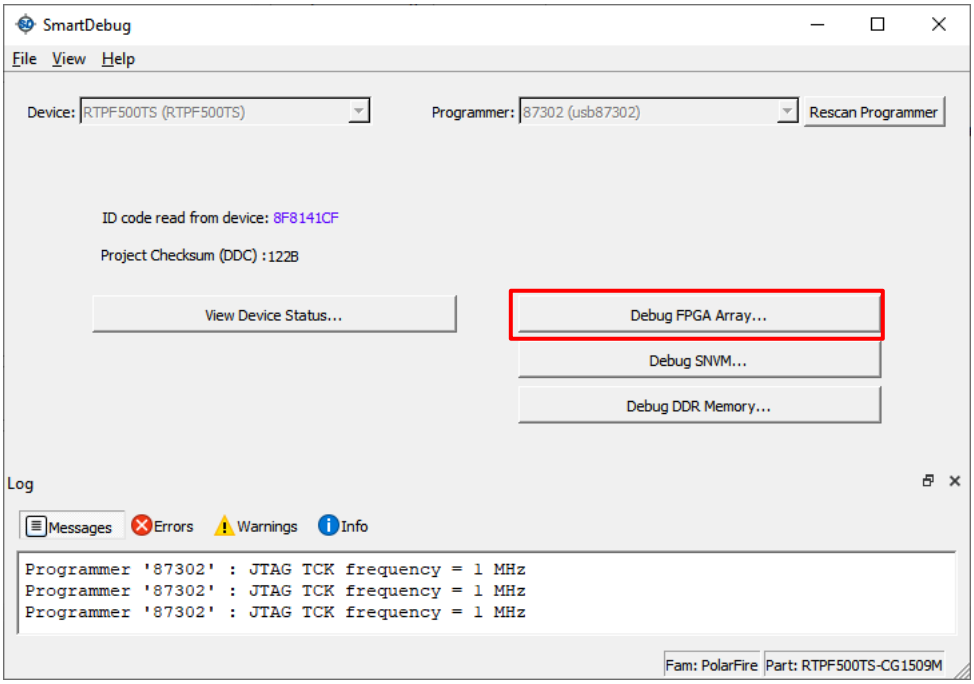
Note: To program the device using FlashPro Express, see 4. Appendix: Programming the Device using FlashPro Express.

3.2 Running the Design

Follow these steps to verify the DDR read data using Debug FPGA Array in SmartDebug tool built in the Libero SoC software.

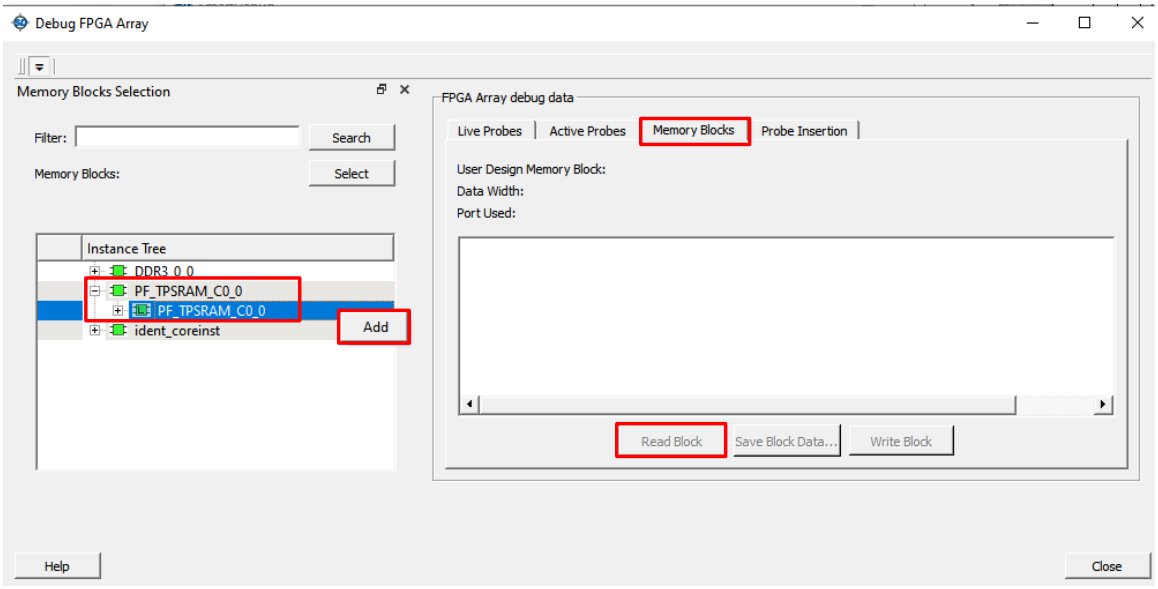
1. In the **Design Flow** tab, double-click **Generate SmartDebug FPGA Array Data**. A green tick appears after successful execution.
2. Double-click **SmartDebug Design**. The SmartDebug window appears.
3. Click **Debug FPGA Array** in the **SmartDebug** window as shown in the following figure. The Debug FPGA Array window appears.

Figure 3-1. SmartDebug Window



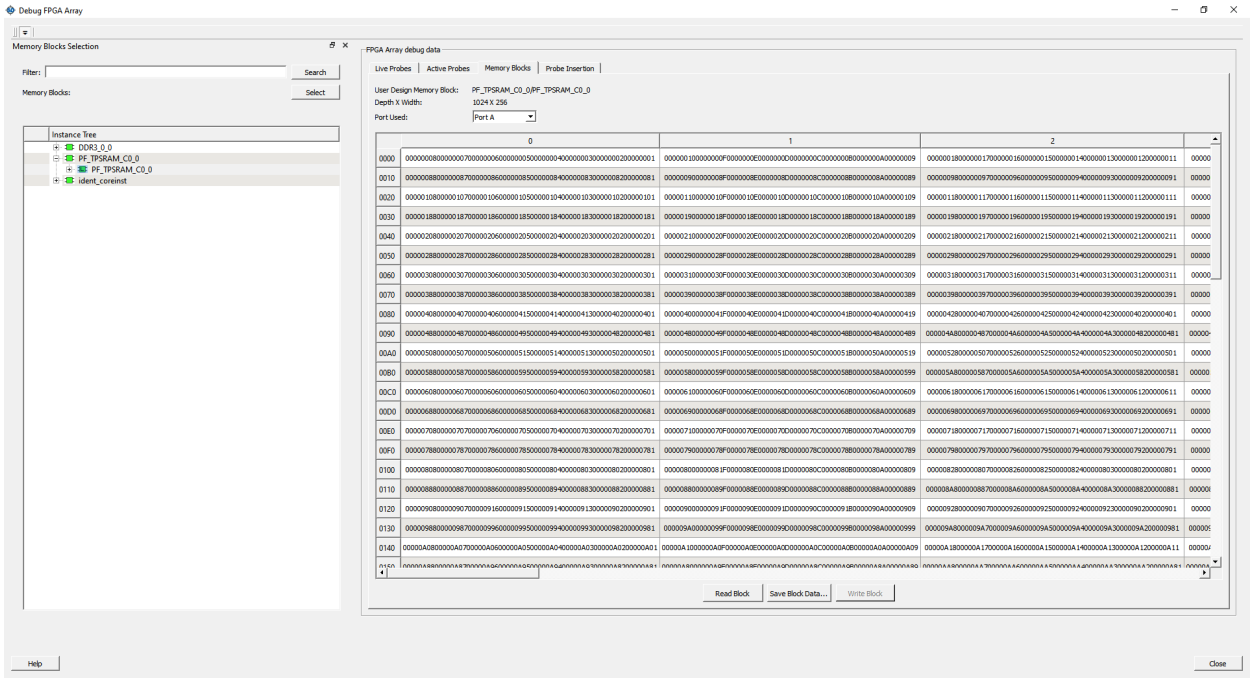
4. In the **Memory Blocks** tab, select **PF_TPSRAM_C0_0** > **Add** and then click **Read Block** as shown in following figure.

Figure 3-2. Debug FPGA Array Window



The DDR read data appears on TPSRAM based pattern selected from the DIP switches. When the DIP switch value is selected as 00 (DIP1 set to 0 and DIP2 set to 0), the incremental data appears in the SmartDebug as shown in the following figure.

Figure 3-3. TPSRAM Data



This concludes the demo.

4. Appendix: Programming the Device using FlashPro Express

This section describes how to program the RT PolarFire device with the `.job` programming file using FlashPro Express. The `.job` file is available at the following design files folder location: <*download_folder*>*Programming_Job*

To program the device, complete the following steps:

1. On the host PC, launch the **FlashPro Express** software.
2. Click **New** or select **New Job Project from Project** menu to create a new job project.
3. Enter the following in the **Create New Job Project** dialog box:
   - **Programming job file**: Click **Browse** and navigate to the location where the `.job` file is located and select the file. The default location is: <*download_folder*>*Programming_Job*
   - **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project.
4. Click **OK**. The required programming file is selected and ready to be programmed in the device.
5. The **FlashPro Express** window appears. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.
6. Click **RUN** to program the device. When the device is programmed successfully, a **PROGRAMMER(S) PASSED** status is displayed.
7. Close **FlashPro Express**, **Project** > **Exit**.

See Running the Demo section to run the demo.

5. Appendix: Running the TCL Script

TCL scripts are provided in the design files folder under directory **TCL_Scripts**. If required, the design flow can be reproduced from Design Implementation before the job file is generated.

To run the TCL, follow these steps:

1. Launch the Libero SoC software.
2. Select **Project > Execute Script....**
3. Click **Browse** and select **script.tcl** from the downloaded TCL_Scripts directory.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within **TCL_Scripts** directory.

For more information about TCL scripts, see ***<design_name>/TCL_Scripts/readme.txt.*** See Libero® SoC TCL Command Reference Guide for more details on TCL commands. Contact Technical Support for any queries encountered when running the TCL script.

6. Revision History

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	02/2022	The first publication of the document.

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