

RT PolarFire[®] FPGA Interoperability with TI ADC12DJ3200 using JESD204B Protocol

Introduction

As the resolution and speed of converters have increased, the demand for a more efficient interface has grown. The JESD204 interface brings this efficiency and offers several advantages over its CMOS and LVDS predecessors in terms of speed, size, and cost. Microchip provides interfacing solutions for analog-to-digital converter (ADC) and digital-to-analog converter (DAC) devices using the JESD204B JEDEC[®] standards. These interfacing solutions are provided as Direct Core soft IPs (CoreJESD204BRX and CoreJESD204BTX) in the Libero[®] SoC software. These IP cores interface with transceivers of RT PolarFire[®] FPGA devices.

The application note demonstrates the interoperability of RT PolarFire FPGA with 12-bit, dual-channel Texas Instruments (TI) ADC12DJ3200 device using JESD204B protocol. The ADC12DJ3200 device supports the JESD204B serial interface with data rates up to 12.8 Gbps with two or four lanes per ADC. In this application, an analog signal is transmitted through the ADC12DJ3200 EVM and received at the JESD204B Rx IP output on RT PolarFire FPGA. This application note describes the RT PolarFire FPGA design, JESD204B link parameters, hardware test setup, and equipment used for this interoperability test.

Design Requirements

The following table lists the hardware and software requirements for this demo design.

Table 1. Design Requirements

Requirement	Description
Hardware	
 RT PolarFire Evaluation Kit (RTPF500TS-1CG1509M) 12V DC - Power supply adapter External FlashPro 4 Programmer 	Rev 0.1 (Pre-release Version)
ADC12DJ3200EVM Evaluation Board5V DC - Power supply adapterUSB A to Mini-B cable	Rev A
Function generator	-
SMA cable	_
Host PC or Laptop with 64-bit Windows 10	—
Software	
ADC12DJ3200EVM Configuration GUI	_
Libero SoC	See the readme.txt file provided in the design files for the software versions used with this reference design.

Note: Libero SmartDesign and configuration screenshots provided in this application note are for illustration purpose only. See the provided Libero design for the latest updates.

Prerequisites

Before you begin:

- 1. Download and install Libero SoC from the following location: https://www.microsemi.com/product-directory/ design-resources/1750-libero-soc#downloads
- 2. For demo design files download: www.microchip.com/en-us/application-notes/AN4400

References

- CoreJESD204BRX IP Handbook
- CoreJESD204BTX IP Handbook
- ADC12DJ3200EVM
- Identify ME User Guide

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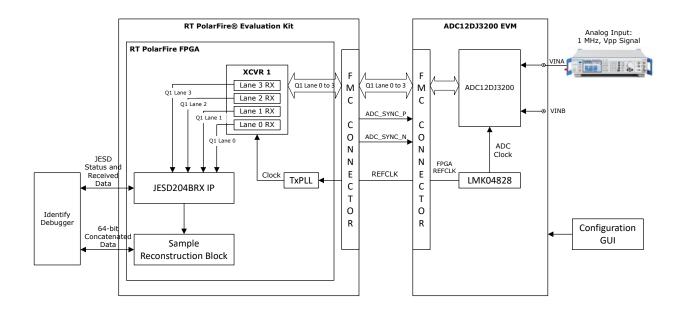
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1. Design Description

The following figure shows the high-level block diagram of RT PolarFire FPGA interoperability with ADC12DJ3200.

The analog input signal is provided to ADC12DJ3200 EVM evaluation board. The ADC12DJ3200 device on the EVM is dual channel, 12-bit ADC, capable of operating at sampling rates up to 3.2 Giga-samples per second (GSPS) in dual channel mode or 6.4 GSPS in single channel mode. The on-board clock generator, LMK04828, generates ADC and FPGA reference clocks for the high-speed serial interface. The ADC12DJ3200 device output data is transmitted over a standard JESD204B high-speed serial interface. ADC JESD204B block transmits the serial data to the RT PolarFire FPGA through FMC connectors. The serial data is received at the FPGA side where it is passed through the XCVR block and further to the CoreJESD204BRx IP block. The digital data from CoreJESD204BRx IP block is sent to sampling reconstruction block, which converts the digital data into analog samples needed to reconstruct the analog signal. This can be monitored on the Identify Debugger.

Figure 1-1. High-level Block Diagram



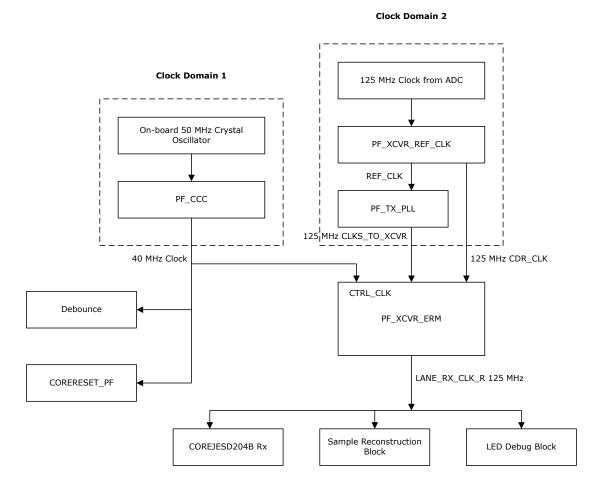
1.1 Clocking Structure

In the reference design, there are two clock domains. The on-board 50 MHz crystal oscillator is connected to the PF_CCC module, which generates 40 MHz. The 40 MHz clock is sourced to CORERESET_PF, Debounce, and CTRL_CLK input of PF_XCVR_ERM module for Enhanced Receiver Management (ERM) logic.

125 MHz differential clock from ADC12DJ3200 EVM drives the PF_XCVR_REF_CLK where differential clock is converted to single-ended clock. This single-ended clock is provided as a reference clock to PF_TX_PLL and CDR in the PF_XCVR_ERM. Recovered clock LANEx_RX_CLK_R is provided to COREJESD204BRx, sample reconstruction module, and LED debug module.

The following figure shows the clocking structure.

Figure 1-2. Clocking Structure

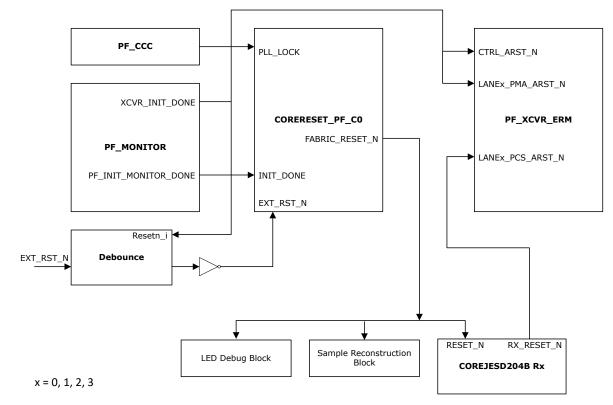


1.2 Reset Structure

In this reference design, CORERESET_PF module generates reset signal to the COREJESD204BRx, sampling reconstruction module, and LED debug module. INIT_DONE input to CORERESET_PF is provided from PF_INIT_MONITOR module whereas EXT_RST_N input is NOT output of the Debounce logic. Input to Debounce logic is connected to the user reset on the RT PolarFire Evaluation kit. XCVR_INIT_DONE output from PF_INIT_MONITOR provides reset to CTRL_ARST_N, LANEx_PMA_ARST_N inputs of PF_XCVR_ERM module. RX_RESET_N output from COREJESD204BRx provides reset to LANEx_PCS_ARST_N inputs of PF_XCVR_ERM module.

The following figure shows the reset structure.

Figure 1-3. Reset Structure

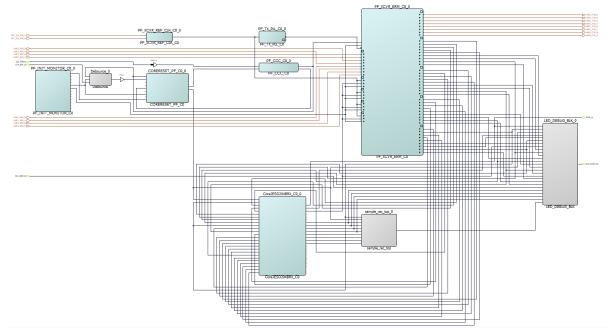


1.3 Design Implementation

This section describes the Libero deisgn implementation, describes IPs used and their configurations. This section also describes the ADC12DJ3200 EVM GUI configuration.

The following figure shows the design implementation in Libero SoC software.

Figure 1-4. JESD204BRx Interface Design



The following IPs are used in this SmartDesign:

- PF_INIT_MONITOR: Indicates the completion of device boot, design and memory initialization by the System Controller. The device initialization includes Fabric, PCIe, Transceiver, SRAM initialization from uPROM/ sNVM/SPI Flash. DEVICE_INIT_DONE is used as a reset to COREJESD204BRx IP and other Fabric modules. XCVR_INIT_DONE is used as a reset to XCVR IP.
- 2. **CORERESET_PF:** Generates a Reset, which is asserted asynchronously and negates synchronously to a specified clock.
- 3. **PF_CCC:** Macro to access PolarFire CCC block. It is used to synthesize 40 MHz clock frequency from the CCC with an on-board 50 MHz reference clock.
- 4. **PF_XCVR_REF_CLK:** The Transceiver Reference Clock Configurator is used to build the correct reference clock input to the transceiver and to the Tx PLL. The user can pick the input type and various input options from the GUI.
- 5. **PF_TX_PLL:** Generates the TxPLL/TxPLL_SSC based on the input provided to the GUI. PF_TX_PLL generates BIT_CLK for the transceiver.
- 6. **PF_XCVR_ERM:** This is a hard IP block that supports high-speed data rates ranging from 250 Mbps to 12.5 Gbps. In this design, the transceiver block (PF_XCVR) is configured in 8b10b mode with a CDR reference clock of 125 MHz to support 5 Gbps data rate. XCVR configuration settings are as follows:
 - Number of Lanes: 4
 - Enhanced receiver management: Enabled
 - Receiver calibration: None (CDR)
 - Transceiver data rate: 5 Gbps
 - TX clock division factor: 1
 - TX PPLL base data rate: 5 Gbps
 - TX PLL bit lock frequency: 2.5 Gbps

- CDR Lock Mode: Lock to data
- CDR Reference Clock Source: Dedicated
- CDR Reference Clock Frequency: 125 MHz
- PCS-Fabric interface width: 32-bit
- 8b/10b Encoding/Decoding: Enabled
- FPGA interface frequency: 125 MHz
- 7. **CoreJESD204BRX:** This is the receiver interface of the JEDEC JESD204B standards. The core configuration of this IP core is as follows:
 - Decoder: Removed
 - Data Width: 32
 - Serdes Mode: 1
 - Scrambling: Enabled
 - Device Subclass Version: Subclass 0
 - JESD204 version: JESD204B
 - No. of Lanes (L+1): 4
 - Checksum calculation type: Octet
 - Frame Alignment Correction: Enabled
 - Link Configuration Error: Enabled
 - RAM Implementation: In LSRAM
 - No. of Octets per Frame: 8
 - No. of Frames per Multi-frame: 4
 - No. of Multi-frames in ILA sequence:4

Note: For information about CoreJESD204BRX Core Link configuration parameters, see Table 2-1.

Debounce logic RTL block is implemented to remove the switch bounces and generates a single pulse to the design when the user reset push button is pressed on the board. Sample reconstruction module is implemented to concatenate two 32-bit JESD output data and frame into 64-bit output. This is done to reconstruct the analog input from the ADC12DJ3200 EVM. The LED_DEBUG_BLK block is used to debug the JESD and XCVR signal status.

The following figure shows the ADC12DJ3200 EVM GUI that is used to program the ADC and clocks.

Figure 1-5. ADC12DJ3200 GUI - EVM Tab

				AD	C12DJxx	00 GUI		Select the device ADC12DJ3200	~
VM	Control	JESD204B	NCO Configuration	Trim	LMK04828	LMX2582	Low Level View	USB Status 🧿	🌼 Reconne
User	Inputs		START HE	RE!					
#2a. #2b. 100 #3.1	Decimation a JMOI	eard selection 0 Msps t Selection MHz and Serial Data M	programmed, User Inputs #1. Clock Sou is selected, cf #2a. On-board DEVCLK, asv #2b. External I Users Guide f #3. Decimatio #4. Program C and ADC.	- How to rce - the I toose the I Fs Select vell as pro Fs Select or details n and Se Clocks an	tabs allow the u program the EV DEVCLK to the A Fs at #2a. If the ction - The PLLA ovide the clock fr on - The user m regarding exter rial Data Mode - d ADC - once all	Iser to configu M clocks and / DC may be su e external clock /CO will be pro or distribution y ust enter the e nal clocks req Choose the di modes have l	re the ADC. ADC: ipplied by the on-board PL is selected, enter the Fs: ogrammed to provide any of at the LMK04828 for the Ji ixternal Fs supplied (in MH- uired. ecimation mode and seria	of the available sampling clock frequ ESD204B clocks. 4z). The PLL/VCO will be powered o I data mode for the ADC. button to write selections to the PLL	e on-board clo uencies to the fown; see the
0	Temp degree 5233 Local Te degree	emp							
			-						

User input configuration settings in ADC12DJ3200 GUI for this design is as follows:

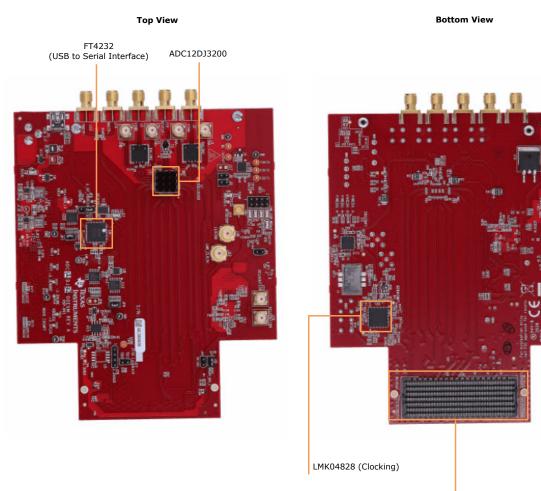
- 1. **Clock Source:** Select **On-board** where LMK04828 is used to generate clock for the ADC and reference clock for the FPGA.
- 2. **On-board Fs Selection:** Select **Fs = 1250 Msps**, where Fs is device clock which is calculated by dividing the JESD204B line rate with the R factor. R is chosen from Table-19 of ADC12DJ3200 Datasheet as per the JMODE used.
- 3. **Decimation and Serial Data Mode:** Select **JMODE2** as per the JESD Rx lane configuration and its other parameters.

2. Interoperability Test Setup

The interoperability test is performed on the RT PolarFire Evaluation Kit board with the RTPF500TS-1CG1509M device and TI ADC12DJ3200 EVM. The design for the test is developed using the Libero SoC software by instantiating the CoreJESD204BRX IP and other required IP cores in the SmartDesign. The design is tested for 5 Gbps data rate with four lanes configuration per ADC device. The register configuration of ADC12DJ3200 is done using ADC12DJ3200 GUI by Texas instruments. ADC12DJ3200 EVM is used to evaluate ADC12DJ3200. It is connected to the FPGA Mezzanine Card High Pin Count (FMC HPC) connector of the RT PolarFire Evaluation Kit.

The following figure shows the ADC12DJ3200EVM evaluation kit board.

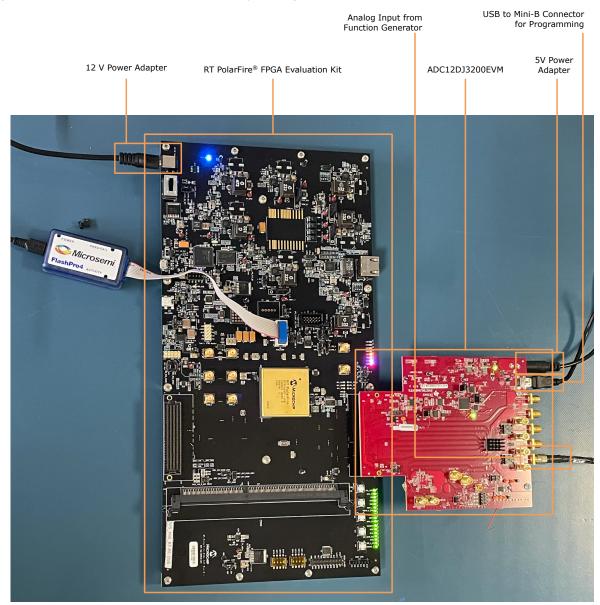
Figure 2-1. ADC12DJ3200EVM



HPC FMC+ Connector

The following figure shows the hardware setup for interoperability tests.

Figure 2-2. Hardware Setup for Interoperability Testing with ADC12DJ3200EVM



2.1 Interoperability Test Settings

CoreJESD204BRX and ADC12DJ3200 are configured, as listed in the following table.

Parameter	CoreJESD204BRX	ADC12DJ3200	Description
SCR	0/1	0/1	Scramble enable/disable
L	4	4 (per link)	Lanes
F	8	8	Octets per frame
К	4	4	Frames per multi-frame
М	4	4 (per link)	Converters
CS	0	0	Control bits per sample
Ν	12	12	Sample resolution
N'	12	12	Sample envelope
S	5	5	Samples per converter per frame
HD	0	0	High density mode
CF	0	0	Control bits per frame
SUBCLASSV	0	0	0

Table 2-1. Configuring CoreJESD204BRX and ADC12DJ3200

2.2 ADC12DJ3200EVM Interoperability Tests

The following interoperability tests were performed on RT PolarFire FPGA and ADC12DJ3200.

- Test 1: Data Link Layer—Code Group Synchronization
- Test 2: Data Link Layer—Initial Lane Alignment Sequence
- Test 3: Receiver Transport Layer
- Test 4: Descrambling

For more information about the preceding interoperability tests, see TR0066: Microsemi PolarFire FPGA CoreJESD204BRX Interoperability for ADC12DJ3200 Test Report.

3. Running the Demo

This section describes the steps to program the RT PolarFire FPGA device with the RTPF JESD design and detailed procedure to test the interoperability of RT PolarFire FPGA with ADC12DJ3200 device using JESD204B protocol.

Before programming the RT PolarFire device, ensure the following settings on the RT PolarFire Evaluation kit:

- 1. Ensure the jumper settings on the board are set to the default except the following:
 - J18—Short pin 5 and 6
 - J22—Short pin 1 and 2
 - J31—Open (when programming through External FlashPro programmer)
- 2. Connect the host PC to the J3 connector using External FlashPro Programmer.
- 3. Connect the power supply to the J19 connector and switch ON the power supply switch, SW7.

On the ADC12DJ3200 EVM, all the jumpers settings are set to default. Ensure the following settings on ADC12DJ3200 EVM:

- Connect 5V DC power supply to J37 connector.
- Connect one end of USB cable to J31 connector on the ADC12DJ3200 EVM while another end is connected to the host PC.
- Connect SMA cable to **VINA** SMA port on the ADC12DJ3200 EVM to provide single-ended analog input from the function generator.
- Connect HPC FMC+ connector of the ADC12DJ3200 EVM with J38 FMC1 connector on the RT PolarFire Evaluation kit.

Analog input can be ramp, sine, square wave, and so on. In this demo, ramp and sine wave inputs are transmitted and received successfully at the RT PolarFire FPGA JESD204B output.

3.1 **Programming the Device using Libero SoC**

To program the device, follow these steps:

- 1. Open the design in Libero SoC software. The Libero **Design Flow** window appears.
- 2. Double-click **Run PROGRAM Action.** After programming the device successfully programmed, a green tick appears on **Run PROGRAM Action**.

Note: To program the device using FlashPro Express, see Appendix: Programming the Device using FlashPro Express.

3.2 Running the Design

After programming the device, debug LEDs glow as per the status of the JESD and XCVR signals. Follow these steps to test the interoperability of RT PolarFire FPGA with the ADC12DJ3200 EVM:

- 1. Install the ADC12DJ3200 application (setup.exe) from the following design files folder: rtpf jesd df\GUI\Volume
- 2. Launch the ADC12DJ3200 application.
- 3. In the **EVM** tab, select:
 - Clock Source: On-board
 - On-board Fs selection: 1250 Msps
 - Decimation and Serial Data Mode: JMODE2

Figure 3-1. ADC12DJ3200 GUI - EVM Tab

				AD	C12DJxx	00 GUI		Select the device ADC12DJ3200	~
VM	Control	JESD204B	NCO Configuration	Trim	LMK04828	LMX2582	Low Level View	USB Status 🔵	🌼 Reconnec
#2a. 0 #2b. 1 1000 #3. 0	lock Source On-bo On-board Fs Fs = 1250 External Fs S Decimation a JMOI	Selection O Msps Selection MHz and Serial Data M	programmed, User Inputs #1. Clock Sour is selected, ch #2a. On-board DEVCLK, as w #2b. External I Users Guide fr #3. Decimation #4. Program C and ADC.	ed to cont the other - How to rce - the (oose the Fs Select or details h and Sei locks an	tabs allow the u program the EV DEVCLK to the A Fs at #2a. If the ction - The PLLV ovide the clock fo on - The user m regarding extern rial Data Mode - d ADC - once all	ser to configur M clocks and A DC may be su external clock (CO will be pro or distribution y ust enter the e nal clocks requ Choose the do modes have b	e the ADC. DC: pplied by the on-board PL is selected, enter the Fs: grammed to provide any or a the LMK04828 for the J xternal Fs supplied (in MH jired. cimation mode and seria	of the available sampling clock frequ- ESD204B clocks. (z). The PLL/VCO will be powered do I data mode for the ADC. Jutton to write selections to the PLL/	e on-board cloc encies to the own; see the
0	Temp degree 5233 Local Te degree Update Te	mp							

- 4. Click Program Clocks and ADC.
- 5. Go to **JESD204B** tab and ensure the parameters are set as shown in the following figure.

		AD	C12DJxx	00 GUI		Select the device ADC12DJ320	v v
VM Control JESD204B	NCO Configuration	Trim	LMK04828	LMX2582	Low Level View	USB Status	Seconnec
C/Bypass Settings:	JESD204	B Block C	Control:				
moor No.		JESD	Block Enable				
JMODE 2			bler Enable				
Operating Mode							
12-bit, Dual Channel, 8 lanes	K Value	er Multifr	K-1 Value				
DDC Gain Boost	4		3				
DB4 Mode Alias Protect	ion 📀	JSYNC	C_N Sync Requ	est			
DB2 Filter Mode				_			
Low-pass Filter	and the second sec	put Sele					
DDC Real Output Spect	rum invert	SYNCSE					
	and an and a second s	est Mode ormal Og		-			
		withat of	reraievin				
ut Mux Select:		SFOR	MAT				
Single Input:		DID					
nput Selection		FCHAR	0				
INA is used 🤝		e ronn	2				
Dual Input:	Serializer	Control:					
AUGH INDUI.	Pre-emp	hasis Str	ength				
Channel Swap							

6. Go to LMK04828 tab and ensure the device clock divider is set as shown in the following figure. Figure 3-3. ADC12DJ3200 GUI - LMK04828 Tab

							AD	C12D	Jxx00	GUI			1	Select the devic	e ADC120	03200		~
EVM	Control	JESD	204B	NCO	Configu	ration	Trim	LMK04	1828 LM	X2582	E Low I	evel V	iew		USB	0 1	Reco	nnect
PLL1	Configura	ation	PLL	2 Coi	nfigura	tion	SYS	REF an	d SYNC	Clock	Outputs							
	ut 0 and 1 Clock & SYSF		CLKout 2 ADC Clock		SREF	CLKout Not Use	4 and 5		CLKout 6 an	id 7	CLKout Alternate			CLKout 10 an Not Used	d 11	CLKout 1 Extra FMC		
Ou	oup Powerdow Itput Drive Leve Input Drive Leve		Group P Output Input	Drive L		Outp	o Powerd ut Drive I ut Drive I	evel 🗌	Output Dr	verdown ive Level ive Level	Outp	t Drive I	lown	Group Powe Output Driv Input Driv			owerdo Drive Li Drive Li	evel
DCL	K Divider		DCLK DN	ider		DCLK	Divider		DCLK Divid	er .	DCLK	ivider		DCLK Divider		DCLK DN	ider	
10		~	1		~	10		~	10		10		~	10	~	10		~
DCL	K Source	-	DCLK So	urce		DCLK	Source		DCLK Sour	be .	DCLK S	ource		DCLK Source		DCLK So	urce	
Divid	der	~	Divider		~	Divide	r	~	Divider		Divider		~	Divider	~	Divider		~
DCU	KType Inve		DCLK TV	pe in	vert	DCLKT	Type I	nvert	DCLK Type	Invert	DCLKT	vpe I	nvert	DCLK Type	Invert 🗌	DCLK TV	e in	vert
LVD)S	~	Powerdo	own	~	Power	rdown	~	Powerdow	n s	and president		~	LVPECL 160	v Vm 0	LVDS		~
SDC	LK Source		SDCLK S	ource		SDCLK	Source		SDCLK Sou	rce	SDCLK	Source		SDCLK Source	e	SDCLK S	ource	
SYS	SREF	~	SYSREF	0	~	Device	Clock		Device Clo	ck 🔍	SYSR	F		SYSREF	~	SYSREF		15
SDC	LK Type Inve		SDCLK T	vpe in	vert	SDCLK	Type I	nvert	SDCLK Typ	e invert	SDCLK	Type I	nvert 🗌	SDCLK Type	Invert []	SDCLK T	vpe in	vert
LVD		~	Powerdo		~		rdown	~	Powerdow		101 January		~	Powerdown	Contract -	Powerd		2
SDC	LK EN/DIS State		SDCLK E	N/DIS S	tate	SDCLK	EN/DIS S	State	SDCLK EN/	DIS State	SDCLK	EN/DIS S	State	SDCLK EN/DR	S State	SDCLK E	N/DIS SI	ate
Act	we/Active	~	Active/A	ctive	~	Active	Active	~	Active/Act	ve 🕓	Active	Active	~	Active/Active	• ~	Active/A	ctive	~
DCL	SDCLKout_I CLKout_DDLY_I CLKout_HSg_I Kout_ADLYg_I CLKout_ADLY	2 N N 8	DCLKor DCLK DCLKout	ut_DDL'	ut_P0 Y_P0 g_P0 y_P0 Y	DCLK	Kout_DDL LKout_H out_ADL	wt_PD Y_PD Sg_PD Y_PD Y_PD Y_PD Y_PD	DCLKout DCLKout DCLKout	LKout_PD DDLY_PD t_HSg_PD DLYg_PD ADLY_PD		out_DDI Kout_H: ut_ADL'	NU_PO Y_PO Sg_PO Y_PO Y_PO	DCLKout_D DCLKout_ DCLKout_AD	HSg_PD	DCLKo DCLK DCLKou	OUL HS	9_PD

7. In the **Low Level View** tab, select **Block** as ADC12DJxx00 with **Address** 0x208 and click **Read Register** to read the JESD status register. The JESD status register bits must be set as shown in the following figure.

			ADC1	2DJ	xx00	Gl	JI							Select the devi	ce Al	DC12DJ32	00	~
EVM Control JESD204B N	CO Configurat	ion Tr	im Ll	MK048	28 L	MX2	582	6	E	.ow L	evel	Vie	w			JSB Status		👂 Reconnect
Register Map 🛛 📅 🗁 🍤 🇐	5						Up	date	Mod	le Im	med	liate	~	Field View				
Register Name	Address	Default	Mode	Size	Value	15	14	13	12	11	10	9	8 ^	RESERVED		1		
ADC12DJxx00						-		-				-		PLL LOCKE	D	1		
CONFIG_A	0x00	0x30	R/W	8	0x30								1.1	_				
DEVICE_CONFIG	0x02	0x00	R/W	8	0x00									ALIGNED		0		
CHIP_TYPE	0x03	0x03	R	8	0x03									REALIGNED		0		
CHIP_ID_0	0x04	0x20 0x00	R	8	0x20									SYNC_STAT	US	1		
CHIP_ID_1 CHIP_VER	0x05 0x06	0x00	R	8	0x00 0x01									LINK UP		1		
VENDOR ID 0	0x00	0x51	R	8	0x51									RESERVED	_			
VENDOR_ID_1	0x0C	0x04	R	8	0x04									RESERVED		1		
USR0	0x10	0x00	R/W	8	0x00													
AC_CTRL1	0x23	0x00	R/W	8	0x00													
CLK CTRL0	0x29	0x00	R/W	8	0x00									-	-			
CLK_CTRL1	0x2A	0x00	R/W	8	0x00										_			
SYSREF_POS_0	0x2C	0x00	R	8	0x00													
SYSREF_POS_1	0x2D	0x00	R	8	0x00													
SYSREF_POS_2	0x2E	0x00	R	8	0x00									-	-			
FS_RANGE_A_0	0x30	0xC4	R/W	8	0xC4									1	_			
FS_RANGE_A_1	0x31	0xA4	R/W	8	0xA4													
FS_RANGE_B_0 FS_RANGE_B_1	0x32 0x33	0xC4 0xA4	R/W R/W	8	0xC4 0xA4													
	0X33	UXA4	R/W	8	UXA4	1							~					
<													>					
Register Description						_												
RESERVED[1:0]						^	BI	ock	-		-		Addres	ss W	rite Da	ata	Rea	d Data_Gen
Reserved								DC12	Div	(00				208 ×		0	x	64
PLL_LOCKED[2:2]							100	0.012			- 12		-			-	_	
When high, indicates that the PLL is loc ALIGNED[3:3]	:Ked					.								V	/rite R	Register	Rea	ad Register

Figure 3-4. ADC12DJ3200 GUI - Low Level View Tab

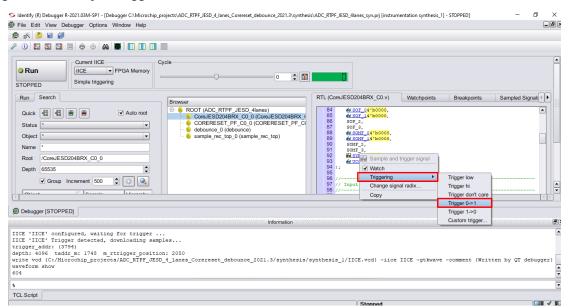
8. When the JESD link is up and **SYNC** Signal status goes HIGH, go to Libero SoC, and invoke Identify Debugger as shown in the following figure.

Figure 3-5. Identify Debug Design

Top Module(ro	ot): ADC_RTPF_JESD_	4anes	[Ξ (Dĸ	1	Ø.
Active Synthes	is Implementation: sy	nthesis_1					
Tool							
	Debug Design Generate Smat SmartDebug Identify Debu Handoff Design Configure Per Export Bitstre Export FlashP Export Job M Export Job M Export SPI Fla Configure Per Export Pin Re Export BSDL Configure Per Export BSDL Configure Per Export BSDL Configure Per Configure Per Export BSDL Configure Per Configure Per Co	SPI Flash Image GRAM_SPI_IMAGE Act artDebug FPGA Array Ig Design for Production rmanent Locks for Pro am tro Express Job anager Data ish Image port	Data	Report			
	 Handoff Design Export Smart 						
	export smart						-
Design Flow	Design Hierarchy	Stimulus Hierarchy	Catalog	Com	ponents	Files	

 When the Identify Debugger opens, ensure the SYNC signal in the JESD204BRX module is set for a trigger on 0 to 1 transition. Right-click on the SYNC signal and select Triggering > Trigger 0->1, as shown in the following figure.

Figure 3-6. Identify Debugger Window



10. Run the **Identify Debugger**. The console window shows that the Identify is waiting for the trigger. Press **SW_URST** switch on the board.

Figure 3-7. Run the Identify Debugger

5 Identify (R) Debugger R-2021.03M-SP1 - [Debugger C:\Microchip_projects\ADC_RTPF_JESD_4_Janes_Corereset_debounce_2021.3\synthes	sis\ADC_RTPF_JESD_4lanes_syn.prj [instrumentation synthesis_1] - RUNNING]	– ø ×
💭 File Edit View Debugger Options Window Help		_82
🌐 🔊 🙆 😸 🥥		
Current IICE IICE FPGA Memory Simple triggering		<u> </u>
Run Search	RTL (CoreJESD204BRX_C0.v) Watchpoints Breakpoints San	mpled Signal
Name Image: Construction of the second s	84 #f 007_0 86 #f 007_0 87 007_0 88 #f 007_0 89 #f 007_0 89 #f 007_0 90 #f 007_0 91 #f 007_0 92 #f 007_0 93 #f 007_0 94 > 95 > 967 // Input 967 // Input	
Bebugger [RUNNING] Information		
Physical Device ID IICEs Signature		•
Partition		
regular dev_0 MPF500 IICE 0x9400744e		-
IICE 'IICE' configured, waiting for trigger		
		T
TCL Script		

11. Click Waveform viewer icon as highlighted in the following figure. GTTKWave window appears.

Figure 3-8. Waverform Viewer

Identify (R) Debugger R-2021.03M-SP1 - [Debugger C:\Microchip_projects\ADC_RTPF_JESD_4_lanes_Corereset_debounce_2021.3\synthesi File Edit View Debugger Options Window Help	s\ADC_RTPF_JESD_4lanes_syn.prj [instrumentation synthesis_1] - STOPPED] – 🗗 X
ORun Current IICE Waveform viewer IICE FPGA Memory STOPPED Simple triggering 0 Image: Simple triggering	
Run Search Browser	RTL (ADC_RTPF_JESD_4lanes.v) Watchpoints Breakpoints Sampled Sig 4
Quick Image: Control of the contro of the control of the control of the control	9 module ADC_RTPF_UTSD_4lanes(10 // inputs 11 ctAr_SOMMe, 12 EXT_BT_N, 13 LaNED_RDO_N, 14 LANED_RDO_N, 16 LANEL_RDO_N, 17 LANED_RDO_N, 18 LANED_RDO_N, 19 LANED_RDO_N, 19 LANED_RDO_N, 20 LANED_RDO_N, 21 REF_CLK_RAD_N, 22 SEL_IN, 23 SEL_IN, 24 CtAR_RDO_N, 24 CtAR_RDO_N, 25 CtAR_RDO_N, 26 CtAR_RDO_N, 27 CtAR_RDO_N, 28 CtAR_RDO_N, 29 CtAR_RDO_N, 20 SEL_IN, 20 CtAR_RDO_N, 20 CtAR_RDO_N, 20 CtAR_RDO_N, 21 REF_CLK_RDO_N, 22 SEL_IN, 23 SEL_IN, 24 CtAR_RDO_N, 24 CtAR_RDO_N, 25 CtAR_RDO_N, 26 CtAR_RDO_N, 27 CtAR_RDO_N, 28 CtAR_RDO_N, 29 CtAR_RDO_N, 20 CtAR_RDO_N, 20 CtAR_RDO_N, 20 CtAR_RDO_N, 20 CtAR_RDO_N, 20 CtAR_RDO_N, 20 CtAR_RDO_N, 20 CtAR_RDO_N, 20 CtAR_RDO_N, 20 CtAR_RDO_N, 21 CtAR_RDO_N, 22 CtAR_RDO_N, 23 CtAR_RDO_N, 24 CtAR_RDO_N, 25 CtAR_RDO_N, 26 CtAR_RDO_N, 27 CtAR_RDO_N, 27 CtAR_RDO_N, 28 CtAR_RDO_N, 29 CtAR_RDO_N, 20 CtAR_
Debugger (STOPPED)	
Information	
regular dev_0_MPF500 IICE 0x94c0744e	
IICE 'IICE' configured, waiting for trigger	
<pre>IICE 'IICE' Trigger detected, downloading samples trigger_addr: (44) depth: 4096 taddr m: 2094 m_rtrigger_position: 2050 write vod (C:/Microchip_projects/ADC_RTFF_IESD_4_lanes_Corereset_debounce_2021.3/synthesis/</pre>	
	•
TCL Script	

12. Right-click **64-bit final_out_x_A** output from each lanes and select data format as **Analog > Interpolated** as shown in the figure.

Figure 3-9. GTKWave Window - Data Format

e Edit Search Time Ma	irkers View Help							
E 🖸 🔍 🔍 🔍		From: 0 sec To: 102400	ns 🛛 🔂 🕅 Marker: 51100 ns 🗍	Cursor: 100 ps				
st	Signals	Waves		Curson, 100 hs				
	Time		20 us 30 us 40 us	50 us	60 us	70 us 8	0 us 90 u	s 100 us
ADC_RTPF_JESD_4lanes	identify o	cvcle =						
	identify sampled							
	RX_STATE_0	[1:0] = 11		00	+)11			
	RX_STATE 1	[1:0] = 11		00)+)11			
	RX_STATE_2	[1:0] = 11		00)+)11			
	RX_STATE_3	[1:0] = 11		00)+)11			
	CGS_ERR			11+ 10000				
	UCC_ERR							
	LINK_CD_ERR			0000	1111			
Signals	SOF_0			0000				
	SOMF_01	Data Format	Hex					******
	SOF_1	Color Format	Decimal	0000		//acae//aca//acae//acae//ac		
	SOMF_1		Signed Decimal	0000	A 66 6 66 666 669			
		Insert Analog Height Extension	Binary					
	AL RE	Insert Blank	Octal					
	EPCS 3 R	Insert Comment	ASCII					
	EPCS 1 R	Alias Highlighted Trace	BitsToReal					
	EPCS 0 R	Remove Highlighted Aliases	RealToBits					
	EPCS 2 R	Cut	Right Justify	•				
	final out 4 A[Сору	Invert	• 0000000 +		+ +		
	final out 1 A	Paste	Reverse Bits	00000000+		+ +	+ +	1. A.
	final out 2 A[Translate Filter File	00000000+	+ +	+ +	+ +	
	final out 3 A[Open Scope	Translate Filter Process	00000000+	+ +	+ +	+ +	
	PLL	LOCK =	Transaction Filter Process					
	FABRIC_RES	SET_N =	Analog	Off				
:	EXT_F	RST_N =	Range Fill	Step				
1			Gray Filters	Interpola				
pend Insert Replace			Popent	Internola	ted Annotated			

13. When ramp signal is provided as an input signal to ADC12DJ3200 EVM, the ramp signal is successfully reconstructed in the RT PolarFire FPGA device as shown in the following figure.

•					
GTKWave - IICE.vcd		- 0 ×			
File Edit Search Time Mar	kers View Help				
x 🕞 📴 I 🔍 Q Q	🦩 🙀 🗍 🗍 🖨 🛶 From: 0 se	cc To: 204800 ns 🛛 🛙 🔂 🗍 Marker: 104900 ns Cursor: 134790 ns			
▼ <u>S</u> ST	Signals	Waves			
ADC_RTPF_JESD_4lanes	Time identify cycle=52	is 140 us 150 us 160 us 170 us 190			
	identify sampleclock=1				
	RX_STATE_0[1:0] =10	11			
	RX_STATE_1[1:0] =10	11			
	RX_STATE_2[1:0] =10				
	RX_STATE_3[1:0] =10	11			
	SOMF_0[3:0] =0000	() · · · · · · · · · · · · · · · · · · ·			
	SOF_0[3:0] =1000				
	SOMF_1[3:0] =0000	() + + () + + + + + + + + + + + + + + +			
Type Signals	SOF_1[3:0] =1000				
int identify_cycle	UCC_ERR[3:0] =0000	0000			
	CGS_ERR[3:0] =0000	9000			
reg identify_sampleclock	LINK_CD_ERR[3:0] =1111	1111			
	RESET_N=1				
	SYNC_N=1				
	ALIGNED =1				
	EPCS_0_RX_VAL =1				
	EPCS_1_RX_VAL =1				
	EPCS_2_RX_VAL =1				
	EPCS_3_RX_VAL =1				
	final_out_1_A[63:0] =00000				
	final_out_2_A[63:0] =00000				
	final_out_3_A[63:0] =00000				
lter:	final_out_4_A[63:0]=00000				
Append Insert Replace	•				

Figure 3-10. GTKWave Window

14. When Sinusoidal signal is provided as an input signal to ADC12DJ3200 EVM, the sinusoidal signal is successfully reconstructed in the RT PolarFire FPGA device as shown in the following figure.

Figure 3-11. GTKWave Window

GTKWave - IICE.vcd ile Edit Search Time Mark	ers View Help	- 0
		To:204800 ns 🔰 🔂 Marker: 32400 ns Cursor: 117100 ns
SST	Signals	- Waves
ADC_RTPF_JESD_4lanes	Time	120 us 130 us 140 us 150 us 160 us 170 us 180 us 190 us 200 us
- CORERESET_PF_C0_0	identify_cycle =-1398	
- CoreJESD204BRX_C0_	identify_sampleclock=1	
- debounce_0 debounce_top_0	RX_STATE_0[1:0] =11	11
- sss sample_rec_top_o	RX_STATE_1[1:0] =11	11
	RX_STATE_2[1:0] =11	11
	RX_STATE_3[1:0] =11	
	SOMF_0[3:0] =0000	
•	SOF_0[3:0] =0000	
	SOMF_1[3:0] =0000	
e Signals	SOF_1[3:0] =0000	
	CGS_ERR[3:0] =0000	0000
	LINK_CD_ERR[3:0] =1111	1111
	UCC_ERR[3:0] =0000	0000
	SYNC_N =1	
1	RESET_N=1	
	ALIGNED =1	
	EPCS_0_RX_VAL =1	
	EPCS_2_RX_VAL =1	
	EPCS_1_RX_VAL =1	
	EPCS_3_RX_VAL=1	
	final_out_1_A[63:0] =11001011110111	
	final_out_2_A[63:0] =01111011111010	
	final_out_4_A[63:0]=0010101111110	
	final_out_3_A[63:0] =0001101111110	
pend Insert Replace		

This concludes running the demo.

Note: When the Identify Debugger is in RUN state, the design is already up and running. When reset is asserted, re-initialization and re-alignment happens as seen in the waveforms.

Note: LIND_CD_ERR = 1 indicates configuration parameters of link configuration data do not match with the configuration parameters of the JESD204BRX core. In the preceding waveforms, LINK_CD_ERR is equal to 1 because ADC12DJ3200 is using JMODE2 which configures the ADC for dual channel, eight lanes configuration while JESD204BRX IP is only configured for four lanes in the design. Only four lanes of ADC device are used with the JESD204BRX device resulting in design working successfully.

4. Appendix: Programming the Device using FlashPro Express

This section describes how to program the RT PolarFire device with the .job programming file using FlashPro Express. The .job file is available at the following design files folder location: <download_folder>\Programming_Job

To program the device, complete the following steps:

- 1. On the host PC, launch the **FlashPro Express** software.
- 2. Click New or select New Job Project from Project menu to create a new job project.
- 3. Enter the following in the Create New Job Project dialog box:
 - Programming job file: Click Browse and navigate to the location where the .job file is located and select the file. The default location is: <download_folder>\Programming_Job
 - FlashPro Express job project location: Click Browse and navigate to the location where you want to save the project.
- 4. Click **OK**. The required programming file is selected and ready to be programmed in the device.
- 5. The **FlashPro Express** window appears. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.
- 6. Click **RUN** to program the device. When the device is programmed successfully, a **PROGRAMMER(S) PASSED** status is displayed.
- 7. Close FlashPro Express, Project > Exit.

See 3. Running the Demo section to run the demo.

5. Appendix: Running the TCL Script

TCL scripts are provided in the design files folder under the directory **TCL_Scripts**. If required, the design flow can be reproduced from Design Implementation before the job file is generated.

To run TCL, follow these steps:

- 1. Launch the Libero software
- 2. Select **Project > Execute Script....**
- 3. Click Browse and select script.tcl from the downloaded TCL_Scripts directory.
- 4. Click Run.

Note: To use the scripts provided along with the design, add the identify instrumentor in the design manually and then rerun the complete flow.

After successful execution of the TCL script, the Libero project is created within the TCL_Scripts directory.

For more information about TCL scripts, see <design_name>/TCL_Scripts/readme.txt.

See Libero[®] SoC TCL Command Reference Guide for more information about TCL commands. Contact Technical Support for any queries about running the TCL script.

6. Revision History

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 6-1. Revision History

Revision	Date	Description
A	01/2022	Initial document.

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