MICROCHIP

AN4400

RT PolarFire® FPGA Interoperability with TI ADC12DJ3200 using JESD204B Protocol

Introduction

As the resolution and speed of converters have increased, the demand for a more efficient interface has grown. The JESD204 interface brings this efficiency and offers several advantages over its CMOS and LVDS predecessors in terms of speed, size, and cost. Microchip provides interfacing solutions for analog-to-digital converter (ADC) and digital-to-analog converter (DAC) devices using the JESD204B JEDEC® standards. These interfacing solutions are provided as Direct Core soft IPs (CoreJESD204BRX and CoreJESD204BTX) in the Libero® SoC software. These IP cores interface with transceivers of RT PolarFire® FPGA devices.

The application note demonstrates the interoperability of RT PolarFire FPGA with 12-bit, dual-channel Texas Instruments (TI) ADC12DJ3200 device using JESD204B protocol. The ADC12DJ3200 device supports the JESD204B serial interface with data rates up to 12.8 Gbps with two or four lanes per ADC. In this application, an analog signal is transmitted through the ADC12DJ3200 EVM and received at the JESD204B Rx IP output on RT PolarFire FPGA. This application note describes the RT PolarFire FPGA design, JESD204B link parameters, hardware test setup, and equipment used for this interoperability test.

Design Requirements

The following table lists the hardware and software requirements for this demo design.

Table 1. Design Requirements

Requirement	Description
Hardware	
RT PolarFire Evaluation Kit (RTPF500TS-1CG1509M) • 12V DC - Power supply adapter • External FlashPro 4 Programmer	Rev 0.1 (Pre-release Version)
ADC12DJ3200EVM Evaluation Board • 5V DC - Power supply adapter • USB A to Mini-B cable	Rev A
Function generator	—
SMA cable	—
Host PC or Laptop with 64-bit Windows 10	—
Software	
ADC12DJ3200EVM Configuration GUI	—
Libero SoC	See the `readme.txt` file provided in the design files for the software versions used with this reference design.

Note: Libero SmartDesign and configuration screenshots provided in this application note are for illustration purpose only. See the provided Libero design for the latest updates.

Prerequisites

Before you begin:

1. Download and install Libero SoC from the following location: https://www.microsemi.com/product-directory/design-resources/1750-libero-soc#downloads
2. For demo design files download: www.microchip.com/en-us/application-notes/AN4400

References

- CoreJESD204BRX IP Handbook
- CoreJESD204BTX IP Handbook
- ADC12DJ3200EVM
- Identify ME User Guide

Table of Contents

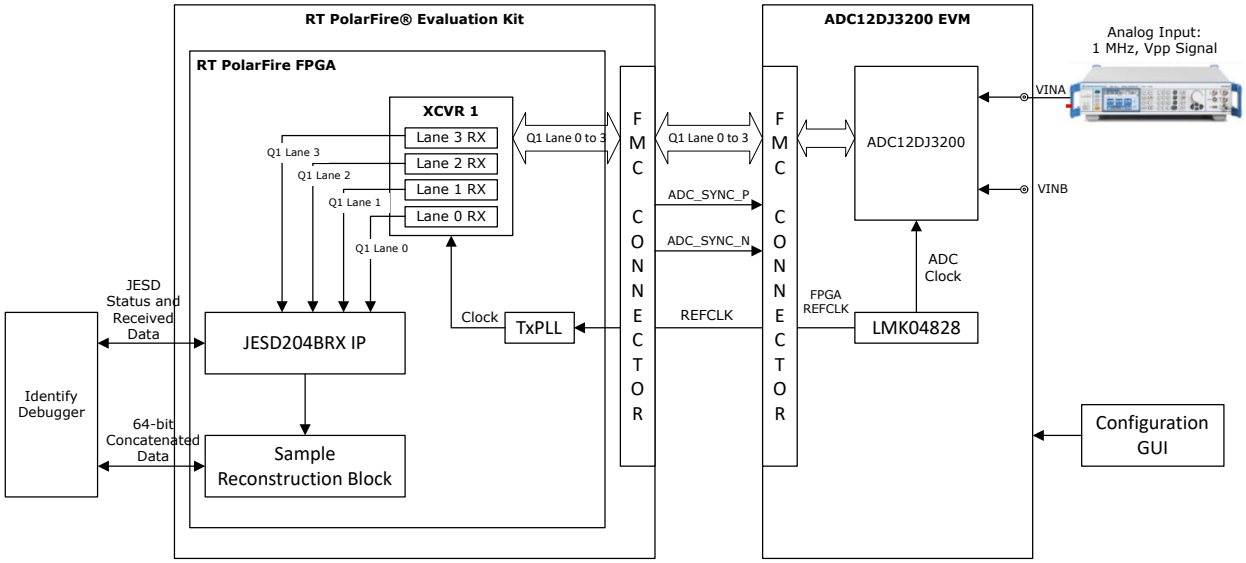
Introduction....1
1. Design Requirements....1
2. Prerequisites....2
3. References....2
1. Design Description....4
1.1. Clocking Structure....5
1.2. Reset Structure....6
1.3. Design Implementation....7
2. Interoperability Test Setup....10
2.1. Interoperability Test Settings....12
2.2. ADC12DJ3200EVM Interoperability Tests....12
3. Running the Demo....13
3.1. Programming the Device using Libero SoC....13
3.2. Running the Design....14
4. Appendix: Programming the Device using FlashPro Express....20
5. Appendix: Running the TCL Script....21
6. Revision History....22
Microchip FPGA Support....23
The Microchip Website....23
Product Change Notification Service....23
Customer Support....23
Microchip Devices Code Protection Feature....23
Legal Notice....24
Trademarks....24
Quality Management System....25
Worldwide Sales and Service....26

1. Design Description

The following figure shows the high-level block diagram of RT PolarFire FPGA interoperability with ADC12DJ3200.

The analog input signal is provided to ADC12DJ3200 EVM evaluation board. The ADC12DJ3200 device on the EVM is dual channel, 12-bit ADC, capable of operating at sampling rates up to 3.2 Giga-samples per second (GSPS) in dual channel mode or 6.4 GSPS in single channel mode. The on-board clock generator, LMK04828, generates ADC and FPGA reference clocks for the high-speed serial interface. The ADC12DJ3200 device output data is transmitted over a standard JESD204B high-speed serial interface. ADC JESD204B block transmits the serial data to the RT PolarFire FPGA through FMC connectors. The serial data is received at the FPGA side where it is passed through the XCVR block and further to the CoreJESD204BRx IP block. The digital data from CoreJESD204BRx IP block is sent to sampling reconstruction block, which converts the digital data into analog samples needed to reconstruct the analog signal. This can be monitored on the Identify Debugger.

Figure 1-1. High-level Block Diagram



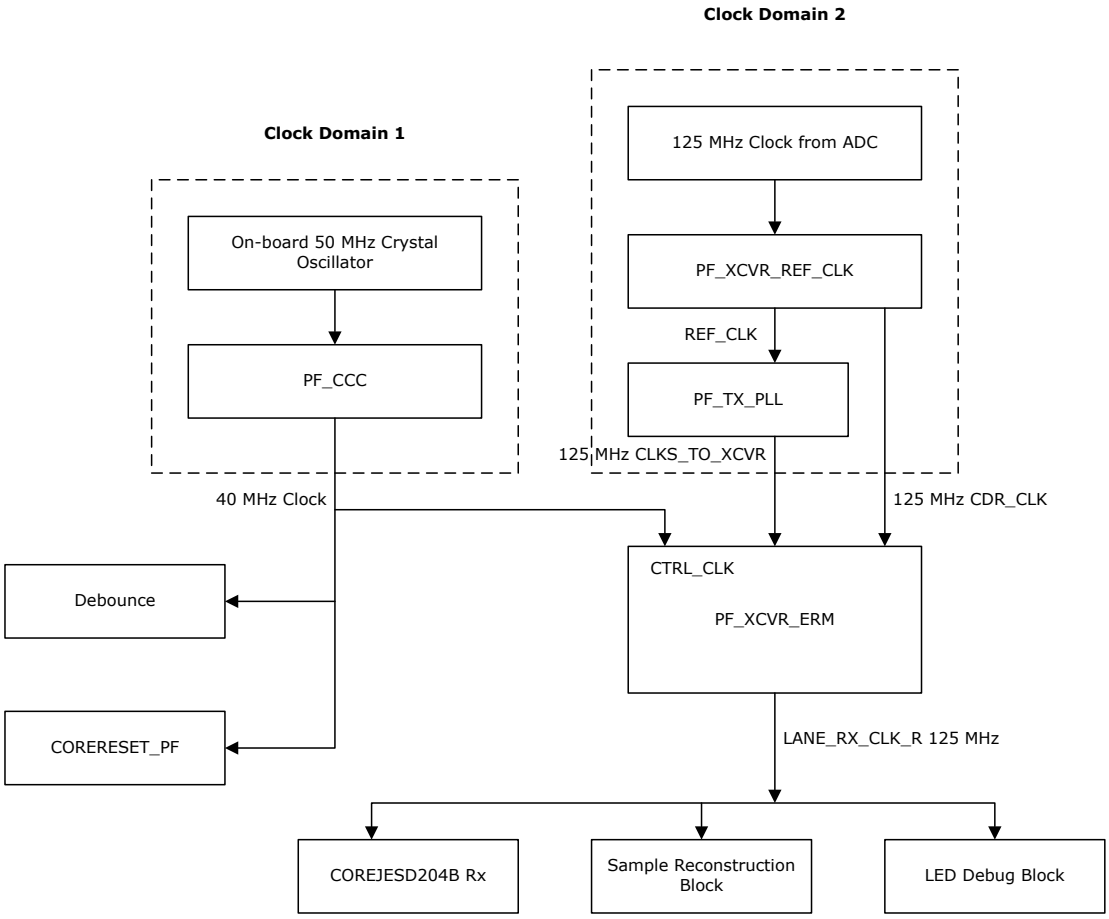
1.1 Clocking Structure

In the reference design, there are two clock domains. The on-board 50 MHz crystal oscillator is connected to the PF_CCC module, which generates 40 MHz. The 40 MHz clock is sourced to CORERESET_PF, Debounce, and CTRL_CLK input of PF_XCVR_ERM module for Enhanced Receiver Management (ERM) logic.

125 MHz differential clock from ADC12DJ3200 EVM drives the PF_XCVR_REF_CLK where differential clock is converted to single-ended clock. This single-ended clock is provided as a reference clock to PF_TX_PLL and CDR in the PF_XCVR_ERM. Recovered clock LANEx_RX_CLK_R is provided to COREJESD204BRx, sample reconstruction module, and LED debug module.

The following figure shows the clocking structure.

Figure 1-2. Clocking Structure

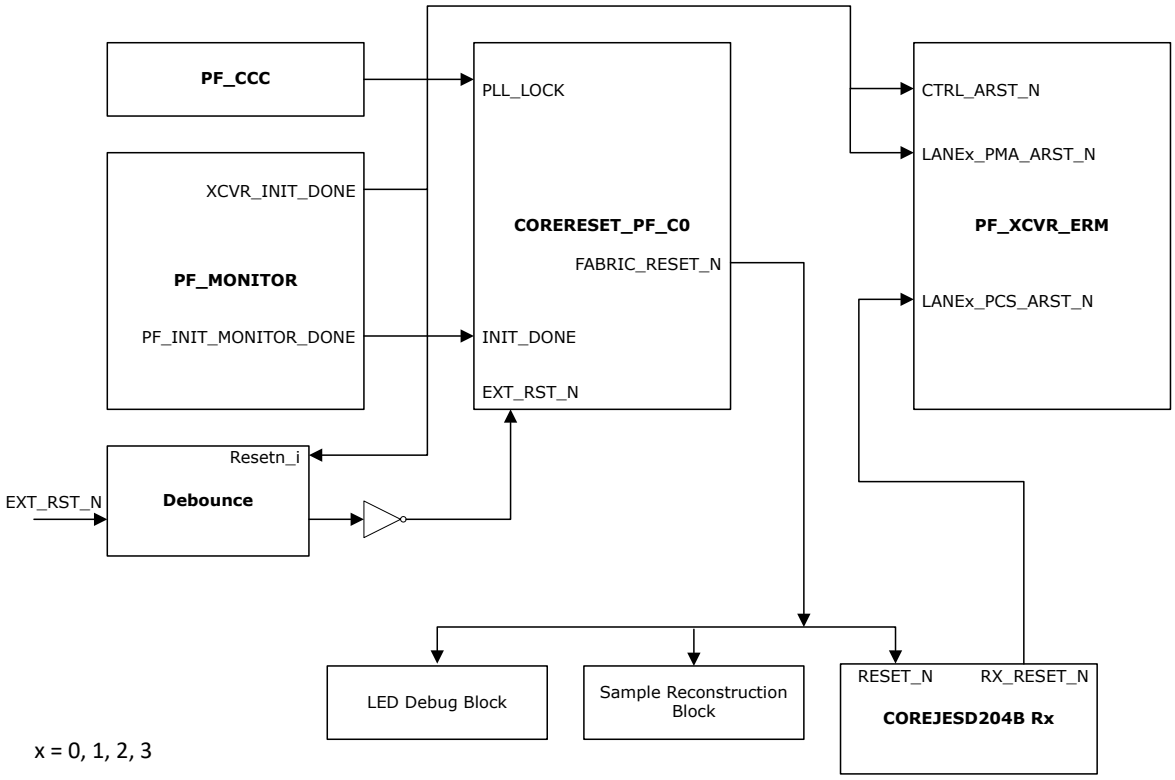


1.2 Reset Structure

In this reference design, CORERESET_PF module generates reset signal to the COREJESD204BRx, sampling reconstruction module, and LED debug module. INIT_DONE input to CORERESET_PF is provided from PF_INIT_MONITOR module whereas EXT_RST_N input is NOT output of the Debounce logic. Input to Debounce logic is connected to the user reset on the RT PolarFire Evaluation kit. XCVR_INIT_DONE output from PF_INIT_MONITOR provides reset to CTRL_ARST_N, LANEx_PMA_ARST_N inputs of PF_XCVR_ERM module. RX_RESET_N output from COREJESD204BRx provides reset to LANEx_PCS_ARST_N inputs of PF_XCVR_ERM module.

The following figure shows the reset structure.

Figure 1-3. Reset Structure

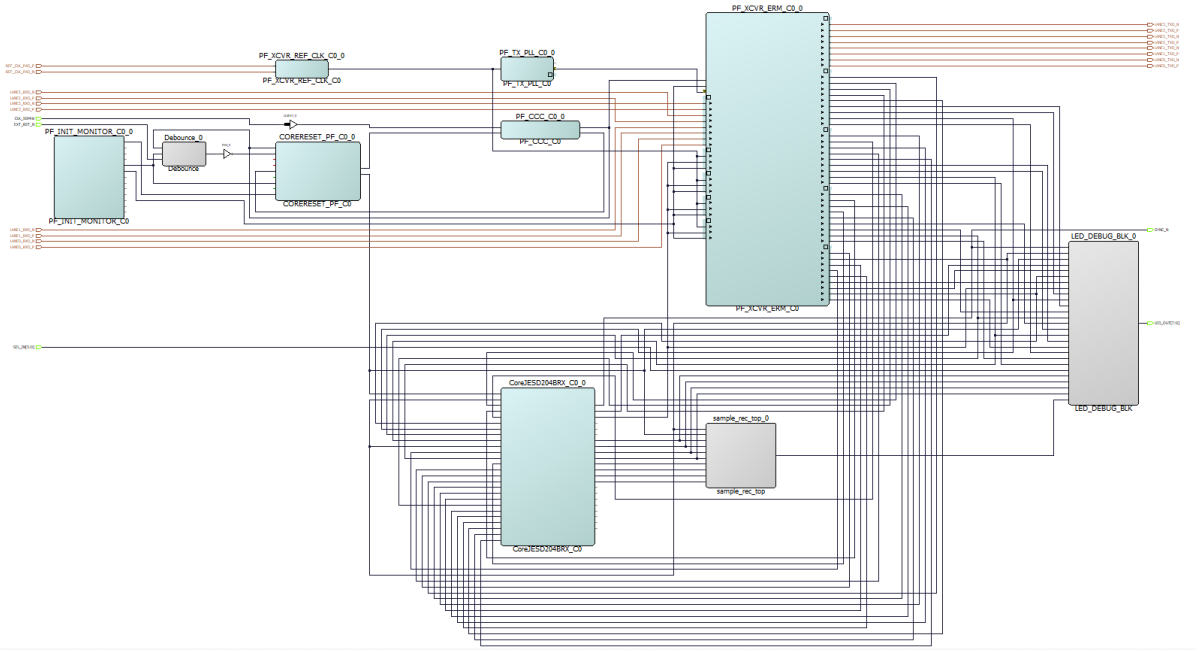


1.3 Design Implementation

This section describes the Libero deisgn implementation, describes IPs used and their configurations. This section also describes the ADC12DJ3200 EVM GUI configuration.

The following figure shows the design implementation in Libero SoC software.

Figure 1-4. JESD204BRx Interface Design



The following IPs are used in this SmartDesign:

1. **PF_INIT_MONITOR:** Indicates the completion of device boot, design and memory initialization by the System Controller. The device initialization includes Fabric, PCIe, Transceiver, SRAM initialization from uPROM/ sNVM/SPI Flash. DEVICE_INIT_DONE is used as a reset to COREJESD204BRx IP and other Fabric modules. XCVR_INIT_DONE is used as a reset to XCVR IP.
2. **CORERESET_PF:** Generates a Reset, which is asserted asynchronously and negates synchronously to a specified clock.
3. **PF_CCC:** Macro to access PolarFire CCC block. It is used to synthesize 40 MHz clock frequency from the CCC with an on-board 50 MHz reference clock.
4. **PF_XCVR_REF_CLK:** The Transceiver Reference Clock Configurator is used to build the correct reference clock input to the transceiver and to the Tx PLL. The user can pick the input type and various input options from the GUI.
5. **PF_TX_PLL:** Generates the TxPLL/TxPLL_SSC based on the input provided to the GUI. PF_TX_PLL generates BIT_CLK for the transceiver.
6. **PF_XCVR_ERM:** This is a hard IP block that supports high-speed data rates ranging from 250 Mbps to 12.5 Gbps. In this design, the transceiver block (PF_XCVR) is configured in 8b10b mode with a CDR reference clock of 125 MHz to support 5 Gbps data rate. XCVR configuration settings are as follows:
   - Number of Lanes: 4
   - Enhanced receiver management: Enabled
   - Receiver calibration: None (CDR)
   - Transceiver data rate: 5 Gbps
   - TX clock division factor: 1
   - TX PPLL base data rate: 5 Gbps
   - TX PLL bit lock frequency: 2.5 Gbps

  - CDR Lock Mode: Lock to data
  - CDR Reference Clock Source: Dedicated
  - CDR Reference Clock Frequency: 125 MHz
  - PCS-Fabric interface width: 32-bit
  - 8b/10b Encoding/Decoding: Enabled
  - FPGA interface frequency: 125 MHz
7. **CoreJESD204BRX:** This is the receiver interface of the JEDEC JESD204B standards. The core configuration of this IP core is as follows:
  - Decoder: Removed
  - Data Width: 32
  - Serdes Mode: 1
  - Scrambling: Enabled
  - Device Subclass Version: Subclass 0
  - JESD204 version: JESD204B
  - No. of Lanes (L+1): 4
  - Checksum calculation type: Octet
  - Frame Alignment Correction: Enabled
  - Link Configuration Error: Enabled
  - RAM Implementation: In LSRAM
  - No. of Octets per Frame: 8
  - No. of Frames per Multi-frame: 4
  - No. of Multi-frames in ILA sequence:4

Note: For information about CoreJESD204BRX Core Link configuration parameters, see Table 2-1.

Debounce logic RTL block is implemented to remove the switch bounces and generates a single pulse to the design when the user reset push button is pressed on the board. Sample reconstruction module is implemented to concatenate two 32-bit JESD output data and frame into 64-bit output. This is done to reconstruct the analog input from the ADC12DJ3200 EVM. The LED_DEBUG_BLK block is used to debug the JESD and XCVR signal status.

The following figure shows the ADC12DJ3200 EVM GUI that is used to program the ADC and clocks.

Figure 1-5. ADC12DJ3200 GUI - EVM Tab

User input configuration settings in ADC12DJ3200 GUI for this design is as follows:

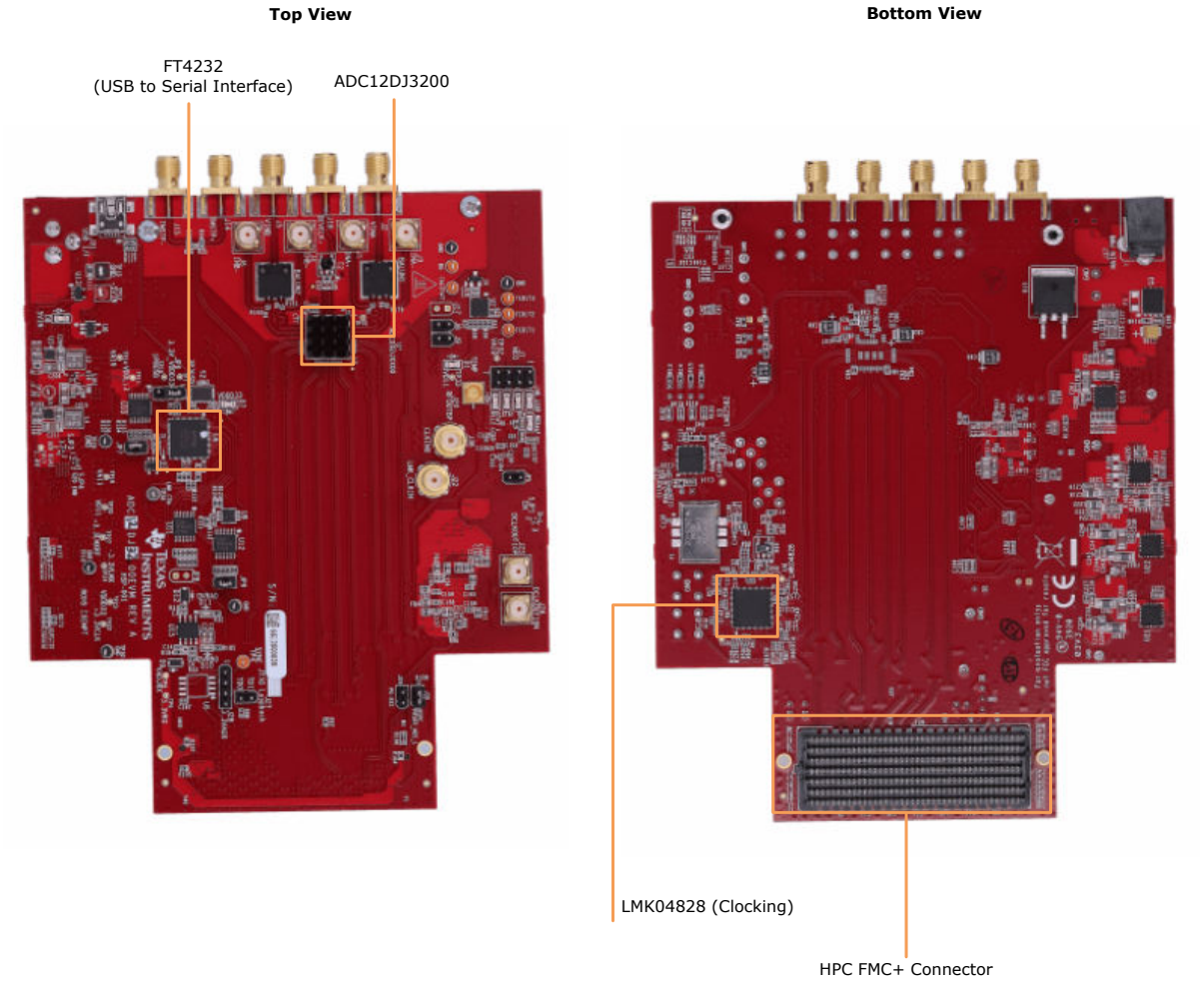
1. **Clock Source:** Select **On-board** where LMK04828 is used to generate clock for the ADC and reference clock for the FPGA.
2. **On-board Fs Selection:** Select **Fs = 1250 Msps**, where Fs is device clock which is calculated by dividing the JESD204B line rate with the R factor. R is chosen from Table-19 of ADC12DJ3200 Datasheet as per the JMODE used.
3. **Decimation and Serial Data Mode:** Select **JMODE2** as per the JESD Rx lane configuration and its other parameters.

2. Interoperability Test Setup

The interoperability test is performed on the RT PolarFire Evaluation Kit board with the RTPF500TS-1CG1509M device and TI ADC12DJ3200 EVM. The design for the test is developed using the Libero SoC software by instantiating the CoreJESD204BRX IP and other required IP cores in the SmartDesign. The design is tested for 5 Gbps data rate with four lanes configuration per ADC device. The register configuration of ADC12DJ3200 is done using ADC12DJ3200 GUI by Texas instruments. ADC12DJ3200 EVM is used to evaluate ADC12DJ3200. It is connected to the FPGA Mezzanine Card High Pin Count (FMC HPC) connector of the RT PolarFire Evaluation Kit.

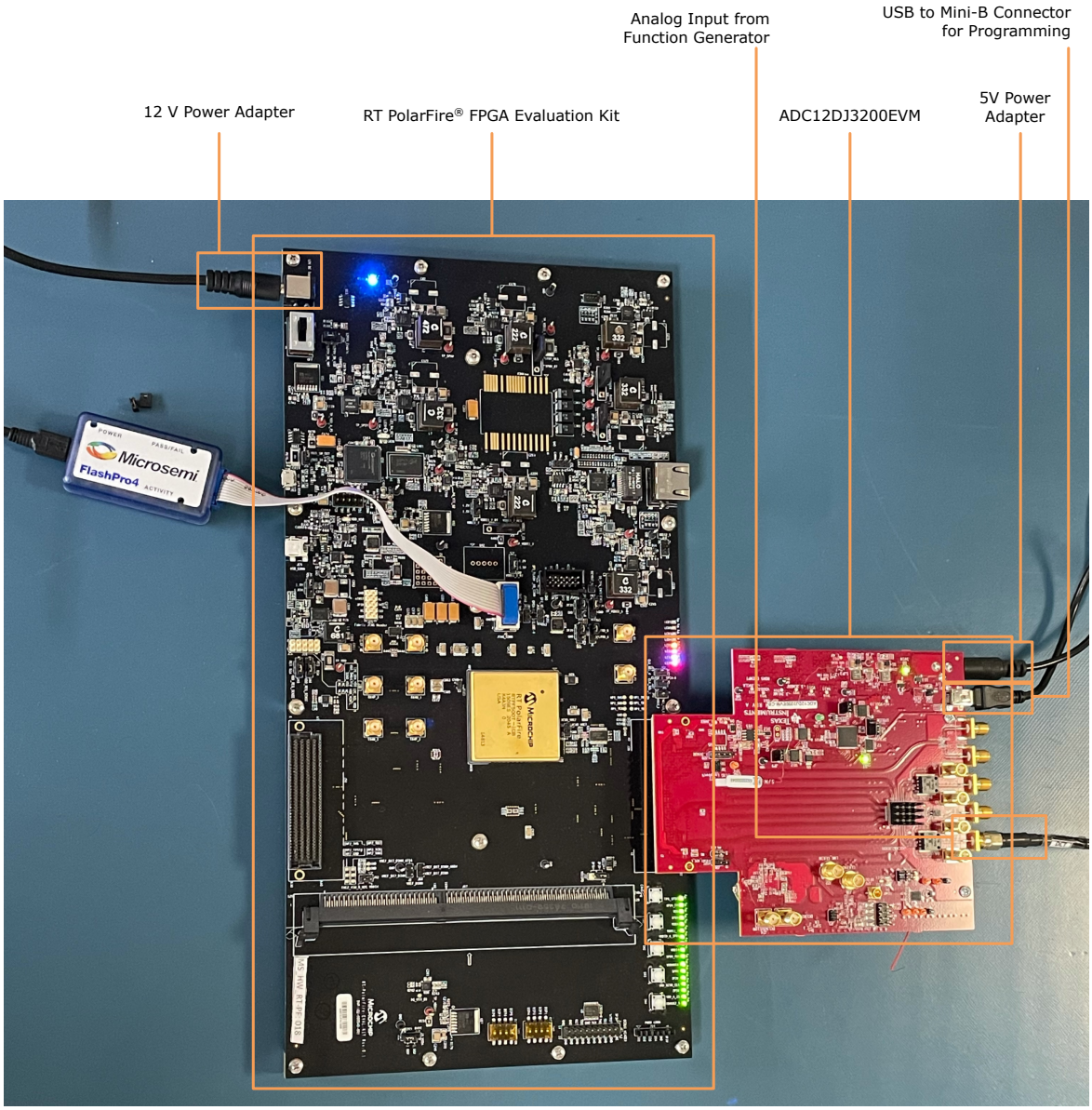
The following figure shows the ADC12DJ3200EVM evaluation kit board.

Figure 2-1. ADC12DJ3200EVM



The following figure shows the hardware setup for interoperability tests.

Figure 2-2. Hardware Setup for Interoperability Testing with ADC12DJ3200EVM



2.1 Interoperability Test Settings

CoreJESD204BRX and ADC12DJ3200 are configured, as listed in the following table.

Table 2-1. Configuring CoreJESD204BRX and ADC12DJ3200

Parameter	CoreJESD204BRX	ADC12DJ3200	Description
SCR	0/1	0/1	Scramble enable/disable
L	4	4 (per link)	Lanes
F	8	8	Octets per frame
K	4	4	Frames per multi-frame
M	4	4 (per link)	Converters
CS	0	0	Control bits per sample
N	12	12	Sample resolution
N'	12	12	Sample envelope
S	5	5	Samples per converter per frame
HD	0	0	High density mode
CF	0	0	Control bits per frame
SUBCLASSV	0	0	0

2.2 ADC12DJ3200EVM Interoperability Tests

The following interoperability tests were performed on RT PolarFire FPGA and ADC12DJ3200.

- Test 1: Data Link Layer—Code Group Synchronization
- Test 2: Data Link Layer—Initial Lane Alignment Sequence
- Test 3: Receiver Transport Layer
- Test 4: Descrambling

For more information about the preceding interoperability tests, see TR0066: Microsemi PolarFire FPGA CoreJESD204BRX Interoperability for ADC12DJ3200 Test Report.

3. Running the Demo

This section describes the steps to program the RT PolarFire FPGA device with the RTPF JESD design and detailed procedure to test the interoperability of RT PolarFire FPGA with ADC12DJ3200 device using JESD204B protocol.

Before programming the RT PolarFire device, ensure the following settings on the RT PolarFire Evaluation kit:

1. Ensure the jumper settings on the board are set to the default except the following:
   - J18—Short pin 5 and 6
   - J22—Short pin 1 and 2
   - J31—Open (when programming through External FlashPro programmer)
2. Connect the host PC to the J3 connector using External FlashPro Programmer.
3. Connect the power supply to the J19 connector and switch ON the power supply switch, SW7.

On the ADC12DJ3200 EVM, all the jumpers settings are set to default. Ensure the following settings on ADC12DJ3200 EVM:

- Connect 5V DC power supply to J37 connector.
- Connect one end of USB cable to J31 connector on the ADC12DJ3200 EVM while another end is connected to the host PC.
- Connect SMA cable to **VINA** SMA port on the ADC12DJ3200 EVM to provide single-ended analog input from the function generator.
- Connect HPC FMC+ connector of the ADC12DJ3200 EVM with J38 FMC1 connector on the RT PolarFire Evaluation kit.

Analog input can be ramp, sine, square wave, and so on. In this demo, ramp and sine wave inputs are transmitted and received successfully at the RT PolarFire FPGA JESD204B output.

3.1 Programming the Device using Libero SoC

To program the device, follow these steps:

1. Open the design in Libero SoC software. The Libero **Design Flow** window appears.
2. Double-click **Run PROGRAM Action.** After programming the device successfully programmed, a green tick appears on **Run PROGRAM Action**.

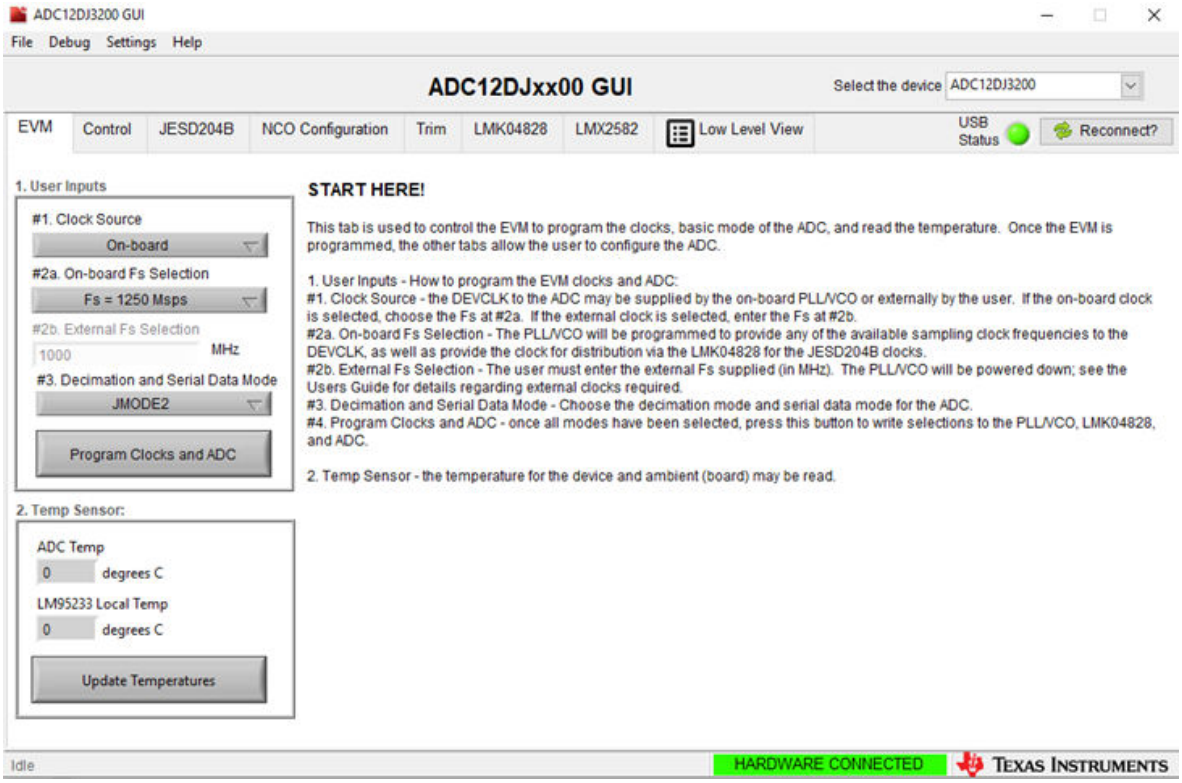
Note: To program the device using FlashPro Express, see Appendix: Programming the Device using FlashPro Express.

3.2 Running the Design

After programming the device, debug LEDs glow as per the status of the JESD and XCVR signals. Follow these steps to test the interoperability of RT PolarFire FPGA with the ADC12DJ3200 EVM:

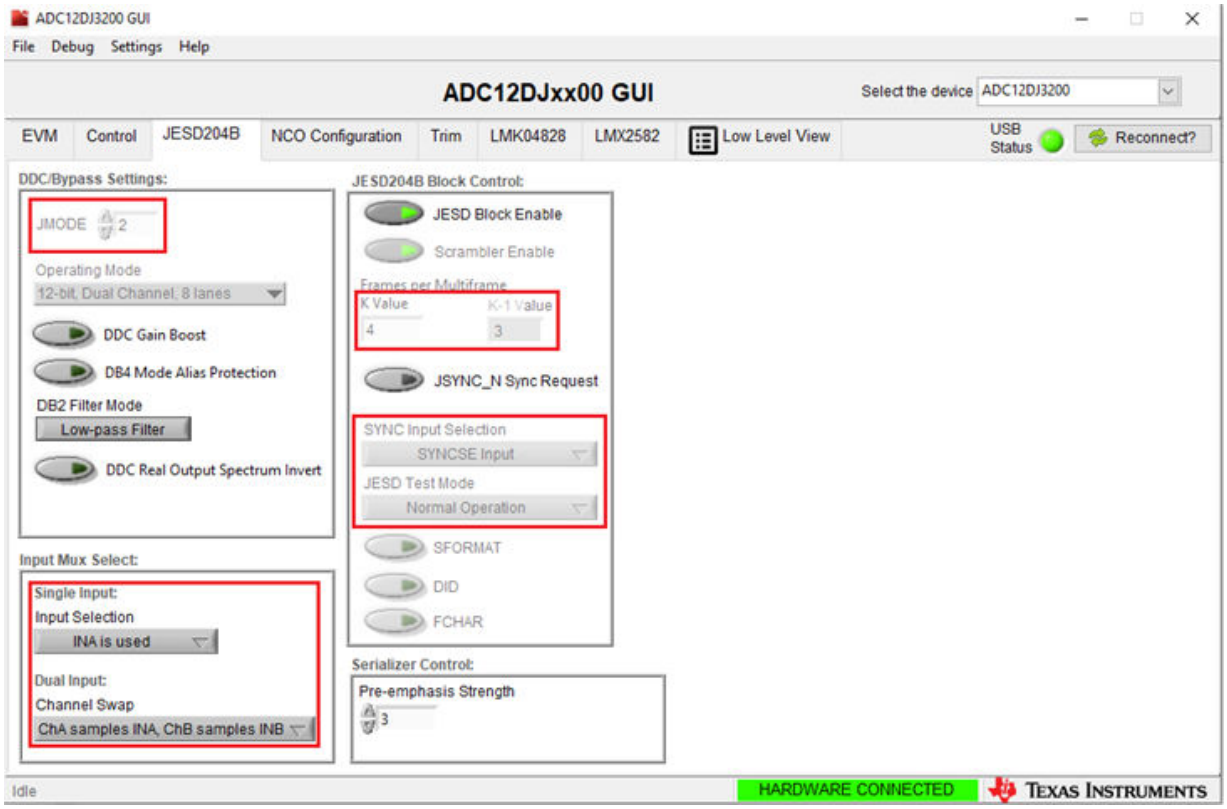
1. Install the ADC12DJ3200 application (`setup.exe`) from the following design files folder: `rtpf_jesd_df\GUI\Volume`
2. Launch the ADC12DJ3200 application.
3. In the **EVM** tab, select:
   - Clock Source: On-board
   - On-board Fs selection: 1250 Msps
   - Decimation and Serial Data Mode: JMODE2

Figure 3-1. ADC12DJ3200 GUI - EVM Tab



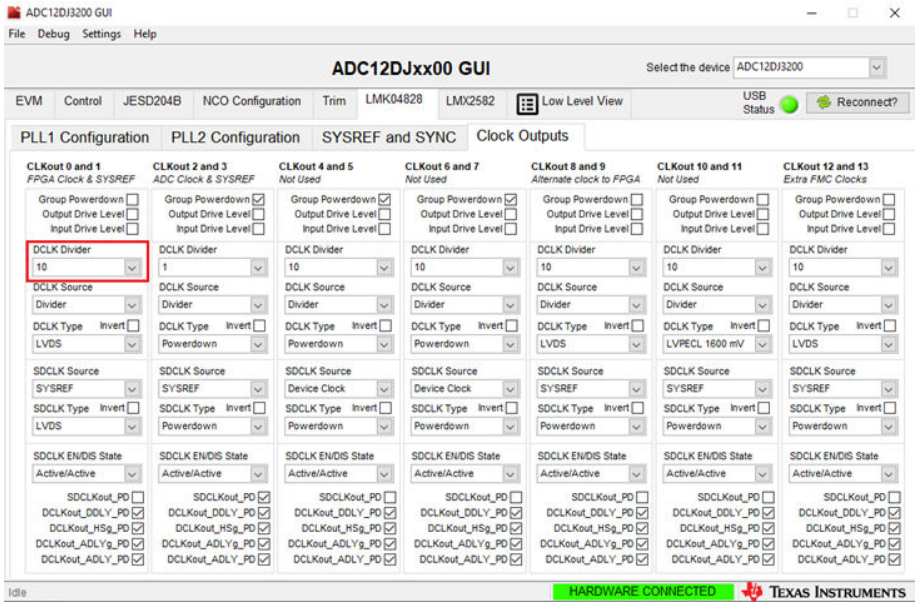
4. Click **Program Clocks and ADC.**
5. Go to **JESD204B** tab and ensure the parameters are set as shown in the following figure.

Figure 3-2. ADC12DJ3200 GUI - JESD204B Tab



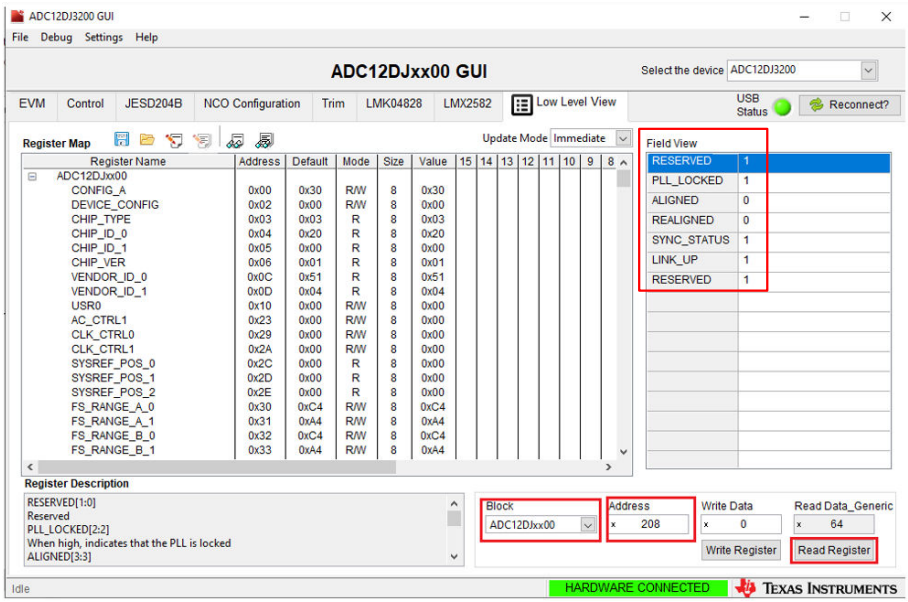
6. Go to **LMK04828** tab and ensure the device clock divider is set as shown in the following figure.

Figure 3-3. ADC12DJ3200 GUI - LMK04828 Tab



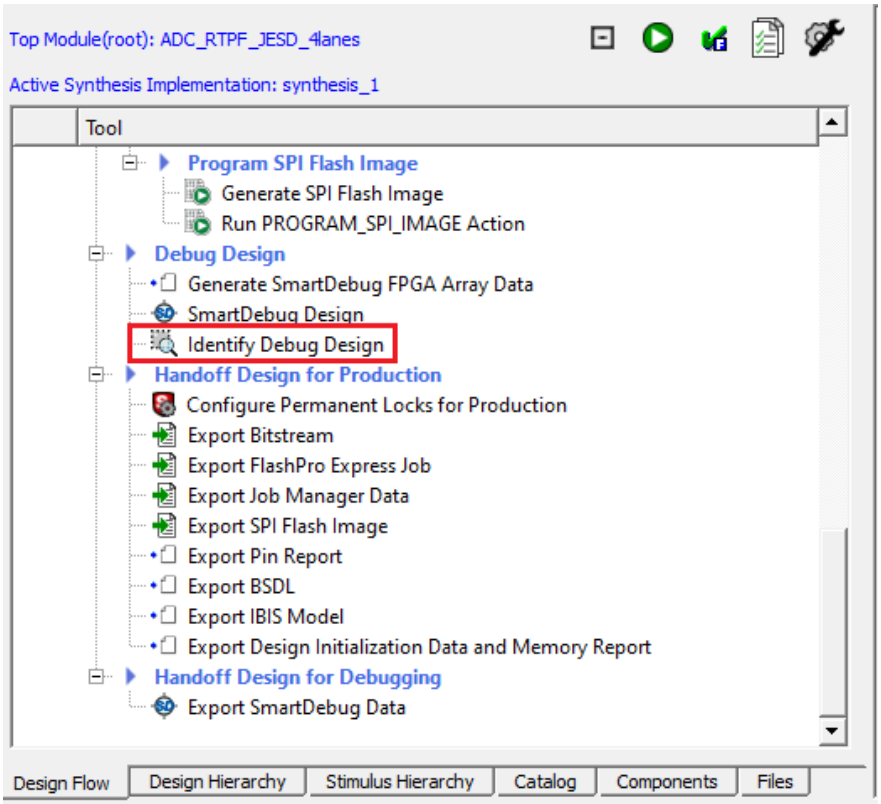
7. In the **Low Level View** tab, select **Block** as ADC12DJxx00 with **Address** 0x208 and click **Read Register** to read the JESD status register. The JESD status register bits must be set as shown in the following figure.

Figure 3-4. ADC12DJ3200 GUI - Low Level View Tab



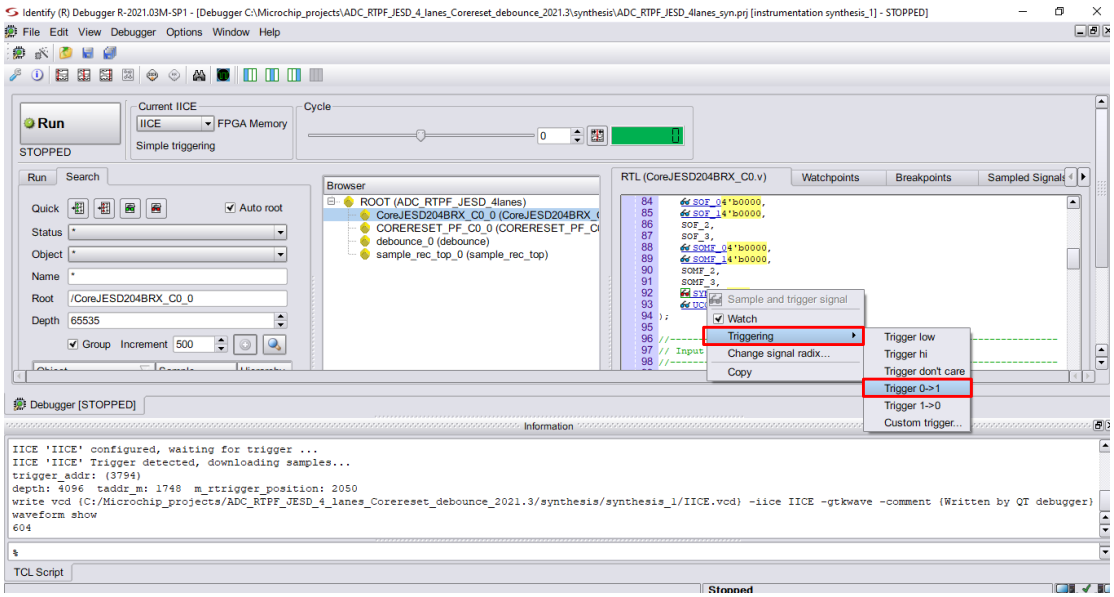
8. When the JESD link is up and **SYNC** Signal status goes HIGH, go to Libero SoC, and invoke Identify Debugger as shown in the following figure.

Figure 3-5. Identify Debug Design



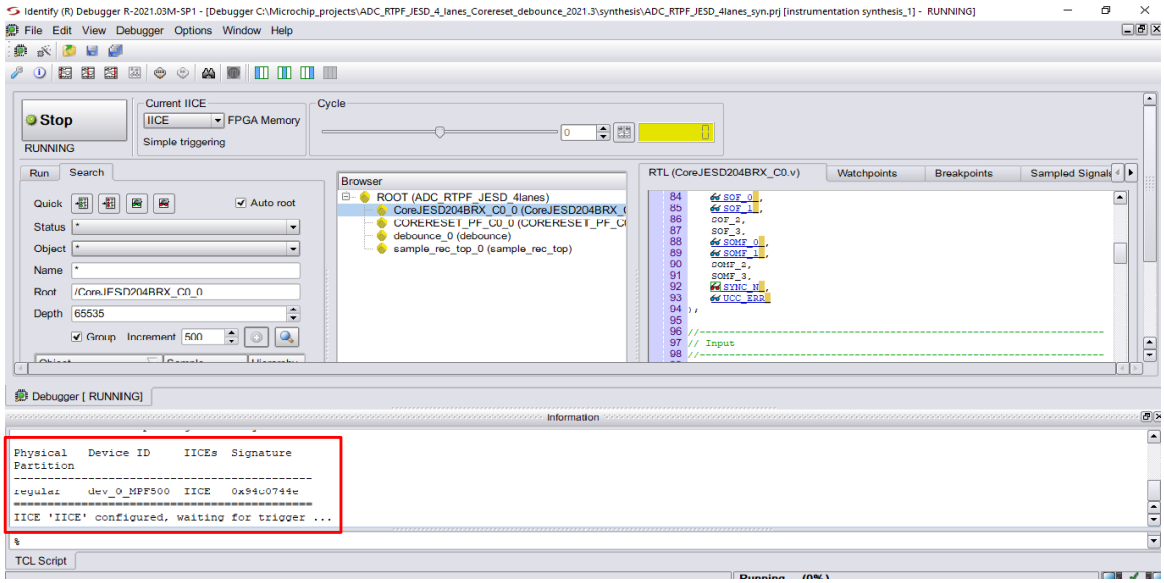
9. When the Identify Debugger opens, ensure the **SYNC** signal in the JESD204BRX module is set for a trigger on 0 to 1 transition. Right-click on the SYNC signal and select **Triggering** > **Trigger 0->1**, as shown in the following figure.

Figure 3-6. Identify Debugger Window



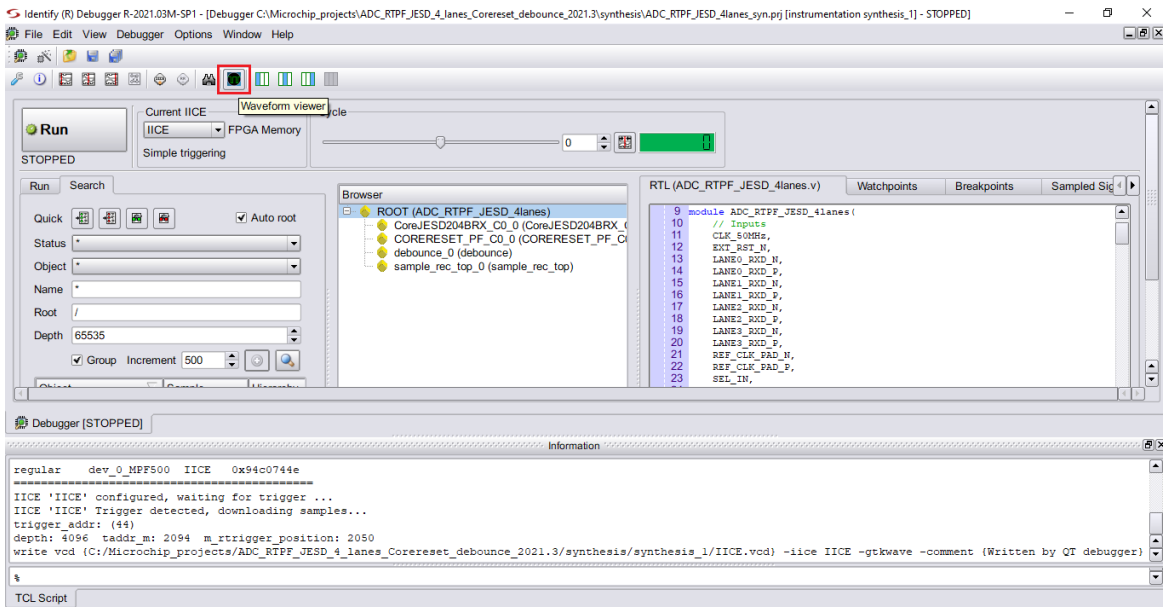
10. Run the **Identify Debugger**. The console window shows that the Identify is waiting for the trigger. Press **SW_URST** switch on the board.

Figure 3-7. Run the Identify Debugger



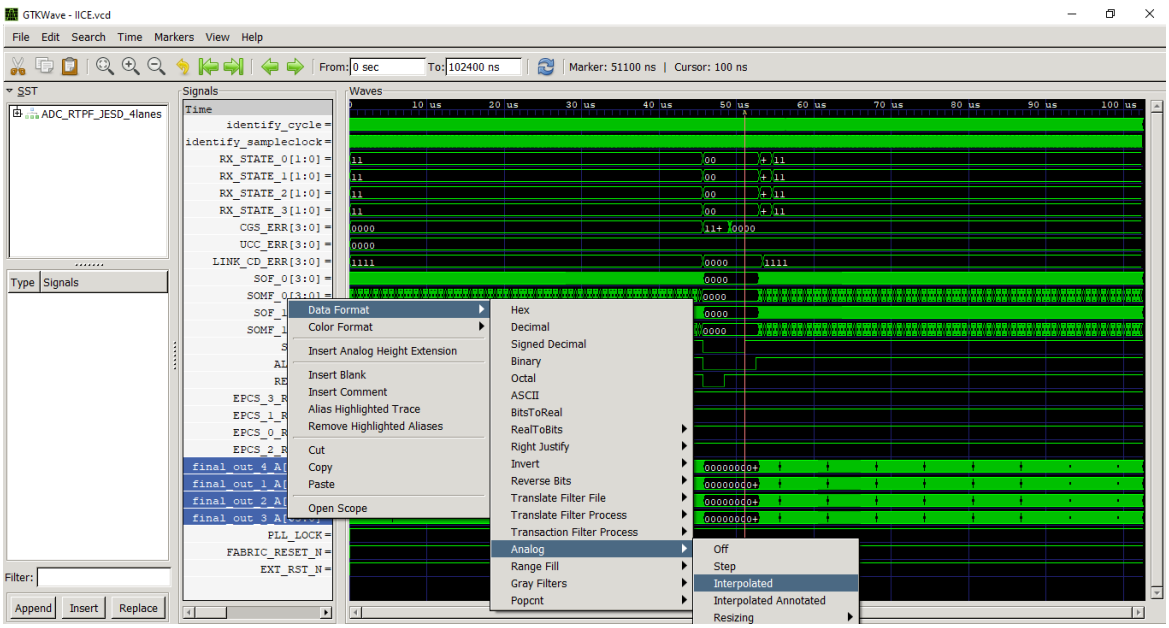
11. Click **Waveform viewer** icon as highlighted in the following figure. GTTKWave window appears.

Figure 3-8. Waveform Viewer



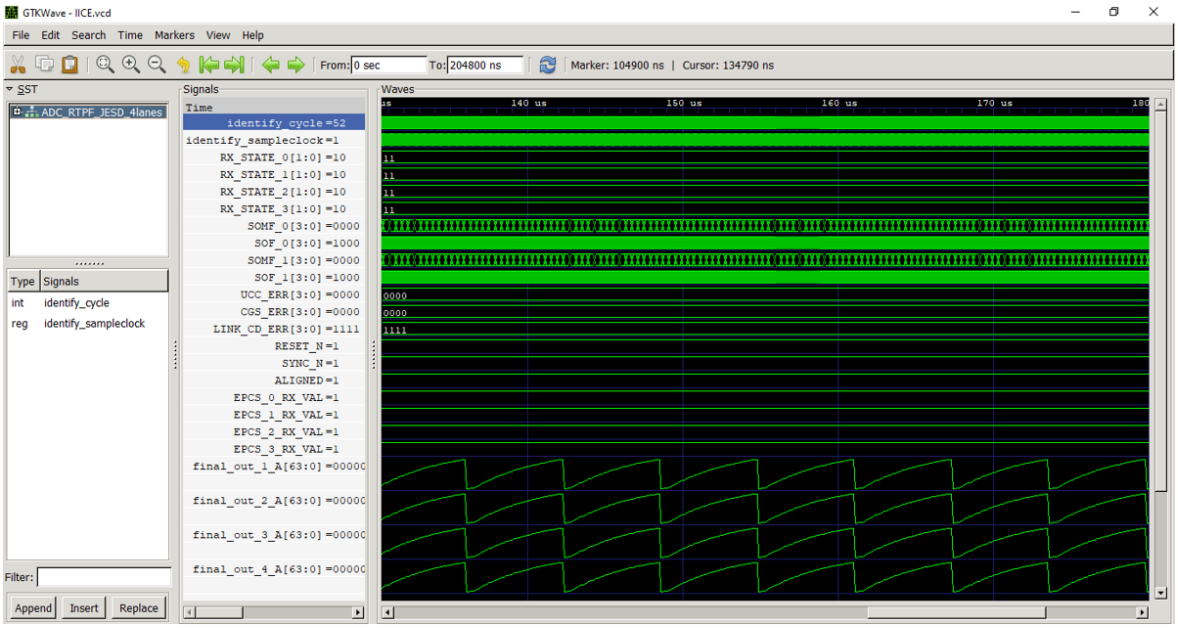
12. Right-click **64-bit final_out_x_A** output from each lanes and select data format as **Analog > Interpolated** as shown in the figure.

Figure 3-9. GTKWave Window - Data Format



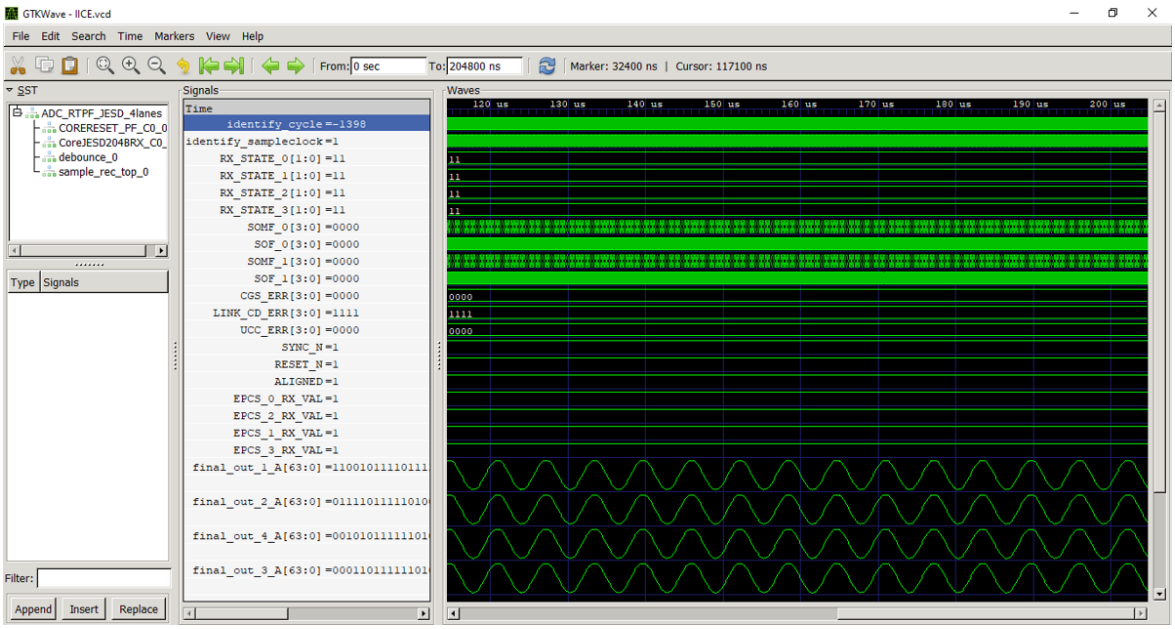
13. When ramp signal is provided as an input signal to ADC12DJ3200 EVM, the ramp signal is successfully reconstructed in the RT PolarFire FPGA device as shown in the following figure.

Figure 3-10. GTKWave Window



14. When Sinusoidal signal is provided as an input signal to ADC12DJ3200 EVM, the sinusoidal signal is successfully reconstructed in the RT PolarFire FPGA device as shown in the following figure.

Figure 3-11. GTKWave Window



This concludes running the demo.

Note: When the Identify Debugger is in RUN state, the design is already up and running. When reset is asserted, re-initialization and re-alignment happens as seen in the waveforms.

Note: LIND_CD_ERR = 1 indicates configuration parameters of link configuration data do not match with the configuration parameters of the JESD204BRX core. In the preceding waveforms, LINK_CD_ERR is equal to 1 because ADC12DJ3200 is using JMODE2 which configures the ADC for dual channel, eight lanes configuration while JESD204BRX IP is only configured for four lanes in the design. Only four lanes of ADC device are used with the JESD204BRX device resulting in design working successfully.

4. Appendix: Programming the Device using FlashPro Express

This section describes how to program the RT PolarFire device with the `.job` programming file using FlashPro Express. The `.job` file is available at the following design files folder location: <*download_folder*>*Programming_Job*

To program the device, complete the following steps:

1. On the host PC, launch the **FlashPro Express** software.
2. Click **New** or select **New Job Project** from **Project** menu to create a new job project.
3. Enter the following in the **Create New Job Project** dialog box:
   - **Programming job file**: Click **Browse** and navigate to the location where the `.job` file is located and select the file. The default location is: <*download_folder*>*Programming_Job*
   - **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project.
4. Click **OK**. The required programming file is selected and ready to be programmed in the device.
5. The **FlashPro Express** window appears. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.
6. Click **RUN** to program the device. When the device is programmed successfully, a **PROGRAMMER(S) PASSED** status is displayed.
7. Close **FlashPro Express, Project** > **Exit**.

See 3. Running the Demo section to run the demo.

5. Appendix: Running the TCL Script

TCL scripts are provided in the design files folder under the directory **TCL_Scripts**. If required, the design flow can be reproduced from Design Implementation before the job file is generated.

To run TCL, follow these steps:

1. Launch the Libero software
2. Select **Project > Execute Script....**
3. Click **Browse** and select **script.tcl** from the downloaded TCL_Scripts directory.
4. Click **Run**.

Note: To use the scripts provided along with the design, add the identify instrumentor in the design manually and then rerun the complete flow.

After successful execution of the TCL script, the Libero project is created within the **TCL_Scripts** directory.

For more information about TCL scripts, see ***<design_name>/TCL_Scripts/readme.txt*.**

See Libero® SoC TCL Command Reference Guide for more information about TCL commands. Contact Technical Support for any queries about running the TCL script.

6. Revision History

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 6-1. Revision History

Revision	Date	Description
A	01/2022	Initial document.

Microchip FPGA Support

Microchip FPGA products group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. Customers are suggested to visit Microchip online resources prior to contacting support as it is very likely that their queries have been already answered.

Contact Technical Support Center through the website at www.microchip.com/support. Mention the FPGA Device Part number, select appropriate case category, and upload design files while creating a technical support case.

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.

- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet- Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, NVM Express, NVMe, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY,

ISBN: 978-1-5224-9644-1

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-72400 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820