RT PolarFire® FPGA Single Event Latch-Up Test Report

TAMU June 20th 2019, LBNL Sep 9th 2019, and TAMU Oct 31st 2020

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SUMMARY

Heavy Ion testing was performed on Microchip's RT PolarFire FPGA at two facilities, Texas A&M University (TAMU) on 06/20/19 and 10/31/20 and Lawrence Berkeley National Laboratory (LBNL) on 09/06/19. The main objective of these test campaigns was to test the product for Single Event Latch-up (SEL). For these tests, the MPF500T device was tested since the RTPF500 device was not available at the time of testing. The silicon for the two devices is identical, the only difference is the top metal layers to accommodate a ceramic package for RTPF500 device. Therefore, we do not expect the SEL results to change once we test the RTPF500 device. The testing results are summarized below:

1. The SEL occurrence depends on the General Purpose I/O (GPIO) V_{DDI} and V_{DDAUX} power supply domains (refer to Channel I-4 in Table I), and their biases are varied with two values, 1.89 V and 2.625 V for the 06/20/19 TAMU test and 09/06/19 LBNL test. For the 10/31/20 TAMU test refer to Table II for the bias of the V_{DDI} and V_{DDAUX} power supply domains.
    a. The SEL LET threshold at 2.625V (V_{DDAUX} and V_{DDI}) and 100°C is between 58.3 and 60 MeV-cm^2/mg.
    b. The SEL LET threshold at 1.89V V_{DDI} and 2.575V V_{DDAUX}, 100°C, is higher than 80 MeV-cm^2/mg.
2. Previous tests showed the SEL LET threshold at 3.465V (V_{DDAUX} and V_{DDI}) and 100°C is between 25 and 48 MeV-cm2/mg.
3. No SEL was observed in the High Speed I/O (HSIO)

The SEL LET threshold for different supported GPIO V_{DDI} and V_{DDAUX} are summarized in Table III.

Table I. Power supply domains and bias for the 06/20/19 TAMU test and 09/06/19 LBNL test

Channel Number	Max Voltage (V)	Power Supply Domain
I-1	1.08	V_{DD}, V_{DDA}
I-2	1.89	V_{DD18}, V_{DDI0}, V_{DDI1}, V_{DDI6}, V_{DDI7}
I-3	2.625	V_{DD25}, V_{DDA25}, V_{DDSREF}, SERDESVREF
I-4	1.89 or 2.625	V_{DDAUX2}, V_{DDAUX4}, V_{DDAUX5}, V_{DDI2}, V_{DDI3}, V_{DDI4}, V_{DDI5}

Table II. Power supply domains and bias for the 10/31/20 TAMU test

Channel Number	Max Voltage (V)	Power Supply Domain
I-1	1.08	V_{DD}, V_{DDA}
I-2	1.89	V_{DD18}, V_{DDI0}, V_{DDI1}, V_{DDI6}, V_{DDI7}
I-3	2.625	V_{DD25}, V_{DDA25}, V_{DDSREF}, SERDESVREF
I-4	2.575 and 2.625	V_{DDAUX2}, V_{DDAUX4}, V_{DDAUX5}
II-1	1.89	V_{DDI2} (GPIO)
II-2	1.89	V_{DDI3} (JTAG)
II-3	1.89	V_{DDI4}(GPIO)
II-4	1.89	V_{DDI5}(GPIO)

Table III. SEL LET threshold vs. supported GPIO V_{DDI} and V_{DDAUX}

GPIO V_{DDI}	GPIO V_{DDAUX}	SEL LET_{TH} (MeV-cm^2/mg)	Support
3.3V ±5%	3.3V ±5%	$25 < LET_{TH} < 48$	Fully Supported including LVDS
2.5V ±5%	2.5V ±5%	$58.3 < LET_{TH} < 60$	Fully Supported including LVDS
1.8V ±5%	2.5V ±3%	$80 < LET_{TH}$	Fully Supported including LVDS
1.8V ±5%	1.8V ±5%	$80 < LET_{TH}$	Not Supported

I. TEST OBJECTIVE

The primary objective is to characterize the SEL of the RT PolarFire (RTPF) device. The goal is to find the SEL LET threshold at high temperature of approximately 100°C. Based on customers' requirement, there are two targeted milestones for LET threshold, 60 MeV-cm^2/mg and 80 MeV-cm^2/mg.

II. DEVICE UNDER TEST

The device under test (DUT) is the PolarFire MPF500T, and Table IV lists the DUT information.

Table IV. DUT information

Device	MPF500T
Package	FCG1152
Foundry	UMC
Technology	28 nm
Revision	F
Lot Number (Test Date)	K71SR (06/20/19 & 09/06/19), K77JR (06/20/19 & 09/06/19), K818M/K808N (10/31/20)
Quantity Tested	11
DUT Design	G5_dynamic_avionics

III. TEST METHODS

In general, the test follows the guidelines of two testing standards: ASTM standard F1192M-95 "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation on Semiconductor Devices" and JEDEC standard JESD57 "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation."

1. Heavy-Ion Irradiation

The 25 MeV/nucleon beam at TAMU and the 16 MeV/nucleon beam at LBNL provide a range of ions to perform well-controlled experiments to investigate single event effects (SEE) of integrated-circuit chips; in this test only Xe ion was tested to reach the two LET targets of 60 MeV-cm^2/mg and 80 MeV-cm^2/mg. The high energy beam is critical for penetrating the back-side silicon layer of the flip-chip FPGA and to reach the sensitive circuits on the front side. The back-side thickness of the PolarFire FPGA, which is about 775 µm, must be thinned down to approximately 100 µm to allow sufficient ion penetration.

2. DUT Design

The DUT is programmed with a design named "G5_dynamic_avionics", to collect soft error data on Flip-Flops, SRAM memories, Mathblocks and PLL. The Temperature-Voltage Sensor (TVS) is instantiated in the design to monitor the chip temperature during irradiation. During the test, the I/Os were active as soft error data was collected on the Flip-Flops, SRAMs, Mathblocks and PLL and the temperature was monitored. The DUT board (being irradiated) was connected to a mother board and continuously sending and receiving data during the test to collect soft errors on the blocks mentioned above.

IV. RESULTS AND DISCUSSIONS

Tables VII, VIII and IX summarize the results for all three tests, the 06/20/19 TAMU test, the 09/06/19 LBNL test and 10/31/20 TAMU test, respectively. The SEL occurrence depends on the GPIO V_{DDAUX} and V_{DDI} power supply domains (refer to Channel I-4 in Table I), and their biases are varied with two values, 1.89V and 2.625V for the 06/20/19 TAMU test and 09/06/19 LBNL test. For the 10/31/20 TAMU test refer to Table II for the bias of the V_{DDI} and V_{DDAUX} power supply domains.

- The SEL LET threshold (LET_{TH}) at 2.625V V_{DDAUX} and V_{DDI}, and 100°C is between 58.3 and 60 MeV-cm^2/mg

- The SEL LET threshold at 1.89 V_{DDAUX} and $V_{DDI,}$ 100°C is higher than 80 MeV-cm^2/mg. At the time of writing, values of V_{DDAUX} less than 2.5V nominal are not supported in PolarFire or RT PolarFire.
- The SEL LET threshold at 1.89V V_{DDI} and V_{DDAUX} 2.575V, 100°C, is higher than 80 MeV-cm^2/mg.
- Previous tests showed the SEL LET threshold at 3.465V V_{DDAUX} and $V_{DDI,}$ and 100°C is between 25 and 48 MeV-cm^2/mg.

No SEL was observed in High Speed I/O (HSIO) or JTAG bank (V_{DDI3}). During irradiation, both TCK (JTAG test clock) and TRSTB (JTAG test reset) pins were grounded.

Figure 1 shows all four power supply current domains and the temperature for one of the runs (run 12 in Table VII below). For this run the temperature was ~101°C and increased to ~126°C after the SEL occurred. The black curve shows the GPIO V_{DDI} and V_{DDAUX} SEL; for this test, the power supply clamp was set to 1A. The power supply clamp was set to 1A for the TAMU test and 0.5A for the LBNL test.

Multiple runs were performed on the part after SEL was observed and the part was functional. This is true for multiple parts. However, no long-term reliability study was performed to check for any latent damage. The SEL location was determined to be the ESD power clamps on V_{DDAUX} and V_{DDI}. Section IV. 1. below describes the current steps shown by the green curve in Figure 1.

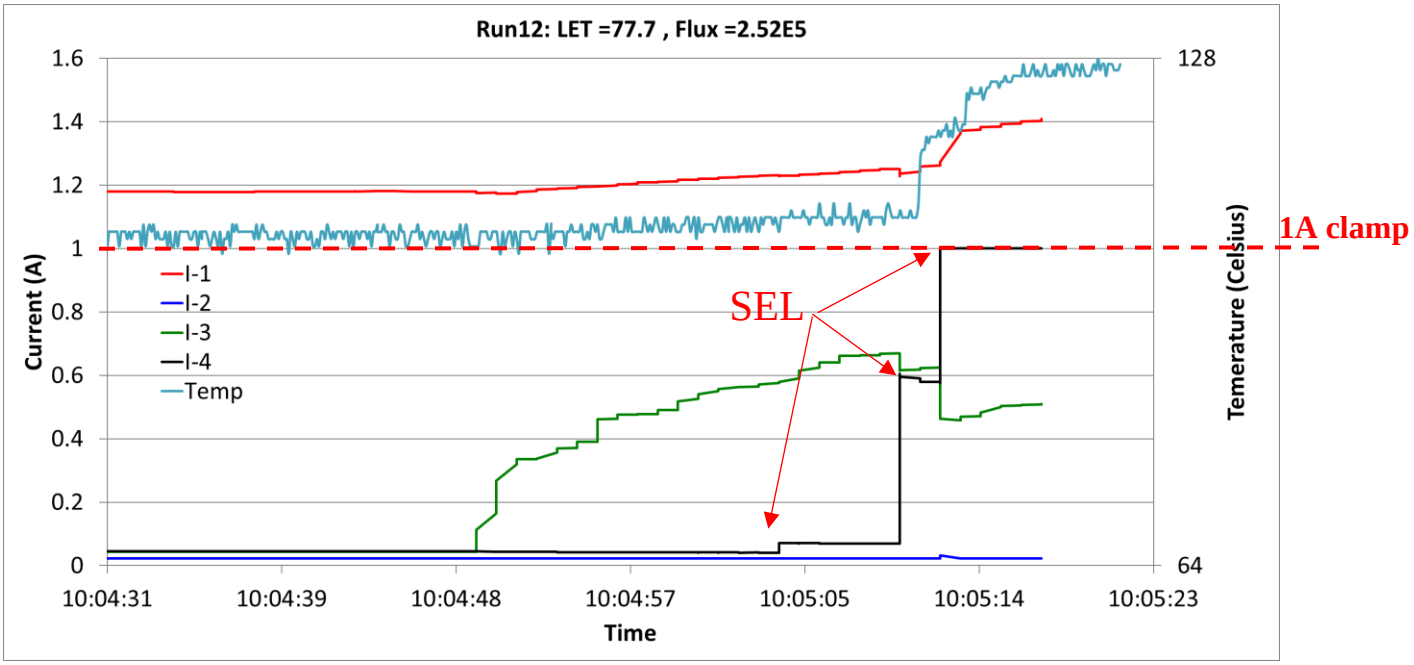

Figure. 1. All Four Power supply currents (refer to Table I) and temperature reading for run 12 (see Table III below), LET=77.7 MeV-cm^2/mg, 2.625V V_{DDAUX} and V_{DDI} and the fluence is 2.52×10^5 ions/cm^2.

2.5V current steps

The current steps shown by the green curve on Figure 1 are occurring on both VDD25 (FPGA core and FPGA PLL high voltage supply) and VDDA25 (Transceiver PLL high-voltage supply) supplies only at high temperature (not observed at room temperature). The current ramps in discrete steps (12-30mA) and saturates (around 0.7A) which shows there is a limited number of structures causing the ramp. The number of steps matches the number of 2.5V triple-well ESD structures on these supplies. The current is caused by local latch-up of the 2.5V triple-well ESD structures, also confirmed by laser testing. The current steps disappear after power cycle and do not affect SERDES or fabric functionality. The current steps cross sections observed on VDD25 and VDDA25 are shown in Figure 2. The error rate for GEO orbit, Solar Min, 100mils Aluminum shielding is 2.43×10^{-4} current steps/device/day, or 1 current step every 27 years. The Weibull parameters are summarized in Table V.

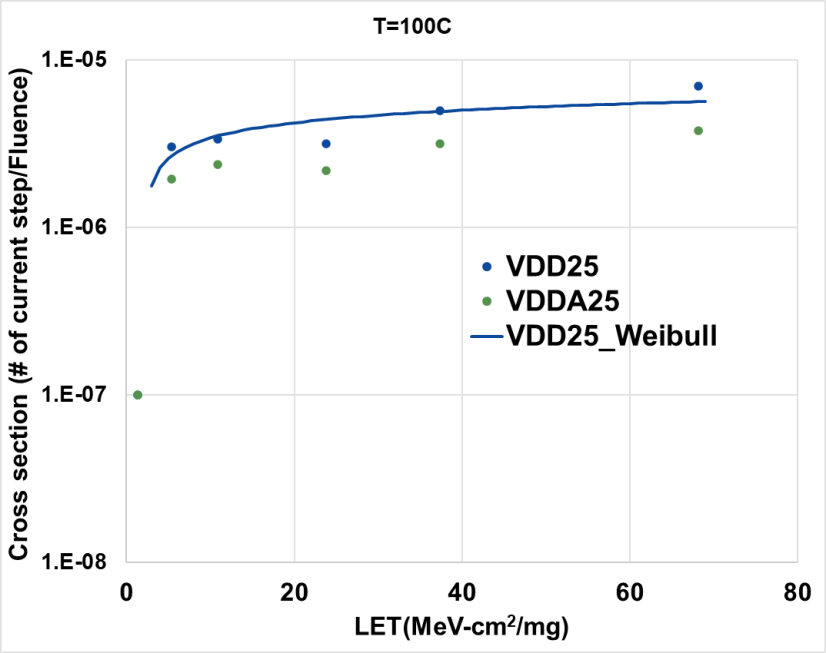

Figure. 2. Current steps cross sections observed on VDD25 and VDDA25 at 100°C.

Table V. Current steps Weibull parameters.

L0	W	S	A0
1.3	100	0.323	9.688×10^{-6}

The current steps were not observed in proton testing at high temperature up to a total fluence of 1.05×10^{12} p^{+}/cm^{2}. The upper bound cross section in Table VI is provided here to calculate an example LEO error rate using the JPSS-1 orbit parameters. The error rate for LEO environment (JPSS-1) is $<1.069\times10^{-5}$ current step/device/day, <1 current step every 256 years.

Table VI. Current steps proton results summary.

Fluence (p^{+}/cm^{2})	Cross section (cm^{2}/Chip)
1.05×10^{12}	$<9.52\times10^{-13}$

Tables VII, VIII and IX below summarize the results for all three tests, the 06/20/19 TAMU test, the 09/06/19 LBNL test and 10/31/20 TAMU test, respectively.

Table VII. TAMU (06/20/19) SEL results summary

Run#	DUT#	Ion	Energy	Tilt (deg)	LET_{eff}	I-4 (V_{DDI} and V_{DDAUX})	SEL	Fluence (ions/cm^{2})
7	9	Xe	25MeV	0	49.5	1.89V	No SEL	1.00×10^{7}
2	12	Xe	25MeV	0	50.9	1.89V	No SEL	9.98×10^{5}
3	12	Xe	25MeV	0	50.9	1.89V	No SEL	9.00×10^{6}
8	9	Xe	25MeV	-25	56	1.89V	No SEL	1.00×10^{7}
10	9	Xe	25MeV	30	60	1.89V	No SEL	1.00×10^{7}
13	1	Xe	25MeV	45	76.2	1.89V	No SEL	1.00×10^{7}

9	9	Xe	25MeV	-25	56	2.625V	No SEL	1.00×10^{7}
14	1	Xe	25MeV	30	58.3	2.625V	No SEL	1.00×10^{7}
6	7	Xe	25MeV	-30	60	2.625V	SEL	1.27×10^{6}
11	9	Xe	25MeV	30	60	2.625V	No SEL	1.00×10^{7}
4	12	Xe	25MeV	30	61.6	2.625V	SEL	2.05×10^{6}
5	12	Xe	25MeV	30	61.6	2.625V	SEL	1.27×10^{6}
12	9	Xe	25MeV	45	77.7	2.625V	SEL	2.52×10^{5}

Table VIII. LBNL (09/06/19) SEL Results Summary

Run#	DUT#	Ion	Energy	Tilt (deg)	LET_{eff}	I-4 (V_{DDI} and V_{DDAUX})	SEL	Fluence (ions/cm^2)
2	4	Xe	16MeV	0	68.8	1.89V	No SEL	5.74×10^{6}
3	4	Xe	16MeV	0	68.8	1.89V	No SEL	4.30×10^{6}
4	4	Xe	16MeV	30	79.4	1.89V	No SEL	5.00×10^{6}
20	8	Xe	16MeV	30	79.4	1.89V	No SEL	1.00×10^{7}
22	6	Xe	16MeV	30	79.4	1.89V	No SEL	8.02×10^{6}
1	4	Xe	16MeV	0	68.8	2.625V	SEL	3.87×10^{5}
18	8	Xe	16MeV	0	68.8	2.625V	SEL	5.88×10^{6}
19	8	Xe	16MeV	30	79.4	2.625V	SEL	5.21×10^{5}
21	6	Xe	16MeV	30	79.4	2.625V	SEL	1.15×10^{6}

Table IX. TAMU (10/31/20) SEL Results Summary

Run#	DUT#	Ion	Energy	Tilt (deg)	LET_{eff}	II-1-4 (V_{DDI2-5})	I-4 (V_{DDAUX})	SEL	Fluence (ions/cm^2)
1	50	Xe	25MeV	-41	80	1.89V	2.625V	Yes	3.40×10^{6}
2	50	Xe	25MeV	-41	80	1.89V	2.575V	No	1.00×10^{7}
3	50	Xe	25MeV	-41	80	1.89V	2.575V	No	1.00×10^{7}
4	50	Xe	25MeV	-41	80	1.89V	2.575V	No	1.00×10^{7}
5	50	Xe	25MeV	-41	80	2.575V	2.575V	Yes	1.00×10^{6}
6	50	Xe	25MeV	-41	80	1.89V	2.575V	No	1.00×10^{7}
7	52	Xe	25MeV	-43	80.3	1.89V	2.575V	No	1.00×10^{7}
8	52	Xe	25MeV	-43	80.3	2.575V	2.575V	Yes	Fluence not recorded
9	52	Xe	25MeV	-43	80.3	1.89V	2.625V	No	1.00×10^{7}
10	52	Xe	25MeV	-43	80.3	2.625V	2.625V	Yes	Fluence not recorded
11	48	Xe	25MeV	-42	80.2	1.89V	2.625V	No	1.00×10^{7}
12	48	Xe	25MeV	-42	80.2	1.89V	2.625V	No	1.00×10^{7}
13	48	Xe	25MeV	-42	80.2	2.625V	2.625V	Yes	Fluence not recorded
14	48	Xe	25MeV	-42	80.2	1.89V	2.575V	No	1.00×10^{7}
15	35	Xe	25MeV	-44	80.1	1.89V	2.625V	No	1.00×10^{7}
16	35	Xe	25MeV	-44	80.1	1.89V	2.625V	No	1.00×10^{7}

V. REVISION HISTORY

REVISION	DATE	DESCRIPTION
1	12/10/2021	Changed the 2.5V local latch-up rate to once in 27 years in GEO solar min conditions in section IV, under the heading “2.5V Current Steps”
N/A	1/25/2021	Initial Version