In Orbit Programming and SEE characterization of the Microchip RT PolarFire® FPGA Fabric

Nadia Rezzak, *Member, IEEE,* R. Chipana, C. Lao, G. Bakker, *Member, IEEE,* J. Mccollum, *Member, IEEE,* F. Hawley, *Member, IEEE,* K. O'Neill and E. Hamdy, *Senior Member, IEEE*

***Abstract*—Microchip Radiation Tolerant (RT) PolarFire Field Programmable Gate Array (FPGA) fabric in orbit programming is investigated using Total Ionizing Dose (TID), proton and heavy ion in-beam programming tests. In-beam programming results show that in orbit programming can be achieved and programming must be followed by stand-alone verify to ensure programming success. Single Event Effect (SEE) characterization of the FPGA fabric and Single Event Latch-up (SEL) using heavy ion and proton are also presented.**

***Index Terms*—Single-Event Effects, FPGA, SONOS.**

I. Introduction

Microchip Technology's Radiation Tolerant (RT) PolarFire® is a radiation tolerant non-volatile field programmable gate array (FPGA) fabricated in United Microelectronics Corporation (UMC) 28 nm technology, featuring a non-volatile, reprogrammable Silicon Oxide Nitride Oxide Silicon (SONOS) based FPGA fabric with high reliability and industry's lowest power to enable new capabilities for space applications. The 28nm non-volatile process yields very low static power. RT PolarFire FPGA delivers 481K Logic Elements (LEs), 24 lanes of 10 Gbps transceivers, 1,480 math blocks (DSP) and 33 Mbits of embedded Static Random Access Memory (SRAM) with Single Error Correction and Double Error Detection (SECDED) encoding.

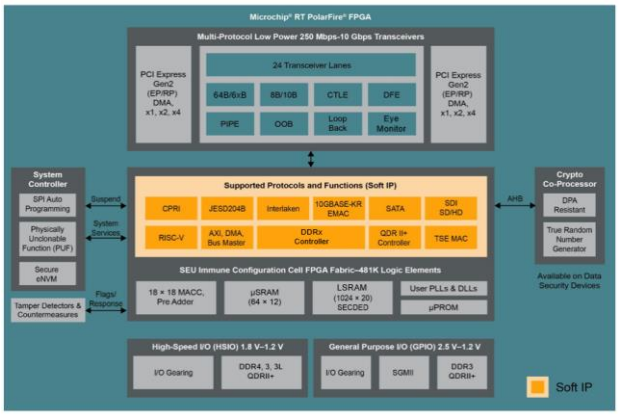

Figure. 1. RT PolarFire FPGA block diagram [1].

This Manuscript was submitted Sep 8th, 2021.
Nadia Rezzak, Raul Chipana, Chio Lao, Gregory Bakker, John Mccollum, Frank Hawley, Ken O'Neill and Esmat Hamdy are with Microchip FPGA business unit, 3850 N. 1st Street, San Jose, CA, 95134, USA (e-mail: nadia.rezzak@microchip.con).

RT PolarFire FPGAs are available in a hermetically sealed ceramic column grid array package and will be qualified to Qualified Manufacturers List (QML) standards, including QML class V, the highest qualification and screening standard for circuits in space.

II. In Orbit Programming

In-beam programming is investigated in this paper using TID, proton and heavy ion tests to determine whether RT PolarFire FPGAs can be programmed in orbit. In orbit programming in RT PolarFire FPGAs is supported using either Joint Test Action Group (JTAG) or Serial Peripheral Interface (SPI) interface [2]. During radiation testing, the JTAG interface and FlashPro programmer (Microchip programming system) were used, and the programming file was stored in an external computer. Even though only the JTAG interface was tested, the radiation results are expected to be the same for both JTAG and SPI interfaces. The circuits involved during programming are similar for both interfaces, the amount of logic associated with the JTAG interface is approximately the same as for SPI and both are small compared to the overall size of the controller (most of which is used during programming regardless of the interface used). The in-beam programming results presented in this paper are for the fabric only. The embedded Non-Volatile Memory (eNVM) block will be tested in the future.

A. TID Results

The TID testing was conducted at the Defense Microelectronics Activity (DMEA) in McClellan, CA. High temperature retention testing is performed at Microchip before TID testing. Because RT PolarFire FPGAs are expected to operate for 10 years at 110°C [3], 12 devices are baked unbiased for 4.3 months at 160°C, equivalent to 10 years retention at 110°C. TID testing of the MPF500T device is performed post-retention at DMEA. The MPF500T device was tested since the RTPF500T device was not available at the time of testing. The silicon for the two devices is identical, the only differences are changes to the top metal layers to accommodate a ceramic package for RTPF500T FPGA. Therefore, we do not expect the TID results to change when we test the RTPF500T device. The FPGA is irradiated at room temperature with a cobalt-60 gamma ray at a dose rate of 10 krad(SiO_2)/min, up to a maximum dose of 100krad(SiO_2). The FPGA is biased during irradiation, and programming followed by stand-alone verify is performed after irradiation. Twelve parts were tested and no programming or stand-alone verify failures were observed at 100 krad(SiO_2).

B. Proton Results

High energy proton experiments are performed at the Crocker Nuclear Laboratory (CNL) using the 64 MeV proton source. CNL's cyclotron can produce high-intensity, external beams of light ions that can be tuned to energies between 4 MeV and 67.5 MeV. The flux used is 1.2×10^6 p+/cm^2/s. The part is programmed 10 consecutive times, after each programming success a stand-alone verify is performed. The total fluence is 4.45×10^9 p+/cm^2. for all 10 programming and 10 stand-alone verify. Programming passed 10 times out of 10 attempts in proton beam. Stand-alone verify also passed 10 times out of 10 attempts in proton beam.

C. Heavy Ion Results

Heavy ion testing is performed at Texas A&M University (TAMU) using the 24.8 MeV/u beam, Ag ion, and 40 degrees tilt to reach LET=60.5 MeV-cm^2/mg. Two MPF500T DUTs were tested, the DUTs were thinned down to ~100µm, and the test was performed at the lowest flux available, the average flux was 19.5 ions/cm^2/s, which is still highly accelerated relative to space environment. The total fluence is 1.54×10^5 ions/cm^2 and two LETs were tested, 42 MeV-cm^2/mg and 60.5 MeV-cm^2/mg for destructive events. The flux in GEO orbit solar minimum (min) for LET=42 MeV-cm^2/mg, is 4.11×10^{-10} ions/cm^2/s and for LET=60.5 MeV-cm^2/mg, is ~1.03×10^{-10} ions/cm^2/s. For both LETs the accelerated flux is >10 orders of magnitude higher than the flux in space.

The part is reprogrammed while the beam is on and after each programming success, a stand-alone verify is performed. The testing procedure is summarized in Figure. 2.

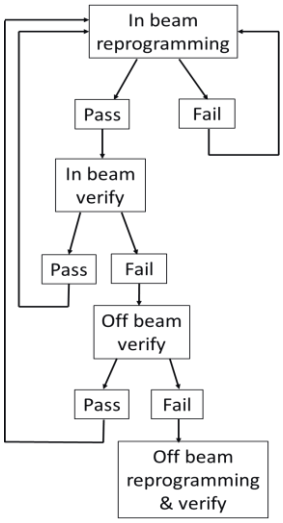

Figure. 2. In-beam programming and stand-alone verify testing procedure.

The programming operation includes an embedded verify. This verify uses the same data loaded into the FPGAs as programming. If the data is corrupted during load or programming, then verify will be performed using corrupted data, hence the need to perform a stand-alone verify after programming reports success. If programming fails, another programing is attempted. If programming passes, in-beam stand-alone verify is performed. If both programming and stand-alone verify pass, the programming is successful. Stand-alone verify uses a new load of the programming data, hence it is used as an independent test to check that programming completed successfully. Note that stand-alone verify itself may give a false failure, and so performing a second stand-alone verify is advised, if programming reports success and first stand-alone verify reports failure. Finally, if stand-alone verify fails in beam, stand-alone verify is attempted off beam and if off beam verify passes, we can conclude that it is a true programming pass. However, if it fails, we try off beam programming followed by stand-alone verify to make sure there is no destructive event during programming or stand-alone verify.

The results show no destructive events up to the test limit of 60.5 MeV-cm^2/mg. 6 out of 29 (20%) attempts successfully completed programming and stand-alone verify. We did observe false programming passes during radiation testing. For this reason, customers must perform stand-alone verify after each successful programming attempt. The results are summarized in Figure. 3.

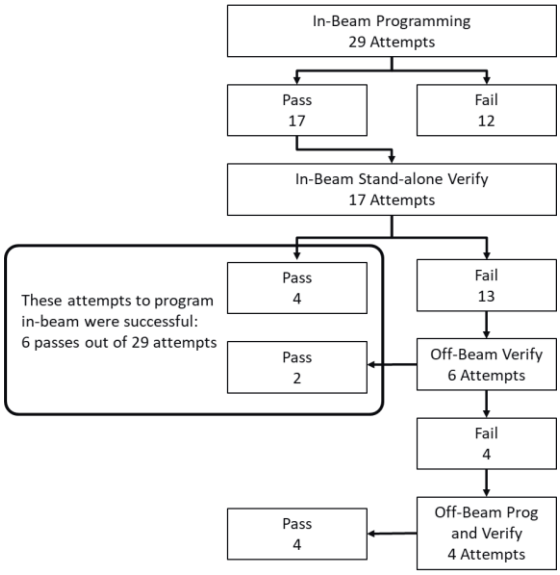

Figure. 3. In-beam programming and stand-alone verify results.

Failure to program is due to bit line or system controller flip-flop (FF) upset. The flip-flop cross section, programming time and number of bit line flip-flops are used to calculate the probability of programming failure in GEO orbit, solar min, 100 mils aluminum shielding.

Probability of programming failure = program time × #bit line FF × FF upset rate = 5.18×10^{-5} program failure/device/day, corresponding to 1 failure every 19,287 programming attempts in GEO orbit. Program time is ~8 min (480s), the number of bit line flip-flops is 40,576 bits, the flip-flop upset rate for GEO orbit, solar min is 2.3×10^{-7} errors/bit-day. The probability of programming success is > 99% in GEO orbit. RT PolarFire FPGAs support 500 programming cycles @ –40 °C to 100 °C.

When reprogramming fails, the device is erased but not damaged, and the next attempt to reprogram also has > 99% chance of success. In-beam reprogramming and verify are both non-destructive, there is an extremely low chance of destroying the part, the results show no destructive effects up to LET > 60 MeV-cm^2/mg. The programming circuits are functional after

heavy ion irradiation, to the LET level tested. Additional heavy ion SEL tests to total fluence of 8×10^7 ions/cm^2, LET = 80 MeV-cm^2/mg, T=100°C, show the parts were programmed and verified successfully. No destructive event was observed on the programming circuit during normal device operation up to LET = 80 MeV-cm^2/mg. Programming must be followed by stand-alone verify to ensure programming success:

1. If programming fails, attempt programming again
2. If stand-alone verify fails, attempt stand-alone verify again
3. If stand-alone verify fails a second time, attempt programming again

Based on the TID, proton and heavy ion results, we can conclude that successful in orbit reprogramming can be achieved in RT PolarFire FPGAs.

III. SEL Results

Two types of non-destructive SEL signatures were observed in RT PolarFire's General Purpose I/O (GPIO), 2.5V V_{DD25} and 2.5V V_{DDA25} supplies:

A. GPIO SEL Results

SEL testing was performed at high temperature up to ~100°C and maximum bias per datasheet (nominal+5%) [3]. Non-destructive SEL was observed in the GPIO and auxiliary supplies and the LET threshold depends on the GPIO and auxiliary supplies bias. These results were presented [4] and new results from tests performed at TAMU in Oct 2020 with GPIO V_{DDI} at 1.89V and V_{DDAUX} at 2.575V are included in this paper. The SEL LET threshold for different supported GPIO V_{DDI} and V_{DDAUX} are summarized in Table I. No SEL was observed in the High Speed I/O (HSIO). Figure. 4 shows no SEL in the GPIO supplies for LET=80 MeV-cm^2/mg, temperature of ~100°C, V_{DDAUX} =2.575V and V_{DDI}=1.89V and fluence=1×10^7 ions/cm^2. The temperature data points >100°C shown in Figure. 4 occur when the chip experiences a Single Event Functional Interrupt (SEFI) or a chip level reset, where the chip experiences an unintended reset with a momentarily loss of functionality. The SEFI self-recovers and no additional reset or power cycle is required to regain functionality of the design. The SEFI error rate with System Controller Suspend Mode (SCSM) deployed for GEO orbit is one functional failure every 40 years and has been reported in a 2020 RADECS workshop [4].

TABLE I
SEL LET THRESHOLD VS. SUPPORTED GPIO V_{DDI} AND V_{DDAUX}

GPIO V_{DDI}	GPIO V_{DDAUX}	SEL LET_{TH} (MeV-cm^2/mg)
3.3V ±5%	3.3V ±5%	$25 < LET_{TH} < 48$
2.5V ±5%	2.5V ±5%	$58.3 < LET_{TH} < 60$
1.8V ±5%	2.5V ±3%	$LET_{TH} > 80$

B. 2.5V (V_{DD25}, V_{DDA25}) SEL Results

Small and non-destructive ≤ 30mA SEL current steps are observed on both V_{DD25} (FPGA core and FPGA PLL high voltage supply) and V_{DDA25} (transceiver PLL high-voltage supply) at high temperature only. The SEL was not observed at room temperature up to LET of 68 MeV-cm^2/mg and fluence $>1\times10^7$ ions/cm^2. The green curve on Figure. 4 shows the current steps of ~10-30mA (a zoomed in view up to one minute of irradiation time is also shown in Figure. 4) and saturates around 0.2A, which shows there is a limited number of structures causing the current steps. At this current level there is no electromigration issue since the clamps were designed with enough metal to handle electrostatic discharge (ESD) levels of over 1.33A each. Also, the increase in local temperature caused by the increased current is very small (less than 5°C) and is dispersed in the large ESD structures. The number of steps matches the number of 2.5V triple-well ESD structures on these supplies. The current is caused by local latch-up of the 2.5V triple-well ESD structures, also confirmed by Two Photon Absorption (TPA) laser testing performed at the University of Saskatchewan. Scanning the area with ESD structures showed similar SEL observed in heavy ion testing. The current steps or SEL can be cleared with power cycle and does not affect the transceiver or fabric functionality.

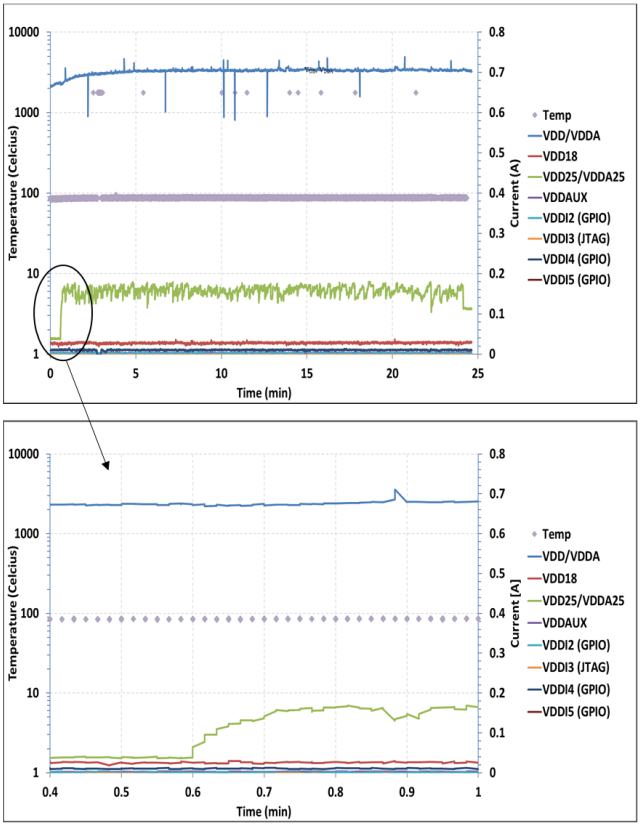

Figure. 4. Power supply currents and temperature reading, LET=80 MeV-cm^2/mg, V_{DDAUX} =2.575V and V_{DDI}=1.89V, fluence is 1×10^7 ions/cm^2 and flux is ~1×10^4 ions/cm^2/s.

The current steps cross section (from previous LBNL Apr'19 and latest TAMU Oct'20 heavy ion tests) is shown in Figure 5. The error rate for GEO orbit, solar min, 100 mils aluminum shielding is 1.01×10^{-4} current steps/device/day, or one current step every 27 years. The Weibull parameters are summarized in Table II.

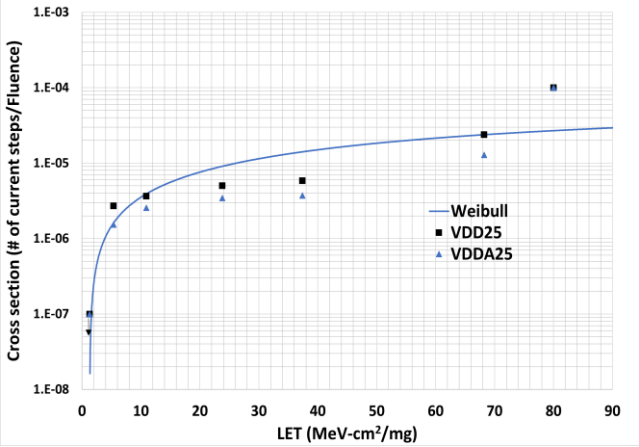

Figure. 5. 2.5V (V_{DD25}, V_{DDA25}) SEL cross section.

TABLE II
2.5V V_{DD25} V_{DDA25} SEL WEIBULL PARAMETERS

L0	W	S	A0
1.3	115	1.05	5.50×10^{-5}

The 2.5V (V_{DD25} and V_{DDA25}) SEL was not observed in proton testing using the 64 MeV beam at high temperature (~100°C) up to a total fluence of 1.05×10^{12} p^+/cm^2. The upper bound cross section in Table III is provided here to calculate an example LEO error rate using the JPSS-1 orbit parameters [5]. The error rate for LEO environment (JPSS-1) is $<1.069\times10^{-5}$ current step/device/day, <one current step every 256 years.

TABLE III
2.5V V_{DD25} V_{DDA25} SEL PROTON RESULTS SUMMARY

Fluence (p^+/cm^2)	Cross section (cm^2/Chip)
1.05×10^{12}	$<9.52\times10^{-13}$

IV. FABRIC SEU RESULTS

A. Global Clock Upset

The clock hierarchy in RT PolarFire FPGAs from the highest to the lowest level of clock resources is the following: chip level (T) clock, row level (R) clock, sector level (S) clock and finally cluster level clock, where each cluster contains 12 flip-flops as shown in Figure. 6.

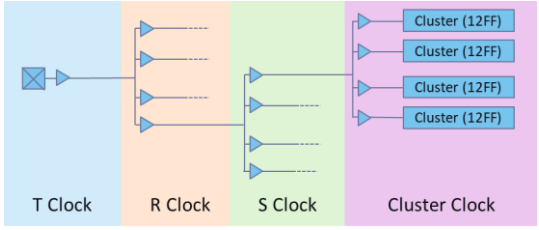

Figure. 6. The clock hierarchy in RT PolarFire FPGAs.

The cross sections for each clock level, T, R, S and cluster level clock circuit are shown in Figure. 7 (a) for T, R, S clock and Figure. 7 (b) for cluster clock level. The cluster clock Weibull parameters are shown in Table IV. The testing design with constrained placement and Synthesized Triple Modular Redundancy (TMR) flip-flop was used to get the different cross sections for the different clock levels (T, R and S). Cluster level clock upsets can be mitigated by automated constrained placement, available in Microchip's Libero® SoC v12.4 tool suite, combined with the synthesized TMR flip-flop, where TMR flip-flop results were reported in a RADECS workshop [4]. However, if customers decide to use non-TMR flip-flop, the cluster clock upset is shown in Figure. 7 (b) and non-TMR flip-Flop cross section was reported in HEART 2019 proceedings [6]. The cluster clock error rate for GEO orbit, solar min, 100 mils aluminum shielding is 2.54×10^{-4} upset/cluster clock/day, or one cluster clock upset every 10 years. The cluster clock Weibull parameters are shown in Table IV. The error rates for T, R and S clock are 3.56×10^{-7} upset/T clock/day, 1.61×10^{-8} upset/R clock/day, 5.63×10^{-9} upset/S clock/day respectively. The total error rate depends on the number of clock resources used in the specific FPGA design. A fully populated MPF500T device has 24 T clock circuits, 1440 R clock circuits and 9120 S clock circuits. Thus, for a fully populated FPGA using all T, R, and S clock resources, the upset rates are one T clock upset every 320 years, one R clock upset every 118 years and one S clock upset every 53 years. Typically, most designs rarely use more than 50% of the available clock resources. The T, R, and S clock Weibull parameters are shown in Table V.

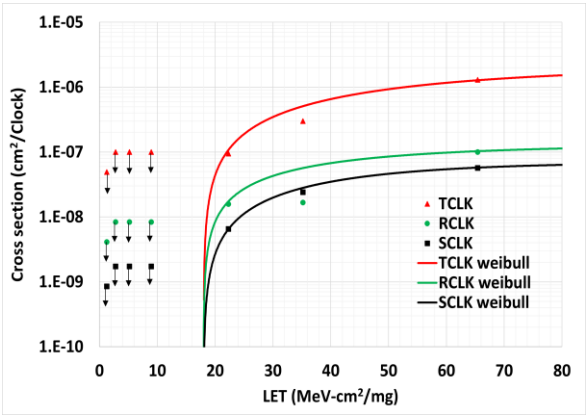

Figure. 7 (a). T, R, and S clock cross sections.

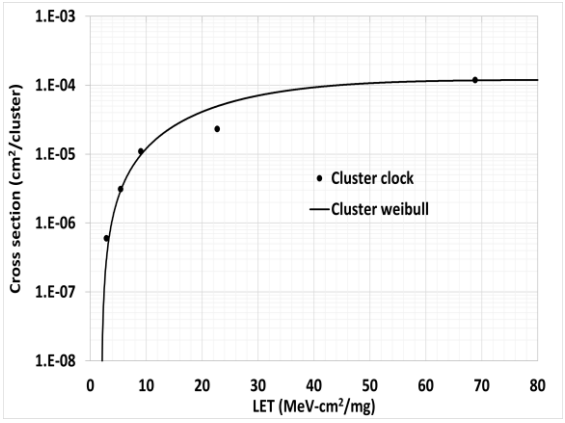

Figure. 7 (b). Cluster clock cross section.

TABLE IV
CLUSTER CLOCK WEIBULL PARAMETERS

L0	W	S	A0
2	30	1.7	1.20×10^{-4}

TABLE V
T, R, S CLOCK WEIBULL PARAMETERS

Circuit	L0	W	S	A0
T clock	18	50	1.2	2.10×10^{-6}
R clock	18	30	1.0	1.30×10^{-7}
S clock	18	30	1.2	7.00×10^{-8}

B. Math block Results

The math block design has two parallel math block chains with fixed coefficients A, B and C. 10 stages of math blocks were used in each chain performing the operation P = A*B + C. The math block cross section is shown in Figure. 8 and the error rate for GEO orbit, solar min, 100 mils aluminum shielding is 1.31×10^{-6} upset/Math block/day; the Weibull parameters are shown in Table VI.

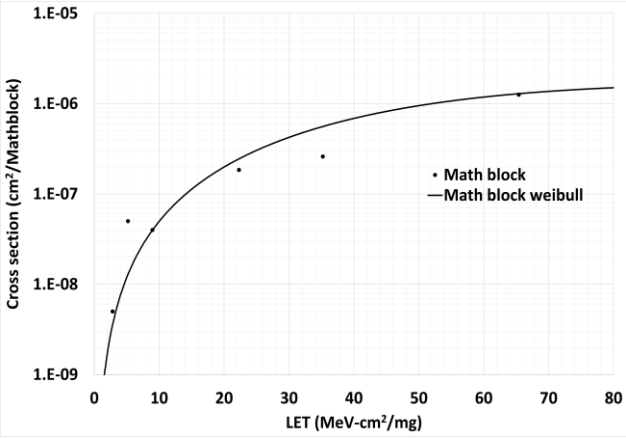

Figure. 8. Math block cross section.

TABLE VI
MATH BLOCK WEIBULL PARAMETERS

L0	W	S	A0
0.1	55	2.05	1.70×10^{-6}

C. SRAMs with EDAC results

Large SRAM (LSRAM) with hard wired Error Detection and Correction (EDAC) and Micro SRAM (µSRAM) with soft EDAC Intellectual Property (IP) are both tested. SRAMs without EDAC results are reported in HEART 2019 proceedings [6]. The LSRAM with EDAC design instantiates one LSRAM block and 65,536 words × 33 bits/word for a total of 2.2Mb. Scrubbing is implemented to rewrite the same address when the "correctable" flag, indicating when a Single Bit Upset (SBU) is corrected, from the LSRAM with EDAC macro is active and continues scrubbing. If two or more bit-flips within the same word are detected, we consider that as a Multi Bit Upset (MBU) and re-write the whole memory. The µSRAM with EDAC design instantiates one µSRAM block and 8,192 words × 24 bits/word for a total of 197Kb. Like the LSRAM design, scrubbing is implemented to rewrite the same address when the "correctable" flag from the µSRAM with EDAC macro is active and continues scrubbing.

The LSRAM and µSRAM with EDAC results are shown in Figure. 9. EDAC is working as expected, all Single Bit Upsets were corrected by the hard wired EDAC (for LSRAM) and soft EDAC IP (for µSRAM). Upper bound cross sections for both LSRAM uncorrectable SBU and µSRAM uncorrectable SBU are shown here to calculate an upper bound error rate for reference. Table VII summarizes the LSRAM and µSRAM correctable and uncorrectable SBUs Weibull parameters and error rates for GEO orbit, solar min, 100 mils aluminum shielding.

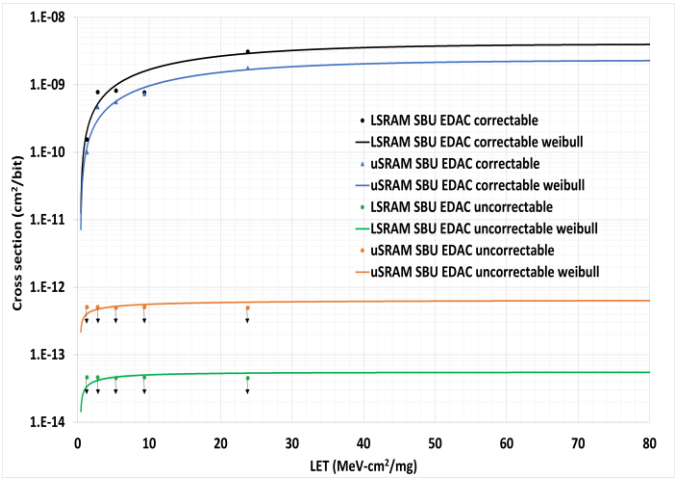

Figure. 9. LSRAM and µSRAM with EDAC correctable SBU sections and upper bound cross sections for uncorrectable SBU. All SBUs were corrected by hard wired EDAC and soft EDAC IP.

TABLE VII
LSRAM AND µSRAM WITH EDAC CORRECTABLE AND UNCORRECTABLE SBUS WEIBULL PARAMETERS

Circuit	L0	W	S	A0	Error rate (upset/bit/day)
LSRAM correctable SBU	0.4	18	0.98	4.01×10^{-9}	4.74×10^{-8}
µSRAM correctable SBU	0.4	18	0.98	2.31×10^{-9}	2.28×10^{-8}
LSRAM uncorrectable SBU	0.4	1	0.4	5.50×10^{-14}	$<9.00\times10^{-14}$
µSRAM uncorrectable SBU	0.4	1	0.3	6.50×10^{-13}	$<4.81\times10^{-13}$

Figure. 10 shows the LSRAM and µSRAM MBU cross sections. The LSRAM block has built in interleaving to mitigate MBUs, whereas the µSRAM block does not have any interleaving solution. The LSRAM and µSRAM MBU error rates for GEO orbit, solar min, 100 mils aluminum shielding are 4.74×10^{-15} upset/bit/day and 9.48×10^{-10} upset/bit/day

respectively. The interleaving solution for LSRAM is effective at mitigating MBUs, the upset rate is low enough. Table VIII summarizes the LSRAM and µSRAM MBU Weibull parameters.

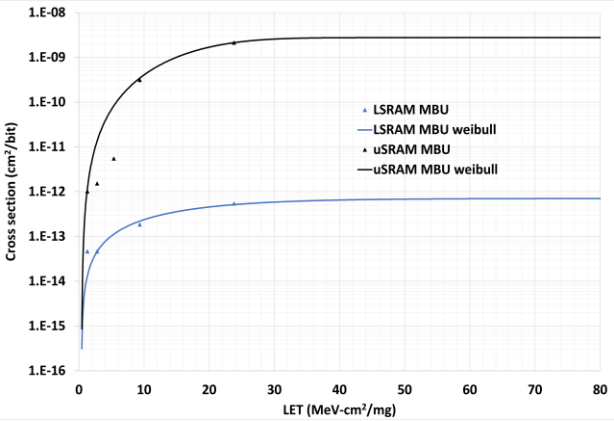

Figure. 10. LSRAM and µSRAM with EDAC MBU cross sections.

TABLE VIII
LSRAM AND µSRAM WITH EDAC MBU WEIBULL PARAMETERS

Circuit	L0	W	S	A0
LSRAM MBU	0.4	19	1.3	7.03×10^{-13}
µSRAM MBU	0.4	20	2.5	2.75×10^{-9}

V. CONCLUSION

In-beam programming results show that in orbit programming can be achieved in RT PolarFire and programming must be followed by stand-alone verify to ensure programming success. Two types of non-destructive SEL signatures were observed in RT PolarFire's GPIO, 2.5V V_{DD25} and 2.5V V_{DDA25} supplies. GPIO SEL_{thr} >80 MeV-cm^2/mg under specific GPIO/Auxiliary supplies bias conditions (V_{DDAUX} =2.575V and V_{DDI}=1.89V). 2.5V SEL was observed on both V_{DD25} (FPGA core and FPGA PLL supply) and V_{DDA25} (Transceiver supply), however the orbital rate is low (1 SEL every 27 years). Global clock upset, LSRAM with hard wired EDAC, µSRAM with soft EDAC IP and Math block cross section results and error rates are presented in this paper.

VI. REFERENCES

[1] https://www.microsemi.com/product-directory/rad-tolerant-fpgas/5559-rt-polarfire-fpgas#documents
[2] https://www.microsemi.com/document-portal/doc_download/136523-ug0714-polarfire-fpga-programming-user-guide.
[3] https://www.microsemi.com/document-portal/doc_download/136519-ds0141-polarfire-fpga-datasheet.
[4] N. Rezzak, J.J. Wang, R. Chipana, C. Lao, G. Bakker, F. Hawley, and E. Hamdy, "Heavy Ion and Proton Induced Single Event Effects on Microchip RT PolarFire FPGA", *in Radiation Effects Data Workshop (REDW), RADECS20*.
[5] https://earth.esa.int/web/eoportal/satellite-missions/j/jpss
[6] J.J. Wang, N. Rezzak, F. Hawley, G. Bakker, J. McCollum, and E. Hamdy, "Radiation characteristics of field programmable complementary-SONOS configuration cell" *HEART 2019 proceedings*.