RT PolarFire Heavy Ion Results

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I. TEST OBJECTIVE

Heavy Ion testing was performed on Microchip's RT PolarFire FPGAs. The main objective of this test campaign is to test the product for Single Event Effects (SEEs) in the FPGA Fabric, including Triple Modular Redundancy (TMR) and non TMR Flip-Flop, SRAMs with and without error detection and correction (EDAC) encoding, Math block, Clock tree, PLL and Power-On-Reset (POR).

II. DEVICE UNDER TEST

Two RTPF500T RT PolarFire FPGAs were irradiated. The samples were prepared by removing packaging material to expose the die and the samples were thinned down to ~100µm to allow ion penetration since the DUTs are flip chip FPGAs. The testing was performed at room temperature of ~25°C and nominal bias. Table 1 shows the testing parameters and Table 2 shows the DUT thickness and bias during irradiation.

Table 1. Heavy Ion Testing Parameters

Condition	Setting
Beam Energy	16 MeV/Nucleon
Temperature	Room Temperature
Bias	1.05V, 1.8V, 2.5V & 2.5V
Sample Preparation	Back grinded RTPF500T, thickness is ~100 µm.

Table 2. DUT thickness and bias during irradiation

DUT#	Product	Thickness (µm)	Nominal Bias
17	RTPF500T	98	1.05/1.8/2.5/2.5
24	RTPF500T	98	1.05/1.8/2.5/2.5

III. TEST METHODS

The test generally follows the guidelines of two SEE testing standards: ASTM standard F1192M-95, "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation on Semiconductor Devices," and JEDEC standard JESD57, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation."

1. Facility

The 88-inch cyclotron at Lawrence Berkley National Laboratory (LBNL) in Berkeley CA, provides the heavy-ion source. For this SEE test, the 16 MeV/n cocktail was used. The target fluence for each run was $1x10^7$ ions/cm^2 and the flux varied from 2×10^3 to 4×10^4 ions/cm^2/s.

2. Irradiation

Table 3 lists the ions and their respective LETs as well as the adjusted LETs based on the DUT thickness.

Table 3. Ion and adjusted LET for each DUT.

Product	DUT#	Thickness (µm)	Ion	LET	Adjusted LET
RTPF500T	17, 24	98	N	1.16	1.28
			Ne	2.39	2.8
			Si	4.35	5.19
			Ar	7.28	8.97
			Cu	16.6	22.3
			Kr	25.2	35.2
			Xe	49.1	65.4

IV. DUT Design

Single event effects data were collected on Triple Modular redundant (TMR) and non-TMR Flip-Flops, Large SRAM (LSRAM) and Micro SRAM (µSRAM) with and without EDAC, global clock tree network, Math blocks and PLL. The testing was done with system controller disabled (System Controller Suspend Mode, SCSM) since the system controller in RT PolarFire FPGAs is not hardened.

Figure 1 below shows a setup description, all the data comparison is done off the DUT board on the master side. The master design is used to drive, collect and process DUT signals. The DUT board is connected to the master board through FMC connector and data from the master is sent through ethernet to the SEE counter software to collect SEE data. The power is monitored on the DUT using two NP6700 high precision power supplies and data is collected via computer running custom Java software.

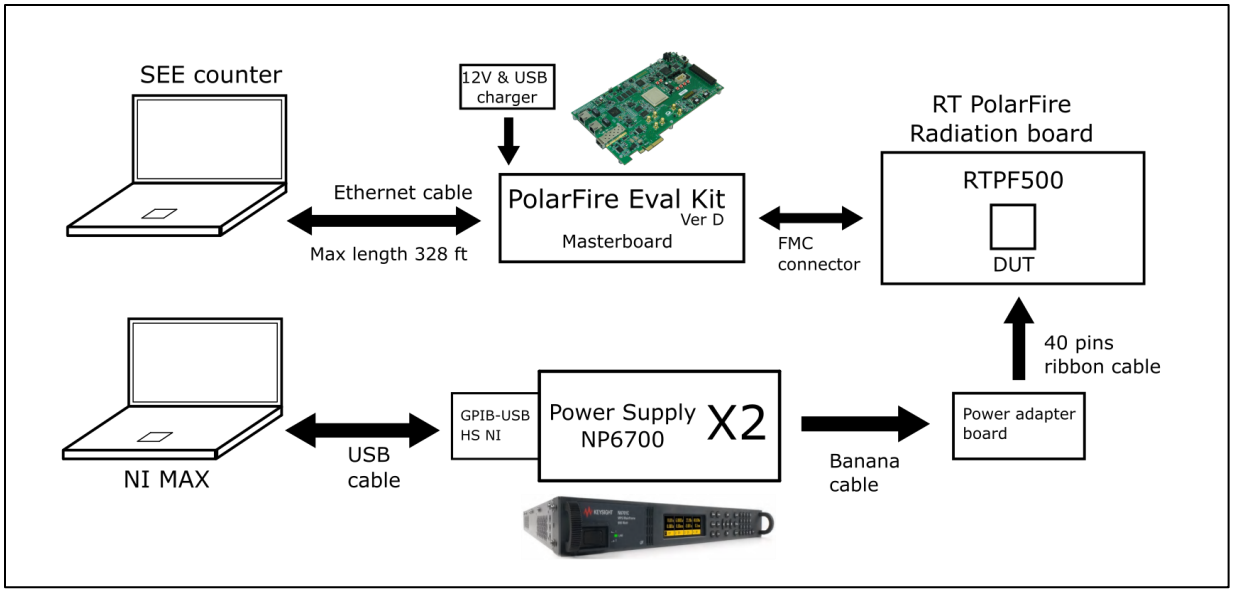

Figure. 1. Setup description

The following is a brief description of the designs used to obtain data on each respective block.

1. Flip-Flop and Clock Tree Design

Four shift register chains with 4000 stages per chain were tested. Each Flip-Flop chain uses a different data input pattern: All 0s/1s, checkerboard and checkerboard slow data patterns. The same design is used to test TMR Flip-Flop and non-TMR Flip-Flop. RTPF500T has only individual Flip-Flops and does not have built-in TMR Flip-Flops. TMR Flip-Flops using Synthesized TMR (Synplify Pro) with constrained placement and cluster separation are tested. Cluster level clock upsets are mitigated by automated constrained placement, available in Libero SoC v12.4 tool suite, combined with the Synthesized TMR. The Flip-Flops are constrained to attempt to obtain data on the global clock tree network, the clock hierarchy in RT PolarFire from the highest to the lowest level of clock resources is the following: Chip level (T) clock, Row level (R) clock, Sector level (S) clock and finally Cluster level clock. The Flip-Flops are driven using an external clock source and data driver.

- Chain 1 – input 0s with toggling clock at 10MHz
- Chain 2 – input 1s with toggling clock at 10MHz
- Chain 3 – input checkerboard with clock at 10MHz and 5MHz data rate
- Chain 4 – Slowed down checkerboard (1.25MHz data rate) with clock at 10MHz

2. SRAMs Design

RT PolarFire Large SRAM (LSRAM) blocks have hard wired error detection and correction SECDED encoding capabilities and built-in interleaving to mitigate MBUs. Soft CoreEDAC IP is available with Micro-SRAM (µSRAM) blocks and no built-in interleaving was implemented for µSRAM blocks. Both LSRAM and µSRAM blocks were tested with and without EDAC.

i. LSRAM without EDAC

The LSRAM without EDAC design instantiates 69 LSRAM blocks and 64 words x 18 bits/word. The SRAM data is read continuously and compared to a model on the master (expected data) to identify if there are any errors.

ii. LSRAM with EDAC

The LSRAM with EDAC design instantiates one LSRAM block and 65536 words x 33 bits/word for a total of 2.2Mb. Scrubbing with a frequency of 1MHz is implemented to rewrite the same address when the "correctable" flag from the LSRAM with EDAC macro is active and continue scrubbing. If two or more bits flip within the same word are detected, we consider that as a MBU and re-write the whole memory.

iii. µSRAM without EDAC

69 µSRAM blocks were instantiated, 64 words x 12 bits/word. The SRAM data is read continuously and compared to a model on the master (expected data) to identify if there are any errors.

iv. µSRAM with EDAC

The µSRAM with EDAC design instantiates one µSRAM block and 8192 words x 24 bits/word for a total of 197Kb. Scrubbing with a frequency of 1MHz is implemented to rewrite the same address when the "correctable" flag from the µSRAM with EDAC macro is active and continue scrubbing. If two or more bits flip within the same word are detected, we consider that as a MBU and re-write the whole memory.

3. Math Block Design

The design has 2 parallel math block chains with fixed coefficients A, B and C is equal to the input of the previous stage. 10 stages of Math blocks were used in each chain performing the operation P = A*B + C.

4. Phase Locked Loops

The PLL is monitored using a lock signal and a counter tracks the number of clock cycles when the PLL goes out of lock. 8 PLLs are instantiated in this design, two at each corner of the chip.

5. POR Test

The POR test consists of performing 10 consecutive power cycle of the part in-beam to determine if the FPGA can be powered up in beam successfully.

6. SEFI Chip Level Reset

Any SEFI will be continuously monitored during the test by looking at the different counters for the different blocks instantiated in the design.

V. RT PolarFire Results

No SEL was observed on any of the parts tested, all the runs were done at room temperature and nominal bias as shown in Table 2.

1. TMR and Non-TMR Flip-Flop

Figure 2 shows the non-TMR Flip-Flop cross sections and Figure 3 shows the TMR Flip-Flop cross sections for different data patterns, All 0s, All 1s, checkerboard (with two data rates 5MHz and 1.25MHz) with a clock running at 10MHz. The error rate is calculated using CREME96 for GEO orbit, Solar Min, 100 mils Aluminum shielding.

For non-TMR Flip-Flop, the error rates for All 0s and All 1s data patterns are 3.15×10^{-8} upset/bit/day and 4.08×10^{-8} upset/bit/day respectively. For checkerboard data pattern with 1.25MHz data rate the upset rate is 7.43×10^{-8} upset/bit/day and for 5MHz data rate the upset rate is 2.39×10^{-7} upset/bit/day. The Weibull parameters are shown in Table 4.

For TMR Flip-Flop, the error rate for All 0s data pattern is 5.42×10^{-11} upset/bit/day, for checkerboard data pattern with 1.25MHz data rate the upset rate is 4.77×10^{-11} upset/bit/day and for 5MHz data rate the upset rate 1.22×10^{-11} upset/bit/day. The Weibull parameters are shown in Table 5.

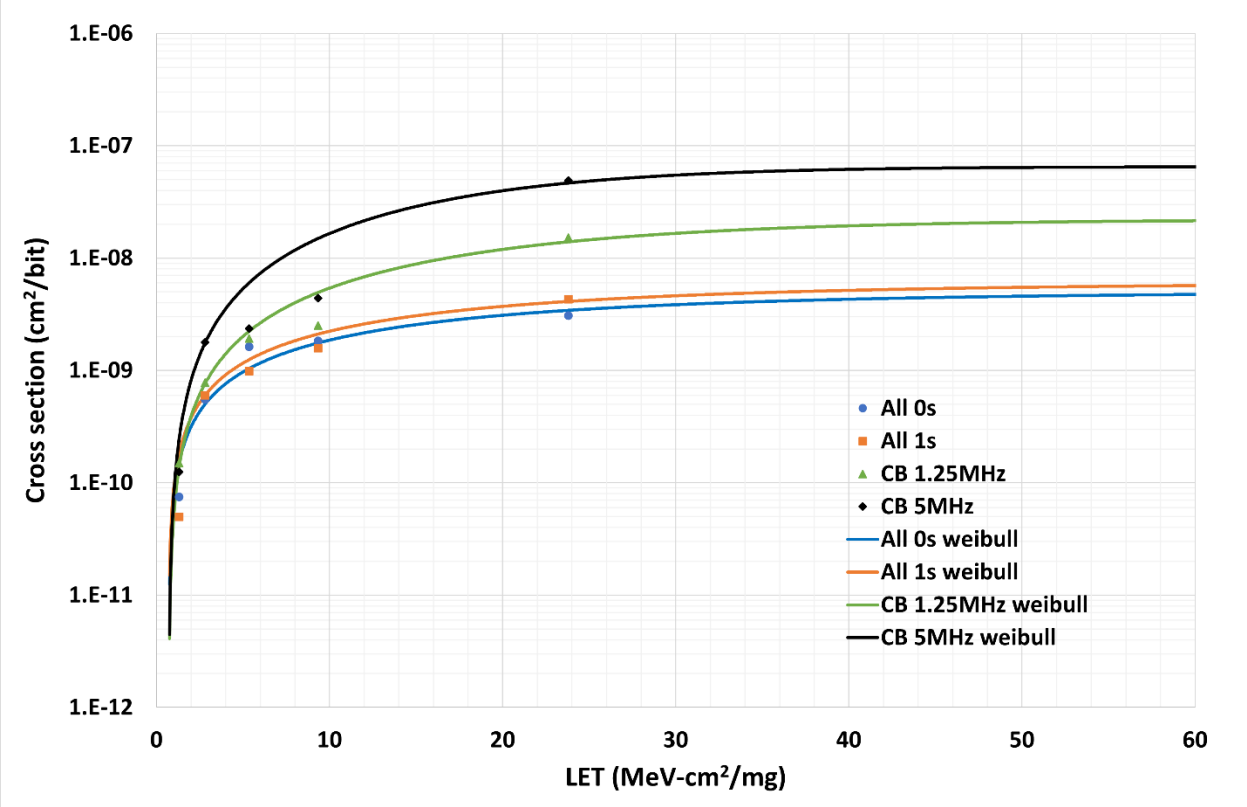

Figure 2. Non-TMR Flip-Flop cross section for different data patterns.

Table 4. Non-TMR FF Weibull parameters for different data patterns

Circuit	L0	W	S	A0
All 0s	0.7	20	1	5.00×10^{-9}
All 1s	0.7	20	1	6.00×10^{-9}
CB 1.25MHz	0.7	23	1.4	2.20×10^{-8}
CB 5MHz	0.7	20	1.6	6.50×10^{-8}

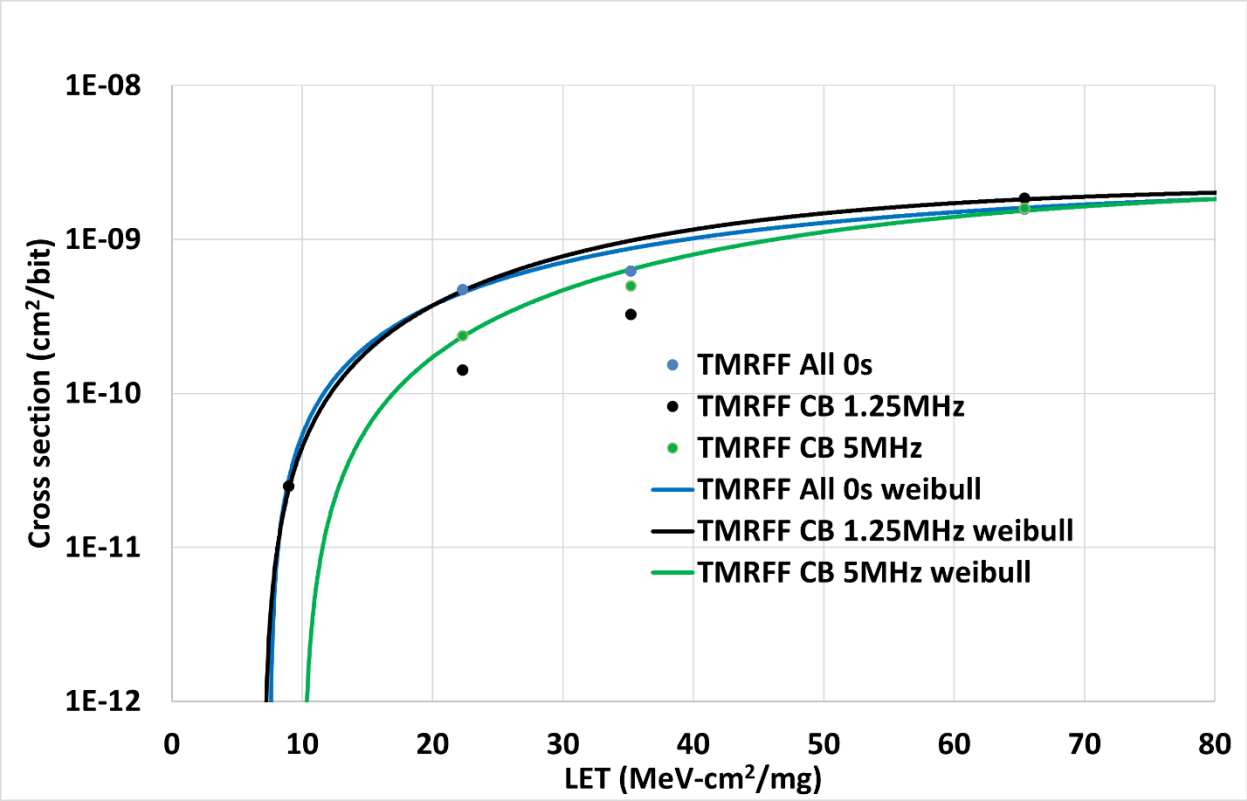

Figure 3. TMR Flip-Flop cross section for different data patterns.

Table 5. TMR FF Weibull parameters for different data patterns

Circuit	L0	W	S	A0
All 0s	7.5	50	1.25	2.30×10^{-9}
CB 1.25MHz	7	40	1.5	2.20×10^{-9}
CB 5MHz	10	52	1.55	2.30×10^{-9}

2. Global Clock Upset

The clock hierarchy in RT PolarFire from the highest to the lowest level of clock resources is the following: Chip level (T) clock, Row level (R) clock, Sector level (S) clock and finally Cluster level clock as shown in Figure 4. The cross sections for each clock level, T, R, S are shown in Figure 5. The testing design with constrained placement was used to get the different cross sections for the different clock levels. Cluster level clock upsets were mitigated by automated constrained placement, available in Libero SoC v12.4 tool suite, combined with the Synthesized TMR.

The error rates for T, R and S clock are 3.56×10^{-7} upset/T clock/day, 1.61×10^{-8} upset/R clock/day, 5.63×10^{-9} upset/S clock/day respectively. The total error rate depends on the number of clock resources used in the specific FPGA design. A fully populated RTPF500T device has 24 T clock circuits, 1440 R clock circuits and 9120 S clock circuits. Thus, for a fully populated FPGA using all T, R, S clock resources, the upset rates are 1 T clock upset every 320 years, 1 R clock upset every 118 years and 1 S clock upset every 53

years. Typically, most designs rarely use more than 50% of the available clock resources. The T, R, S clock Weibull parameters are shown in Table 6.

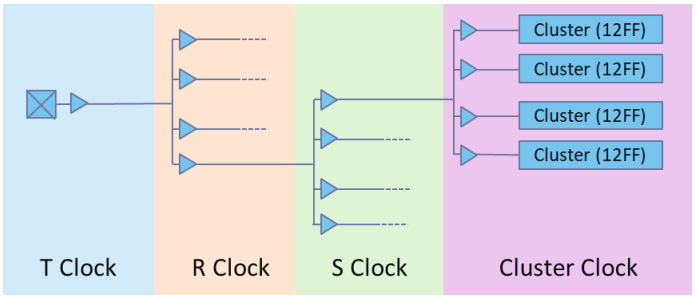

Figure 4. The clock hierarchy in RT PolarFire.

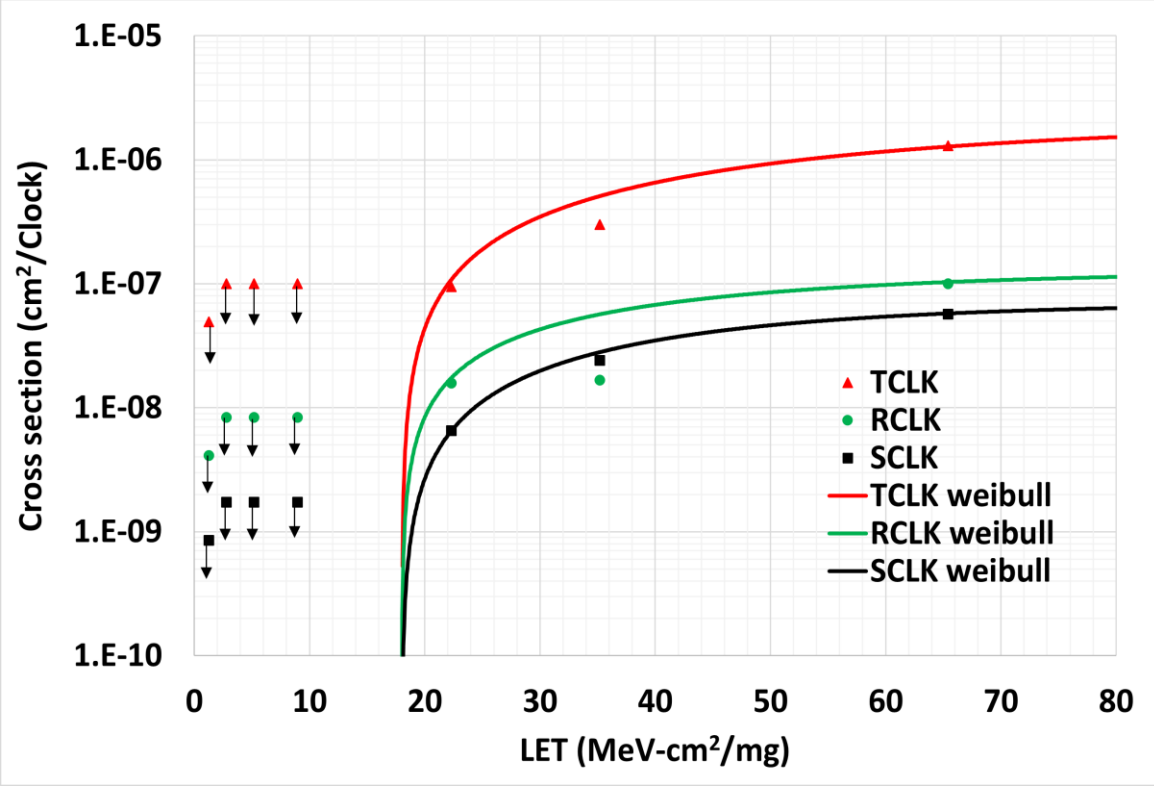

Figure 5. T, R, S clock cross sections.

Table 6. T, R, S Weibull parameters

Circuit	L0	W	S	A0
T clock	18	50	1.2	2.10×10^{-6}
R clock	18	30	1.0	1.30×10^{-7}
S clock	18	30	1.2	7.00×10^{-8}

3. Math block Results

The Math block design has two parallel Math block chains with fixed coefficients A, B and C. 10 stages of Math blocks were used in each chain performing the operation P = A*B + C. The Math block cross section is shown in Figure 6 and the error rate for GEO orbit, solar min, 100 mils aluminum shielding is 1.31×10^{-6} upset/Math block/day; the Weibull parameters are shown in Table 6.

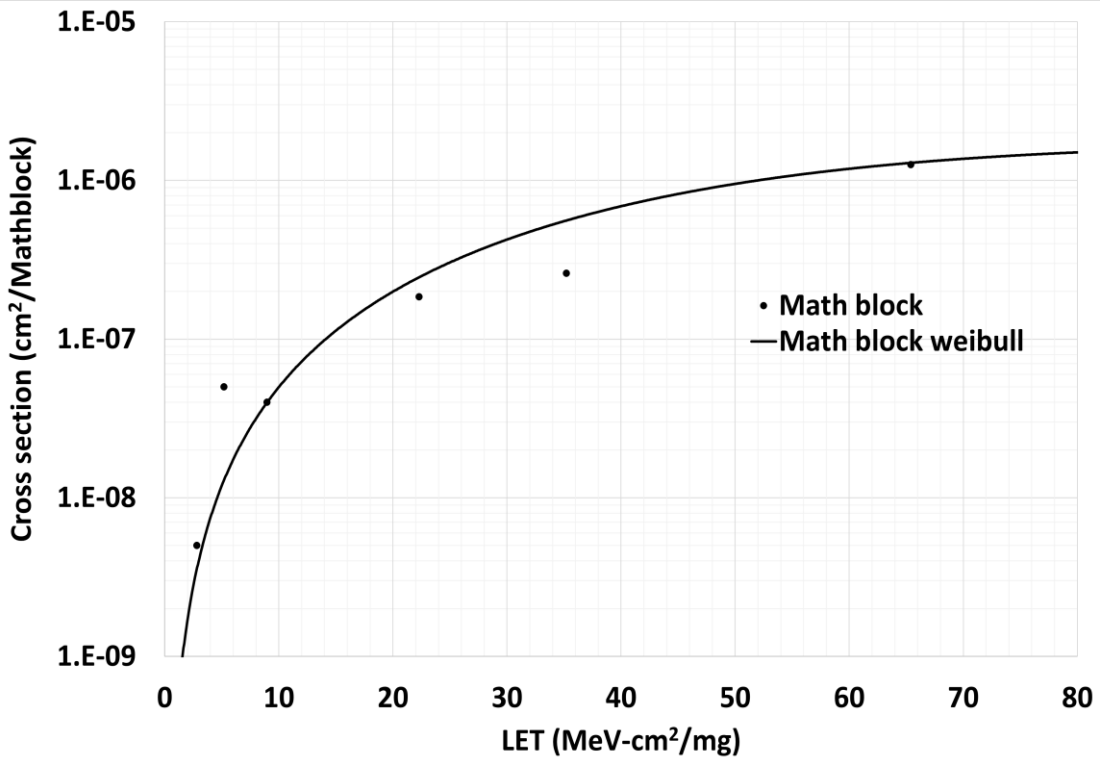

Figure 6. Math block cross section.

Table 7. Math block Weibull parameters

L0	W	S	A0
0.1	55	2.05	1.70×10^{-6}

4. SRAMs with EDAC results

Large SRAM (LSRAM) with hard wired Error Detection and Correction (EDAC) and Micro SRAM (µSRAM) with soft EDAC Intellectual Property (IP) are both tested. The LSRAM with EDAC design instantiates one LSRAM block and 65,536 words × 33 bits/word for a total of 2.2Mb. Scrubbing is implemented to rewrite the same address when the "correctable" flag, indicating when a Single Bit Upset (SBU) is corrected, from the LSRAM with EDAC macro is active and continues scrubbing. If two or more bit-flips within the same word are detected, we consider that as a Multi Bit Upset (MBU) and re-write the whole memory. The µSRAM with EDAC design instantiates one µSRAM block and 8,192 words× 24 bits/word for a total of 197Kb. Like the LSRAM design, scrubbing is implemented to rewrite the same address when the "correctable" flag from the µSRAM with EDAC macro is active and continues scrubbing.

The LSRAM and µSRAM with EDAC results are shown in Figure 7. EDAC is working as expected, all Single Bit Upsets were corrected by the hard wired EDAC (for LSRAM) and soft EDAC IP (for µSRAM). Upper bound cross sections for both LSRAM uncorrectable SBU and µSRAM uncorrectable SBU are shown here to calculate an upper bound error rate for reference. Note that no uncorrectable SBU events were detected in either the LSRAM or µSRAM. Table 7 summarizes the LSRAM and µSRAM correctable and uncorrectable SBUs Weibull parameters and error rates for GEO orbit, solar min, 100 mils aluminum shielding.

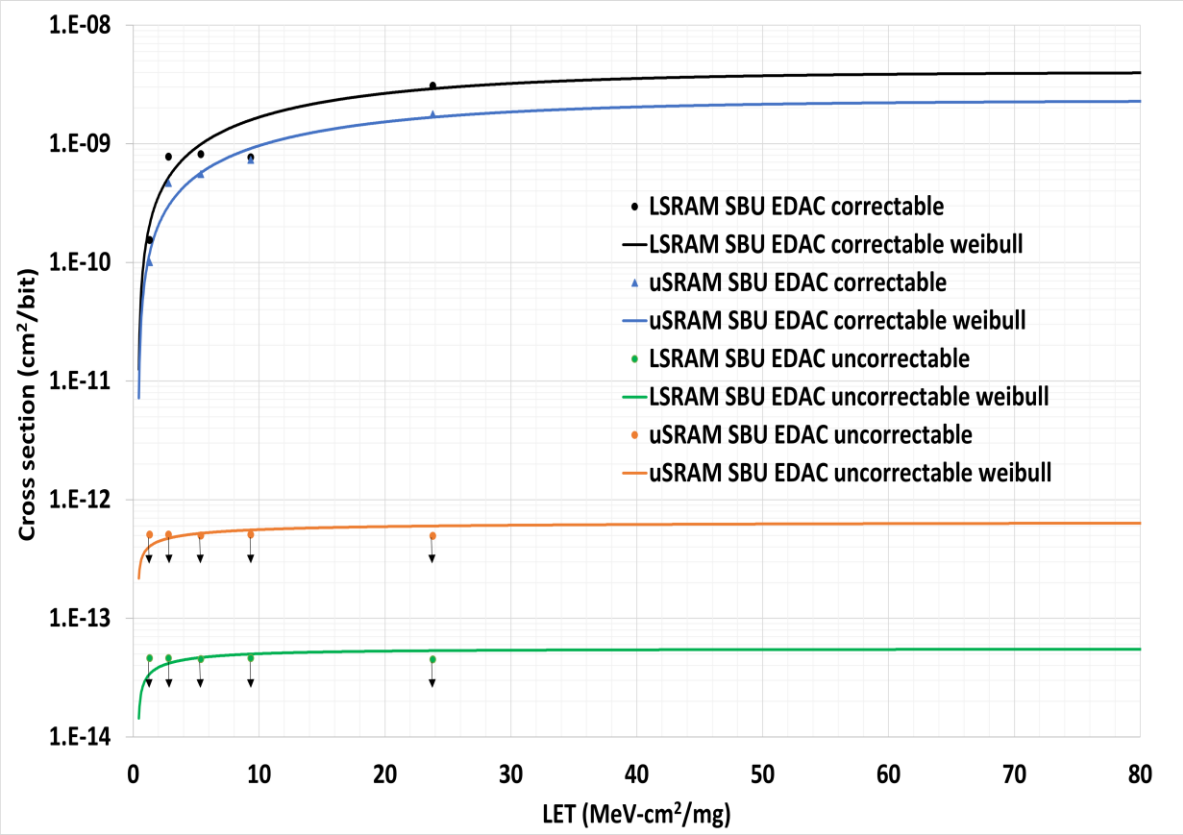

Figure 7. LSRAM and µSRAM with EDAC correctable SBU sections and upper bound cross sections for uncorrectable SBU. All SBUs were corrected by hard wired EDAC and soft EDAC IP.

Table 8. LSRAM and µSRAM with EDAC correctable and uncorrectable SBUs Weibull parameters.

Circuit	L0	W	S	A0	Error rate (upset/bit/day)
LSRAM correctable SBU	0.4	18	0.98	4.01×10^{-9}	4.74×10^{-8}
µSRAM correctable SBU	0.4	18	0.98	2.31×10^{-9}	2.28×10^{-8}
LSRAM uncorrectable SBU	0.4	1	0.4	5.50×10^{-14}	$<9.00\times10^{-14}$
µSRAM uncorrectable SBU	0.4	1	0.3	6.50×10^{-13}	$<4.81\times10^{-13}$

Figure 8 shows the LSRAM and µSRAM MBU cross sections. The LSRAM block has built-in interleaving to mitigate MBUs, whereas the µSRAM block does not have any interleaving solution. The LSRAM and µSRAM MBU error rates for GEO orbit, solar min, 100 mils aluminum shielding are 4.74×10^{-15} upset/bit/day and 9.48×10^{-10} upset/bit/day respectively. The interleaving solution for LSRAM is effective at mitigating MBUs, the upset rate is low enough. Table 8 summarizes the LSRAM and µSRAM MBU Weibull parameters.

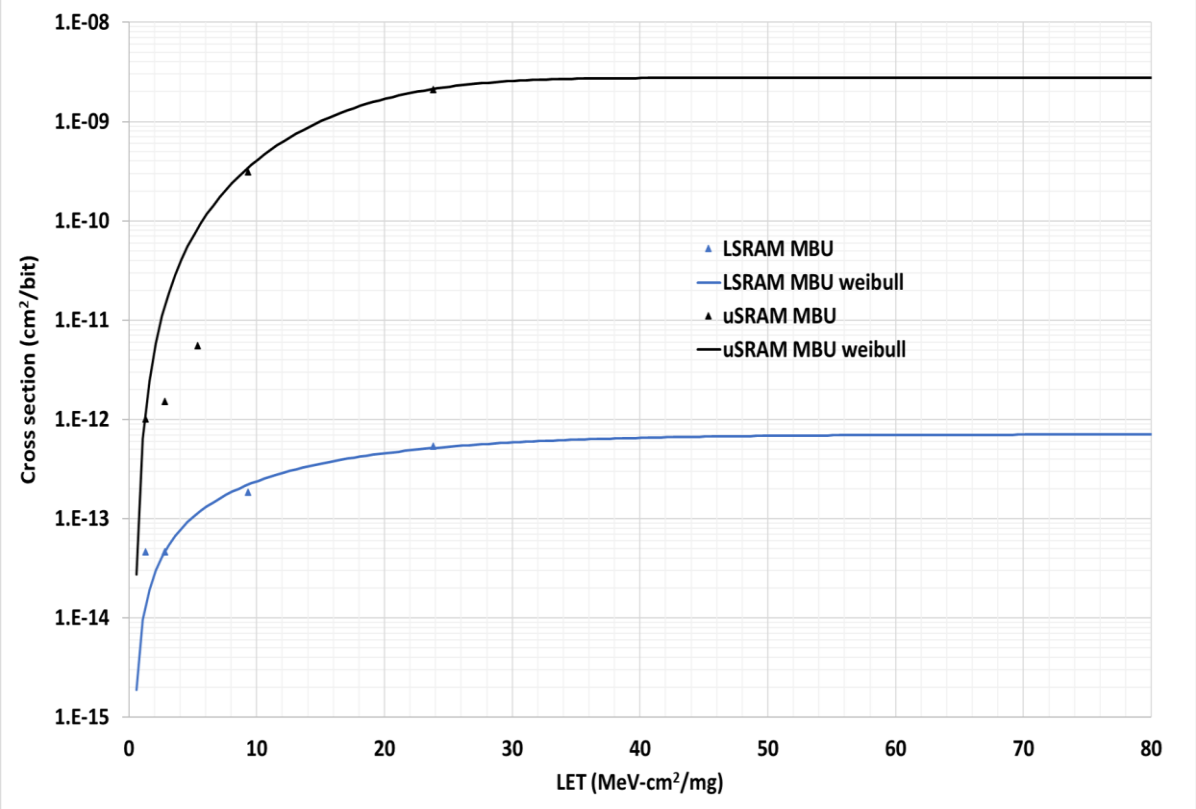

Figure 8. LSRAM and µSRAM with EDAC MBU cross sections.

Table 9. LSRAM and µSRAM with EDAC MBU Weibull parameters.

Circuit	L0	W	S	A0
LSRAM MBU	0.4	19	1.3	7.03×10^{-13}
µSRAM MBU	0.4	20	2.5	2.75×10^{-9}

5. PLL Results

All PLL loss of lock were recovered by the SEFI events, and the cross section is shown below in Figure 9. There were few instances where the PLL lost lock and did not recover at the lower LETs where the SEFI event did not occur (the SEFI events occur starting at LET threshold = 8.97 MeV-cm^2/mg). At LET=2.8 and 5.9 MeV-cm^2/mg, the lock did not recover, and no loss of lock was observed at LET=1.28 MeV-cm^2/mg. All PLL lock signals were recovered by power cycle at the end of the run.

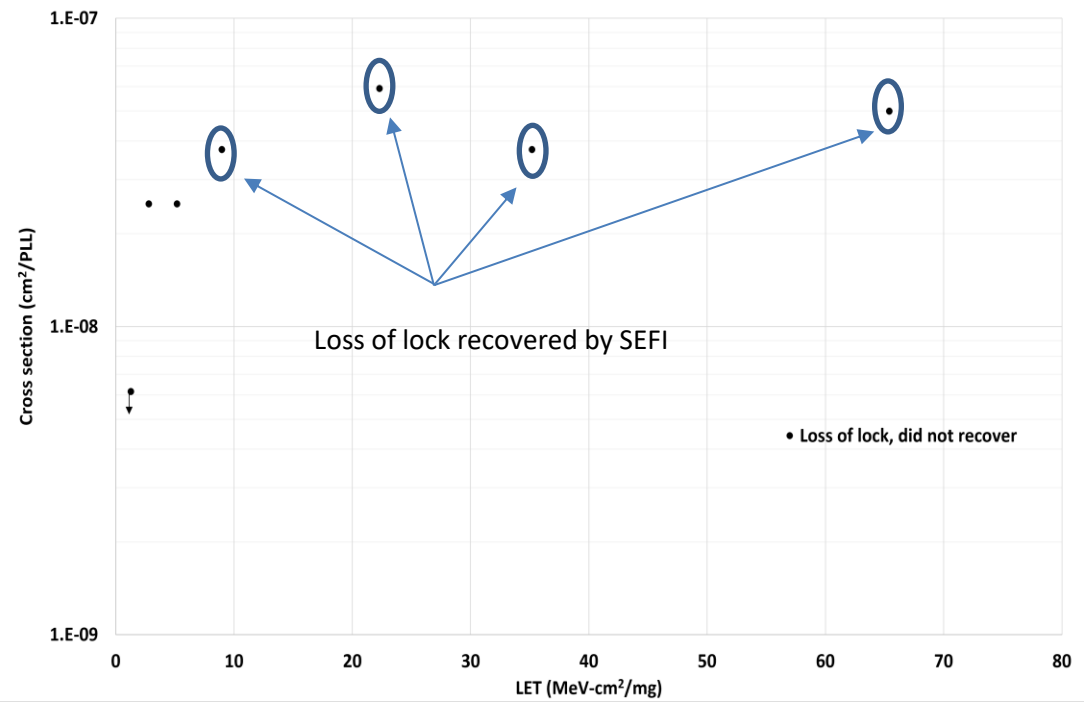

Figure 9. PLL loss of lock cross section vs LET.

6. POR test Results

Power cycle of the FPGA was performed 10 consecutive times at LET=35.2 MeV-cm^2/mg and 10 consecutive times at LET=65.4 MeV-cm2/mg while the beam was ON; all power cycle were successful.

7. SEFI Results

During heavy ion testing, a SEFI or a chip level reset was observed, where the chip experiences an unintended reset with a momentarily loss of functionality. The SEFI self-recovers and no additional reset or power cycle is required to regain functionality of the design. For this test, the system controller was in system controller suspend mode, which is the recommended condition for space-flight. The SEFI cross section is shown in Figure 10. The error rate for a GEO orbit, Solar Min, 100 mils Aluminum shielding is 1.46×10^{-5} SEFI/device/day, or one SEFI every 187 years. The Weibull parameters are shown in Table 10.

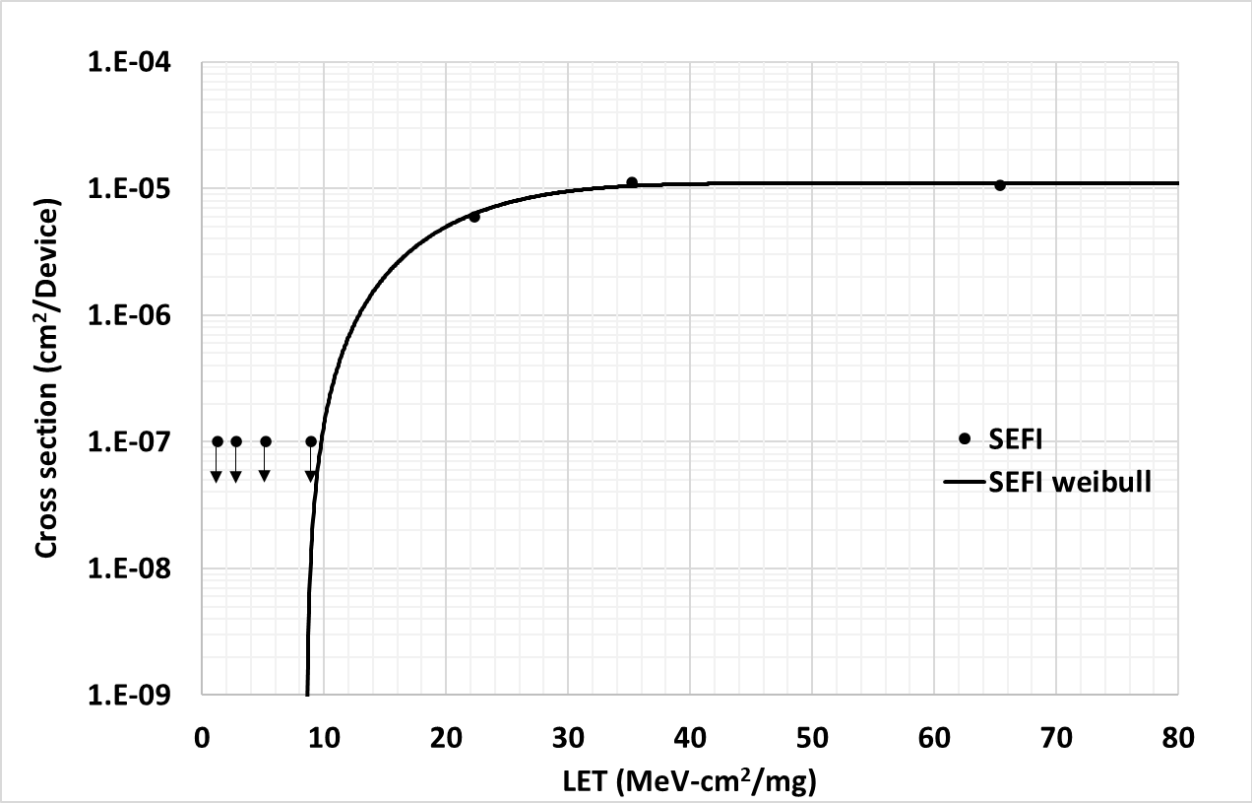

Figure 10. SEFI cross section vs LET.

Table 10. SEFI Weibull parameters.

L0	W	S	A0
8.5	15	1.9	1.10×10^{-5}