Measurement of Worst Case Execution Time on PolarFire® SoC FPGA

Introduction

Microchip's PolarFire® SoC FPGAs include the industry's RISC-V based Microprocessor Subsystem (MSS), and FPGA fabric inherits all the features of the PolarFire family. The PolarFire SoC MSS includes 5x 64-bit RISC-V processor cores, AXI Switch, DDR Controller, Fabric Interface Controllers (FIC), and a rich set of peripherals.

Worst Case Execution Time (WCET) is the upper-bound time taken by a software task to execute on a specific hardware platform for any set of inputs. WCET is an important measurement for checking whether the execution time of a task complies with real-time requirements.

This white paper describes the WCET results obtained from running a bare metal task on the PolarFire SoC MPFS250T device. The following table lists the system configuration used for this WCET measurement.

System Configuration	Description
Product and Architecture	PolarFire® SoC FPGA, RISC-V 64-bit
Development Board	PolarFire® SoC Icicle Kit
Example WCET Task	32 x 32 Matrix Multiplication
CPU Core Frequency	600 MHz
External Memory Configuration	LPDDR4, 800 MHz
Compiler	GCC
Toolchain for Bare Metal	riscv64-unknown-elf-gcc (v8.3.0)
Design Suite	Libero® SoC v2021.1
Software IDE	SoftConsole v2021.1

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1. Latency Factors

In PolarFire SoC devices, the following hardware and software factors affect the upper-bound of the software execution time.

- Memory region—placement of code, data, and stack segments affect the execution time of a task. Code placed in Instruction Tightly Integrated Memory (ITIM) executes faster than the code placed in DDR memory. Similarly, data placed in DDR memory (cached region) can be accessed faster than data in Loosely Integrated Memory (LIM).
- Cache configuration—LIM, scratchpad, and L2 cache.
- Interrupts—outside event can trigger an interrupt, which might not be in the user's control. In such events, the CPU core halts the execution of the current task and executes the interrupt handler. As a result, the execution time gets incremented.
- Total concurrent tasks in the system.
- Branch prediction and execution pipeline also increment the execution time.
- Toolchain settings (ISA, optimization settings) and Programming Style (Efficiency of the code).

For the WCET task used for this white paper, WCET is measured in terms of execution cycles using the hardware performance monitoring register. For more information about the hardware performance monitoring register, ITIM and LIM, and other MSS functional blocks, see PolarFire SoC MSS Technical Reference Manual.

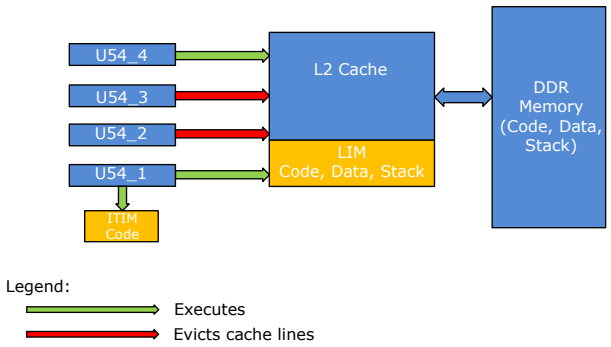
The following section describes an example bare metal application used for white paper.

2. WCET Measurement

A bare metal application was developed for realizing how various latency factors increase the upper-bound of the software execution time. Using this bare metal application, the normal execution time and WCET are measured by disabling and enabling the latency factors. In the application, the device eNVM stores a custom bootloader. At device power-up, the E51 monitor core executes the bootloader for loading separate binary files in the DDR memory for each U54 application core. The bootloader executes from eNVM (code) and scratchpad (data).

The following figure shows the memory hierarchy and the interaction of application cores with different memory regions in the example application.

Figure 2-1. Interaction of Application Cores with Different Memory Regions



The following table lists the task executed by each U54 application core and the memory region used for fetching and executing the code. The bootloader loads all the binary files to different DDR regions.

Application Core	Task(s)	Memory Region	Description
U54_1	Executes the 32 x 32 matrix multiplication task and prints the results on serial terminal.	Executes from ITIM and LIM.	The bootloader loads the 32 x 32 matrix multiplication task to DDR and U54_1 copies this task to ITIM and LIM for executing it. This scenario demonstrates the predictability of execution time. Because, the non-predictability caused by caching is eliminated in this scenario.
U54_2	Continuously flushes L2 cache lines using the L2 flush register.	Executes from cached DDR.	This task acts as adversarial to tasks running on U54_1 and U54_4 cores. The effects of continuously evicting or flushing the L2 cache lines on tasks executing from ITIM/LIM and DDR can be observed by executing this task. This scenario helps in analyzing the effects of L2 cache flush and refresh function on the execution time.
U54_3	Continuously reads data from DDR, which results in cache evicts.	Executes from cached DDR.	
U54_4	Executes 32 x 32 matrix multiplication task and prints results on serial terminal.	Executes from cached DDR address range.	DDR cached scenario demonstrates unpredictability of execution times due to presence of caches. This scenario is for comparison purpose only.

The normal execution time is measured by excluding U54_2 and U54_3 application cores and by disabling branch prediction trashing in U54_1 and U54_4 cores. WCET is measured by including the U54_2 and U54_3 cores, and by enabling branch prediction trashing and a 1000 mcycle interrupt routine in U54_1 and U54_4 cores. At device power-up, bootloader provides an option to enable or disable U54_2 and U54_3 cores via the serial terminal. To calculate WCET, the U54_1 and U54_4 applications require a rebuild because the latency factors are enabled in the code. The normal execution time and WCET are measured based on scenarios highlighted in Figure 2-1.

1. To measure the normal execution time on U54_1 (ITIM and LIM) and U54_4 (cached DDR), the following sequence is followed:
   a. U54_2 and U54_3 are excluded > U54_1 and U54_4 execute the task without branch prediction trashing and interrupt routine. U54_4 executes the task from cached DDR region.
2. To measure WCET on U54_1 (ITIM and LIM) and U54_4 (cached DDR), the following sequence was followed:
   a. U54_2 and U54_3 are included > U54_1 and U54_4 execute the task with branch prediction trashing and interrupt routine. The U54_4 core executes the task from cached DDR region.

Bare metal user applications are built from the PolarFire SoC Bare Metal library, which includes hardware abstraction layer and drivers to access various MSS blocks such as L1 cache, L2 cache, timer, Interrupt registers, and peripherals. For more information about the Bare Metal library, see https://github.com/polarfire-soc/polarfire-soc-bare-metal-examples.

2.1 Toolchain Settings

The following toolchain settings were applied for all U54 application cores in the bare metal application used for this white paper.

Table 2-1. Toolchain Settings

Attribute	Setting
Architecture	rv64g
Integer ABI	lp64
Floating point ABI	(d) Double precision
Tuning	Toolchain default
Code model	Medium Any (-mcmodel=medany)
small data limit	8
Align	Strict (-mstrict-align)
Optimization Level	None(O0)
Debug Level	Maximum(-g3)
Language standard	GNU ISO C11 (-std=gnu11)

2.2 WCET Results

The following table lists the normal execution time and WCET of a 32 x 32 matrix multiplication task measured using the example application.

Program Segment	U54_1 Core		U54_4 Core[4]
Code (bytes)	ITIM (12736)	LIM (80496[1])	DDR cached
Data	LIM (78000[2])	LIM	DDR cached
Stack	LIM	LIM	DDR cached
Normal Execution Time (±deviation) in mcycles	8407148 (±21 cycles) (14.0119 ms)	8407167 (±4 cycles) (14.0119 ms)	1955036 (±136 cycles) (3.258 ms)
WCET[3]	8409198 (±61 cycles) (14.0153 ms)	8409426 (±200 cycles) (14.0157 ms)	1971234 (±1653 cycles) (3.285 ms)

1. All sections are combined.
2. Data and stack are combined.
3. WCET includes the following:
    a. Branch prediction trashing and branch prediction scheme (static) are enabled in core U54_4 and U54_1.
    b. Adversarial runs on U54_3; cache flush runs on U54_2.
    c. Interrupt with execution time (1000 mcycle).
4. The DDR cached execution timings are given for comparison purpose only.

Note: WCET (seconds) = (1／(CPU Core Frequency in MHz × 1000 × 1000)) × (number of execution cycles), where CPU Core Frequency = 600 MHz

3. Conclusion

In this white paper, the WCET results for a 32 x 32 matrix multiplication task in bare metal were analyzed by executing the task from ITIM, LIM, and DDR cached regions. In all three cases, the task execution time increased due to the latency factors which resulted in WCET. The effects of L2 cache refresh and flush functions were negligible when the tasks were executing from ITIM or LIM.

On U54_1, when the task was executing from ITIM with LIM as target memory for data and stack, the additional latency resulted mainly from the interrupt execution latency factor.

On U54_1, when the task was executing from LIM (code, data, and stack), the additional latency resulted mainly from the interrupt execution latency factor. In this case, when the task was executed multiple times, there was a deviation in the execution time mainly due to branch prediction trashing.

On U54_4, when the task was executing from DDR cached region (code, data, and stack), the additional latency and execution time deviation were higher when compared to the above two cases. This is due to the L2 cache refresh/flush and interrupt execution latency factors. However, the minimum execution time was achieved due to the presence of caches.

Based on the above results, the task executing from ITIM with LIM as target memory for data and stack gave more deterministic behavior.

4. Revision History

Revision	Date	Description
A	10/2021	The first publication of this document.

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ISBN: 978-1-5224-9011-1

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