PolarFire® SoC FPGA: Application Waypointing

Introduction

The application waypointing is a technique to detect faults in a system with two processors running the identical applications where the outputs from each processor are compared periodically. The two processors running the identical applications provide the spatial separation, and the temporal separation can be introduced by starting the second processor after a certain delay. This white paper describes how to implement application waypointing on PolarFire SoC FPGAs, and presents the measured temporal separation for different target memories.

The application waypointing is implemented for CoreMark application which is 62 KB in size. The CoreMark application is executed from different target memories (LPDDR4 memory, ScratchPad, or LIM) and the results are captured. The temporal separation between the processors is application dependent. As an example, the temporal separation of 50 µs or 5 ms has been used in this white paper.

The following table lists the system configuration for waypointing application.

Table 1. System Configuration

System Configuration	Description
Product and Architecture	PolarFire SoC FPGA, RISC-V 64-bit
Hardware Platform	Icicle Kit
BareMetal Application	CoreMark (Size, 62 KB)
Temporal Separation	50 µs or 5 ms
CPU Core Frequency	600 MHz
External Memory Access	LPDDR4
LPDDR4 Frequency	800 MHz
Compiler	GCC
Toolchain	riscv64-unknown-elf-gcc (v8.3.0)

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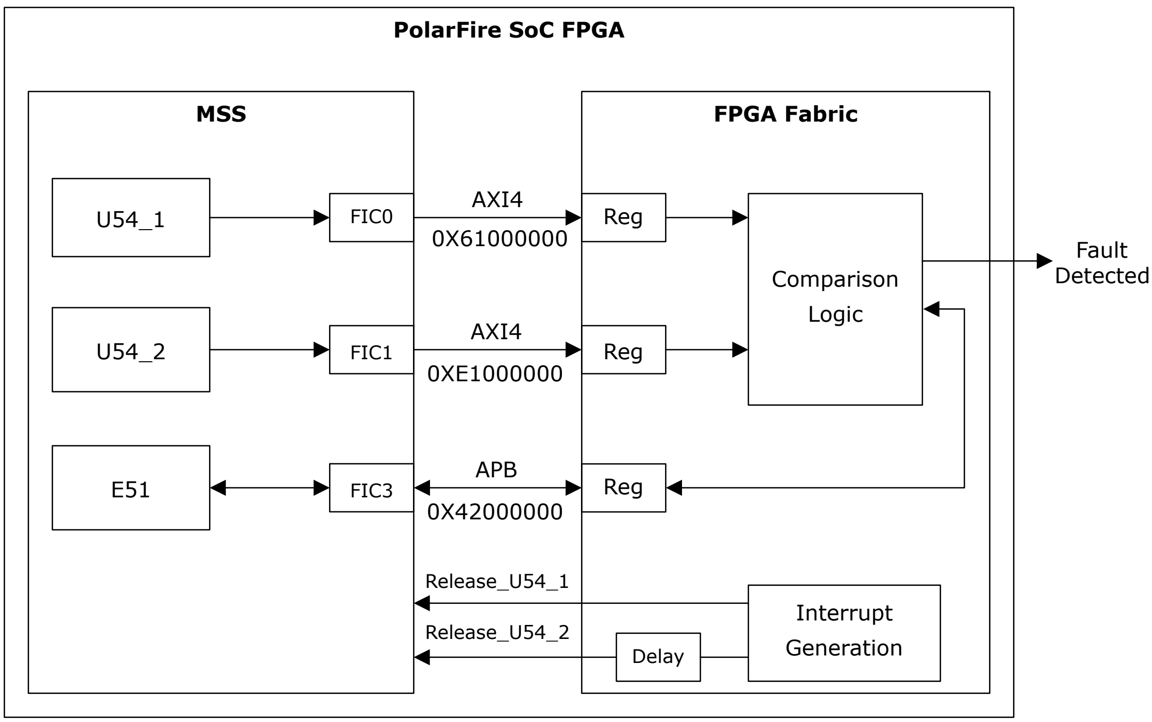
1. Waypointing Implementation

The following block diagram shows the waypointing method. The E51 processor core copies the same application into two different regions of the target memory (LPDDR4/LIM/Scratchpad) for U54 processor cores. U54_1 and U54_2 are held in wait for interrupt (WFI) mode after reset. E51 requests the fabric logic to generate two interrupts to release the U54 processor cores from WFI mode. The U54_1 and U54_2 processor core execution is separated temporally by 50 µs. The temporal separation delay is application dependent. U54_1 writes incremented data pattern to a fabric register accessible at address 0x61000000 periodically (at every 100 µs) through the FIC0 interface. U54_2 writes incremented data pattern to a fabric registers accessible at address 0xE1000000 periodically (at every 100 µs) through the FIC1 interface. The periodic AXI writes from the processor must be greater than the temporal separation value. The time difference between the two AXI write (`awvalid`) signals is sent to the E51 processor using fabric logic through the FIC3 APB interface. The fabric logic compares the data and measures the temporal separation between the two processor writes. The E51 processor core reads the same.

Figure 1-1. Waypointing Block Diagram

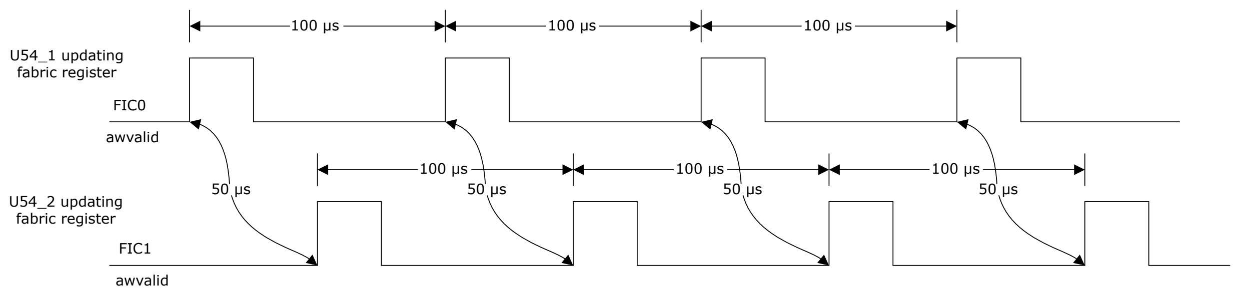


The waypointing is implemented using CoreMark application. The code, data, and stack are placed in the target memory. The target memory can be LIM, ScratchPad, or LPDDR4.

2. Temporal Separation Measurement

The temporal separation is measured in the FPGA fabric logic that runs at a 125 MHz clock. When an `awvalid` rising edge is detected on either one of the FIC interfaces, a 64-bit counter is started. This counter keeps counting until the `awvalid` pulse is detected on the other FIC. This counter value is read by E51 through the APB interface, which is the actual temporal separation. The counter values are reset back to 0 again until the next `awvalid` pulse arrives on either one of the FIC interfaces. The following timing diagram shows the temporal difference between two `awvalid` signals in an ideal scenario. The temporal separation may vary based on the application.

Figure 2-1. Temporal Separation Timing Diagram



3. Results

The temporal separation was measured in the fabric while executing the applications from different target memories (LIM/Scratchpad/LPDDR4). The data from the two processors is equal and the measured temporal separation is constant with a few fabric clock cycles deviation with respect to expected temporal separation. The fabric is operating at 125 MHz.

The following table lists the clock cycle deviation with respect to expected temporal separation. The same clock cycles deviation is observed with a temporal delay of 50 µs and 5 ms between the processors.

Table 3-1. Clock Cycles Deviation with respect to Expected Temporal Separation

Target Memory		Clock Cycles Deviation
Code	**Data and Stack**	**CoreMark Application**
LPDDR4	LPDDR4	±10
ScratchPad	ScratchPad	±10
LIM	ScratchPad	±10
LIM	LIM	±150 [1]

Note:

1. This deviation is expected due to the bus contention while accessing LIM simultaneously from more than one application core. When executing applications from LIM, the instructions and data are not cached.

4. Conclusion

This white paper describes the application waypointing implementation in PolarFire SoC FPGAs. The temporal separation was measured while executing the applications from different target memories (LIM/Scratchpad/LPDDR4). The data from the two processors is equal and the measured temporal separation is constant with ± 10 clock cycles deviation with respect to expected temporal separation. It is recommended to implement application waypointing using scratchpad or LPDDR4 as the target memory.

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