



RTG4™ FCCC with Enhanced PLL Calibration Configurator

Release Notes

Introduction

The RTG4FCCC with Enhanced PLL Calibration core generated circuit includes soft logic that performs calibration at power-up or when the PLL is reset. This ensures that the PLL lock is stable during normal operation within the supported RTG4 operating junction temperature range.

The RTG4FCCC with Enhanced PLL Calibration core does calibration on power-up and does recalibration whenever PLL loses lock. This core provides options to configure Single CCC, both the CCC together or in dynamic configuration.

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1. Software Features and Enhancements

1.1 Option to Select Reset Type

A new option to select the reset type has been added to the RTG4FCCC with Enhanced PLL Calibration core configurator. The following are the available reset types:

- Synchronous with CLK_50MHZ
- Async Assert, Sync De-assert

The **Async Assert, Sync De-assert** option will have asynchronous assertion and de-assertion of reset synchronous to CLK_50MHZ. When selecting the **Async Assert, Sync De-assert** reset type, it is recommended to use a SET mitigated approach when connecting an asynchronous reset signal to the PLL_RST_N input of this core.

For example, an external reset can enter the device using a CLKBUF macro on a GB# pin, or a RGRESET macro can be manually instantiated and connected to a triplicated internal logic core. For more information, refer to [AC463: RTG4 Radiation Mitigated Clock and Reset Network Usage Application Note](#).

1.2 Dynamic Configuration Option

CLK_50MHZ clock will be used for both the PLL Calibration soft IP and the user dynamic configuration APB interface. The user logic generating APB signals during normal operation must synchronize the APB signals to CLK_50MHZ.

2. Migrating Designs to Libero SoC

2.1 Core Enhancements and Upgrades

The following table lists the RTG4FCCC with Enhanced PLL Calibration Core enhancements and upgrades.

Table 2-1. Core Enhancements and Upgrades

Core	Version	Changes
RTG4 FCCC with Enhanced PLL Calibration	2.1.010	New Core
RTG4FCCCECALIB	2.2.005	For more information, see CN19009C .
RTG4FCCCECALIB	2.2.007	<p>The following changes have been made. For more information, see the Libero SoC v2022.2 Release Notes.</p> <ul style="list-style-type: none"> Updated core to expose <code>GLx_Yx_ARST_N</code> and <code>GLx_Yx_EN</code> inputs by default to better align with guidelines described in the UG0586: RTG4 Clocking Resources User Guide. Added simulation model support for PLL feedback delay, enabling post-layout timing simulations to account for the PLL feedback delay path. This is useful when simulating CCC configurations using PLL external feedback mode (within the FPGA) or negative CCC/PLL delay settings.

2.2 Updating the Core Version

On opening the designs having RTG4FCCCECALIB core with core versions older than 2.2.005, the corresponding designs will become invalidated. You are suggested to upgrade the version of RTG4FCCCECALIB core to the latest available core.

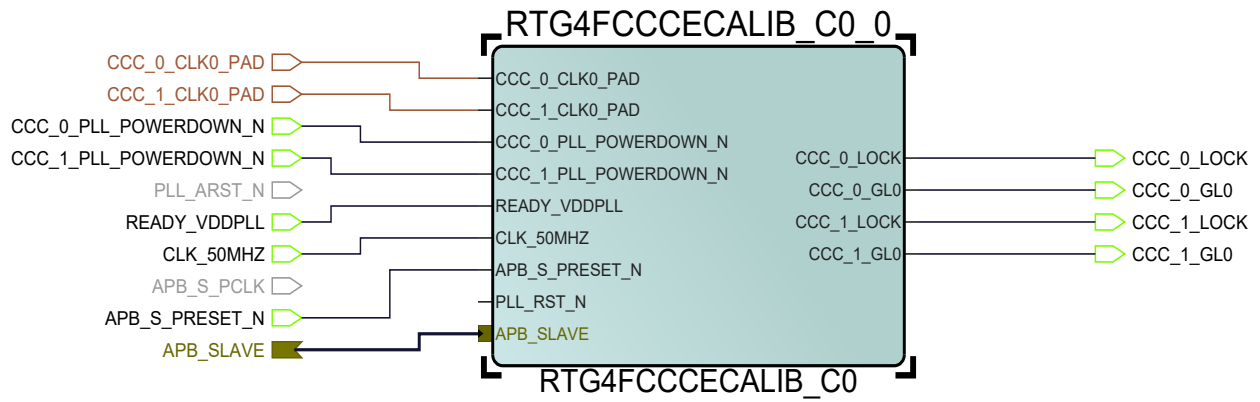
To update a core version:

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version by right-clicking on the core component in the design hierarchy and selecting **Replace Component Version**.
3. Regenerate the core.
4. Derive the timing constraints again using the **Constraint Manager** tool to use the latest generated core timing constraints.
5. Rerun the design flow.

On replacing the core version from previous release core versions, the following changes are visible in the core:

- External port `PLL_ARST_N` becomes unconnected.
- If dynamic configuration is used in the design, port `APB_S_PCLK` becomes unconnected.

Figure 2-1. RTG4FCCCECALIB core



3. Known Issues and Limitations

There are no known issues.

4. Revision History

Revision	Date	Description
B	2/2023	Added the RTG4FCCCECALIB core in section 2.1. Core Enhancements and Upgrades .
A	08/2021	Initial Revision

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