Libero® SoC v2021.2

I/O Editor User Guide

Introduction

The I/O Editor displays all assigned and unassigned I/O macros and their attributes in a spreadsheet-like format. Use the I/O Editor to view, sort, filter, select and set I/O attributes of the SmartFusion®2, IGLOO®2, RTG4™, or PolarFire® device.

The I/O attributes can be viewed by port name or by package pin. Click the Ports View tab to view I/O attributes by port name. Click the Pin View tab to view I/O attributes by pin name.

The I/O Editor provides the following views for I/O assignment and planning:

- Port View — I/O spreadsheet sorted by port name
- Pin View — I/O spreadsheet sorted by pin number
- Package View — Package pin graphical view of the device

Notes: The following views are available for Polar Fire FPGA and PolarFire SoC devices as well.

- Memory View — I/O view specific to the memory interface
- IOD View — I/O view specific to the IOD Lane Controller interface
- XCVR View — I/O view specific to the transceiver interface
- Floorplanner View — Detailed cell level device view of the entire chip

Note: This user guide shows a PolarFire device in the example figures.

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1. Invoking the I/O Editor

The design must be in the post-synthesis state before the I/O Editor can be invoked. A warning message appears if the I/O Editor is invoked in the pre-synthesis state.

The I/O Editor can be invoked in two ways from the Constraint Manager:

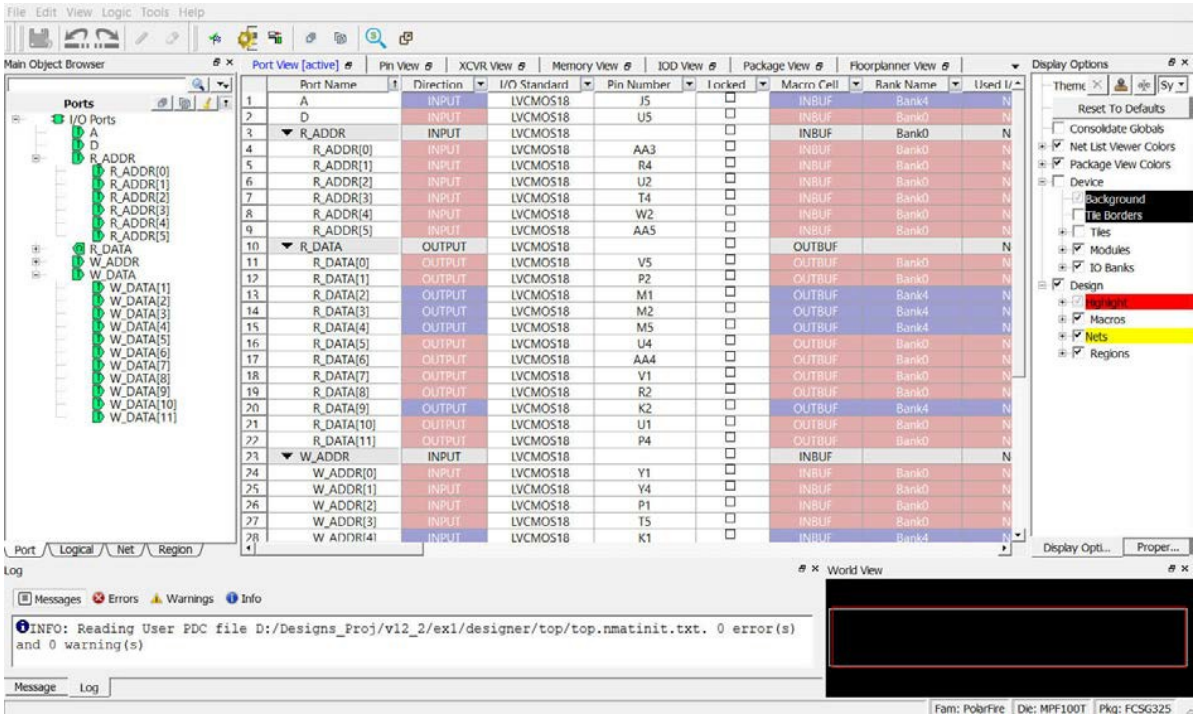
- **Design Flow window > Manage Constraints > Open Manage Constraints View > Constraint Manager > I/O Attributes > Edit > Edit with I/O Editor**
- **Design Flow window > Manage Constraints > Open Manage Constraints View > Constraint Manager > I/O Attributes > View**

The **Edit with I/O Editor** option in the Constraint Manager allows you to save or commit your changes to PDC files, whereas the **View** option shows the post-Place and Route design including the final placement and the I/O attributes in read-only mode. You cannot save or commit any changes made in the I/O Editor opened using the **View** option.

However, you can export and save the physical constraints using **File > Export Physical Constraint (PDC)** in both options and save them. These constraints can later be used in your design as input files, depending on the design's requirement.

The I/O Editor opens with view tabs across the top of the graphical interface, as shown in the following figure.

Figure 1-1. I/O Editor



2. Port View

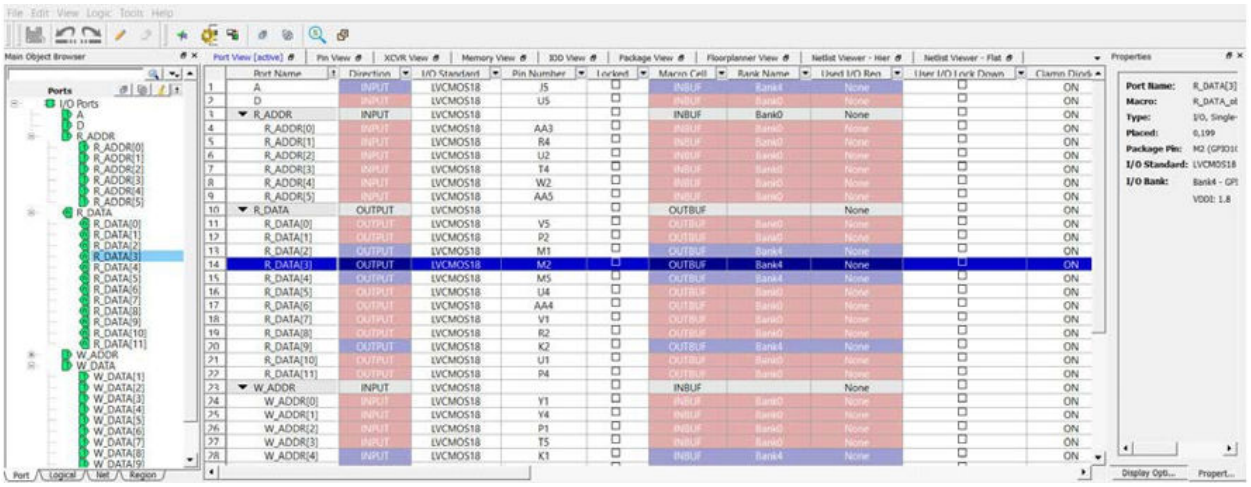
The Port View displays the I/O attributes in a spreadsheet-like format. Each row corresponds to an I/O port in the design, sorted by the port name. The column headings specify the names of the I/O attributes in your design. The first few column headings are standard and common for all families. The remaining columns display family-specific attributes. Only attributes applicable to a specific device appear in the I/O Editor attributes table. For some I/O attributes, you will choose from a drop-down menu; for others, you might enter a value and for others, the field is read-only and not editable.

Displayed columns can be sorted alphabetically, numerically, or filtered.

In the I/O Editor, the ports can be viewed in a spreadsheet-like format or in the Design Tree View window of the Port tab. A port selected in the Port tab is also selected in the Port View spreadsheet and vice versa. The following figure shows the DM[0] selected in the spreadsheet and the Design Tree port view.

The Port View also displays the memory width and data rate of the DDR instance in the design (if it exists in the design) in the top left row under the Port Name column, as shown in the following figure.

Figure 2-1. Port View



Notes: See the following documents for more information about the I/O standards supported by each attribute:

- PDC Commands User Guide for SmartFusion2, IGLOO2, and RTG4
- PDC Commands User Guide for PolarFire FPGA

2.1 Port Name

This is the port list of the design. The ports of the design are displayed in a structured manner according to group name/functions. Ports can be expanded or collapsed. The port list can be sorted, or filtered, in a way similar to the Windows spreadsheet operations. For example, entering RESET in the match field in the filter returns a list of port names that have RESET in the port name.

2.2 Direction

Non-editable field that denotes Input, Output, or Inout.

2.3 I/O Standard

This field specifies the I/O standard the device supports. Different I/O types have different I/O standards. The pull-down list displays the valid I/O standards for that particular type of I/Os. The list of valid I/O standards is limited to what the I/O bank (to which the I/O belongs) can support.

2.4 Pin Number

This is the package pin number specific to the die and package of the device.

2.5 Locked

Set this option to lock all I/O banks so the I/O Bank Assigner cannot unassign and reassign the technologies in the design.

2.6 Macro Cell

This is a read-only field that identifies the name of the Macro cell associated with the Port.

2.7 Bank Name

This is a read-only field to identify the I/O bank the I/O pin is associated with. Depending on the device size, devices may have, six, or eight I/O Banks (Bank 0 through Bank 7) user I/O banks, Each pin is associated with an I/O bank. The I/O banks on the north side of the device support only HSIO. Each I/O bank has dedicated I/O supplies and grounds. Each I/O within a given bank shares the same VDDI power supply, and the same VREF reference voltage. Only compatible I/O standards can be assigned to a given I/O bank.

2.8 User I/O Lock Down

If checked, the current pin assignment cannot be changed during layout.

2.9 I/O State in Flash Freeze Mode

By default, all I/Os become tristated when the device goes into Flash*Freeze mode. You can override this default behavior by setting one of the following two values:

- LAST_VALUE - When set to this value, it preserves the previous state of the I/O. This means the I/O remains in the same state in which it was functioning before the device went into Flash*Freeze mode.
- LAST VALUE_WP - When set to this value, it preserves the last value with weak pull-up.

2.10 Clamp Diode

PolarFire devices have internal PCI clamp diodes for both HSIO and GPIO. PCI clamp diodes help reduce the voltage level at the input, and are mainly used when the voltage overshoot exceeds the maximum allowable limit. If signaling levels of the receiver are greater than the VDDIx of the bank, the clamp diode must be off to support hot-socketing insertion.

For GPIO, use this field to program the clamp diode to be ON or OFF.

For HSIO, the internal clamp diode is always ON by default.

2.11 Resistor Pull

Use this field to allow the inclusion of a weak resistor for either pull-up or pull-down of the input or output buffer. The available options are None, Up (pull-up), Down (pull-down), or Hold. The default value is Up.

Note: Not all I/O standards have a selectable resistor pull option.

2.12 I/O Available in Flash*Freeze Mode

Use this field to indicate if the I/O is available or unavailable in Flash*Freeze mode. The default value is “no” and the I/O is unavailable in Flash*Freeze mode.

2.13 Use I/O Calibration from the Lane

The **Use I/O Calibration from the Lane** option supports the PolarFire® and PolarFire® SoC devices. This feature allows you to configure I/O to opt-out of recalibration. Use this feature either to delay or sequence calibration themselves or to account for VT impact on I/O performance. Default is OFF.

If you open an old design and you open the I/O Editor, you will not see this option. You must rerun compile to see the option.

Note: The **Use I/O Calibration from the Lane** option is not supported for ES and XT devices.

2.14 Schmitt Trigger

GPIO and HSIO can be configured as a Schmitt Trigger input. When configured as ON, it exhibits a hysteresis that helps to filter out the noise at the receiver and prevents double-glitching caused by noisy input edges. Default configuration is OFF (Schmitt Trigger disabled).

2.15 Vcm Input Range

Use this field to set the Vcm input range.

Direction: Input

2.16 On-Die Termination

On-Die Termination (ODT) is an option used to terminate input signals in PolarFire devices. Terminating input signals helps to maintain signal quality, save board space, and reduces external component costs. In SmartFusion2, IGLOO2, RTG4, and PolarFire FPGAs, ODT is available in receive mode and also in bidirectional mode when the I/O acts as an input. If ODT is not used or not available, the I/O standards may require external termination for better signal integrity.

ODT can be a pull-up, pull-down, differential, or Thévenin termination with both static and dynamic control available, and is set using either the Libero SoC software I/O attribute editor or by using a PDC command.

In addition, ODT can be controlled dynamically for individual I/Os as well as for all I/Os in a lane simultaneously on a per-lane basis.

2.17 ODT Static

On-die termination (ODT) is the technology where the termination resistor for impedance matching in transmission lines is located inside a semiconductor chip instead of on a printed circuit board. Possible values are listed in the following table.

Value	Description
on	Yes, the termination resistor for impedance matching is located inside the chip.
off	No, the termination resistor is on the printed circuit board.

2.18 ODT Dynamic

Note: This option is supported for RTG4 production devices only.

This option is used to opt in or out of the dynamic odt set on a bank. Possible value are listed in the following tables.

Value	Description
ODT_STATIC=On ODT_DYNAMIC=On	Illegal
ODT_STATIC=On ODT_DYNAMIC=Off	The ODT resistor is always turned on.

Value	Description
ODT_STATIC=Off ODT_DYNAMIC=Off	The ODT resistor is always turned off.
ODT_STATIC=Off ODT_DYNAMIC=On	The ODT resistor is on or off based on the ODT Dynamic bank setting.

The following I/O standards are supported:

- LVDS
- RSDS
- MINILVDS
- LVPECL
- HSTLI
- HSTLII
- SSTL15I
- SSTL15II
- SSTL18I
- SSTL18II
- HSTL18I
- HSTL18II
- LPDDRI
- LPDDRII

Note:
There is a known issue in the Libero SoC IO Editor and the pin report. A software limitation exists where a design cannot have different values for the P and N sides. Currently, both must have the same value. Libero SoC does program the P and N side correctly for programming. In IOEditor or pin report, if RES_PULL is Up on both, it means the N side is programmed as Down or visa-versa.

2.19 ODT Value

If the ODT option is turned on, the ODT Value (ohm) field can be set to any one of the values in the pull- down list. The ODT Value varies with different I/O standards.

2.20 ODT Imp (ohm)

Port Configuration (PC) bits are static configuration bits set during programming to configure the I/O(s) as per your choice. Refer to your device data sheet for a full range of possible values.

2.21 Low Power Exit

For single-ended I/Os, the Lower Power Exit value can be set from the drop-down list. The supported values for single-ended IOs are Off, Wake On Change, Wake On 0, Wake On 1. The default is Off.

The diff I/Os are marked as read-only fields and will be set to off.

2.22 Input Delay

Sets the Input Delay.

Input Delay applies to all I/O standards. The range of values supported varies depending on the device selected. The default value is OFF.

Note: This attribute will not appear in the I/O attributes and cannot be used in the PDC for some I/Os with dynamic delays, such as DDR I/Os.

2.23 Slew

The slew rate is the amount of rise or fall time an input signal takes to get from logic low to logic high or vice versa. It is commonly defined to be the propagation delay between 10% and 90% of the signal's voltage swing. The I/O Editor supports slew rate control in non-differential output mode. Turning the slew rate on results in faster slew rate, which improves the available timing margin. When slew rate is turned off, the device uses the default slew rate to reduce the impact of simultaneous switching noise (SSN). By default, the slew control is OFF. Not all I/O standards support the slew rate control.

2.24 Pre-Emphasis

The pre-emphasis rate is the amount of rise or fall time an input signal takes to get from logic low to logic high or vice versa. It is commonly defined to be the propagation delay between 10% and 90% of the signal's voltage swing. Possible values are shown in the table below.

Value	Description
NONE	Sets to none (default)
MIN	Sets to minimum
MEDIUM	Sets to medium
MAX	Sets to maximum

2.25 Output Drive

Use the Output Drive (mA) field to set the output drive strength. The output drive strength that can be set is different with different I/O standards and can vary from 1 mA to 20 mA. Select the drive strength value from the list of valid values in the pull-down list.

2.26 Impedance

Use the Impedance (Ohm) field in the I/O Editor to program the output impedance values. The Impedance value is different with different I/O standards and can vary from 22 Ohm to 240 Ohm. Click on the Impedance (Ohm) field to open a pull-down list containing valid values.

2.27 Output Load

The Output Load (pF) field indicates the output capacitance value based on the I/O standard. If necessary, you can double-click on the respective I/O port to change the output capacitance value to improve timing definition and analysis. Output capacitance affects output propagation delay.

SmartTime, Timing-driven layout, and Backannotation automatically use the modified delay model for delay calculations.

2.28 Source Termination

The Source Termination (Ohm) field is the Near End termination for a differential output I/O. The default is OFF.

Direction: Output

2.29 Output Delay

Sets the Output Delay.

Output Delay applies to all I/O standards. The default value is OFF.

Direction: Output

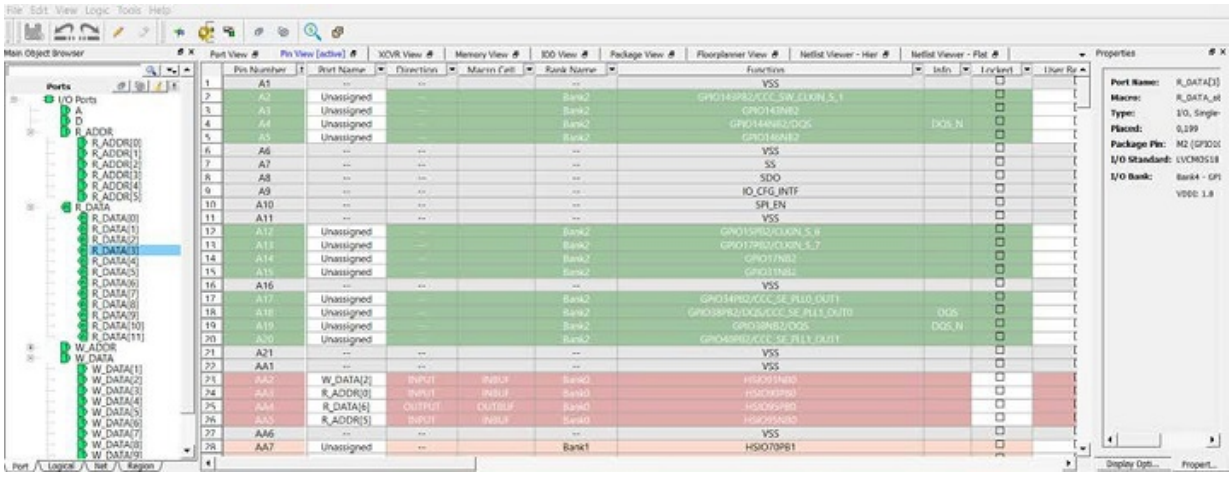
Note: This attribute will not appear in the I/O attributes and cannot be used in the PDC for some I/Os with dynamic delays, such as DDR I/Os.

3. Pin View

The Pin view displays the I/O attributes of I/O attributes in a spreadsheet-like format. Each row corresponds to an I/O macro (port) in the design, sorted by pin number. The column headings specify the names of the I/O attributes in your design. The first few column headings are standard and common for all families. The remaining columns display family-specific attributes. Only attributes applicable to a specific device appear in the I/O Editor attributes. For some I/O attributes, you will choose from a drop- down menu; for others, you may enter a value and for the rest, the field is read-only and not editable.

The display in the columns can be sorted alphabetically, numerically or filtered. See the following figure.

Figure 3-1. Pin View



Notes: Refer to the following documents for more information about the I/O standards supported by each attribute:

- PDC Commands User Guide (SmartFusion2, IGLOO2, and RTG4)
- PDC Commands User Guide (PolarFire)

3.1 Pin Number

This is the read-only package pin number specific to the die and package of the device.

3.2 Port Name

This is an editable field for the assignment of a port to that particular pin number. It contains a pull-down list of the assignable and available Ports for the pin. Select Unassigned to leave the pin unassigned.

3.3 Direction

Non-editable field that denotes Input, Output, or Inout.

3.4 Macro Cell

This is a read-only field that identifies the name of the macro cell associated with the port.

3.5 Bank Name

This is a read-only field to identify the I/O bank the I/O pin is associated with. Devices may five, six, or eight user I/O banks (Bank 0 through Bank 7), depending on the device size. Each pin is associated with an I/O bank. The I/O banks on the north side of the device support only HSIO. Each I/O bank has dedicated I/O supplies and grounds. Each I/O within a given bank shares the same VDDI power supply, and the same VREF reference voltage. Only compatible I/O standards can be assigned to a given I/O bank.

3.6 Function

The function name identifies the functions of the pin/port. This is the same as what is listed in the Public Pin Assignment Table (PPAT) for the selected device and package. For details, see the device data sheet of the die/package.

The function name may contain the following information:

- Type of I/O: GPIO or HSIO
- Special-purpose I/Os (for example, XCVR)
- The I/O Bank Number
- Positive/Negative Pad of differential I/Os
- VSS or Ground

3.7 Locked

Set this option to lock all I/O banks, so the I/O Bank Assigner cannot unassign and reassign the technologies in the design.

3.8 User Reserved

For the I/O pin you want to reserve for use in another design, check the User Reserved checkbox to reserve it. When a pin is reserved, you cannot assign it to a port.

3.9 Dedicated

If checked, the pin is reserved for some special functionality, such as UJTAG, Power, XVCR Reference Clock, device reset, and clock functions.

3.10 Vref

Any GPIO and HSIO pad on the device can be configured to act as an external VREF to supply all inputs within a bank. Use this field to configure the I/O as VREF to other I/Os. When an I/O pad is configured as Vref (voltage referenced), all I/O buffer modes and terminations on that pad are disabled.

3.11 User I/O Lock Down

If checked, the current pin assignment cannot be changed during layout.

3.12 I/O State in Flash*Freeze Mode

By default, all the I/Os become tristated when the device goes into Flash*Freeze mode. You can override this default behavior by setting its value to one of the following two values:

- LAST_VALUE - Preserves the previous state of the I/O. This means the I/O remains in the same state in which it was functioning before the device went into Flash*Freeze mode.

- LAST VALUE_WP - Preserves the last value with weak pull-up.

3.13 Clamp Diode

PolarFire devices have internal PCI clamp diodes for both HSIO and GPIO. PCI clamp diodes help reduce the voltage level at the input, and are mainly used when the voltage overshoot exceeds the maximum allowable limit. If signaling levels of the receiver are greater than the VDDIx of the bank, the clamp diode must be off to support hot-socketing insertion.

For GPIO, use this field to program the clamp diode to be ON or OFF.

For HSIO, the internal clamp diode is always on by default.

3.14 Resistor Pull

Use this field to allow inclusion of a weak resistor for either pull-up or pull-down of the input or output buffer. The available options are None, Up (pull-up), Down (pull-down), or Hold. The default value is None.

Note: Not all I/O standards have a selectable resistor pull option.

3.15 I/O Available in Flash*Freeze Mode

Use this field to indicate if the I/O is available or unavailable in Flash*Freeze mode. The default value is “no” and the I/O is unavailable in Flash*Freeze mode.

3.16 Schmitt Trigger

GPIO and HSIO can be configured as a Schmitt Trigger input. When enabled as such (YES), it exhibits a hysteresis that helps to filter out the noise at the receiver and prevents double-glitching caused by noisy input edges. Default value is OFF.

3.17 Vcm Input Range

Values for all I/O standards are MID and LOW. The default is MID.

3.18 On-Die Termination

On-Die Termination (ODT) is an option used to terminate input signals in PolarFire devices. Terminating input signals helps to maintain signal quality, save board space, and reduces external component costs. In PolarFire FPGAs, ODT is available in receive mode and also in bidirectional mode when the I/O acts as an input. If ODT is not used or not available, the I/O standards may require external termination for better signal integrity.

ODT can be a pull-up, pull-down, differential, or Thévenin termination with both static and dynamic control available, and is set using either the Libero SoC software I/O attribute editor or by using a PDC command.

In addition, ODT can be controlled dynamically for individual I/Os as well as for all I/Os in a lane simultaneously on a per-lane basis.

3.19 ODT Static

On-die termination (ODT) is the technology where the termination resistor for impedance matching in transmission lines is located inside a semiconductor chip instead of on a printed circuit board. Possible values are listed in the table below.

Value	Description
on	Yes, the termination resistor for impedance matching is located inside the chip.
off	No, the termination resistor is on the printed circuit board.

3.20 ODT Dynamic

Note: This option is supported for RTG4 production devices only.
This option is used to opt in or out of the dynamic odt set on a bank. Possible value are listed in the following table.

Value	Description
ODT_STATIC=On ODT_DYNAMIC=On	Illegal
ODT_STATIC=On ODT_DYNAMIC=Off	The ODT resistor is always turned on.
ODT_STATIC=Off ODT_DYNAMIC=Off	The ODT resistor is always turned off.
ODT_STATIC=Off ODT_DYNAMIC=On	The ODT resistor is On or Off based on the ODT Dynamic bank setting.

The following I/O standards are supported:

- LVDS
- RSDS
- MINILVDS
- LVPECL
- HSTLI
- HSTLII
- SSTL15I
- SSTL15II
- SSTL18I
- SSTL18II
- HSTL18I
- HSTL18II
- LPDDRI
- LPDDRII

3.21 ODT Value

If ODT option is turned on, the ODT Value (Ohm) field can be set to any one of the values in the pull-down list. The ODT Value varies with different I/O standards.

Values vary depending on the I/O standard.

3.22 ODT Imp (ohm)

On-die termination (ODT) is the technology where the termination resistor for impedance matching in transmission lines is located inside a semiconductor chip instead of on a printed circuit board.

Port Configuration (PC) bits are static configuration bits set during programming to configure the I/O(s) as per your choice. Refer to your device datasheet for a full range of possible values.

3.23 Low Power Exit

For single-ended I/Os, the Lower Power Exit value can be set from the drop-down list. The supported values for single-ended IOs are Off, Wake On Change, Wake On 0, and Wake On 1. The default is Off.

The differential I/Os are marked as read-only fields and will be set to off.

3.24 Input Delay

Sets the Input Delay.

Input Delay applies to all I/O standards. The range of values supported varies depending on the device selected. The default value is OFF.

Note: This attribute will not appear in the I/O attributes and cannot be used in the PDC for some I/Os with dynamic delays, such as DDR I/Os.

3.25 Slew

The slew rate is the amount of rise or fall time an input signal takes to get from logic low to logic high or vice versa. It is commonly defined to be the propagation delay between 10% and 90% of the signal's voltage swing. The I/O Editor supports slew rate control in non-differential output mode. Turning the slew rate on results in faster slew rate, which improves the available timing margin. When slew rate is turned off, the device uses the default slew rate to reduce the impact of simultaneous switching noise (SSN). By default, the slew control is OFF. Not all I/O standards support the slew rate control.

Note: Slew rate control is not available in PolarFire HSIO buffers. However, these buffers have built-in PVT-compensated slew rate controllers for optimized signal integrity.

3.26 Pre-Emphasis

The pre-emphasis rate is the amount of rise or fall time an input signal takes to get from logic low to logic high or vice versa. It is commonly defined to be the propagation delay between 10% and 90% of the signal's voltage swing. Possible values are shown in the following table.

Value	Description
NONE	Sets to none (default)
MIN	Sets to minimum
MEDIUM	Sets to medium
MAX	Sets to maximum

3.27 Output Drive

Use the Output Drive (mA) field to set the output drive strength. The output drive strength that can be set is different with different I/O standards and can vary from 1 to 20 mA. Select the drive strength value from the list of valid values in the pull-down list.

3.28 Impedance

Use the Impedance (Ohm) field in the I/O Editor to program the output impedance values. Impedance values are different for different I/O standards, and can vary from 22 Ohm to 240 Ohm. Use the pull-down list to select the desired Ohm value.

3.29 Output Load

The Output Load (pF) field indicates the output capacitance value based on the I/O standard. If necessary, you can double-click on the respective I/O port to change the output capacitance value to improve timing definition and analysis. Output capacitance affects output propagation delay.

SmartTime, Timing-driven layout, and Backannotation automatically use the modified delay model for delay calculations.

3.30 Source Termination

The Source Termination (Ohm) field is the Near End termination for a differential output I/O. The default is OFF.

Direction: Output

3.31 Output Delay

Sets the Output Delay.

Output Delay applies to all I/O standards. The range of values supported varies depending on the device selected. The default value is OFF. The default value is OFF.

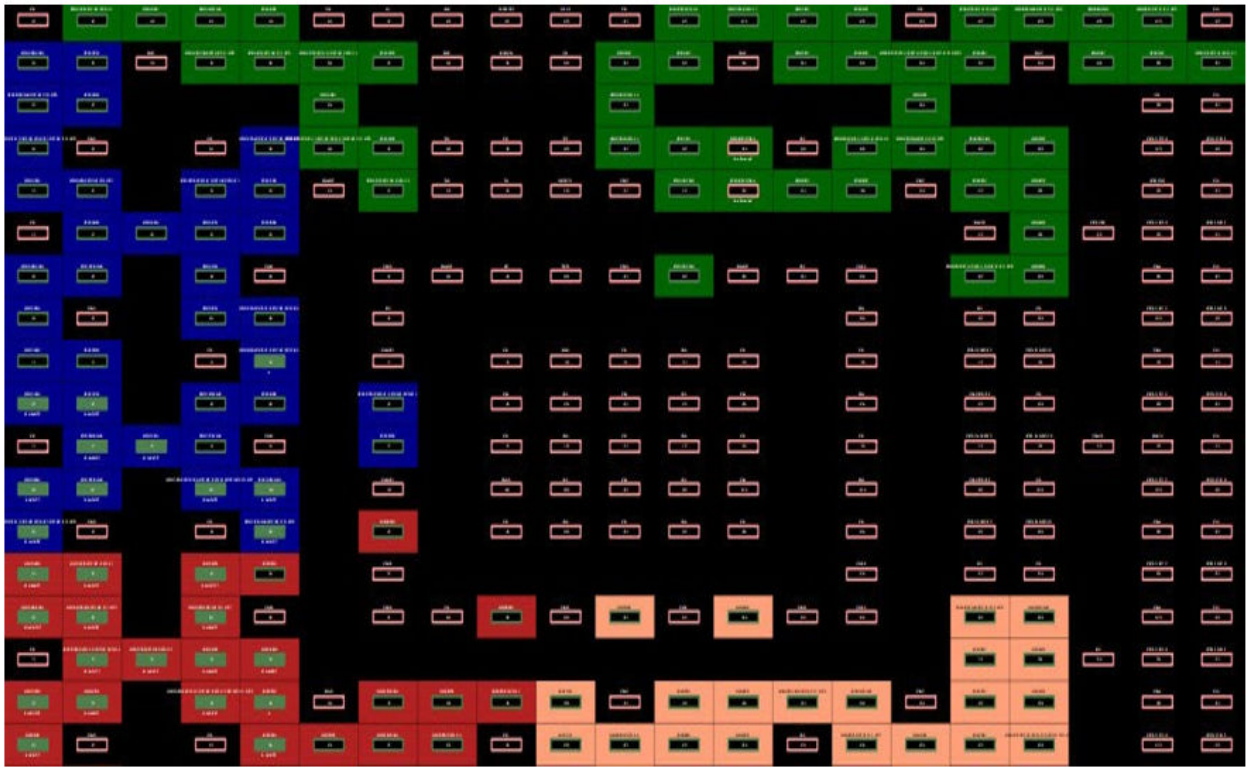
Direction: Output

Note: This attribute will not appear in the I/O attributes and cannot be used in the PDC for some I/Os with dynamic delays, such as DDR I/Os.

4. Package View

The Package View displays the Package pin views of the particular die/package of the PolarFire device. The color for the display of the pins are determined by the settings in Display Options. The following figure shows the regular pins in green, special pins in blue, reserved pins in red and unconnected pins in grey.

Figure 4-1. Package View



5. Interface-Specific I/Os and Views

The PolarFire architecture is designed and optimized to support Memory interface, IOD interface and Transceiver interface. The I/O Editor for PolarFire provides three special views specifically for I/O assignments of these interfaces.

For optimal Quality of Result (QOR) and timing performance, the architecture of the PolarFire silicon requires the Memory Interface, IOD Interface and Transceiver Interface be placed in specific and pre- defined locations of the chip. Assignment of these interfaces are checked against PolarFire DRC rules and illegal assignments are flagged.

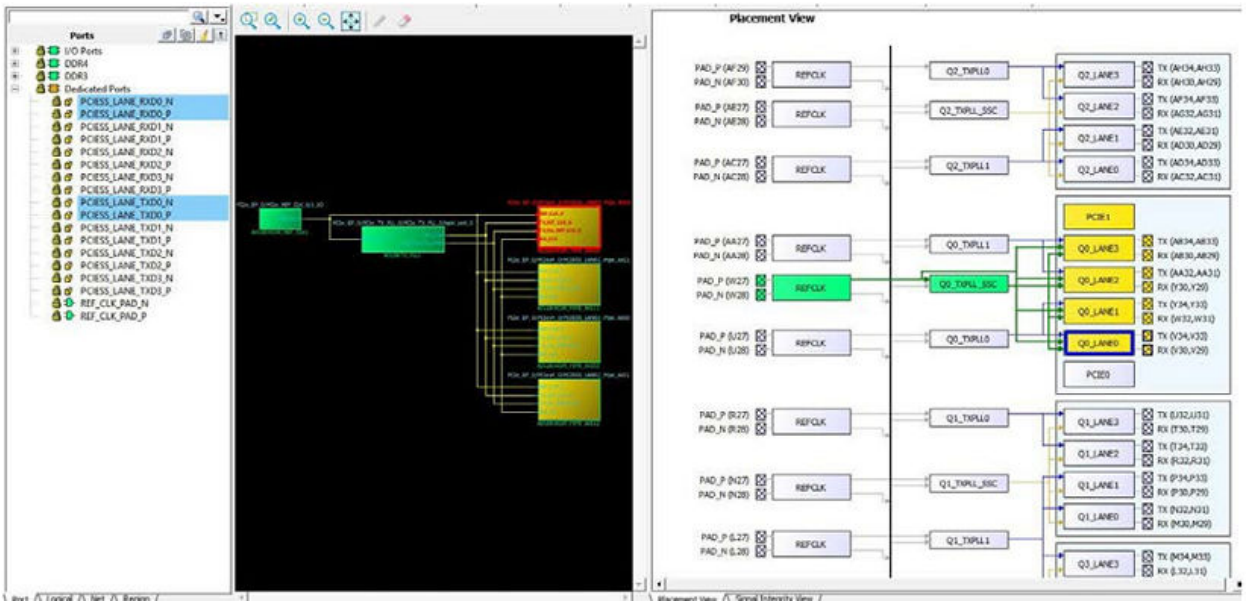
The I/O Editor is a graphical user interface (GUI) tool designed to make Interface I/O pin assignments graphically and user-friendly, as an alternative to writing PDC commands. When the pin assignment is committed and saved in I/O Editor, a PDC file is created. This PDC file can then be passed to the Place and Route tool as a Physical Design Constraint.

5.1 Interface-Specific I/O Views

In addition to the Pin view, Port view and Package view, the I/O Editor provides three views specific to PolarFire-supported interfaces I/Os:

- Memory View - for I/O pin assignments of Memory interfaces such as DDR3/4,LPDDR3, and QDR.
- XCVR View - Presents a physical view of the Transceiver connectivity, including Transceiver lanes, and Reference Clock (REFCLK), and Transmit PLL lines.
- IOD Lane Controller View - Presents the I/O Digital block view, used for non-memory interfaces using the FPGA I/Os.

Figure 5-1. I/O Editor - XCVR View



6. Memory Interface View

The Memory Interface view presents a spreadsheet-like view of the I/Os available in the PolarFire silicon for different Memory interface types.

6.1 Memory Type

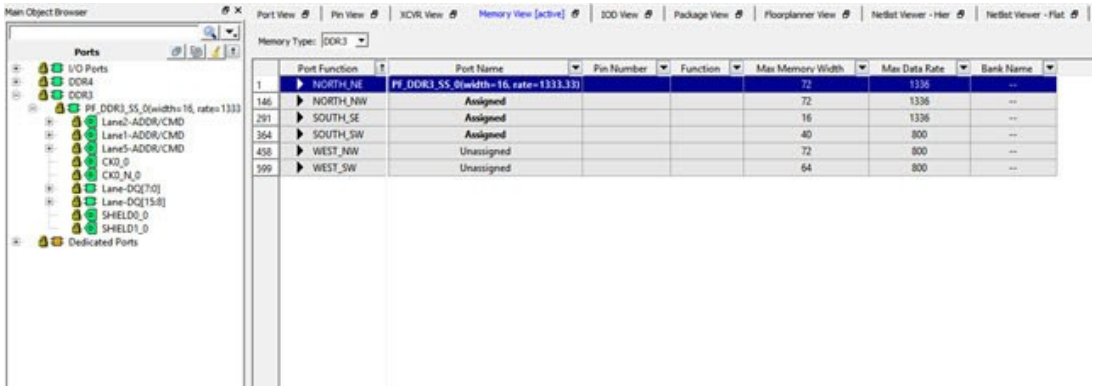
The supported Memory Interface types include:

- DDR3
- DDR4
- LPDDR3
- QDRII+

Use the pull-down menu to select the type of Memory Interface used in the design. Only the specific type of memory used in the design are displayed in the pull-down list.

The Ports view also displays the memory width and data rate of the DDR instance in the design (if it exists in the design) in the top left row under the Port Name column, as shown in the following figure.

Figure 6-1. Memory Interface Type Menu



6.2 Edge_Anchors for Memory Placement

The PolarFire silicon architecture requires that the Memory interface be placed in specific and pre- defined locations of the chip to achieve optimal QOR and timing performance. These specific location are called Edge_Anchors and are used to identify the specific location in the PolarFire chip for optimal Memory Interface I/O placement. See the PolarFire FPGA DDR Memory Controller User Guide for a mapping of DDR memory interface types to Edge_Anchor locations. The Edge_Anchors are as follows:

- NORTH_NE
- NORTH_NW
- SOUTH_SE
- SOUTH_SW
- WEST_NW
- WEST_SW

The ports for each Edge_Anchor is represented by a different color for easy identification. The list of possible Edge_Anchors is context-sensitive to the Memory Interface type and represents the legal and optimal locations for the specific Memory interface type. The list of Edge_Anchors for DDR4, for example, is different from the list for DD2/DDR3. DDR4 has fewer locations (Edge_Anchors) for I/O placement than DDR2/DD3.

6.3 Memory Interface View Columns

The Memory Interface view detects the type of Memory Interface in the design and presents the ports in the Ports View. The Memory Interface view displays the following I/O information in the view. Each of the column can be sorted (ascending/descending order) or filtered:

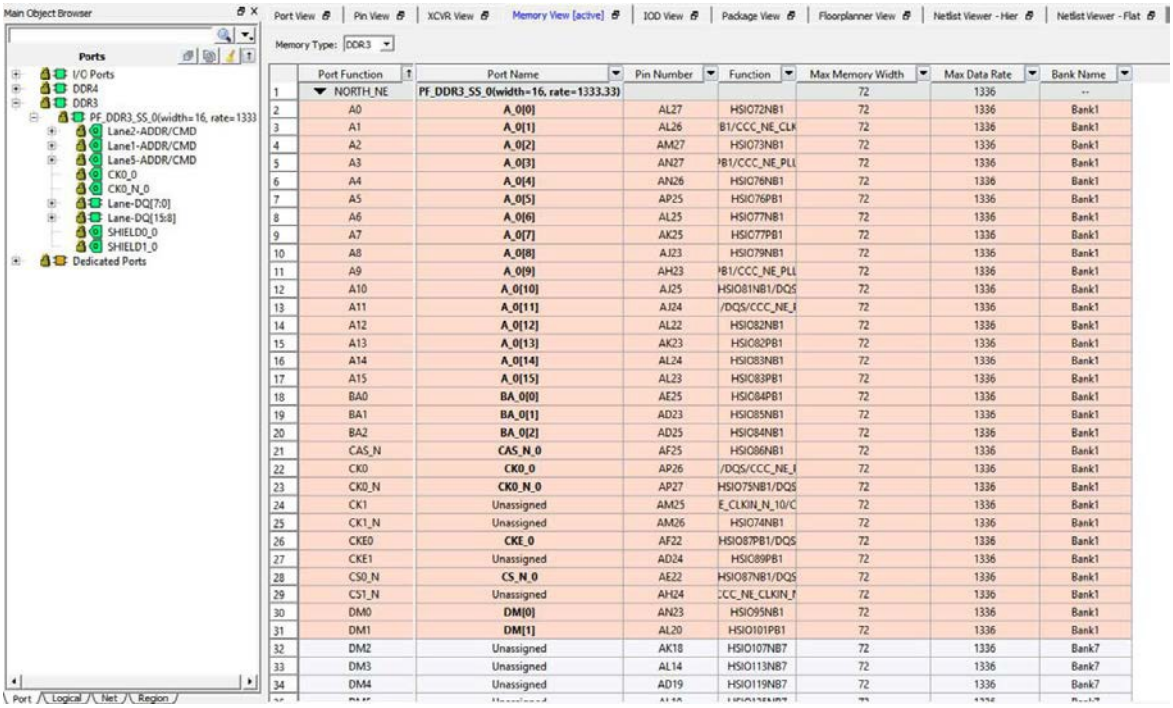
- Port Function - Formal port name of the Memory Interface. The ports specific to the memory interface type are loaded into the Port view.
- Port Name - Port name of the Memory Interface instance in the design.
- Pin Number - Package pin number assigned to the port of the Memory Interface
- Function - More descriptive function name of the Port, which identifies the type of I/O (for example, HSIO for High-speed I/Os or GPIO (General-purpose IO)
- Max Memory Width - Maximum memory width of the DDR. This is a fixed read-only value specific to the Edge_Anchor and is different with different Edge_Anchors.
- Max Data Rate - Maximum data rate in Mbps. This is a fixed read-only value specific to the Edge_Anchor and is different with different Edge_Anchors.

Notes: When making DDR placement, refer to the memory width and data rate of the DDR Memory used in the design (as displayed in the Ports View). Make sure that the Edge_Anchor location, where you want to place the DDR memory, can accommodate the DDR memory in terms of the memory width and the data rate. This will avoid invalid placement.

- Bank Name - the I/O bank name of the port
- High-speed I/O Clocks - specifies the number of High Speed I/O clocks

The Pin Number and Function are the same as what are listed in the PPAT for the selected device and package. The PPAT for each PolarFire package are provided in the PolarFire_<package> Pinouts file on the PolarFire Documentation web page.

Figure 6-2. Memory Interface View



6.4 Making I/O Assignments

To make I/O assignment for the Memory Interface instance in the design:

1. Select the Memory Interface type from the drop-down menu.
2. From the Ports tab in the Design Tree View, drag the Memory Interface instance and let the mouse hover over one of the Edge_Anchor locations available for the Memory Interface type. A tooltip reports whether it is a legal or illegal location for the Interface instance.
3. Drop the Interface instance into a legal Edge_Anchor location.

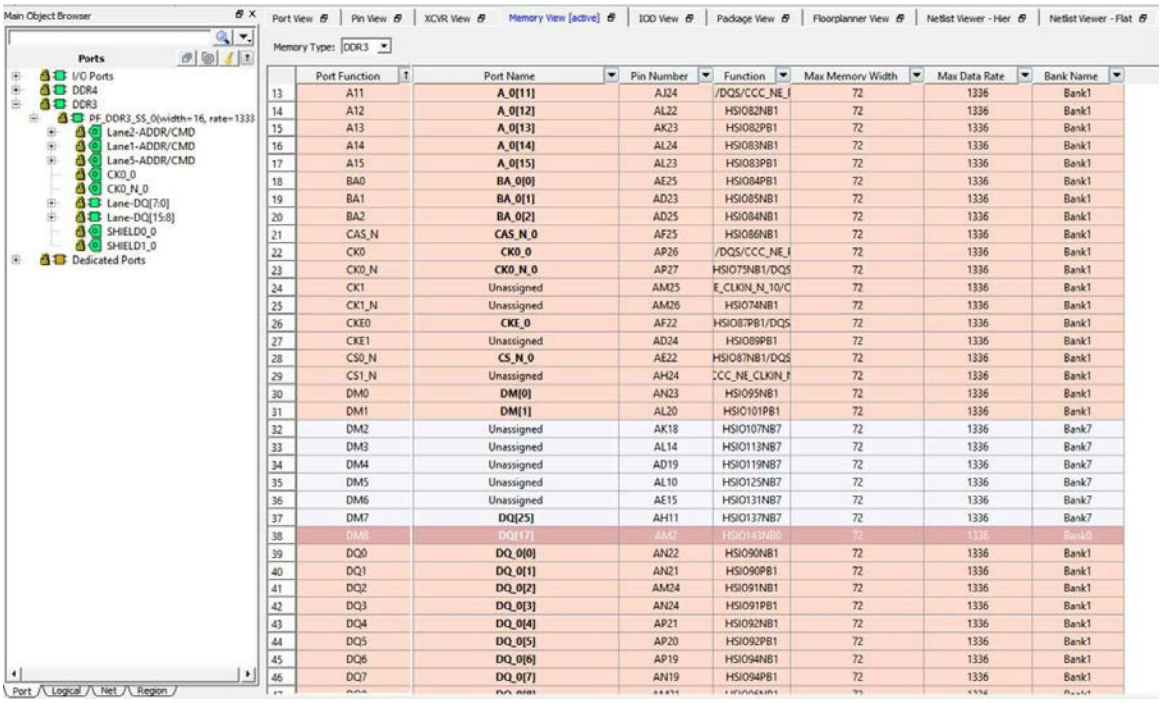
Note: DRC rules are enforced. Drag-and-drop I/O placement that violates the DRC rules are reported in the Log window. For Memory Interface, the DRC checks the Data Width and the Data Rate compliance*. If the specific location cannot accommodate the Data Width or the Data Rate of the Memory interface, no I/O assignment is made. An error is reported in the Log Window with a message that explains why the assignment is not accepted. In the following figure, the DRC error message reports that the ddr3 instance requires 64 ports, but the SOUTH_SE location can accommodate only 58 pins.

Note: *Data Rate compliance will be enforced in a later release.

Figure 6-3. DRC Checks in Log Window

4. Check that no DRC error messages are reported in the Log window and the I/O assignments are accepted (see the following figure). The Lock icon in the Ports tab indicates that the I/O assignment is accepted and locked.

Figure 6-4. Memory Interface Assignments Accepted



6.5 IO_PDC File

When the I/O assignment is committed and saved in the I/O Editor, the assignment is saved in a PDC file in the <project_folder/constraints/io/user.pdc file. The PDC file contains set_io commands on each of the DDR Memory Interface I/O.

The following figure shows PDC file generation after Memory interface I/O assignment in the I/O Editor.

Figure 6-5. PDC File Generation after Memory Interface I/O Assignment in I/O Editor

```
set_io -port_name {DQ[24]}  \
    -pin_name AG11          \
    -fixed true             \
    -ODT_VALUE 60           \
    -DIRECTION INOUT


set_io -port_name {DQ[25]}  \
    -pin_name AH11          \
    -fixed true             \
    -DIRECTION INOUT


set_io -port_name {DQ[26]}  \
    -pin_name AG12          \
    -fixed true             \
    -DIRECTION INOUT


set_io -port_name {DQ[27]}  \
    -pin_name AH12          \
    -fixed true             \
    -DIRECTION INOUT


set_io -port_name {DQ[28]}  \
    -pin_name AJ10          \
    -fixed true             \
    -DIRECTION INOUT


set_io -port_name {DQ[29]}  \
    -pin_name AJ11          \
    -fixed true             \
    -DIRECTION INOUT
```

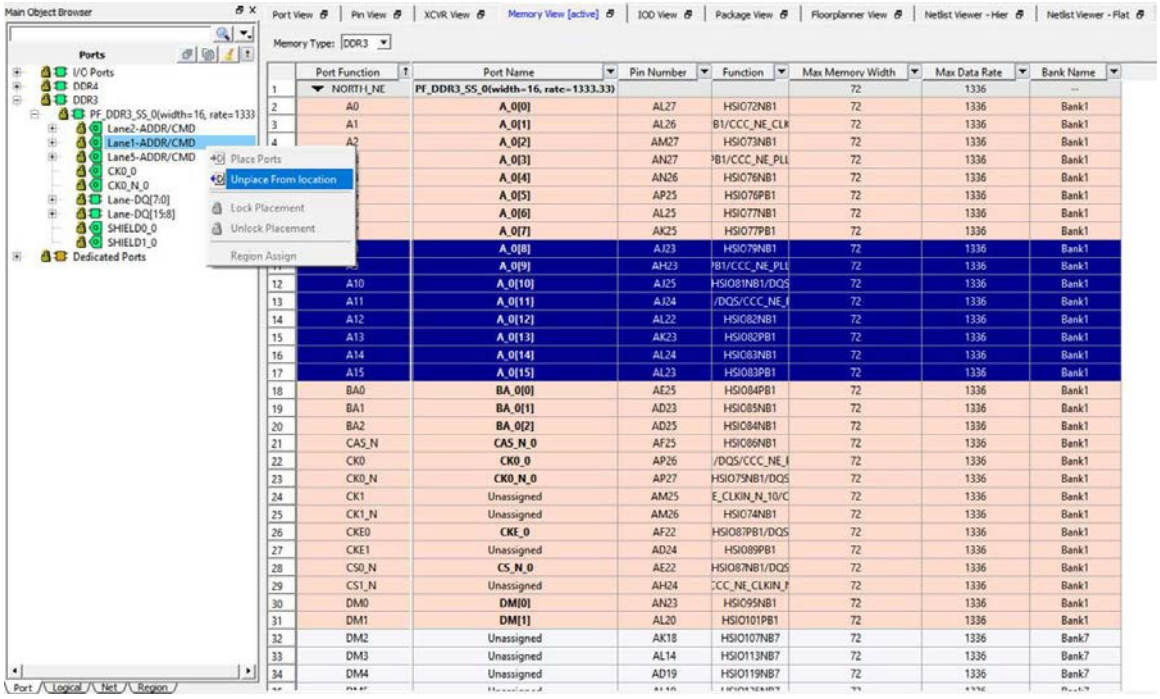
6.6 Removing I/O Assignments

To remove a DDR Memory Interface I/O assignment:

1. Select the Port tab in the Design Tree view.
2. Right-click the Memory Interface in the Design Tree view.
3. Select Unplace <memory_interface_name> .

   See the following figure.

Figure 6-6. Removing Memory Interface I/O Assignment



7. XCVR View

The XCVR View allows the user to make assignments for Transceiver Lanes, Reference Clocks and Transmit PLLs. It presents the following views:

- A schematic view of the Reference Clock (REFCLK), the TransmitPLL, and the Transceiver Lanes they drive. See Figure 7-1.
- A graphical placement view of the REFCLK, its connection from the PADS, to the TransmitPLL, to the Transceiver Lanes. See Figure 7-2.
- A Signal Integrity View for a Transceiver Lane, showing TX Emphasis Amplitude, TX Impedance, TX Transmit Common Mode Adjustment, RX and TX Polarity, RX Insertion Loss, RX CTLE, RX Termination, RX P/N Board Connection, and RX Loss of Signal Detector (Low and High). See Figure 7-3.

Figure 7-1. XCVR Interface - Schematic View

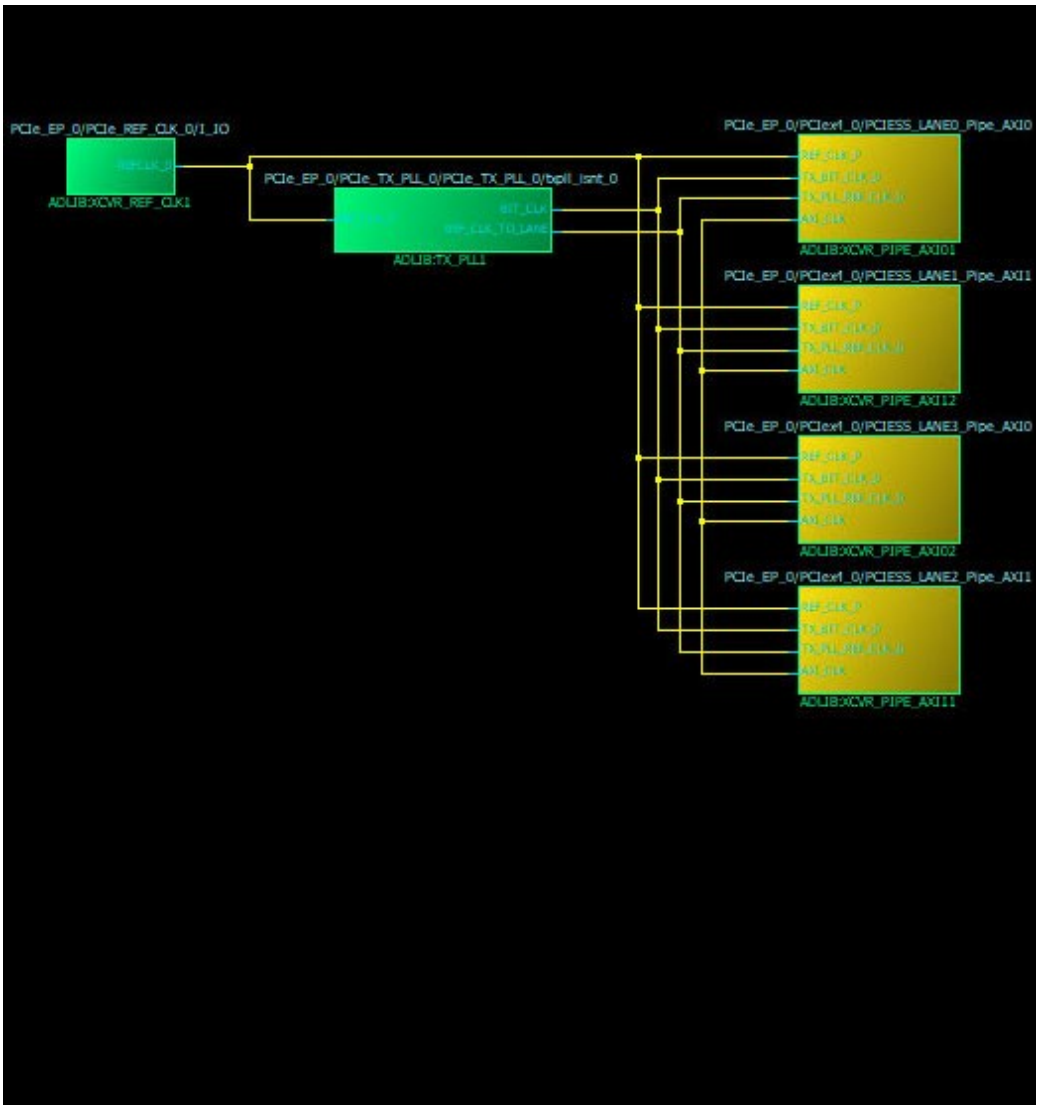


Figure 7-2. XCVR Interface - Graphical Placement View

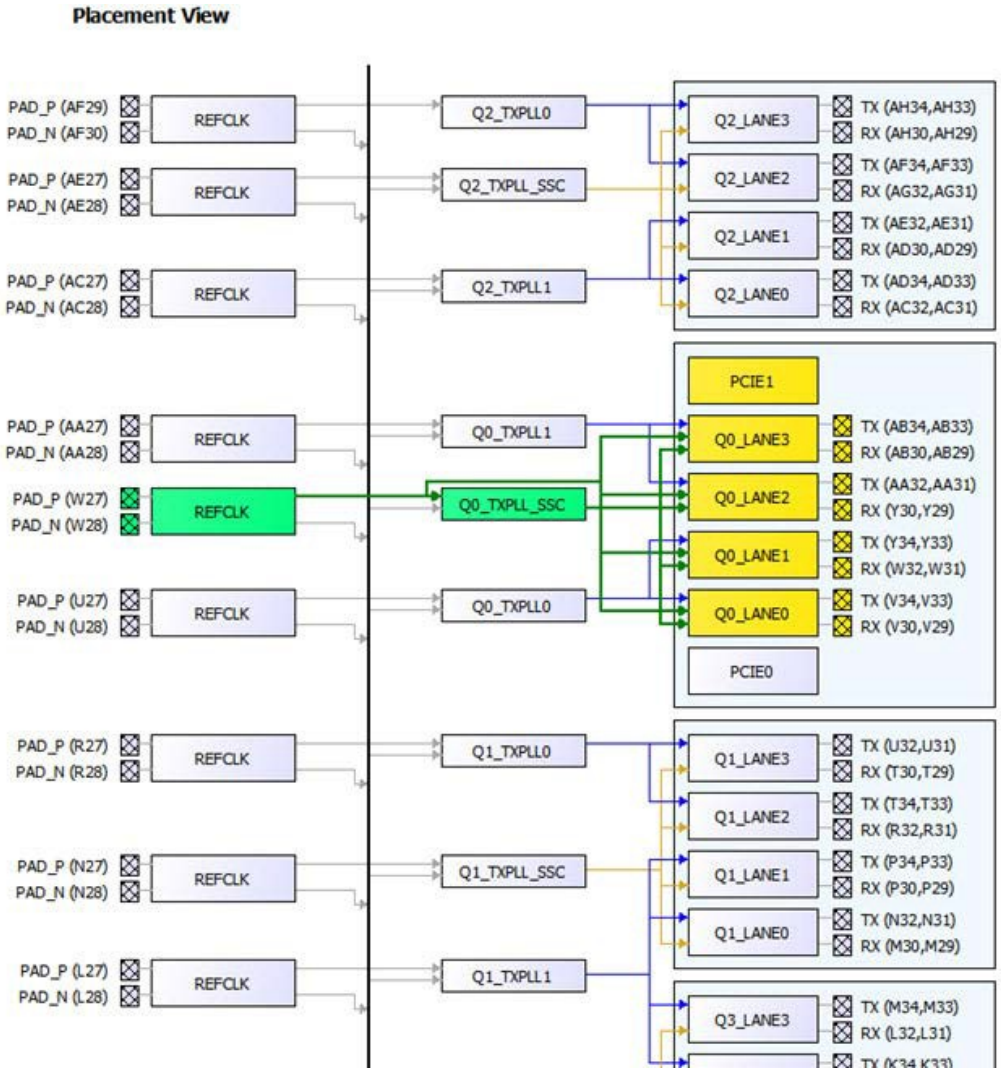
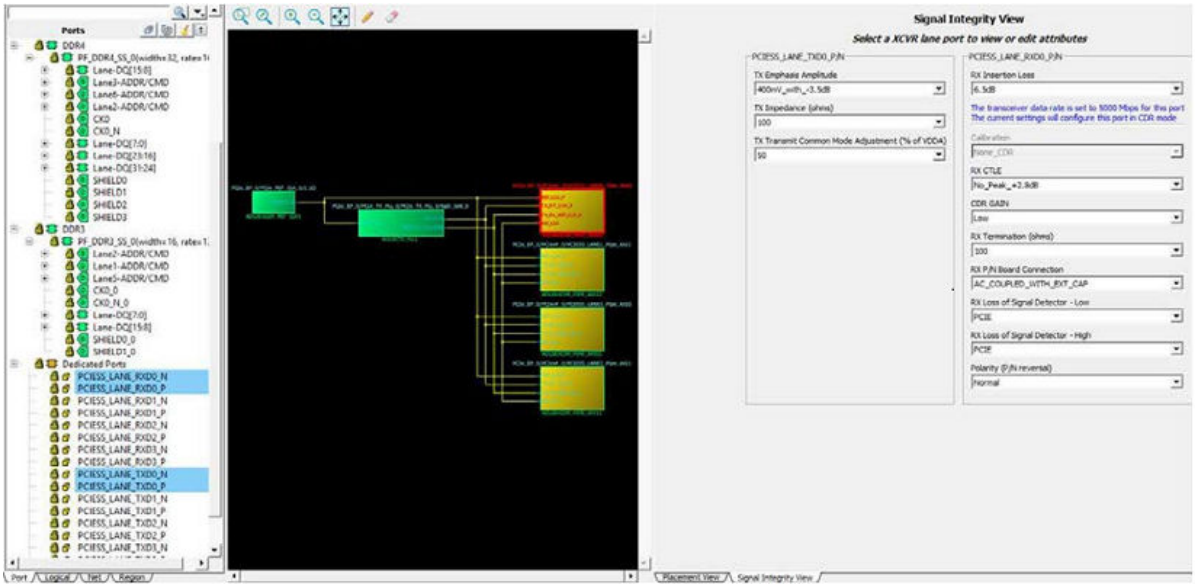


Figure 7-3. I/O Editor - XCVR View - Signal Integrity View



The Signal Integrity View for a Transceiver Lane shows the following:

- TX Emphasis Amplitude
- TX Impedance
- TX Transmit Common Mode Adjustment
- RX and TX Polarity, RX Insertion Loss, RX CTLE
- RX Termination
- RX P/N Board Connection
- RX Loss of Signal Detector (Low, High, Calibration, and CDR Gain)

7.1 XCVR Interface I/O Assignment

To make XCVR Interface I/O assignment, use the XCVR view in the I/O Editor to make assignment in the following order:

1. Transceiver Lanes
2. TX PLL
3. REFCLK

7.2 Direct Versus Cascaded Connection

The PolarFire XCVR reference clock network provides rich connectivity to the TX_PLL and Transceiver lanes. The connectivity allows the user to share common reference clock inputs to reduce fanout buffers on the board and reduce costs.

The two types of connections between the reference clock and the TX _PLL and Transceiver lanes are as follows:

- Direct Connection
- Cascaded Connection

Direct connections are used when the reference clock pin and the TX_PLL or the Transceiver lanes are in the same Quad location. Cascaded connections are used when the reference clock pin and the TX_PLL or the Transceiver lanes are not in the same quad location. Cascade connections are only available going from the top of the device towards the bottom. The cascaded connection is denoted in the XCVR view by the black vertical line down the middle of the placement view.

Note: A REFCLK can connect to all the lanes beside or below it in any quad (down the cascade path) but not those above it (up the cascade path).

The red lines denote cascaded REFCLK connection to the TX_PLL and the Transceiver lanes in the quad.

Connection/Assignment up the Cascade path (from REFCLK to TX_PLL and Transceiver lanes which are above the REFCLK) are illegal and indicated by red lines in the XCVR view.

Each Reference Clock (REFCLK) has a direct dedicated connection to its corresponding TX_PLL and to the lane that the TX_PLL drives in the same quad.

Selecting a dedicated connection or a cascaded connection depends on the trade-off you want to make. A direct dedicated connection from the REFCLK to the TX_PLL gives better signal integrity for the Transceiver whereas a cascaded connection reduces external components and reduces overall power.

Figure 7-4. Direct Dedicated Path and Cascade Path

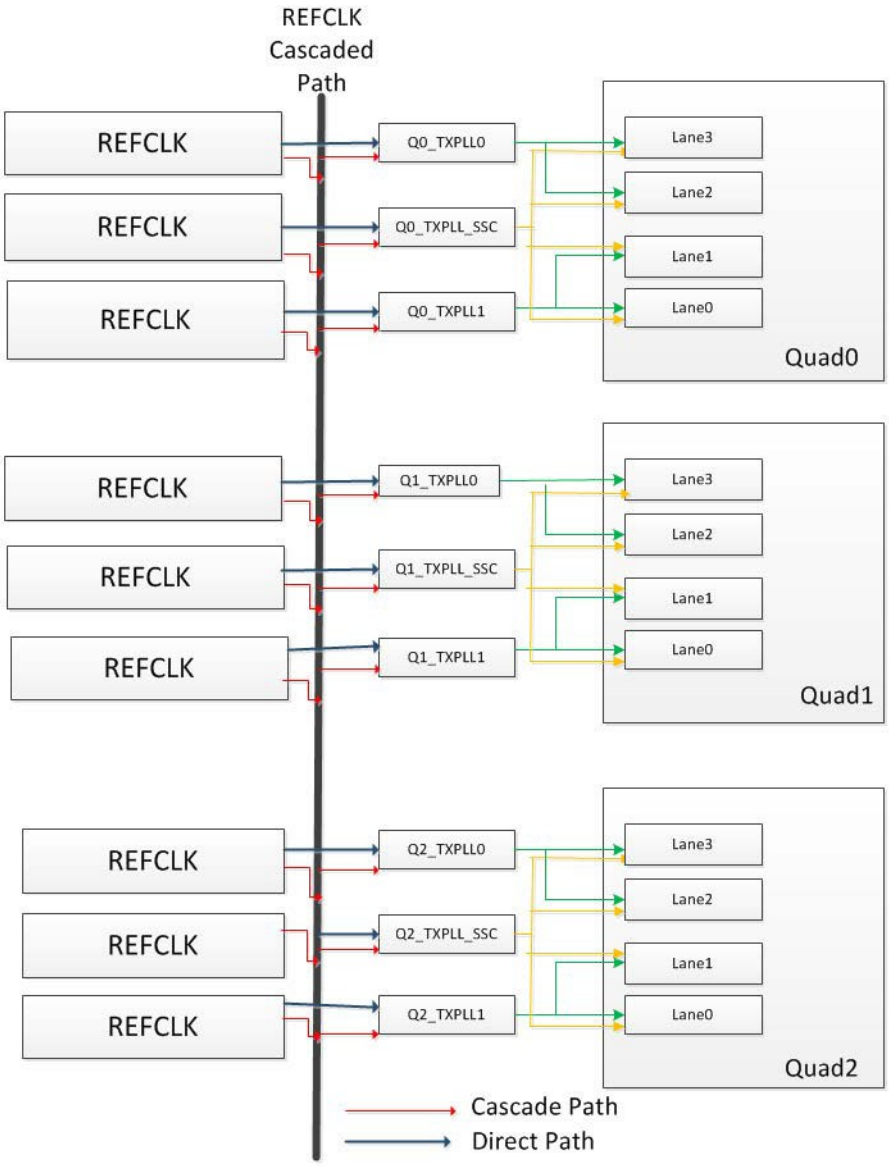
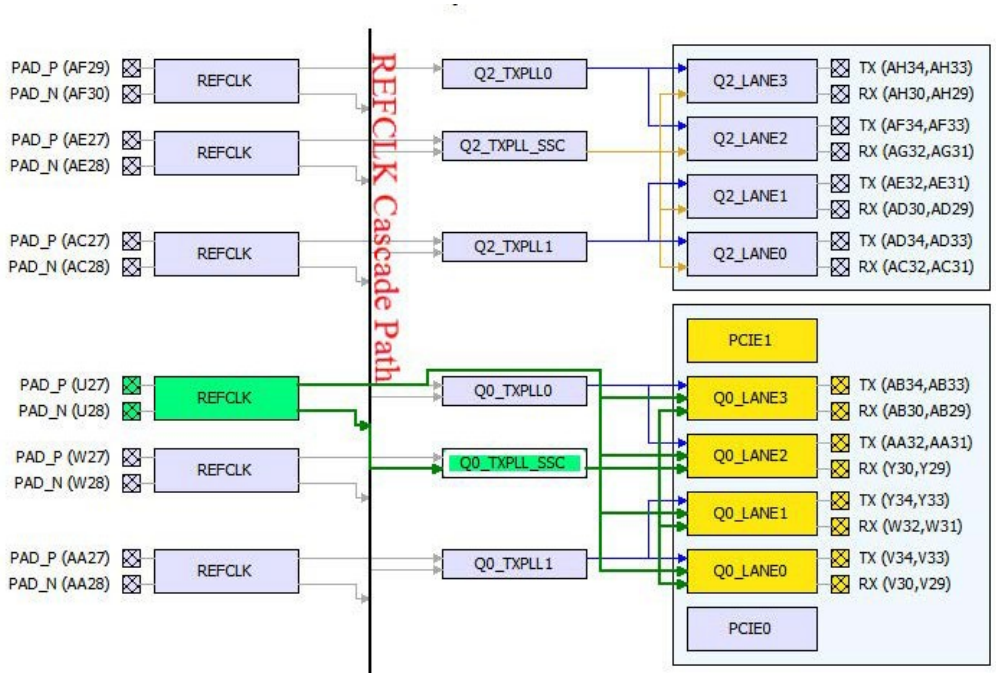


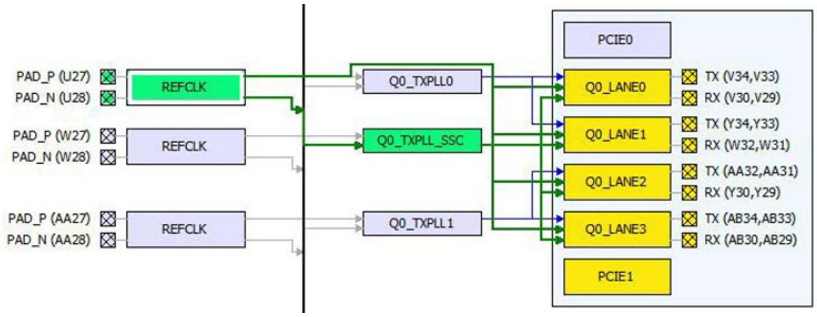
Figure 7-5. XCVR View



7.3 Reference Clock (REFCLK) I/O Assignments

To make I/O assignments, click and drag the REFCLK pin from the Schematic View to the pin location you desire in the Graphical Placement View. If the assignment is legal (no DRC violations), green lines appear to denote the accepted connection between the REFCLK pin through the Q(x)_TXPLL_SSC to the Transceiver lanes.

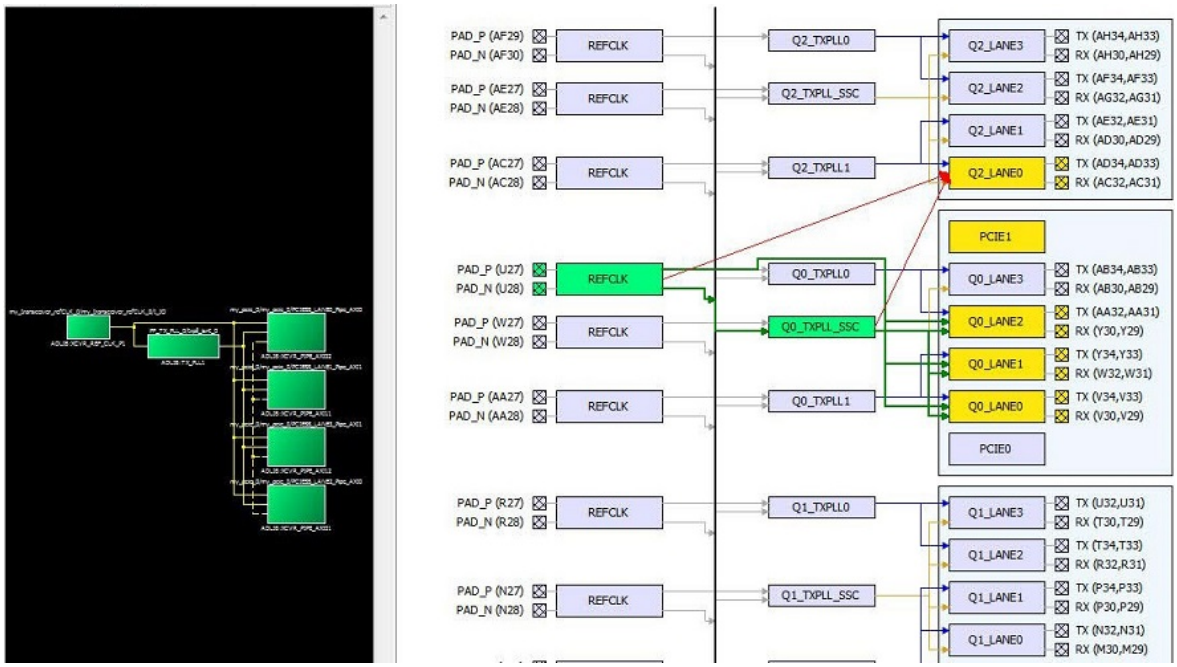
Figure 7-6. Legal and Accepted Reference Clock I/O Assignment



If the I/O assignment violates the DRC rule, the assignment is not accepted. Red arrows denotes DRC violations. The following figure shows two illegal assignments:

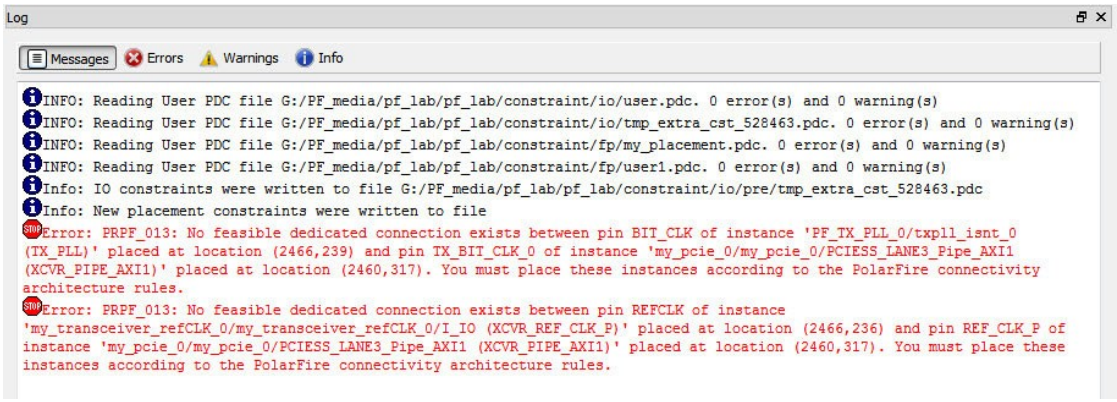
- From the Reference Clock (REFCLK) to the Lanes (Red arrow from REFCLK to the Q2_Lane0)
- From the Transmit PLL to the lanes (Red arrow from TXPLL_SSC to Q2_Lane0)

Figure 7-7. Illegal I/O Assignment



An error message appears in the Log window to identify the DRC rules violated. In this case, there is no feasible dedicated connection from the REFCLK to the Lane and from the Transmit PLL to the Lanes.

Figure 7-8. Log Window Message

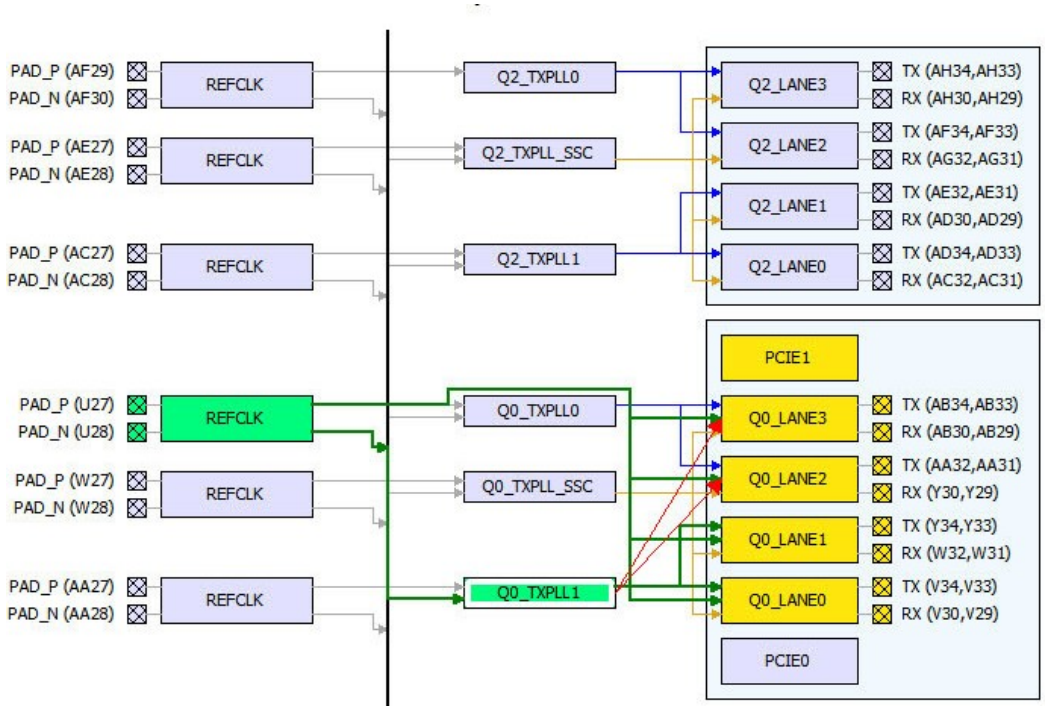


Note: I/O assignments can be made for REFCLK, TXPLL, and Transceiver Lanes for all Transceiver protocols except the PCIe Protocol. For the PCIe Protocol, Transceiver Lanes are assigned to predefined locations and cannot be removed.

7.4 Transmit PLL Assignment

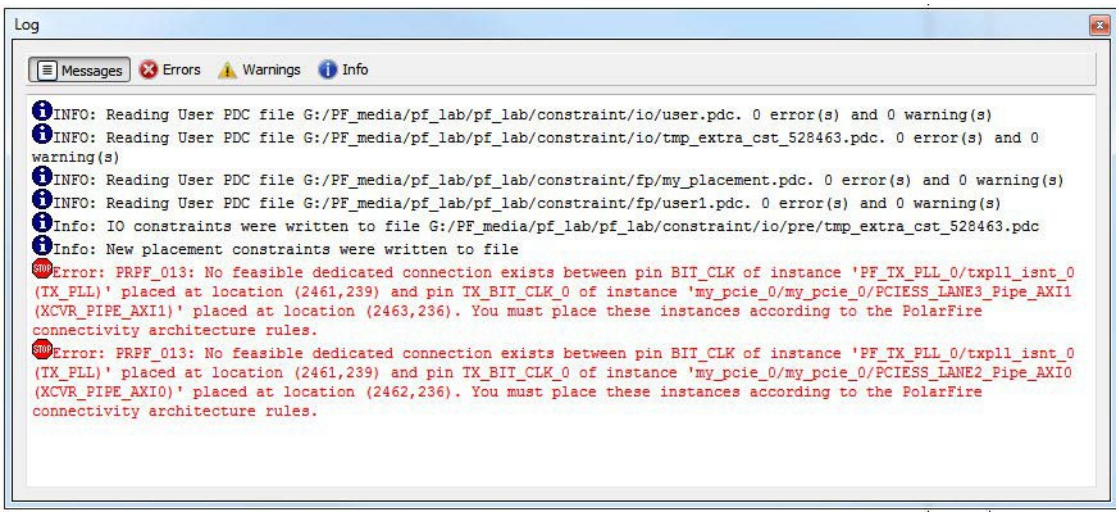
Drag and drop the Transmit PLL instance into the desired location. Illegal locations are flagged with error messages in the Log window and the illegal connections are indicated by red lines.

Figure 7-9. Illegal Transmit PLL to Lane Assignment



The Log window displays two error messages about the illegal assignments, one for each illegal connection. In this case, the assignment is illegal because there are no feasible dedicated connections.

Figure 7-10. Log Window



7.5 Placement DRC Rules

The I/O Editor enforces the DRC rules when Transceivers are placed. Any illegal connection is highlighted as a red line in the Placement View and a corresponding message is displayed in the Log window.

Lane assignments are always legal. DRC rules are enforced for the following:

- Connection from Transmit PLL (TXPLL) to the Lanes
- Connection from the Reference Clock (REFCLK) to the Transmit PLL (TXPLL)
- Connection from the Reference Clock (REFCLK) to the Lanes

7.5.1 DRC - TXPLL to LANES Connectivity

A TXPLL_SSC can connect to all the lanes of a quad (shown in brown lines in the Placement View).

Figure 7-11. TXPLL Connection To All Four Lanes Before Placement

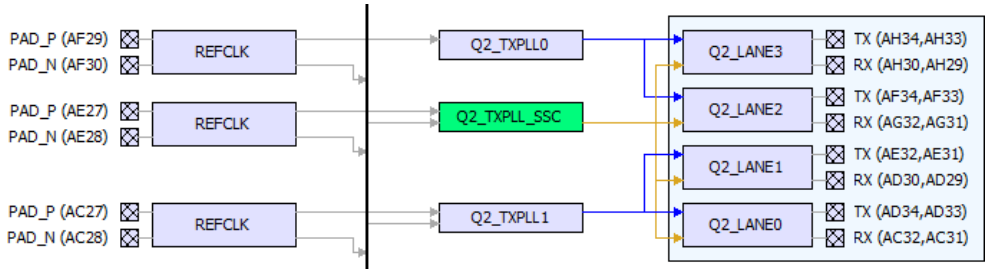
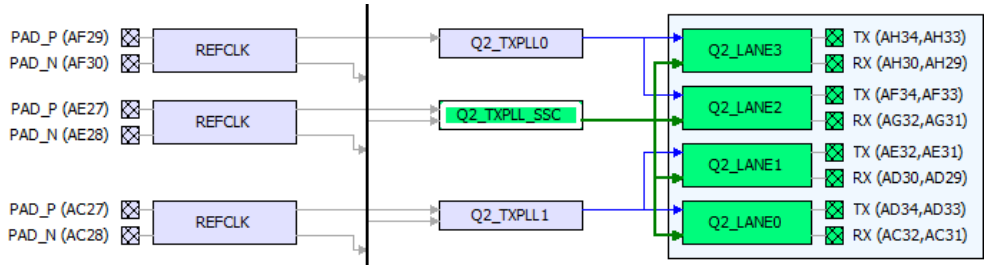


Figure 7-12. TXPLL Connection To All Four Lanes After Placement



A TXPLL (non-SSC) can connect to two lanes beside it normally (shown in blue lines in the Placement View)

Figure 7-13. TXPLL Connection To Two Lanes (Before Placement)

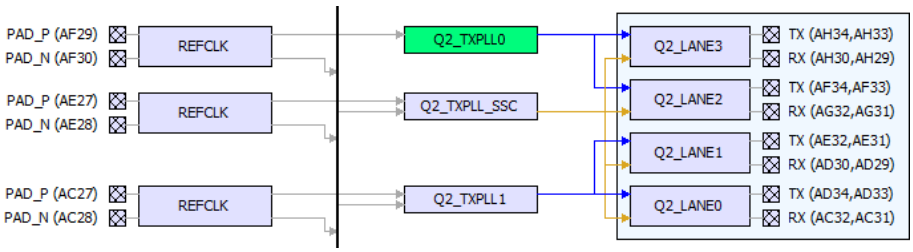


Figure 7-14. TXPLL Connection To Two Lanes (After Placement)

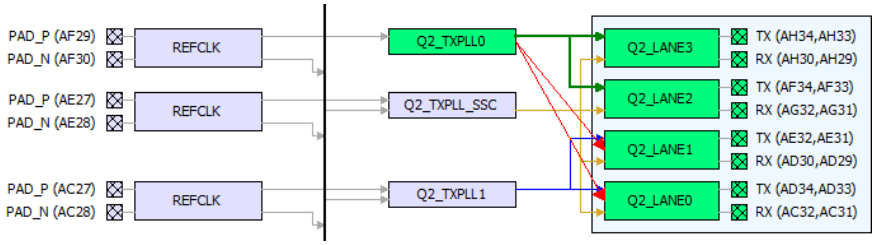


Figure 7-15. Q1_TXPLL1 to Four Lanes Connection (Before Placement)

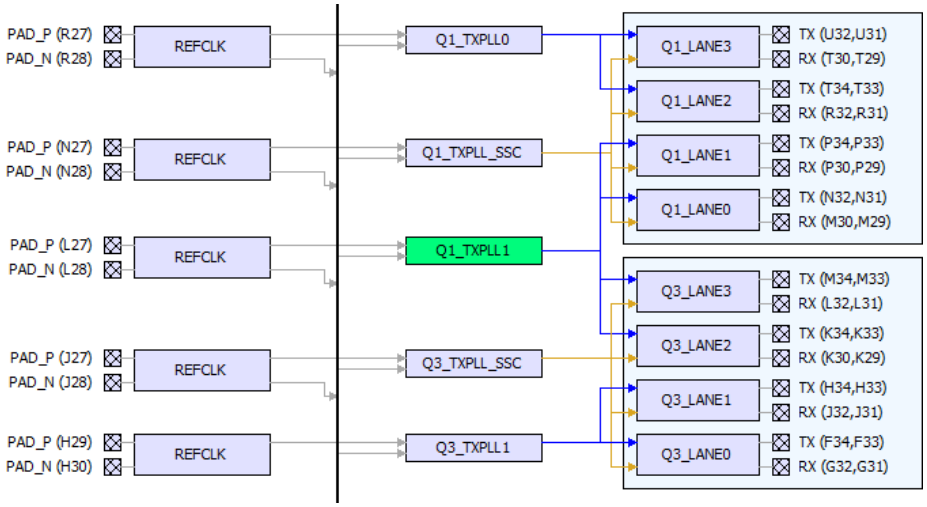
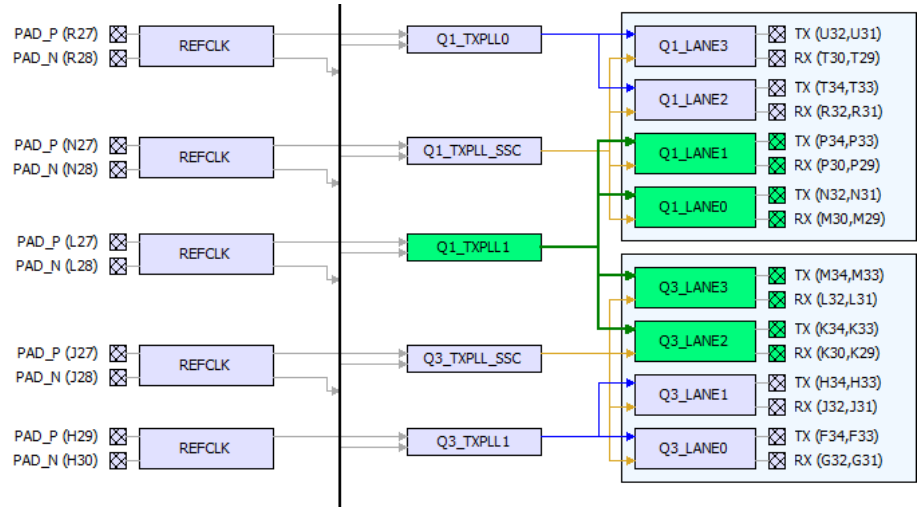


Figure 7-16. Q1_TXPLL1 to Four Lanes Connection (After Placement)

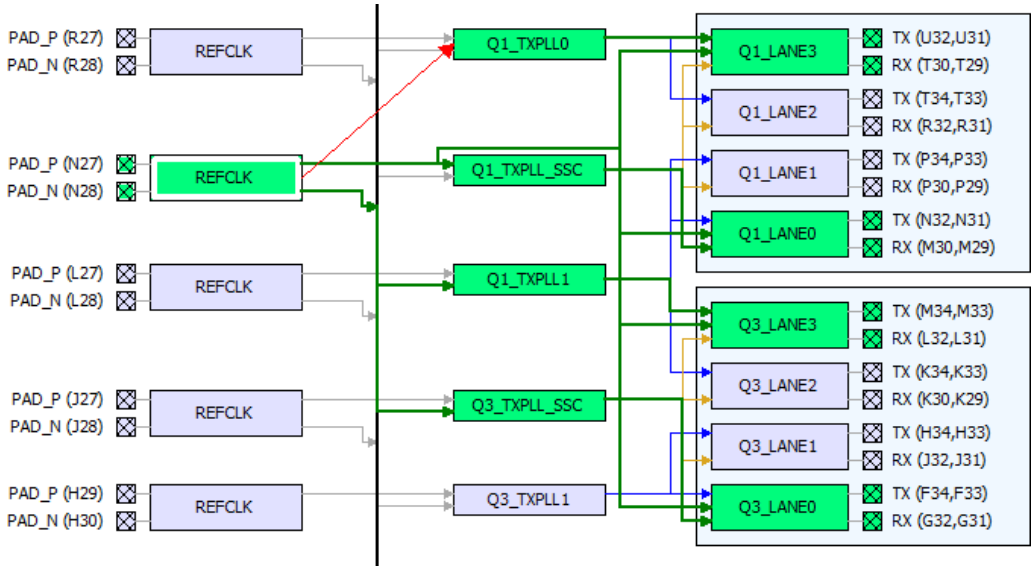


7.5.2 DRC - REFCLK to TXPLL Connectivity

A REFCLK can connect to all the TXPLLs beside and below it (down the Cascade Path) in the Placement View. A REFCLK cannot connect to a TXPLL above it (up the Cascade Path).

A cascade path (represented by the vertical line beside the REFCLKs) is used for the REFCLK to connect to all the TXPLLs below it and the Lanes below it in the Placement View.

Figure 7-17. Illegal Connection From REFCLK to TXPLL Up the Cascade Path

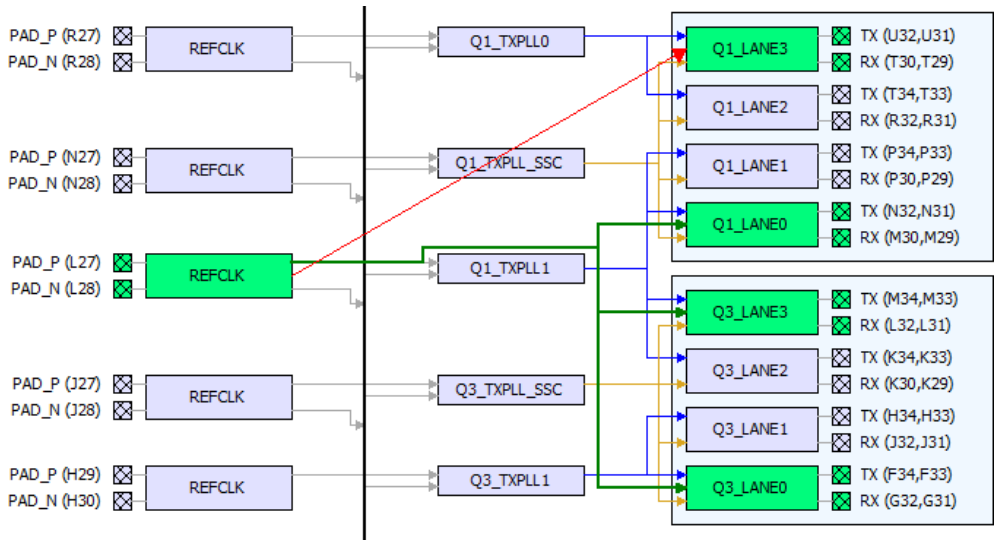


7.5.3 REFCLK to Lanes Connectivity

The REFCLK of a quad can connect to all Lanes of the TXPLL (in addition to that which the REFCLK can connect), as well as all the other Lanes below it (including from different quads). Connection up the Cascade path is illegal.

Green arrows indicate legal connection and red arrows indicate illegal connection from the REFCLK to the Lanes.

Figure 7-18. REFCLK to Lanes Connection - Legal (Down the Cascade Path) and Illegal (Up the Cascade Path)



8. IOD View

The IOD lane controller handles the complex operations necessary for the high-speed interfaces, such as DDR memory interfaces and CDR interfaces. To bridge the lane clock to the bank clock, the lane controller is used to control an I/O FIFO in each IOD. This I/O FIFO interfaces with DDR memory by utilizing the DQS strobe on the lane clock. The lane controller can also delay the lane clock using a PVT- calculated delay code from the DLL to provide a 90° shift. Certain I/O interfaces require a lane controller to handle the clock-domain that results with higher gear ratios.

The lane controller also provides the functionality for the IOD CDR. Using the four phases from the CCC PLL, the lane controller creates eight phases and selects the proper phase for the current input condition with the input data. A divided-down version of the recovered clock is provided to the fabric (DIVCLK).

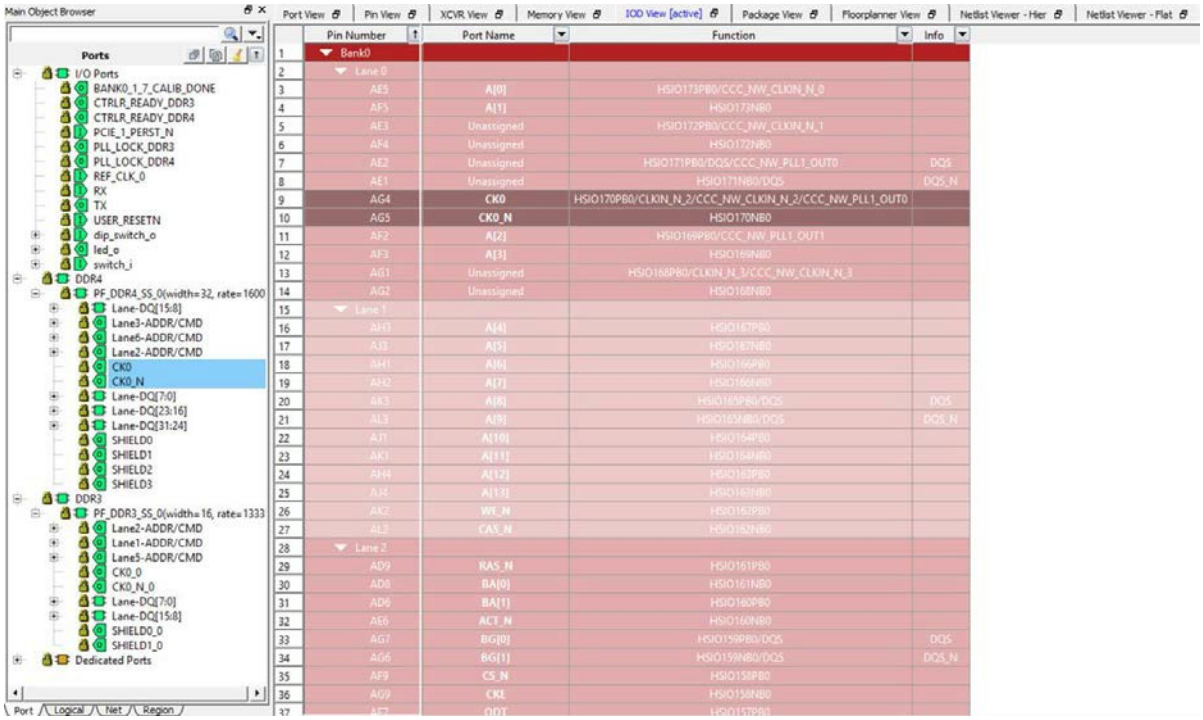
In the I/O Editor, the IOD View allows I/O assignments for IOD (I/O Digital) Interface blocks. Libero SoC currently supports CDR and RX_DDR_L_A/TX_DDR_G_A generic IOD interface. Future releases will add in more interfaces. The IOD views presents a hierarchical view of the generic IOD based on Bank and Lanes. In PolarFire silicon, there may be up to eight banks per chip and six lanes per bank. Bigger dies may have even more lanes per bank.

Note: The actual number of banks and the number of lanes per bank vary with the die.

When the I/O Editor opens the IOD view, it detects the specific IOD Interface standards, groups the I/Os into specific banks/lanes and populates the spreadsheet-like table with the I/O names (specific to the IOD Interface) accordingly.

See the following figure for an example of the IOD View.

Figure 8-1. IOD View



8.1 Generic I/O Assignments

Drag the I/O port from the Ports tab and drop it to the spreadsheet-like table to make the I/O assignment. The multi-line comment shows the locations where you can legally place the I/O port. Green indicates legal placements, and red indicates illegal placements. Illegal assignments are not allowed.

8.2 DRC Rules

The I/O Editor enforces the following list of common Design Rules Check (DRC) rules.

- All I/Os of the same logical lane must be placed within the same physical lane.
- For any one physical lane, only one logical lane is allowed to be placed.
- Non-logical lane I/Os can be placed in any physical lane.
- For RGMII Interface, the *_RXC port must be placed on the CLKIN_S_* side of the physical lane.
- When the CDR is placed in a physical lane, the DQS_N slot is reserved and is not available for I/O placement.

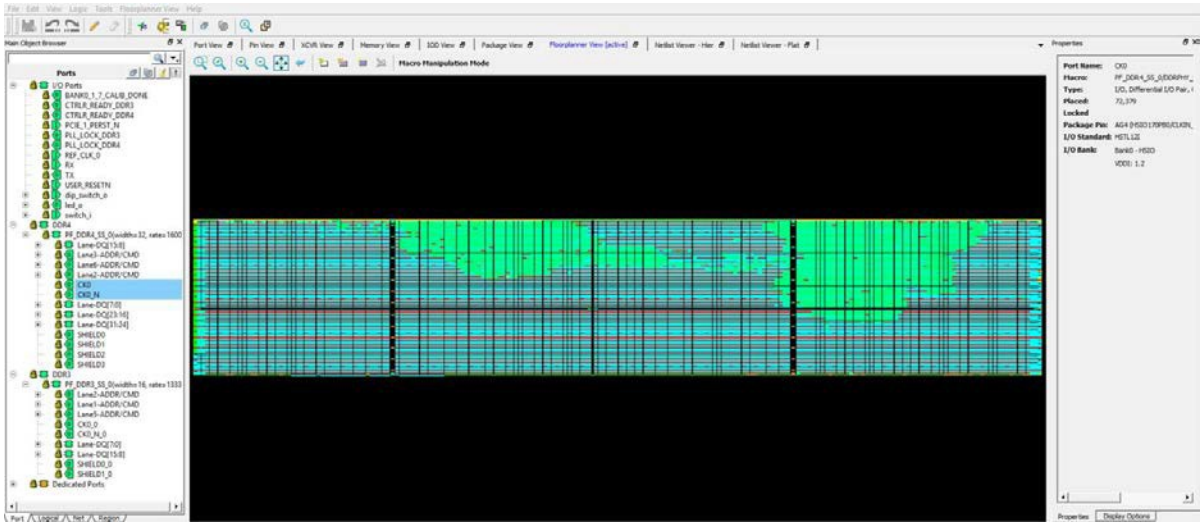
For more information on DRC rules for the IOD I/O placement, see UG0686: PolarFire FPGA User I/O User Guide.

9. Floorplanner View

The Floorplanner View displays all design elements in one window. The selections you make in the views are reflected in the window. The color scheme used in the canvas is dependent on the layers and colors you have selected in the Display Options window.

The following figure shows the Floorplanner View.

Figure 9-1. Floorplanner View



9.1 Operating Modes

The Floorplanner View has two operating modes. Click the **Macro Manipulation Mode** button to switch between Macro Manipulation Mode and Region Manipulation modes:

- Macro Manipulation Mode. Use this mode to work with macros, such as assigning macros to location or unassigning placed macros from locations. You can also view properties of selected macros in the Floorplanner View from the properties window. You can select multiple macros by pressing the **CTRL** key and selecting required macros.
- Region Manipulation Mode. Use this mode to work on regions such as resizing, renaming, or deleting regions, or assigning and unassigning macros or nets to regions.

9.1.1 Display Modes

The Display Options window allows you to customize the layout and the color settings for design elements on the Floorplanner View to meet your personal preferences.

There are three default layers and colors settings group:

- System
- Pin_Planner
- Grey_Scale

You can also see the colors for different component types (nets, modules, pins, etc.) in the Display Options window.

9.1.1.1 Selection

Clicking an item selects that one object in the model. However, you can select multiple items:

- To select contiguous items, click the first item you want to select, and then hold down the Shift key and click the last item you want to select. All items between the two are selected automatically.
- To select items that are not contiguous. click the first item. Then hold down the Ctrl key and click each additional item you want to select.

If you selected multiple items and then change your mind about a selected item, you can deselect the item by holding down the Ctrl key and clicking the item.

Selections follow a symmetrical behavior: If you select a port, all macros attached to it are selected as well. Similarly, if you select a pin object, all corresponding macro objects are also selected.

For example, if you select a port, the macro is also shown as selected. However, the property page still points to the port. Pin selection follows the same behavior.

9.1.1.2 Highlighting

Highlighting allows you to set persistent colors on designated macros, nets, or both.

To set a highlight, go to the Logical Object Browser, select one or more macros and/or components, and click the pencil in the following toolbar:

Figure 9-2. Pencil and Eraser Icons

When you set a highlight, all macros in the design are marked with the selected color. The color remains until you select one of the two middle eraser icons:

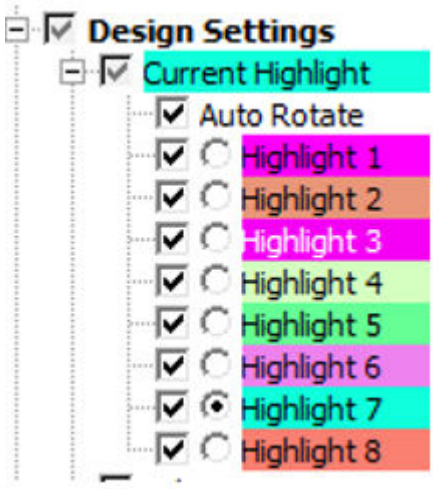
- The left eraser icon removes all highlights.
- The right eraser icon removes highlights only from selected items.

To set the highlights, use the **Current Highlight** check box at the top of the Design Settings docking window. Below this check box are an **Auto Rotate** check box, along with eight **Highlight** check boxes and radio buttons.

- Use the **Highlight** check boxes to enable or disable a highlight.
- Use the **Highlight** radio buttons to designate which highlight is active.

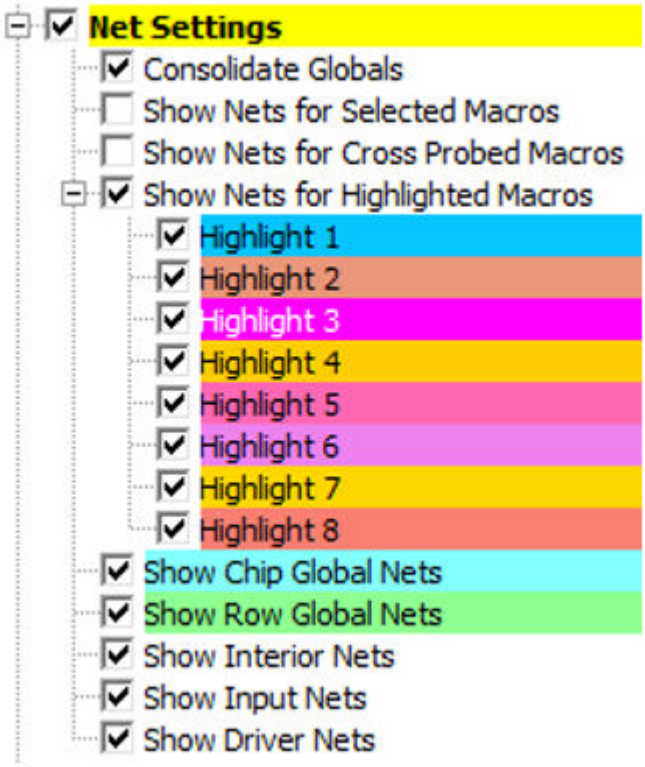
Note: You cannot disable the active highlight.

Figure 9-3. Design Settings Docking Window



The following figure exposes all options under **Nets**.

Figure 9-4. Design Settings Docking Window with All Nets Options Exposed



If **Net Settings** is disabled, all nets everywhere in the system are disabled, except for cross-probe nets. All options that are subordinate to that option are marked with a gray box to show that the option is not used. If the check box next to the **Show Nets for Selected Macros** check box is enabled, all nets are drawn for all macros and/or ports, as well as for the macros attached to selected pins in the net view.

If the **Show Nets for Highlighted Macros** check box is enabled, nets are enabled selectively for the macros or ports that have matching highlights. The nets are drawn in the color selected for this option, while the macros are displayed using the selected highlight color. This allows you to select different colors for macros and nets, so you can differentiate between them.

For example, if you check only **Highlight 5**, nets are drawn only for macros that are highlighted with the green **Highlight 5** option.

Consolidate Globals converts the raw clock display with globals connected to locals as if the sum of the local nets and the global nets are the same net. This is for display purposes only.
The bottom three options in the Design Settings docking window work with groups of macros and ports for which you want to calculate net lines as a single entity:

- **Show Interior Nets** shows lines that connect two different macros in the group.
- **Show Input Nets** shows lines that connect an output port of an exterior macro to one or more input pins in the group.
- **Show Driver Nets** shows drivers in the group that connect with an exterior macro

9.1.1.3 Cross Probing

When an external application performs a cross probe, the elements colored for cross probing and cross probe nets are always displayed, There are no options that allow cross probe to be disabled or turned off.

Any additional cross probes add to the current ones. To clear a cross probe state, use the rightmost eraser icon in the following toolbar.

Figure 9-5. Pencil and Eraser Icons

9.1.2 Floorplanner View Icons

The icons available across the top of the Floorplanner View window allows you to zoom in, zoom out, assign I/O banks, runs DRC checks, create regions for placement.

Figure 9-6. Floorplanner View Icons

The following table lists the functions of each icon.

Table 9-1. Floorplanner View Icons

Icon	Name	Function
	Rubber Band Zoom	Rubber Band Zoom - Drags out an area to enlarge/zoom into.
	Rubber Band Select	Rubber Band Select an area to Zoom into. Click in the Floorplanner View and drag the mouse to delineate an area. Release the mouse and all macros inside the delineated area are selected. Works in the Macro Manipulation Mode.
	Zoom In	Zoom In to canvas.
	Zoom Out	Zoom Out of canvas.
	Zoom to Fit	Zoom to fit the canvas size.
	Zoom to Location	Zoom to a Location Specified by X-Y co-ordinates.
	Zoom to fit Selection	Zoom to fit selected macros and ports. When enabled, the view attempts to center the view on the selected and placed ports.
	Check Design Rules	Run the Prelayout Checker, a preliminary check of the netlist for possible Place and Route issues.
	Check DRC Rules for Selected Interfaces	Check the DRC Rules for selected interfaces.
	I/O Bank Settings	Set the I/O bank to specific I/O Technology.
	Auto Assign I/O Bank	Run the Auto I/O Bank and Globals Assigner. Assigns a voltage to every I/O Bank that does not have a voltage assigned to it and if required, a VREF pin.

.....continued		
Icon	**Name**	**Function**
	Collapse Visible Views	Collapse the visible views.
	Expand Selected Items in Visible Views	Expand selected Items in the visible views.
	Create Empty	Create an empty user region.
	Create Inclusive	Create an inclusive user region.
	Create Exclusive	Create an Exclusive user region.
	Delete	Delete the selected user region.
	Show Nets For Macros	Show all nets connected to the macro. There are often many nets attached to the macro, and it is off by default.

An object or a collection of the objects in the Design View window can be selected and placed in any location that is legal.

The following figure shows an example of a successful placement into the Floorplanner View.

Figure 9-7. Floorplanner View - Successful Placement

The following figure shows an example of an unsuccessful placement attempt into the Floorplanner View.

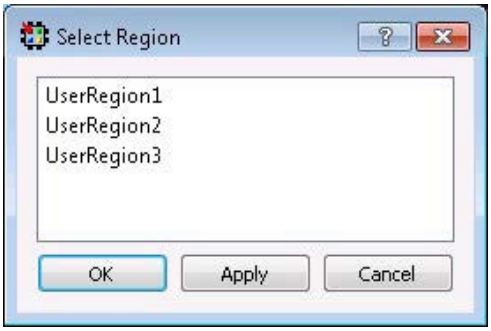
Figure 9-8. Floorplanner View - Unsuccessful Placement Attempt

9.1.3 Region Assignments

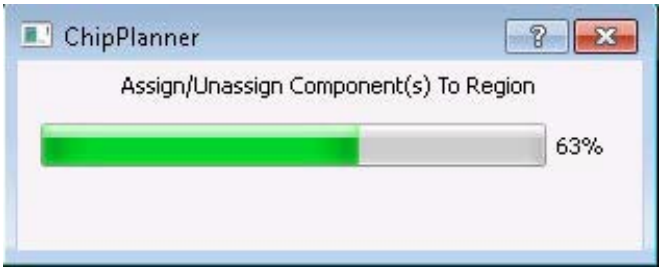
When you right-click an item in one of the tabs in the Main Object Browser, you can choose from available options, which can include placing an item to a location, unplacing an item from a location, locking the placement, and assigning a region.

Multiple items can be selected and assigned to the same region at the same time. You can also select a region assignment by right-clicking an item and choosing **Region Assign**. The dialog box shown below opens. This option is not available for objects in the Region tab.

Figure 9-9. Select Region Dialog Box



The progress of all Region Assign and Unassign commands is shown (see the example below).



Note: This dialog shows only the progress, and does not allow the user to cancel the operation. Closing the dialog does not terminate the operation.

9.2 Netlist Views

Two windows are available for viewing the netlist (a schematic view of the design used to trace the nets and debug) of the design.

- Post-Synthesis Hierarchical View (Netlist Viewer - Hier)
- Post-compile flattened Netlist View (Netlist Viewer - Flat)

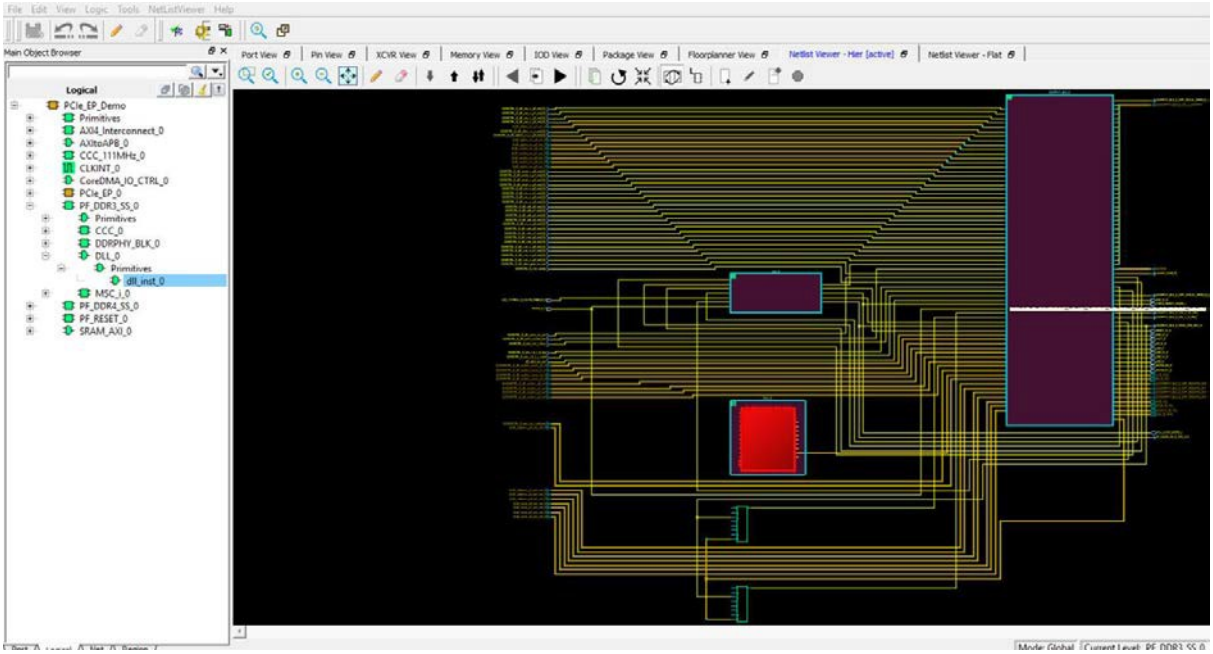
Separate tabs for Hierarchical View and Flattened Netlist View make it easy to switch between the different views.

9.2.1 Netlist Viewer - Hier

The Post-Synthesis Hierarchical View (Netlist Viewer - Hier) is a hierarchical view of the netlist after synthesis and after technology mapping to the Microchip FPGA technology. Click on the Canvas to load the 'Hierarchical view' in Nelist Viewer - Hier. The Chip Planner loads the netlist into the system memory and displays it in the window.

When the netlist is loaded for the first time into memory, a pop-up progress bar indicates the progress of the loading process, which may incur some runtime penalty for a large netlist.

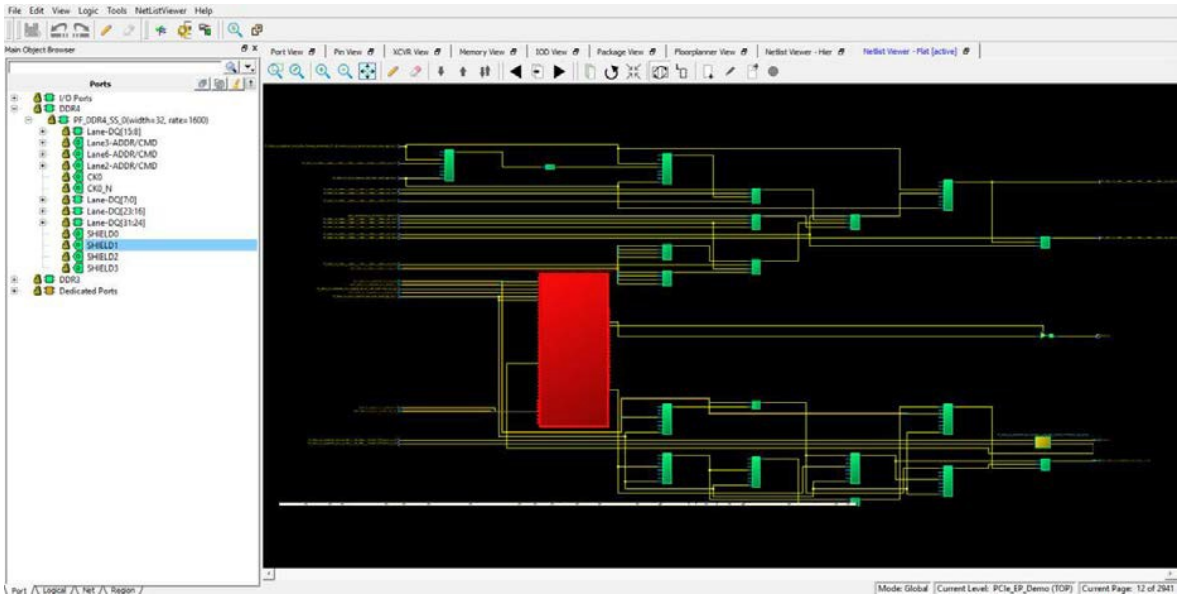
Figure 9-10. Netlist Viewer - Hier View



9.2.2 Netlist Viewer - Flat

This is the flattened (non-hierarchical) netlist generated after synthesis, technology mapping and further optimization based on the DRC rules of the device family and/or die. Click on the Canvas to load the 'Flat' view in the Netlist Viewer - Flat window. The Chip Planner loads the netlist into the system memory and displays it in the window as shown in the following figure.

Figure 9-11. Netlist Viewer - Flat View (Flattened Netlist)



9.2.2.1 Display Across Multiple Pages

Hierarchical or flattened netlists can span multiple pages, in which case the first page is displayed when it opens.

The current page number and the total number of pages are displayed in the status bar at the lower right corner of the window.

Figure 9-12. Status Bar

To go to different pages of the Netlist view, use the left-pointing arrow:

or the right-pointing arrow:

9.2.3 Netlist Viewer Features

See the Netlist Viewer User Guide for details about Netlist Viewer features.

9.2.4 Chip Planner Features

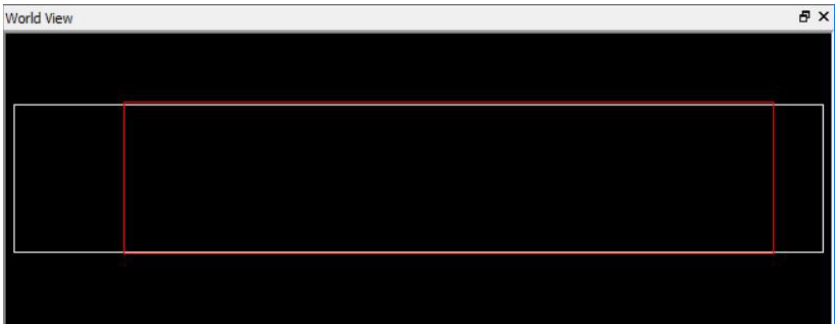
See the Chip Planner User Guide for details about Chip Planner features.

10. Other I/O Editor Windows

10.1 World View Window

The World View shows a red rectangle which reflects what is visible in the Floorplanner View in the context of the die. Changing what is visible in the canvas also changes the red rectangle. Changing the size or position of the red rectangle changes what is seen in the Floorplanner View.

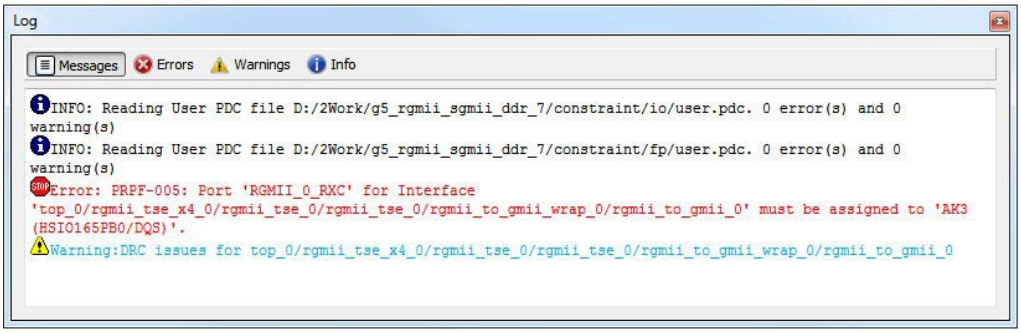
Figure 10-1. World View Window



10.2 Log Window

The Log window displays all messages generated by I/O Editor. You can filter the messages according to the type of message: Error, Warning, and Info. If you have made and saved changes in I/O Editor, the Log window displays the name and location of the PDC file(s) which have been edited/updated to reflect the changes.

Figure 10-2. Log Window



10.3 Object Window

The Object window (Main Object Browser) includes the following tabs:

- Port
- Logical
- Net
- Region

Press **Ctrl-F** to open a floating window for the active tab. See the following example.

Figure 10-3. Floating Object Window Tab Example

The following table lists the Object window icons.

Table 10-1. Object Window Icons

Description
Collapse everything in the tree.
Expand selected.
Clear the filter and refresh the tree reflecting no filters.
Change sort order and allow additional filtering.

10.4 Display Options Window

The Display Options window configures the display of the selected view. Three display options are available as follows:

- Fill Device Cells
- Use Cluster Mode
- Consolidate Globals

10.5 Properties Window

The Properties window displays the properties of the design elements. What is displayed in the Properties window is dependent on what is selected in the design view. Properties displayed may include the following, depending on the type of design elements:

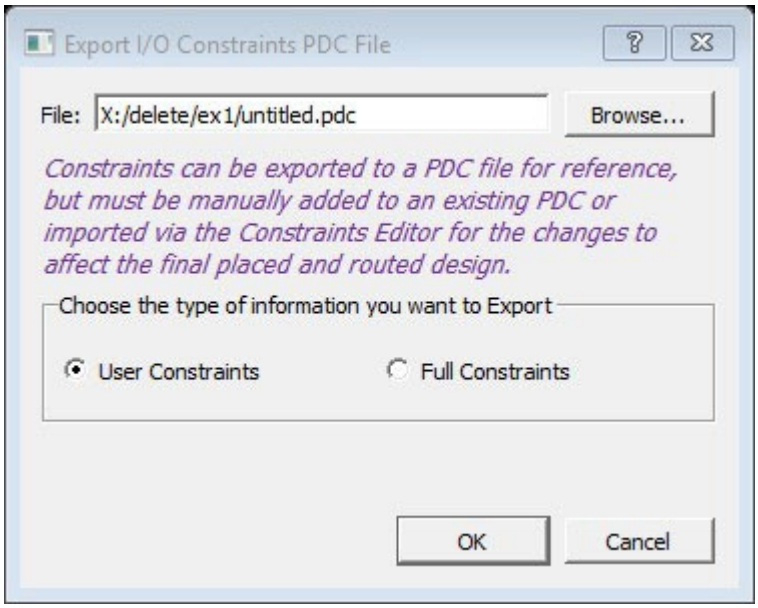
- Macro/Component Name - Full Macro or component name based on selection.
- Cell Type - Resource type based on design element selection.
- Placed (Location) - X-Y coordinates where device element is placed.
- Resource Usage Table - A table showing resources based on component and macro selection.
- Region Attached Table - A table showing region to which selected macro/component is assigned.
- User region (if any) to which it is attached.
- Nets Table - A table showing pins and nets which is associated with the selected macro along with fanout value.
- Locked/Unlocked (Placement) - The selected port is locked or unlocked.
- Port - Port name to which the I/O macro is assigned (only shown for I/O port macros).
- I/O Technology Standard - I/O Technology which is associated with the selected I/O macro (only shown for I/O port macros).
- I/O Bank- I/O bank to which the selected I/O macro is assigned (only shown for I/O port macros).
- Pin (Package Pin) - Pin to which the macro is assigned (only shown for I/O port macros).

Not all properties in the list are displayed. The list of displayed properties varies with the type of design element selected.

11. Export Physical Constraints (PDC)

The I/O Editor allows you to export the physical constraints (I/O Constraints and Floorplan Constraints) of the design in a PDC file to any file location on your disk. You can export the User constraints or the Full constraints of the design. The I/O PDC files can be exported (**File > Export Physical Constraint (PDC) > I/O Constraint**), as shown in the following figure.

Figure 11-1. Export I/O Constraints PDC File Dialog Box



The fp.pdc file can be exported (**File > Export Physical Constraint (PDC) > Floorplan Constraint**), as shown in the following figure.

Figure 11-2. Export Floorplanner Constraints PDC File Dialog Box

12. Appendix

This section describes the support for the PolarFire SoC MSS I/Os in the IO Editor in Libero SoC v12.5.

12.1 MSS I/O Placement

MSS I/O placement is done automatically as each port of the MSS has a fixed location on the package.

12.2 Bank Settings

Table 12-1. Bank Settings

Type of Bank	Bank Name	Supported Voltages
MSS_IO Peripheral IOs	Bank2	VDDI = 1.2 VDDI = 1.5 VDDI = 1.8 VDDI = 2.5 VDDI = 3.3
MSS_IO Peripheral IOs	Bank4	VDDI = 1.2 VDDI = 1.5 VDDI = 1.8 VDDI = 2.5 VDDI = 3.3
MSS_SGMII_IO RefClk and SGMII IOs	Bank5	VDDI = 2.5 VDDI = 3.3
MSS_DDR_IO DDR IOs	Bank6	DDR3. VDDI = 1.5 DDR3L. VDDI = 1.35 DDR4. VDDI = 1.2 LPDDR3. VDDI = 1.2 LPDDR4. VDDI = 1.1

12.3 IOSTD Support per Type of Bank

The following table lists the IOSTD support per type of bank.

Table 12-2. IOSTD Support per Type of Bank

Bank Type	IOSTDs
MSS_IO	LVCMOS12 LVCMOS15 LVCMOS18 LVCMOS25 LVCMOS33

.....continued	
Bank Type	**IOSTDs**
MSS_SGMII_IO	LVTTL PCI LVCMOS33 LVCMOS25 LVCMOS18 SSTL25I SSTL18I LVDS25 LVPECL33 LVDS33 RSDS25 RSDS33 MINILVDS25 MINILVDS33 SUBLVDS25 SUBLVDS33 PPDS25 PPDS33 LCMDS25 LCMDS33
MSS_DDR_IO	SSTL15I SSTL135I POD12I HSTL12I HSUL12I LVSTL11I

12.4 Port IOSTD Settings

The following table shows how I/O standards are computed.

Table 12-3. IOSTD Support per Type of Bank

Ports	IOSTDs
Peripherals on Bank4	1.2: LVCMOS22 1.5: LVCMOS15 1.8: LVCMOS18 2.5: LVCMOS25 3.3: LVCMOS33
Peripherals on Bank2	1.2: LVCMOS22 1.5: LVCMOS15 1.8: LVCMOS18 2.5: LVCMOS25 3.3: LVCMOS33

.....continued	
Ports	**IOSTDs**
REFCLK on Bank5	LVTTL PCI LVCMOS33 LVCMOS25 LVCMOS18 SSTL25I SSTL18I LVDS25 LVPECL33
SGMII on Bank5	LVDS25 LVDS33 RSDS25 RSDS33 MINILVDS25 MINILVDS33 SUBLVDS25 SUBLVDS33 PPDS25 PPDS33 LCMDS25 LCMDS33
DDR IOs on Bank6	DDR3: SSTI15I DDR3L: SSTL135I LPDDR3: HSUL12I LPDDR4: LVSTL11I DDR4 DQ/DQS/DM: POD12I

12.5 Updating the IO Banks and IOSTD

Users cannot update the I/O Bank setting or IOSTD of the MSS I/Os.

These settings apply to the software side in the XML. They do not affect the Libero project and are for the user's reference in ready-only format.

12.6 Designs without an MSS Macro

For designs without an MSS macro, the banks are not set and unlocked. Users can change the values, but the changes will not affect anything.

12.7 Default Bank Settings

If there is an MSS macro in the design and some interfaces are not used, this is the default bank settings that will be used.

Table 12-4. Default Bank Settings

Banks	Default Value
Bank2	VDDI = 3.3
Bank4	VDDI = 3.3

.....continued	
Banks	**Default Value**
Bank5	VDDI = 3.3
Bank6	VDDI = 1.5

12.8 PDC Setting

A PDC file is not needed for these I/Os because the settings from the MSS Configurator are being used. If the user specifies a correct placement and IO standard, the tool will accept the user's settings and will not error-out. But if the user tries to set any of the other specific MSS I/O attributes, it will fail. These constraints will not be written in the generated PDC file from the Chip Planner.

12.9 PolarFireSOC MSS I/O Attributes

These IO attributes are valid only for MSS IOs and are read only in the IO editor. These MSS IO attributes show up to the right side of the default IO attributes and will be visible even when there is no MSS being used in the design.

Reference Clock

The MSS IO attributes for Reference CLK that show up in the IO Editor are as follows:

MSS I/O Attributes	**Values**
MSS Resistor Pull	None, Up
MSS Clamp Diode	OFF, ON
MSS Persist	OFF, ON
MSS User I/O Lock Down	OFF, ON
MSS Odt (Ohm)	OFF, 100
MSS Thevenin (Ohm)	OFF, 150, 75, 50
MSS Schmitt Trigger	OFF, ON

Peripheral I/Os

The MSS IO attributes for Peripheral I/Os that show up in the IO Editor are as follows:

MSS I/O Attributes	**Values**
MSS Resistor Pull	None, Up, Down, Hold
MSS Clamp Diode	OFF, ON
MSS Persist	OFF, ON
MSS User I/O Lock Down	OFF, ON
MSS Schmitt Trigger	Schmitt Trigger is always ON for 1.2, 1.5 and 1.8 V IO Bank values. Otherwise, it can be either ON or OFF. The MSS Schmitt Trigger can have the below values:

	OFF, ON
MSS Low Power Mode Input Receiver	OFF, ON
MSS Low Power Mode Output Buffer	OFF, ON
MSS Output Drive (mA)	1.5, 2, 3, 3.5, 4, 6, 8, 10, 12, 16, 20, 24, 27, 30, 34, 40, 48, 60

DDR I/Os

The MSS IO attributes for DDR IOs that show up in the IO Editor are as follows:

Based on the memory type used, the below memory types have the following values:

- ODT DQ and ODT DQS ports

Memory Type	Value
DDR3/DDR3L	120, 60, 40, 30
DDR4	120, 80, 60, 40, 30
LPDDR3	240, 120, 80, 60, 40, 30
LPDDR4	120, 80, 60, 48, 40

- Outdrive for DQ and DM Ports, DQS Ports, CLK Ports, ADD/CMD Ports

Memory Type	Value (mA)
DDR3/DDR3L	48, 34, 30, 24
DDR4	60, 48, 34, 27
LPDDR3	60, 48, 40, 34
LPDDR4	60, 48, 40, 34

SGMII I/Os

The MSS IO attributes for SGMII that show up in the IO Editor are as follows:

MSS I/O Attributes	Values
MSS Resistor Pull	None, Up, Down, Hold
MSS Odt (Ohm)	OFF, 100
MSS Vcm Input Range	MID, LOW
MSS Source Termination (Ohm)	OFF, 100
MSS Output Drive (mA)	1.5, 2, 3, 3.5, 4, 6

13. Revision History

Revision	Date	Description
D	08/2021	Updated section 8.2 DRC Rules.
C	08/2021	Editorial updates and bug fixes.
B	04/2021	Added 2.13 Use I/O Calibration from the Lane section.
A	11/2020	Document is converted to Microchip format.
8.0	03/2020	Includes the following changes: • Revised the memory assignments for Memory View to examples such as DDR3/4,LPDDR3, and QDR • Revised the supported memory types to DDR3, DDR4, LPDDR3, and QDRI+
7.0	12/2019	Updated Resistor Pull information
6.0	08/2019	Updated to reflect latest software changes and added a new chapter about Export Physical Constraints (PDC)
5.0	12/2018	Updated document template and edited and updated text
4.0	05/2018	Includes the following changes: • Updated I/O information for Port and Pin Views • Minor edits for clarification about Package, XCVR, IOD, and Floorplanner Views
3.0	10/2017	Includes the following changes: • Added new chapter about Floorplanner View • Added new chapter about other windows • Updated I/O attribute information • Updated figures to reflect new tab order and naming • Added information about Signal Integrity View
2.0	05/2017	Updated Memory View and IOD View and updated graphics
1.0	01/2017	Initial Revision

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