PolarFire® and PolarFire SoC DRI User Guide

Introduction

Microchip's PolarFire FPGAs are the fifth-generation family of non-volatile FPGA devices, built on state-of-the-art 28 nm non-volatile process technology. PolarFire FPGAs deliver the lowest power at mid-range densities. PolarFire FPGAs lower the cost of mid-range FPGAs by integrating the industry’s lowest power FPGA fabric, lowest power 12.7 Gbps transceiver lane, built-in low power dual PCI Express Gen2 (EP/RP), and, on select data security (S) devices, an integrated low-power crypto co-processor.

Microchip's PolarFire SoC FPGAs are the fifth-generation family of non-volatile SoC FPGA devices, built on state-of-the-art 28 nm non-volatile process technology. The PolarFire SoC family offers industry's first RISC-V based SoC FPGAs capable of running Linux. The PolarFire SoC family combines a powerful 64-bit 5x core RISC-V Microprocessor Sub-System (MSS), based on SiFive’s U54-MC family, with the PolarFire FPGA fabric in a single device.

Dynamic Reconfiguration Interface (DRI) is an embedded bus within PolarFire and PolarFire SoC FPGAs. DRI is an APB target interconnect providing global access to the following embedded blocks:

- Transceiver lanes
- Transmit PLLs
- PLLs/DLLs (Clock conditioning circuitry or CCCs)

DRI allows modification of these embedded blocks at power-up and during operation. The embedded DRI bus provides dedicated connectivity and register mapped addressing to all the features as APB target peripherals. The DRI connectivity is a fixed dedicated resource that does not require any fabric logic or routing resources. Each transceiver and CCC supports a DRI, which can be enabled to configure its parameters without reprogramming the device. The transceiver, PCIESS, and CCC reconfiguration is controlled by volatile configuration registers that are loaded with values from the flash configuration bits at power-up. It is recommended to carefully use DRI because changing the factory or initialization settings can cause undesired results.

Note: DRI is not available to the user logic, when SmartDebug is being used for debugging.

The following table summarizes DRI access in both PolarFire and PolarFire SoC FPGAs.

Table 1. PolarFire and PolarFire SoC DRI

DRI Access	PolarFire	PolarFire SoC	Description
PF_DRI SgCore IP	✓	✓	The PF_DRI IP enables user access to the embedded APB target bus which provides a mirrored initiator APB target interface to the FPGA fabric. This IP can be used in both PolarFire and PolarFire SoC FPGAs. In PolarFire designs, the APB initiator can be implemented with the Mi-V soft processor IP or the CoreABC IP for controlling and accessing the DRI target peripherals. In PolarFire SoC designs, the APB initiator can be implemented with the PolarFire SoC MSS, the Mi-V soft processor IP, or the CoreABC IP for controlling and accessing the DRI target peripherals.

This user guide describes how DRI is used in PolarFire and PolarFire SoC FPGAs.

Note: AXI and APB protocol standards use the terminology "Manager" and "Subordinate". The equivalent Microchip terminology used in this document is "Initiator" and "Target" respectively.

References

- For detailed information about the PolarFire register map, see PolarFire Device Register Map.
- For detailed information about the PolarFire SoC register map, see PolarFire SoC Device Register Map.
- For more information about PolarFire SoC MSS, see PolarFire SoC FPGA MSS Technical Reference Manual.
- For more information about configuring PolarFire SoC MSS, see *PolarFire SoC Standalone MSS Configurator User Guide* available at www.microsemi.com/product-directory/soc-design-tools/5587-pfsoc-mss-configurator-tool#documents.

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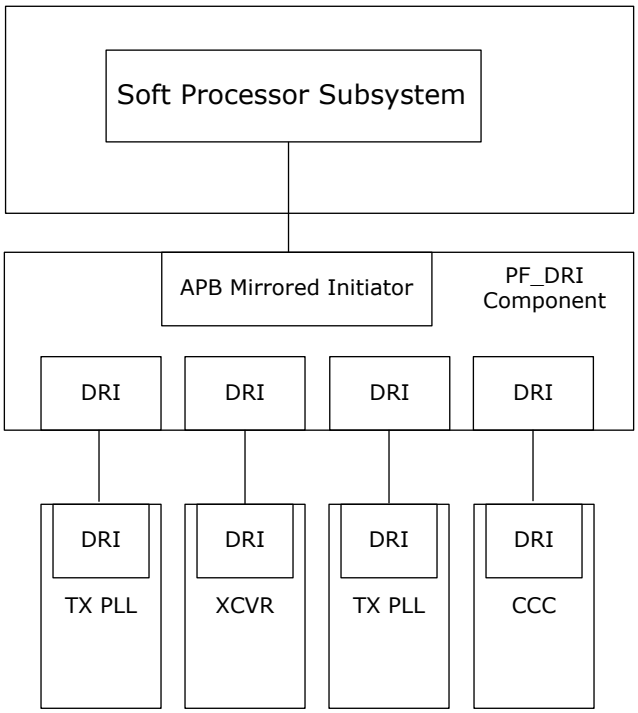
1. PolarFire FPGA DRI Use Model

The following figure shows the high-level block diagram of the DRI implementation in PolarFire devices.

Figure 1-1. High-level Block Diagram of DRI Implementation

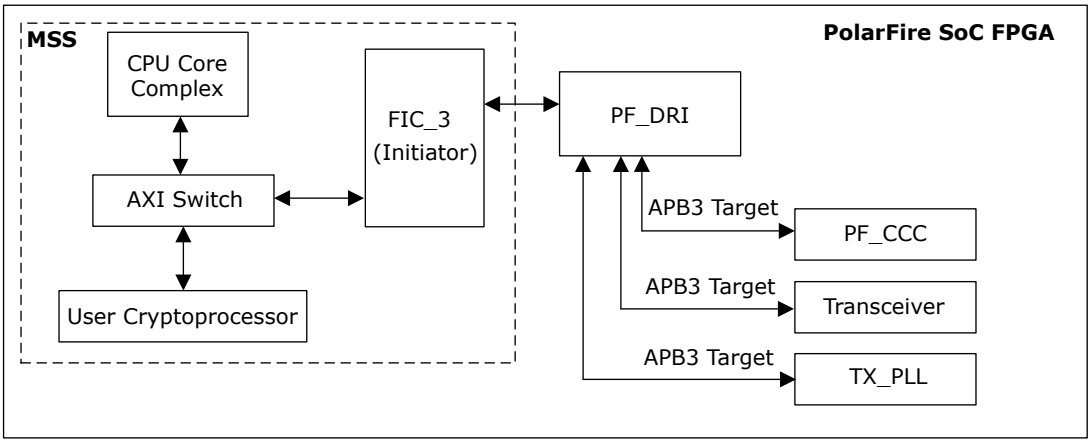


For information about the dynamic reconfiguration of transceiver and CCC using the PF_DRI IP, see AC475: PolarFire FPGA Dynamic Reconfiguration Interface Application Note.

2. PolarFire SoC FPGA DRI Block Diagram

In PolarFire SoC FPGAs, MSS accesses DRI via FIC_3 which is an APB interface. The following block diagram shows how DRI is accessed using the PF_DRI IP from the fabric in PolarFire SoC FPGAs.

Figure 2-1. DRI Accessed Using PF_DRI IP from Fabric



One of the processor cores is used to update the DRI registers of transceiver, CCC, and the TX PLL blocks via the FIC3 interface. For more information about configuring PolarFire SoC MSS, see PolarFire SoC Standalone MSS Configurator User Guide.

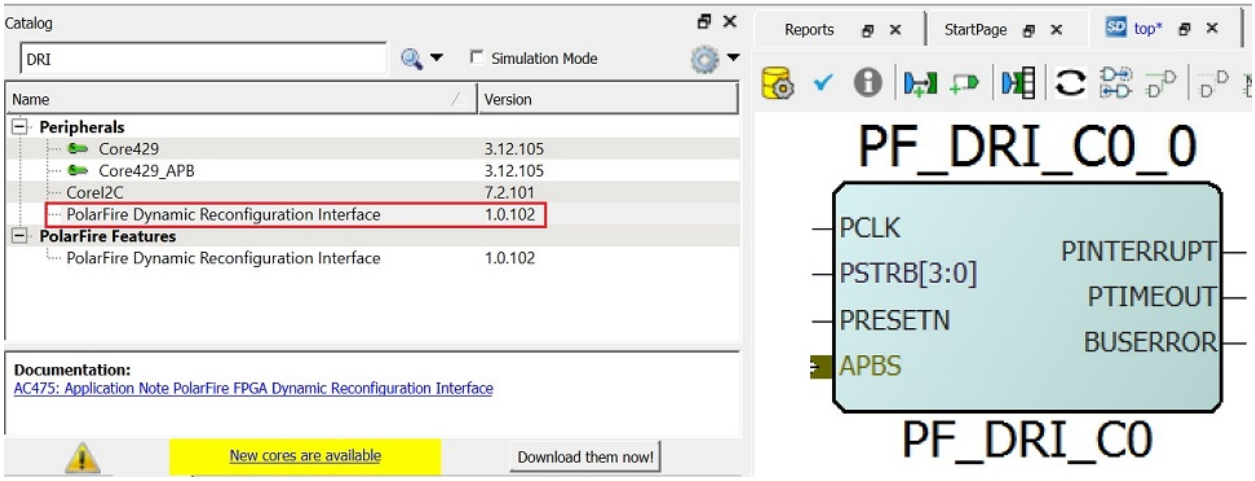
For detailed information about the PolarFire SoC register map, see PolarFire SoC Device Register Map.

For more information about updating the CCC PLL outputs dynamically using the PF_DRI IP, see PolarFire SoC Bare Metal DRI Application.

3. PF_DRI SgCore IP

PolarFire Dynamic Reconfiguration Interface (PF_DRI) SgCore IP is available in the **Catalog** under **Peripherals** as shown in the following figure.

Figure 3-1. The DRI IP with APB Interface



The following table lists the general ports of the PF_DRI SgCore.

Table 3-1. PF_DRI Ports

Port Name	Direction	Width	Description
PCLK	Input	1	Input clock source to DRI. This clock can be sourced from a CCC or an external oscillator. All transfers on the APB bus are clocked with respect to the rising edge of PCLK.
PSTRB[3:0]	Input	4	(Active-High) There is one write strobe for each byte of the write data (PWDATA 32-bit or 4 bytes). PSTRB signal indicates the byte lanes to be updated during a write transfer.
PRESETN	Input	1	(Active-Low) The APB Reset signal from the initiator.
PINTERRUPT	Output	1	(Active-High) Interrupt can be handled by a soft processor or can be handled by other user logic in the fabric. DRI_INTERRUPT is the source of the INTERRUPT.
PTIMEOUT	Output	1	(Active-High) Indicates to the fabric that the bus timed out (no response received). Time-out can occur when accessing a target that is not ready.
BUSERROR	Output	1	(Active-High) Indicates to the fabric that a bus error was detected. Once asserted, this error signal stays active until PRESETN is asserted. Bus error can occur if accessing locked or non-existent targets.

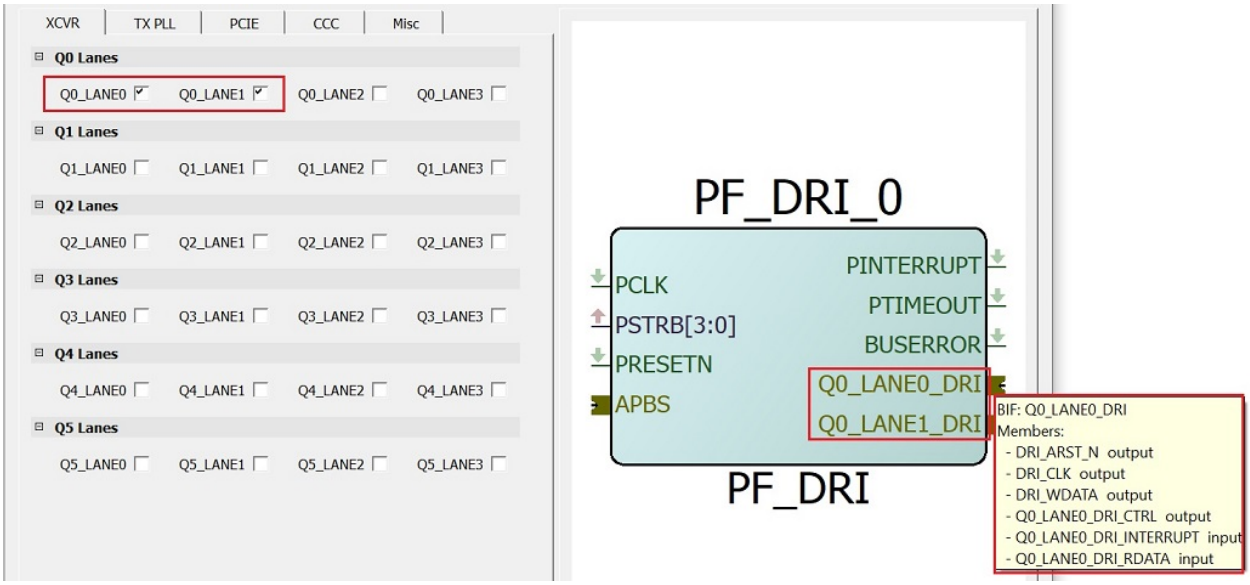
.....continued			
Port Name	**Direction**	**Width**	**Description**
APBS (APB Bus Interface bus signals)	—	—	The APBS port is connected to APB initiator. For example, CoreABC/Mi-V Soft Processor.
	PADDR (input)	29	This is the APB address bus driven by the initiator.
	PENABLE (input)	1	(Active-High) Enable signal from the initiator to trigger APB transfer.
	PRDATA (output)	32	The selected target drives this data to the initiator during read cycles when PWRITE is Low.
	PREADY (output)	1	(Active-High) This signal indicates that APB bus is ready for transfer to target. When PREADY is Low, the target initiates a transfer to DRI.
	PSEL (input)	1	(Active-High) The APB initiator generates this signal to each DRI target. Indicates that the target device is selected and that a data transfer is required. There is a PSELx signal for each target.
	PSLVERR (output)	1	(Active-High) This signal indicates a transfer failure.
	PWDATA (input)	32	(Active-High) This bus is driven by the APB initiator during write cycles when PWRITE is High.
	PWRITE (input)	1	This signal indicates an APB write access when High and an APB read access when Low.

The following sections describe DRI configuration for XCVR, TX PLL, PCIE, and CCC blocks using the **PolarFire Dynamic Reconfiguration Interface Configurator** window.

3.1 DRI Configuration for XCVR

In the XCVR tab, individual lanes (LANE_0 - 3) can be selected for each quad lane (Qn Lanes, n = 0 - 5) as shown in Figure 3-2. For example, when Q0_LANE0 and Q0_LANE1 lane check boxes are selected in Q0 Lanes, Q0_LANE0 and Q0_LANE1 ports are added to the DRI IP block as shown in Figure 3-2.

Figure 3-2. The XCVR Tab



The DRI ports highlighted in the preceding figure are routed through hardwired connections to the transceiver.

The following table describes the DRI ports.

Table 3-2. XCVR DRI Ports

Port Name	Libero BIF	Direction	Width	Description
DRI_ARST_N	—	Output	1	Active-Low asynchronous Reset signal from DRI to target.
DRI_CLK	—	Output	1	Clock source to the target.
DRI_WDATA	—	Output	32	DRI write data bus driven by DRI during write cycles.
Q#_LANE#_DRI_CTRL	Q#_LANE#_DRI	Output	[10:0]	Embedded connection to specified target peripheral. Q# can be 0, 1, 2, 3, 4, 5, LANE# can be 0, 1, 2, 3.
Q#_LANE#_DRI_INTERRUPT	Q#_LANE#_DRI	Input	—	Embedded connection to specified target peripheral. Q# can be 0, 1, 2, 3, 4, 5, LANE# can be 0, 1, 2, 3.
Q#_LANE#_DRI_RDATA	Q#_LANE#_DRI	Input	[32:0]	Embedded connection to specified target peripheral. Q# can be 0, 1, 2, 3, 4, 5, LANE# can be 0, 1, 2, 3.

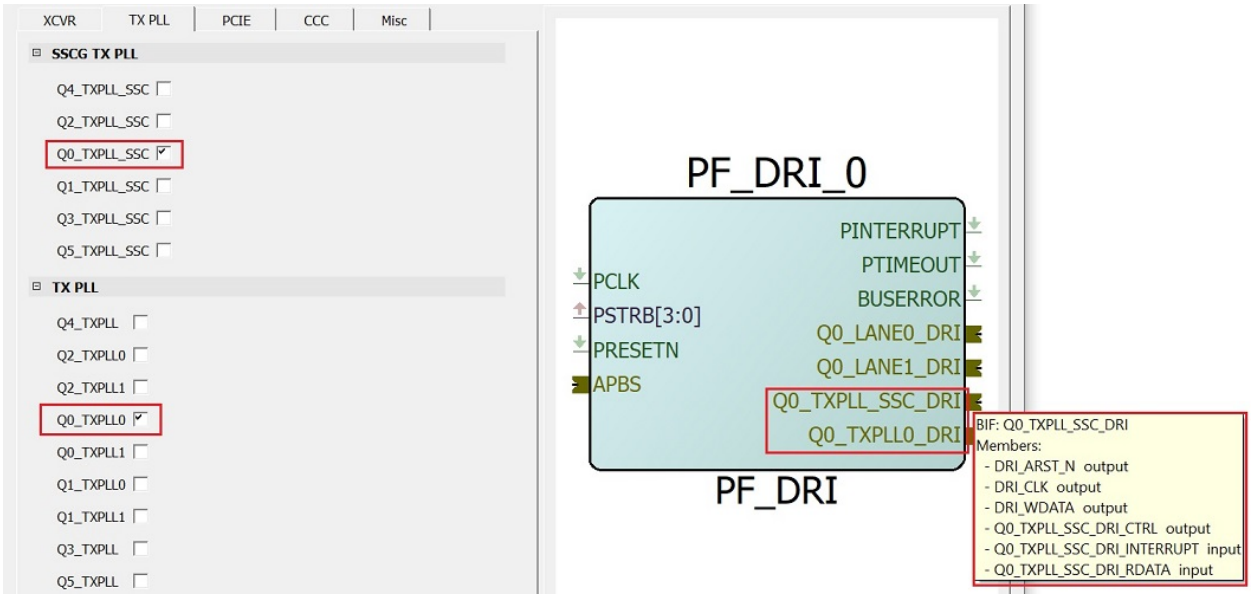
For more information about user connections required while using DRI interface, see AC475: PolarFire FPGA Dynamic Reconfiguration Interface Application Note.

3.2 DRI Configuration for TX PLL

In the TX PLL tab, the required options per quad to enable DRI for both spread spectrum generation capable transmit PLLs (Q#_TXPLL_SSC) and (Q#_TXPLLn) without spread spectrum capabilities can be selected as shown in Figure 3-3.

The DRI option is provided for two Q#_TXPLLn (Q#_TXPLL0, Q#_TXPLL1) within transceiver quad locations. For more information, see the “Transmit PLL” section in UG0677: PolarFire FPGA Transceiver User Guide.

Figure 3-3. The TX PLL Tab



The DRI target ports highlighted in the preceding figure are routed through hardwired connections to the transceiver PLL.

Table 3-3. TX PLL DRI Ports

Port Name	Libero BIF	Direction	Width	Description
Q#_TXPLL_SSC_DRI_CTRL	Q#_TXPLL_SSC_DRI	Output	[10:0]	Embedded connection to specified target peripheral. Q# can be 0, 1, 2, 3, 4, 5.
Q#_TXPLL_SSC_DRI_RDATA	Q#_TXPLL_SSC_DRI	Input	[32:0]	Embedded connection to specified target peripheral. Q# can be 0, 1, 2, 3, 4, 5.
Q#_TXPLL_SSC_DRI_INTERRUPT	Q#_TXPLL_SSC_DRI	Input	—	Embedded connection to specified target peripheral. Q# can be 0, 1, 2, 3, 4, 5.
Q#_TXPLL_DRI_CTRL	Q#_TXPLL_DRI	Output	[10:0]	Embedded connection to specified target peripheral. Q# can be 3, 4, 5.
Q#_TXPLL_DRI_RDATA	Q#_TXPLL_DRI	Input	[32:0]	Embedded connection to specified target peripheral. Q# can be 3, 4, 5.
Q#_TXPLL_DRI_INTERRUPT	Q#_TXPLL_DRI	Input	—	Embedded connection to specified target peripheral. Q# can be 3, 4, 5.
Q#_TXPLL0_DRI_CTRL	Q#_TXPLL0_DRI	Output	[10:0]	Embedded connection to specified target peripheral. Q# can be 0, 1, 2.
Q#_TXPLL0_DRI_RDATA	Q#_TXPLL0_DRI	Input	[32:0]	Embedded connection to specified target peripheral. Q# can be 0, 1, 2.
Q#_TXPLL0_DRI_INTERRUPT	Q#_TXPLL0_DRI	Input	—	Embedded connection to specified target peripheral. Q# can be 0, 1, 2.
Q#_TXPLL1_DRI_CTRL	Q#_TXPLL1_DRI	Output	[10:0]	Embedded connection to specified target peripheral. Q# can be 0, 1, 2.
Q#_TXPLL1_DRI_RDATA	Q#_TXPLL1_DRI	Input	[32:0]	Embedded connection to specified target peripheral. Q# can be 0, 1, 2.
Q#_TXPLL1_DRI_INTERRUPT	Q#_TXPLL1_DRI	Input	—	Embedded connection to specified target peripheral. Q# can be 0, 1, 2.

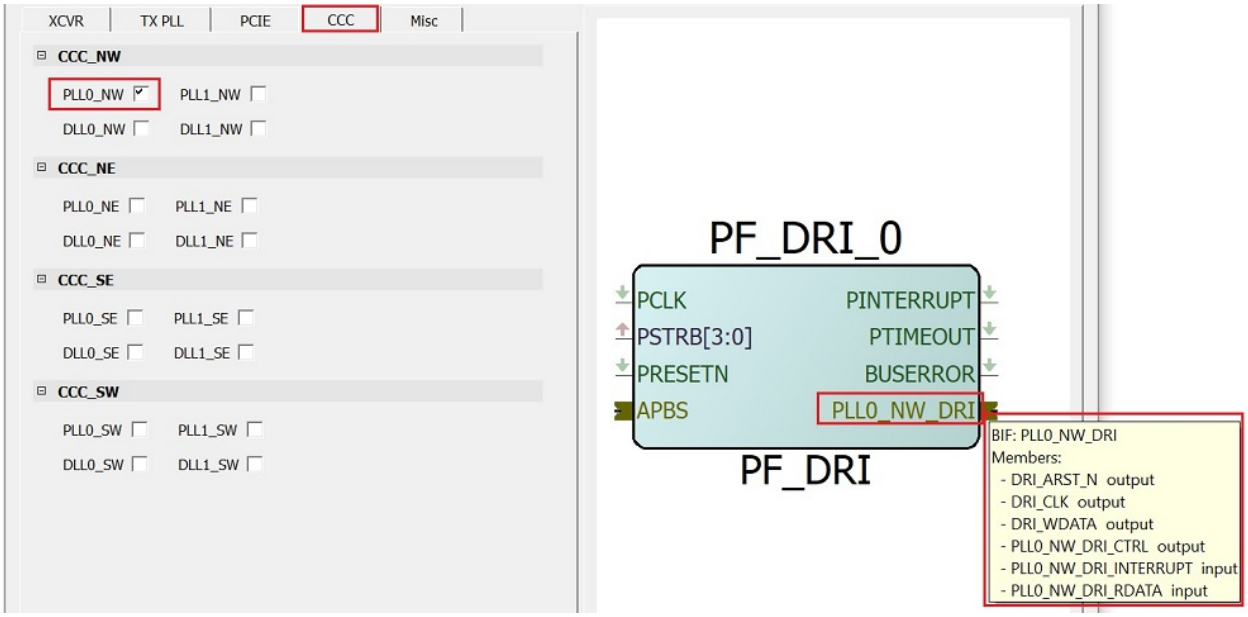
3.3 DRI Configuration for PCIE

PCIE controllers do not connect directly to a DRI port, the associated XCVR lanes must be connected to the DRI for dynamic control of the XCVR features. The PCIE controllers have a dedicated APB port for access to the register control within the PCIE subsystem. For more information, see UG0685: PolarFire FPGA PCI Express User Guide.

3.4 DRI Configuration for CCC

In the CCC tab, the required PLLs and DLLs (in all four corners NW, NE, SE, and SW) can be selected to enable DRI on the selected options and the corresponding DRI target interface is exposed as shown in the following figure.

Figure 3-4. The CCC Tab



The DRI target ports highlighted in the preceding figure are routed through hardwired connections to the CCC.

The following table lists the CCC DRI ports.

Table 3-4. CCC DRI Ports

Port Name	Libero BIF	Direction	Width	Description
PLL0_**_DRI_CTRL	PLL0_**_DRI	Output	[10:0]	Embedded connection to specified target peripheral. ** can be NW, NE, SW, SE.
PLL0_**_DRI_RDATA	PLL0_**_DRI	Input	[32:0]	Embedded connection to specified target peripheral. ** can be NW, NE, SW, SE.
PLL0_**_DRI_INTERRUPT	PLL0_**_DRI	Input	—	Embedded connection to specified target peripheral. ** can be NW, NE, SW, SE.
PLL1_**_DRI_CTRL	PLL1_**_DRI	Output	[10:0]	Embedded connection to specified target peripheral. ** can be NW, NE, SW, SE.
PLL1_**_DRI_RDATA	PLL1_**_DRI	Input	[32:0]	Embedded connection to specified Target peripheral. ** can be NW, NE, SW, SE.
PLL1_**_DRI_INTERRUPT	PLL1_**_DRI	Input	—	Embedded connection to specified target peripheral. ** can be NW, NE, SW, SE.
DLL0_**_DRI_CTRL	DLL0_**_DRI	Output	[10:0]	Embedded connection to specified target peripheral. ** can be NW, NE, SW, SE.
DLL0_**_DRI_RDATA	DLL0_**_DRI	Input	[32:0]	Embedded connection to specified target peripheral. ** can be NW, NE, SW, SE.

.....continued				
Port Name	**Libero BIF**	**Direction**	**Width**	**Description**
DLL0_**_DRI_INTERRUPT	DLL0_**_DRI	Input	—	Embedded connection to specified target peripheral. ** can be NW, NE, SW, SE.
DLL1_**_DRI_CTRL	DLL1_**_DRI	Output	[10:0]	Embedded connection to specified target peripheral. ** can be NW, NE, SW, SE.
DLL1_**_DRI_RDATA	DLL1_**_DRI	Input	[32:0]	Embedded connection to specified target peripheral. ** can be NW, NE, SW, SE.
DLL1_**_DRI_INTERRUPT	DLL1_**_DRI	Input	—	Embedded connection to specified target peripheral. ** can be NW, NE, SW, SE.

3.4.1 Dynamic Configuration of CCC

Each CCC has a DRI which can be enabled to configure CCC parameters without reprogramming the device. The CCC configuration is controlled by the volatile configuration registers that are loaded with values from the flash configuration bits at power-up. An APB bus initiator must be interfaced to the CCC using a DRI macro for dynamic configuration. The APB bus initiator is used to dynamically modify the CCC configuration register values as per design needs. For more information on CCC configuration registers and their bit definitions, see PolarFire Device Register Map.

To meet all the datasheet specifications, certain requirements must be met when configuring the PLL/DLL parameters. The Libero CCC configurator implements all these requirements and creates a valid solution for the requested output clock frequencies and phases. Hence, Microchip recommends that users generate the required configuration using Libero CCC configurator and use the generated parameters in their dynamic configuration solution.

The PLL_POWERDOWN_N input must be asserted before making changes to the PLL configuration parameters.

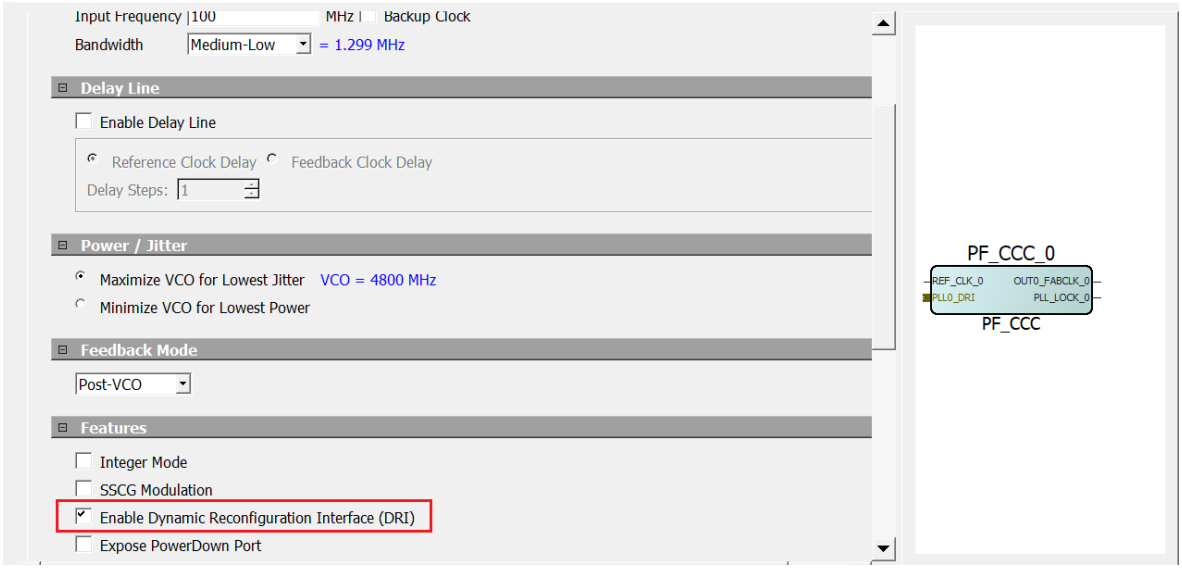
Note: Asserting the PLL_POWERDOWN_N signal resets the PLL operation.

When the CCC is configured in internal Post-VCO feedback mode, if the requirement is to change the phase or output divider configuration then the clock start/stop (OUT#_EN) signals can be used to stop the clock output before making the changes for a glitch free configuration.

The following steps describe how to perform dynamic configuration of CCC:

1. Select **Enable Dynamic Reconfiguration Interface** under the **Features** section of CCC configurator as shown in Figure 3-5.

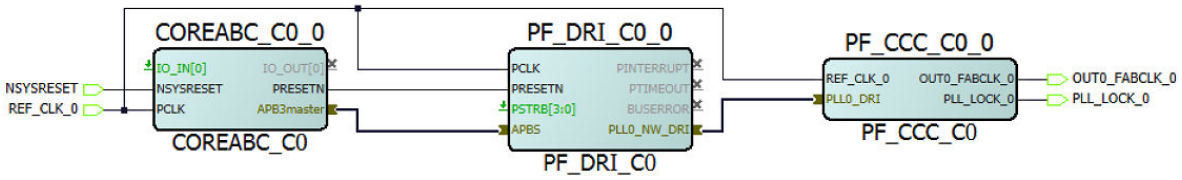
Figure 3-5. DRI Option in CCC



This enables and exposes the DRI on the instantiated CCC component as shown in the above figure.

2. Instantiate and configure a PF_DRI SgCore with the required PLL enabled into the SmartDesign. The dynamic reconfiguration interface macro converts the APB interface signals to CCC dynamic reconfiguration interface signals. The DRI interface for the selected PLL is exposed on the PF_DRI macro. The APB port of DRI are shown in Figure 3-4. The DRI ports cannot be monitored or altered in the Libero design. These ports are used to facilitate HDL simulation of changes made to the CCC over the DRI. The PF_DRI SgCore converts standard APB3 read/writes to DRI transactions.
3. Double click the DRI macro to configure.
4. In the PF_DRI configurator, under the CCC tab, select the PLLs and DLLs that need dynamic configuration. The DRI macro interface is shown in Figure 3-4.
5. Connect the APB initiator port from an APB initiator (for example, CoreABC) to the mirrored initiator port of PF_DRI as shown in the following figure.

Figure 3-6. CCC Dynamic Configuration System

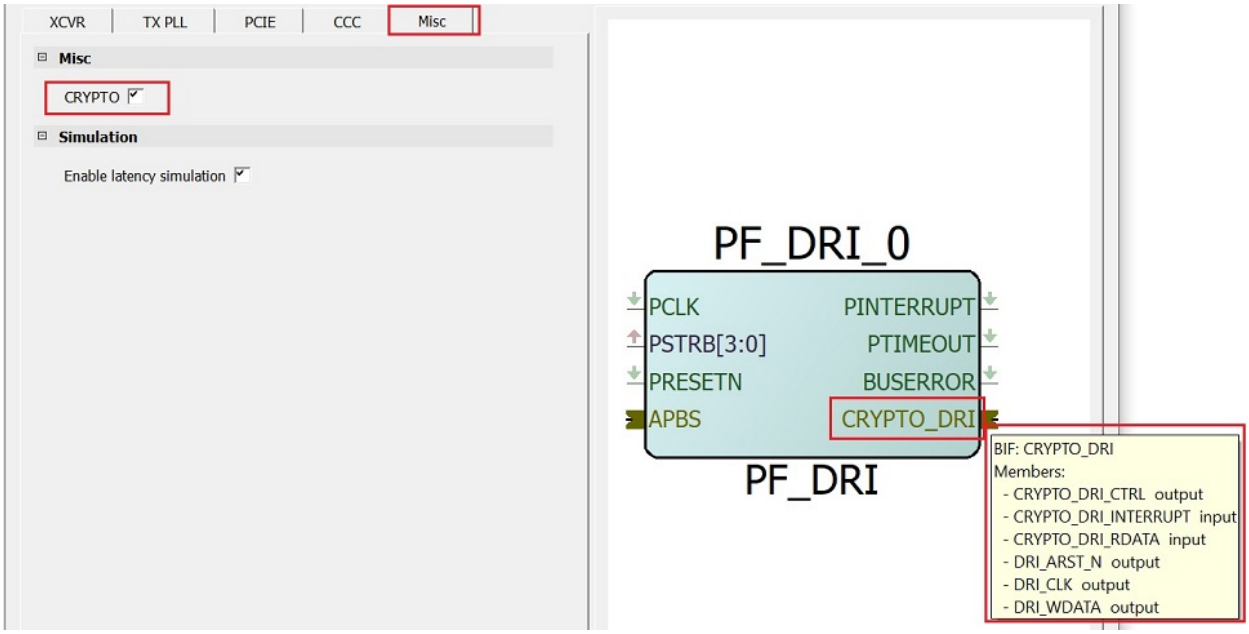


3.5 Misc Tab

In the Misc tab, the **CRYPTO** option can be selected to enable DRI on CRYPTO as shown in Figure 3-7.

Note: The **Enable latency simulation** option is currently not supported.

Figure 3-7. Enabling DRI on CRYPTO



The following table lists the CRYPTO DRI ports.

Table 3-5. CRYPTO DRI Ports

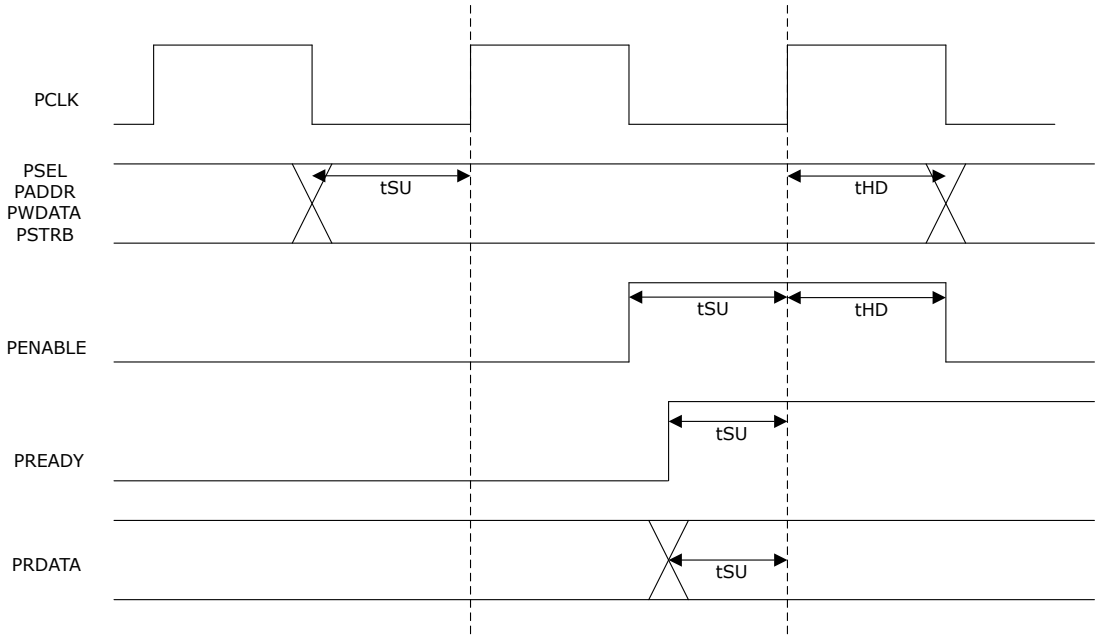
Port Name	Libero BIF	Direction	Width	Description
CRYPTO_DRI_CTRL	CRYPTO_DRI	Output	[10:0]	Embedded connection to specified target peripheral.
CRYPTO_DRI_RDATA	CRYPTO_DRI	Input	[32:0]	Embedded connection to specified target peripheral.
CRYPTO_DRI_INTERRUPT	CRYPTO_DRI	Input	—	Embedded connection to specified target peripheral.

Note: The ports highlighted in the above table are routed through hardwired connections to the User Crypto Processor.

3.6 Functional Timing Diagram

Figure 3-8 shows the DRI timing diagram.

Figure 3-8. APB Initiator Timing Diagram



For more information about FPD_PCLK, see DS0141: PolarFire FPGA Datasheet.

The SDC constraint is derived and generated automatically based on the connection of the PF_DRI IP to its APB initiator and to the DRI peripherals. Static Timing Analysis (STA) of PCLK (FPD_PCLK) with SmartPower gives the minimum and maximum analysis of the APB interface tSU/tHD parameters.

4. Revision History

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	06/2021	The first publication of this document.

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