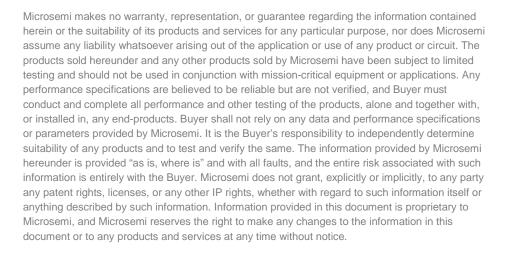
# **SmartPower User Guide**

# Libero SoC v11.8, v11.8 SP1, SP2, and SP3

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# Welcome to SmartPower

Welcome to SmartPower, the Microsemi SoC state-of-the-art power analysis tool. SmartPower enables you to globally and in-depth visualize power consumption and potential power consumption problems within your design, so you can make adjustments – when possible – to reduce power.

SmartPower provides a detailed and accurate way to analyze designs for Microsemi SoC FPGAs: from toplevel summaries to deep down specific functions within the design, such as gates, nets, IOs, memories, clock domains, blocks, and power supply rails.

You can analyze the hierarchy of block instances and specific instances within a hierarchy, and each can be broken down in different ways to show the respective power consumption of the component pieces.

SmartPower also analyses power by functional modes, such as Active, Flash\*Freeze, Shutdown, Sleep, or Static, depending on the specific FPGA family used. You can also create custom modes that may have been created in the design. Custom modes can also be used for testing "what if" potential operating modes.

SmartPower has a very unique feature that enables you to create test scenario profiles. A profile enables you to create sets of operational modes, so you can understand the average power consumed by this combination of functional modes. An example may be a combination of Active, Sleep, and Flash\*Freeze modes – as would be used over time in an actual application.

SmartPower generates detailed hierarchical reports of the power consumption of a design for easy evaluation. This enables you to locate the power consumption source and take appropriate action to reduce the power if possible.

SmartPower supports use of files in the Value-Change Dump (VCD) format, as specified in the IEEE 1364 standard, generated by the simulation runs. Support for this format lets you generate switching activity information from Model *Sim* or other simulators, and then utilize the switching activity-over-time results to evaluate average and peak power consumption for your design.



# **Starting SmartPower**

Note: When you launch SmartPower, you must first set your target clock and data frequencies before you evaluate your power consumption.

You cannot launch SmartPower if your design is not in a post-layout state in Designer. If you invoke SmartPower before compiling your netlist, Designer guides you through the compile and layout process.

There are three ways to invoke the SmartPower analysis tool:

- Choose SmartPower from the Tools menu.
- Click the **SmartPower** icon in the Designer toolbar.
- Click the SmartPower button in Designer design flow.

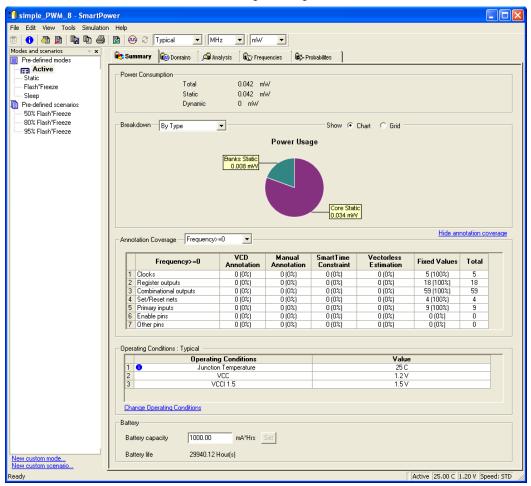


Figure 1 · SmartPower User Interface

# **SmartPower Interface**

# Summary Tab

The Summary tab is divided into five sections: Power Consumption, Breakdown, Annotation Coverage, Operating Conditions, and Battery Life.

-	Sumr	<b>mary</b> 📦 Domains 🗌 🗯 An	alysis 🛛 👘 Frequ	uencies 🛛 🔒 Pr	obabilites ]				
-Po	wer	Consumption							
		Total	0.042 m <sup>v</sup>	W					
		Static	0.042 m <sup>v</sup>	W					
		Dynamic	0 mW						
Bre	Breakdown By Type Show © Chart C Grid								
	Power Usage								
Banks Static 0.008 mVV Core Static 0.034 mVV									
							Little and	notation coverage	
An	nota	ation Coverage — Frequency>	=0 💌					Intation Coverage	
ſ			VCD	Manual	SmartTime	Vectorless			
		Frequency>=0	Annotation	Annotation	Constraint	Estimation	Fixed Values	Total	
	1 0	Clocks	0 (0%)	0 (0%)	0 (0%)	0 (0%)	5 (100%)	5	
	2 F	Register outputs	0 (0%)	0 (0%)	0 (0%)	0 (0%)	18 (100%)	18	
	3 0	Combinational outputs	0 (0%)	0 (0%)	0 (0%)	0 (0%)	59 (100%)	59	
	4 9	Set/Reset nets	0 (0%)	0 (0%)	0 (0%)	0 (0%)	4 (100%)	4	
	5 F	Primary inputs	0 (0%)	0 (0%)	0 (0%)	0 (0%)	9 (100%)	9	
	6 E	Enable pins	0 (0%)	0 (0%)	0 (0%)	0 (0%)	0 (0%)	0	
	7 (	Other pins	0 (0%)	0 (0%)	0 (0%)	0 (0%)	0 (0%)	0	
Operating Conditions : Typical									
- Op	erati								
Ē		Operatin	g Conditions			Value			
F	1	Operating Junction	n Temperature			25 C			
	1 (	Operating Junction	n Temperature VCC			25 C 1.2 V			
	1	Operating Junction	n Temperature			25 C			
	1 ( 2 3	Operating Junction VC	n Temperature VCC			25 C 1.2 V			
	1 ( 2 3	Operating Junction	n Temperature VCC			25 C 1.2 V			
	1 ( 2 3	Operating D Junction VC Ige Operating Conditions	n Temperature VCC			25 C 1.2 V			
Ba	1 Chan	Operating D Junction VC Ige Operating Conditions	n Temperature VCC	Bet		25 C 1.2 V			

Figure 2 · SmartPower Summary Tab

### **Power Consumption**

Displays the total power consumption and the static and dynamic power of the design. (Accurate only after you have entered your target clock and data frequencies).

### **Breakdown**

Displays a breakdown of power consumption in the design. You can specify whether to see the power breakdown by type of component, by voltage rail, or by clock domain from the drop-down list.



### Show

Displays power usage as a chart or as a grid.

When you select **By Type** from the drop-down list, the **Summary** tab displays a breakdown of the design's power usage by the following types:

- Net
- Gate
- I/O
- Memory
- Core Static
- Banks Static
- Analog (for Fusion Designs)

Any static power used by instances of a component in a design will be included in the appropriate category. As a result, the sum of the power in breakdown by type will equal the total of the static and dynamic power consumption of the design. Percentages displayed are fractions of the total power. Global nets are included in the net power types. To obtain the power of a clock, select breakdown by clock domain.

When you select **By Rail** from the drop-down list, the Summary tab displays a breakdown of the power usage by the rail that the power is drawn from and a breakdown for the current usage. For each rail, the power, voltage, and current drawn are displayed.

When you select **By Clock Domain** from the drop-down list, the Summary tab displays a breakdown of the power usage by the clock domain that the power is drawn from. For each clock domain, the power and percentage of power drawn are displayed. Dynamic power is accounted for in breakdown by clock, but static power is not associated by any clock.

When you select **By Mode** — available only when a <u>scenario is selected</u> in the Modes and Scenarios toolbar — the Summary tab displays power consumption, duration and power duration weight by mode.

Whether you selected **By Type**, **By Rail**, **By Mode**, or **By Clock Domain**, you can customize which columns are displayed in the grid by right-clicking the column headers. To exclude a column, remove its checkmark from the right-click menu. Right-click a column header to set the column default size for the selected column or for all columns, sort the values in ascending or descending order, or customize columns.

To sort the contents of a column, double-click a column header.

To export the contents of the grid to a file, from the **File** menu, choose **Export Grid** or click its associated toolbar button.

To print the grid, from the File menu, choose Print Grid or click its associated toolbar button.

To copy the grid, from the Edit menu, choose Copy Grid or click its toolbar button.

To copy the chart, click the contents of the chart, and from the right-click menu, choose **Copy Chart to Clipboard**.

To export the chart, click the contents of the chart, and from the right-click menu, choose **Export Chart to File**.

To rotate the chart by 90 degrees, click the contents of the chart, and from the right-click menu, choose **Rotate Chart Clockwise** or **Rotate Chart Counter-Clockwise**.

### Annotation Coverage

Displays the number and percentage of pins annotated by each source (VCD, manual annotation, SmartTime constraint, vectorless estimation, and fixed values) for all clocks, register outputs, combinational outputs, set/reset nets, primary inputs, enable pins, and other pins.

To hide/show the annotation coverage, click the **Hide annotation coverage** or **Show annotation coverage** link.

Use the **Annotation Coverage Summary** drop-down menu to view probability or frequency annotation statistics (frequency=0 shows statistics for pins that have a frequency of 0).

VCD: displays the number/percentage of pins with frequencies/probabilities imported from a VCD file.

Manual annotation: displays the percentage of pins with manually-annotated frequencies/probabilities.

SmartTime constraint: displays the percentage of pins initialized with SmartTime.

Fixed values: displays the percentage of pins with default frequency/probability.

Vectorless estimation: displays the percentage of pins that have been annotated with vectorless estimation.

### **Operating Conditions**

Displays the temperature and voltage operating conditions for the selected mode or scenario as specified in the <u>Operating Conditions</u> dialog box. When you select a scenario, the temperature and voltage operating conditions for each mode in the scenario are displayed.

To change the operating conditions, click the **Change Operating Conditions** link or from the **Tools** menu, choose **Operating Conditions**.

### **Battery Life**

Enables you to set the battery capacity in mA/hr and reports the battery life.

## **Domains Tab**

The **Domains** tab displays a list of existing domains with their corresponding clock and data frequencies and probabilities.

When you start SmartPower for the first time, it will automatically initialize frequencies from SmartTime with a default data toggle rate of 10%. However, if you update your timing constraints in SmartTime, you can use the <u>Initialize Frequencies and Probabilities dialog box</u> to update SmartPower with new frequencies from SmartTime. If you don't have timing constraints in SmartTime, you can manually initialize clock and data frequencies by directly editing the Domains tab grid, or you can use the Initialize Frequencies and Probabilities dialog box.

If you import a VCD file, the Domains tab will display average clock and data frequencies for each clock domain and input set. This average is calculated using VCD information.

Note: If you change a clock or data frequency in the Domains tab, it will only impact nets using the default estimation source. Nets use the default estimation source when they have not been manually set to a specific frequency in the Frequencies tab, and when they have not been set by importing a VCD file. To see explicitly the list of nets using the default estimation source, refer to the Frequencies tab.

8	Summary	tomains 🔞	🔎 Analysis	Requencies	₽ Probabilites				
Sh	iow: G	Frequencies	C Probab	ilities					
	ck domains	Tequencies	- TIODAL	Allices					
					Clock	s Register	Set/Reset	Primary inputs	Combinational
	Status		Nan	ne	(MHz	) outputs	nets	(MHz)	outputs (MHz)
1	<ul> <li>Image: A second s</li></ul>	CLKIN			100	5 (10 %)	0 (0 %)	5 (10 %)	5 (10 %)
Se	t of pins								Hide set of pi
	Status				Na	me			▲ Data ▲ (MHz)
1	Δ	Input to Out	put						0
Fro		d Drobabilition di	ianlawad in this	tab are default uslue	a They are used for	note that have not be		y method (i.e. VCD or m	
						e percentage of nets		y method (i.e. VCD of fr	iariuai

Figure 3 · SmartPower Domains Tab



Note: Data and clock frequencies are automatically set to zero when in non-active modes.

The Domains tab displays frequencies or probability data for clock domains and sets of pins. In this tab, you can add, edit, or remove domains or sets of pins, and change the clock and/or data frequency of a selected domain.

To hide or display the grid for set of pins, click the Hide/Show set of pins link.

You can edit frequency or probability data directly from the grid.

#### To create a new clock domain or set of pins:

- 1. Right-click the clock domain or set of pins and choose to add a new create new clock domain or create new set of pins.
- 2. Enter a name and click OK. The new clock domain or set of pins appears in the Domains tab.
- 3. Modify the frequency and probability data as needed.

Clock domain frequencies can be initialized by right-clicking the clock domain name and selecting **Initialize Frequencies and Probabilities**. If there is no frequency constraint set for this clock domain in SmartTime, the clock frequency of the domain will not be changed.

The status of a clock frequency or probability is displayed in the first column by an icon. Mouse over the icon to identify the status:

lcon	Description				
Δ	This clock has not been initialized				
Δ	No constraints available for this clock from SmartTime				
✓	Average frequencies/probabilities imported from VCD				
✓	Clock constraints imported from SmartTime				
✓	This clock has been manually initialized				

Note: This feature is only available when in active operating mode or when in a mode based on the Active mode.

The status of a set of pins is displayed in the first column by an icon. Mouse over the icon to identify the status:

Table 2 · Set of Pins Sta
---------------------------

lcon	Description				
Δ	This set has not been initialized				
✓	Average frequencies/probabilities imported from VCD				
<ul> <li>Image: A start of the start of</li></ul>	This set has been manually initialized				

Note: This feature is only available when in active operating mode or when in a mode based on the Active mode.

To remove one or multiple clock domains, select the clock domain(s), and click Remove Selected Domains(s).

#### To edit a clock domain or a set of pins:

1. Select the clock domain and from the right-click menu, choose **Edit Domain**. The Clock Domain or Set-of-Pins window appears.



CLK/Clk1_reg:Q Pins (Clock Domain)	
Any pins that do not belong to a domain are listed in the "Unclassif pin from the 'Unclassified Pins' list box and add it to CLK/Clk1_reg: You may also want select a pin from CLK/Clk1_reg:Q and remove appear in the Unclassified Pins list box).	Q.
Unclassified Pins: CLK/U108:Y CREG/U36:Y CS_N CTRL/U10:Y CTRL/U10:Y CTRL/U11:Y CTRL/U12/U0:Y CTRL/U14:Y CTRL/U15/U0:Y	Clock Pins
× Set Select All	× Set Select All
Help	OK Cancel

Figure 4 · Clock Domain Window

Any pins that do not belong to a domain are listed in the **Unclassified Pins** list box. You can select a pin from the **Unclassified Pins** list box and add it to the current domain. You may also select a pin from the current domain and remove it from the domain (this pin will appear in the **Unclassified Pins** list box).

**Clock Pins and Data Pins:** Select **Clock Pins** from the pull-down list to display all clock pins for the selected domain, or select **Data Pins** to display registers, asynchronous signals, primary input, and combinational signals for the selected domain.

Use the **filter** boxes to narrow your search for a specific pin. The boxes are text filters; \* is a wildcard. 2. Click **OK**.

To delete a clock domain or a set-of-pins, select the clock domain or set-of-pins and from the right-click menu, choose **Remove Domain**.

## Analysis Tab

The **Analysis** tab enables you to inspect detailed hierarchical reports of the power consumption. The **Analysis** tab consists of two windows: the **Hierarchy of Instances** window and the **Analysis** window.



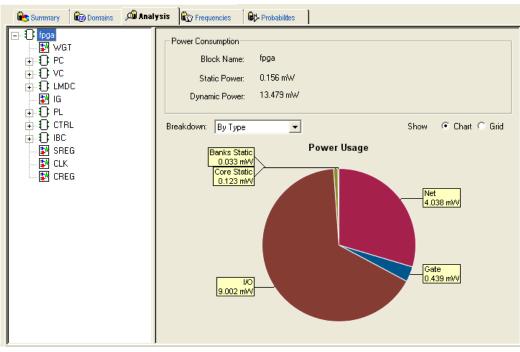


Figure 5 · SmartPower Analysis Tab

### **Hierarchy of Instances Window**

SmartPower displays the hierarchy of instances in a list in the **Hierarchy of Instances** window. Sub-blocks of a block are shown in the tree when you click the plus sign (+) next to the block. Only hierarchical blocks are displayed in this list (no gates or nets).

When you select a block of the hierarchical tree, SmartPower displays its name and power consumption in the Analysis window.

### **Analysis Window**

The Analysis window is divided into two sections: Power Consumption and Breakdown.

### **Power Consumption**

Displays the name of the currently selected block from the hierarchy of instances window, as well as the static and dynamic power consumption of the selected block.

#### Show

Displays power usage as a chart (not available when breakdown by instance is selected) or as a grid.

#### **Breakdown**

Displays a breakdown of power usage of the currently selected block. Use the drop-down list to select whether to display the power breakdown by type of component, instance, or clock domain.

When you select **By Type** from the drop-down list, the Analysis tab displays a breakdown of the selected block's power usage by the following types:

- Net
- Gate
- I/O
- Memory
- Core Static
- Banks Static

#### Analog

Any static power used by instances of a component in a design will be included in the appropriate category. As a result, the sum of the power in breakdown by type will equal the total of the static and dynamic power consumption of the design. Percentages displayed are fractions of the total power. Global nets are included in the net power types. To obtain the power of a clock, select breakdown by clock domain.

When you select **By Clock Domain** from the drop-down list, the Analysis tab displays a breakdown of the power usage by the clock domain that the power is drawn from. For each clock domain, the power and percentage of power drawn are displayed. Dynamic power is accounted for in breakdown by clock, but static power is not associated by any clock.

Whether you selected **By Type**, **By Instance** or **By Clock Domain**, you can customize which columns are displayed in the grid by right-clicking the column headers. To exclude a column, remove its checkmark from the right-click menu. Right-click a column header to set the column default size for the selected column or for all columns, sort the values in ascending or descending order, or customize columns.

To sort the contents of a column, double-click a column header.

To export the contents of the grid to a file, from the **File** menu, choose **Export Grid** or click its associated toolbar button.

To print the grid, from the File menu, choose Print Grid or click its associated toolbar button.

To copy the grid, from the Edit menu, choose Copy Grid or click its toolbar button.

To copy the chart, click the contents of the chart, and from the right-click menu, choose **Copy Chart to Clipboard**.

To export the chart, click the contents of the chart, and from the right-click menu, choose **Export Chart to File**.

To rotate the chart by 90 degrees, click the contents of the chart, and from the right-click menu, choose **Rotate Chart Clockwise** or **Rotate Chart Counter-Clockwise**.

To view an instance properties, right-click any instance and select **Instance Properties.** This brings the **Instance Properties** window, which displays the instance name, type and power and other properties specific to each type of instance, see image below.

nsta	ance Properti	es			2
Г	Property		Value		
ľ	Name		U141		
	Power		0m₩		
	Туре		Gate		
	Macro		ADLIB:INV		
P	Pin List:				
L	Pin Net		Domain	Freq. (MHz)	
	U141:A	BusOutput	CPUClk (data)	0.000	
	U141:Y	DRAMData	CPUClk (data)	0.000	
	Help			Close	

Figure 6 · Instance Properties: Gate

The **Instance Properties** allows you to access a list of pins of a gate and to check their domain and frequency.

#### See Also

Analyze results



Advanced Analysis of I/Os

# **Frequencies Tab**

Use the **Frequencies** tab to attach switching frequency attributes to the interconnects of the design. The **Frequencies** tab is divided into **Switching Frequencies**, **Average Frequencies**, and **Annotation Statistics**.

	er:  * Set	Domain: All	▼ Source: All				
	Driver	Net	Domain	Frequency (MHz)	Source		
1	PWM_out_pad/U0/U1:DOUT	PWM_out_pad/U0/NET1	un1_dataa_int	0	Fixed Values		
2	PWM_out_pad/U0/U0:PAD	PWM_out	un1_dataa_int	0	Fixed Values		
3	nPWM_out_pad/U0/U1:DOU	nPWM_out_pad/U0/NET1	un1_dataa_int	0	Fixed Values		
4	nPWM_out_pad/U0/U0:PAD	nPWM_out	un1_dataa_int	0	Fixed Values		
5	un1_dataa_int_NE:Y	un1_dataa_int_NE	un1_dataa_int	0	Fixed Values		
6	PWM_out:Q	PWM_out_c	un1_dataa_int	0	Fixed Values		
7	nPWM_out:Q	nPWM_out_c	un1_dataa_int	0	Fixed Values		
В	Aclr_pad/U0/U0:Y	Aclr_pad/U0/NET1	PWM_clk (set/	0	Fixed Values		
9	PWM_clk	PWM_clk	PWM_clk (cloc	0	Fixed Values		
10	PWM_clk_pad/U0/U0:Y	PWM_clk_pad/U0/NET1	PWM_clk (cloc	0	Fixed Values		
11	PWM_data_in<5>	PWM_data_in[5]	PWM_clk (prim	0	Fixed Values		
12	PWM_data_in<3>	PWM_data_in[3]	PWM_clk (prim	0	Fixed Values	~	
	Set Frequencies for selected pins	Reset Frequencies for select	ted pins		Select	all	
ver	age Frequencies:	A	Annotation Statistics:				
			VCD Import:		0%		
Pin: 0 MHz Manual Annotation: 0%							

Figure 7 · SmartPower Frequencies Tab

### **Switching Frequencies**

Displays the pins and lists the net, domain, frequency, and frequency source for each pin.

The **Driver** box enables you to filter the list of pins based on the criteria entered. Enter text in the filter box, and click **Set** to apply this text as a filter. Use the \* character to display all pins or as a wildcard.

Use the **Domain** drop-down list to select a different domain (All, CLKIN, Default, or Input to Output).

Use the **Source** drop-down list to select a different source (All, Default, Manual Annotation, or VCD Import).

You can change the frequency by entering a new value in the **Frequency** column or by selecting multiple pins and pressing the **Set frequencies for selected pins** button and entering a new frequency. Use **Reset frequencies for selected pins** to revert to the default frequency.

To select all the pins, click Select All.

### **Average Frequencies**

Displays the average frequency of all pins displayed in the grid.

Average Frequencies are useful when you import a VCD file or SAIF file. Since these files enable you to specify the frequency of each pin individually, it is often useful to know the average clock pin or data pin frequency for a particular clock domain.

If you did not specify a frequency annotation for any clock pin in this clock domain, the average value is equal to the default clock frequency of the clock domain. If you set one or several clock pins, SmartPower takes these specific annotations into account to compute an average value.

If you did not specify a frequency annotation for any data pin in this clock domain, the average value is equal to the default data frequency of the clock domain. If you set one or several data pins, SmartPower takes these specific annotations into account to compute an average value.

### **Annotation Statistics**

VCD import: displays the percentage of pins with frequencies imported from the \*.vcd file.

Manual annotation: displays the percentage of pins with manually-annotated frequencies.

Fixed values: displays the percentage of pins with default frequency.

# **Probabilities Tab**

You can use the Probabilities tab to control the probabilities for all pins.

**Bidirectional and Tristate I/Os:** Controls the output probability of each tristate and bidirectional I/O. The probability is the percent of time that the I/O is used as an output. You can change the default value and set a specific value for each bidirectional or tristate I/O.

**Memories:** Controls the read cycle probability or the write cycle probability of a memory block. The probability is the percent of time that a memory block will be used either in a read cycle or a write cycle. You can change the default value as well as set a specific value for each enable pin of each memory block available in the design.

If an enable pin is active low, assign it a probability of 0% to completely enable the I/O or the memory block, or 100% to disable it completely.

In designs with a cascaded memory, all memory enable pins are shown in the Probabilities tab. To simulate real-world power consumption, selectively enable only some memory enable pins, as specified in the memory cascading structure. For purely vertical cascading, enable the pins belonging to one RAM block. For purely horizontal cascading, enable all pins belonging to all RAM blocks of the cascaded memory. You can find which RAM block corresponds to which pin by cross-probing with the MVN NetlistViewer.

Driver:	Set	Type: All 💌	Polarity: All	•	Source: All	•
	Driver	Net	Туре	Polarity	Probability (%)	Source
1	rst_n	rst_n	Input to		99.9949	Manual A
2	rst_n_pad/U0/U0:Y	rst_n_pad/U0/NET1	Input to		99.9949	Manual A
3	rst_n_pad/U0/U1:Y	rst_n_c	Input to		99.9949	Manual A
4	fpu_op<0>	fpu_op[0]	Input to		0	Manual A
5	fpu_op_pad[0]/U0/U0:Y	fpu_op_pad[0]/U0/NET1	Input to		0	Manual A
6	fpu_op_pad[0]/U0/U1:Y	fpu_op_c[0]	Input to		0.000003	Manual A
7	UUT/un1_fpu_op_3_0_a2	UUT/N_1112	Input to		0.000003	Manual A
8	UUT/fracta_mul_w_0_a2	UUT/N_1111	Input to		0.000003	Manual A
9	fpu_op<1>	fpu_op[1]	Input to		0	Manual A
10	fpu_op_pad[1]/U0/U0:Y	fpu_op_pad[1]/U0/NET1	Input to		0	Manual A
11	fpu_op_pad[1]/U0/U1:Y	fpu_op_c[1]	Input to		0.000003	Manual A
12	UUT/un1_fpu_op_1_0_a2	UUT/N_1026	Input to		0.000003	Manual A
13	fpu_op<2>	fpu_op[2]	Input to		0	Manual A
14	fpu_op_pad[2]/U0/U0:Y	fpu_op_pad[2]/U0/NET1	Input to		0	Manual A
15	fpu_op_pad[2]/U0/U1:Y	fpu_op_c[2]	Input to		0.000003	Manual A
16	UUT/fract_denorm[30]:Q	UUT/fract_denorm[30]	UUT/un3_out_		0.0125	Manual A
17	UUT/fract_denorm[32]:Q	UUT/fract_denorm[32]	UUT/un3_out_		0.0125	Manual A
18	UUT/fract_deporm[31]+0	HUT/fract_denorm[31]	UUT/up3_out		0.0125	Manual A

The Probabilities tab displays the drivers, nets, types, polarity, rates, and source for each pin.

#### Figure 8 · SmartPower Probabilities Tab

The **Driver** box enables you to filter the list of drivers based on the criteria entered. Enter text in the filter box, and click **Set** to apply this text as a filter. Use the \* character as a wildcard.



Use the **Type** drop-down list to filter the pin list by different type (All, All enable, CLKIN, Default, or Input to Output).

Use the Polarity drop-down list to filter the pin list by polarity (Low, High, or All).

Use the **Source** drop-down list to filter the pin list by source (All, Default Estimation, Manual Annotation, Saif Import, or VCD Import).

You can change the rate by entering a new value in the **Rate** column or by selecting multiple pins, pressing the **Set Probabilities for selected pins** button, and entering a new frequency in the Set Default Probabilities dialog box.

Set probability for pin(s)					
Probability:					
50.00					
ОК	Cancel	]			

Figure 9 · Set Probability for Pins Dialog Box

Use Reset Probabilities for selected pins to revert to the default polarity.

You can change the default probability from the Domains tab.

To select all the drivers, click Select All.

You can set or reset the probabilities, set a default probability, copy, export, or print the grid by selecting one or multiple pins and choosing an option from the right-click menu.

#### See Also

Specify probabilities

## **Preferences Toolbar**

The SmartPower Preferences toolbar gives you quick access to commonly used settings. Mouse over the toolbar button to view a description of the command. Use the drop-down list to select your settings.

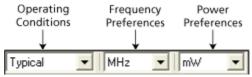


Figure 10 · SmartPower Preferences Toolbar

Operating Conditions: Enables you to set the operating conditions - Best, Typical, or Worst.

The actual voltage and temperature of a given operating condition is defined by the operating condition range selected for the current design (COM, IND, MIL, Auto, TGrade1, TGrade2, and Custom). For SmartPower, unlike SmartTime, the worst voltage is the upper bound of the range. That is, higher (worst-case) power comes from higher voltage, whereas higher voltage results in best-case speed.

Note: Worst-case and best-case calculations are available only for certain families and devices.

**Frequency:** Sets unit preferences for frequency – Hz, KHz, MHz.

**Power Units:** Sets unit preferences for power – W, mW, or uW.

#### See Also

SmartPower toolbar / menu commands

# Modes and Scenarios Toolbar

The Modes and Scenarios toolbar displays all pre-defined modes, custom modes, pre-defined scenarios, and custom scenarios. The Modes and Scenarios toolbar is shown by default, but can be closed or undocked. To view the toolbar, from the **View** menu, choose **Modes and Scenarios toolbar**.

From this toolbar, you can:

- Select a pre-defined mode by clicking the mode name
- Select a custom mode by clicking the mode name
- Select a custom mode for power-driven layout by right-clicking the active-based mode and selecting Use for PDPR
- Re-import a VCD file from an Active mode or a custom mode by right-clicking the VCD file and selecting Re-import VCD File
- Remove a VCD file from an Active mode or a custom mode by right-clicking the VCD file and selecting Remove VCD File from <mode name> Mode; or from the Simulation menu, choose Remove VCD File > <file name>
- Generate a Cycle-Accurate Power report by right-clicking the VCD file and selecting Cycle-Accurate Power Report
- Generate an Activity and Hazards Power report by right-clicking the VCD file and selecting Activity
   and Hazards Power Report
- View the Cycle-Accurate Power analysis by right-clicking the VCD file and selecting Cycle-Accurate Power Analysis
- <u>Create</u> a new custom mode by clicking **Custom modes** and selecting **New Custom Mode**; or by clicking the **New Custom Mode** hyperlink
- <u>Edit</u> and <u>delete</u> a custom mode by right-clicking the mode name and selecting **Edit custom mode** or **Delete custom mode**
- <u>Copy</u> a custom or a pre-defined mode by right-clicking the mode name and selecting **Create a copy of** this mode
- Select a scenario by clicking the scenario name
- <u>Create</u> a new custom scenario by clicking Scenarios and selecting New custom scenario
- <u>Edit</u> and <u>delete</u> a custom scenario by right-clicking the scenario name and selecting Edit custom scenario or Delete custom scenario
- Copy a scenario by right-clicking the scenario name and selecting Create a copy of this scenario

Note: When a scenario is selected, only the Summary tab is available.

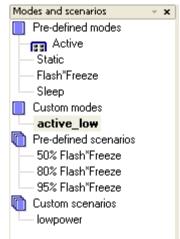


Figure 11 · Modes and Scenarios Toolbar



# SmartPower Standard Toolbar and Menu Commands

The SmartPower standard toolbar contains commands for performing common SmartPower operations on your designs. Roll the mouse pointer over the toolbar button to view a description of the button. Click the button to access the command.

Toolbar Button	Description
0	<u>Commit</u>
0	Settings Summary
<b>B</b>	Operating Conditions
	Options
	Export Path Grid
	Copy Path Grid
4	Print Grid
	Generate Power Report
•	Initialize Frequencies and Probabilities
8	Refreshes Vectorless Estimation

Table 3 · SmartPower Toolbar

The PC and UNIX workstation versions of SmartPower have the same menus. However, some dialog boxes may look slightly different on the two platforms due to the different window environments. The functionality is the same on both platforms, though the locations of the fields and buttons on the dialog boxes may vary. The names of some fields may also vary between the PC and workstation versions.

### **File Menu**

Menu	Description
Commit	Commits power information to Designer. You must commit your changes if you wish to save your settings in SmartPower. If you commit your changes, the information is stored in the .adb file, and your settings are restored the next time you open your design in SmartPower
Export Grid	Exports the selected area of the <b>Report</b> window to a text (.txt) file
Print Grid	Prints the selected area of the <b>Report</b> window
Settings Summary	Displays a summary of the power settings for the current design
Close	Closes SmartPower



### Edit Menu

Menu	Sub-Menu	Description
Domains	New Clock Domain	Adds a clock domain
	New Set of Pins	Adds a set of pins
	Delete Domain	Deletes a clock domain
	Edit Domain	Edits a clock domain
Modes and Scenarios	Use for Analysis > mode or scenario name	Sets the selected mode or scenario to be used for analysis
	Use for PDPR > mode or scenario name	Sets the selected mode or scenario to be used for <u>Power-Driven Layout</u>
	Custom Modes > New Custom Mode	Creates a new custom mode
	Custom Modes > Edit Custom Mode	Edits a custom mode
	Custom Modes > Delete Custom Mode	Deletes a custom mode
	Custom Scenarios > New Scenario	Creates a new custom scenario
	Custom Scenarios > Edit Scenario	Edits a custom scenario
	Custom Scenarios > Delete Scenario	Deletes a custom scenario
Copy Grid	_	Copies the selected cells of the dynamic grid onto the clipboard

### **View Menu**

Menu	Description
Standard Toolbar	Displays or hides the SmartPower Standard toolbar
Preferences Toolbar	Displays or hides the <u>SmartPower Preferences</u> toolbar
Modes and Scenarios Toolbar	Displays or hides the Modes and Scenarios toolbar
Unprocessed Simulation Files Toolbar	Displays or hides the <u>Unprocessed Simulation Files</u> toolbar



Menu	Description
Customize Columns	Selects and orders the columns displayed in the user interface
Reset Window Layout	Resets the window layout to the default layout

### **Tools Menu**

Menu	Sub-Menu	Description
Initialize Frequencies and Probabilities	_	Imports clock constraints from SmartTime and enables the user to input frequencies and probabilities for the design
Operating Conditions	_	Enables the user to customize the <u>operating</u> <u>conditions</u> used in SmartPower
Options	—	Invokes the <u>Options</u> dialog box, where you can set analysis and display preferences
Reports	Power Report	Generates a power report
	Scenario Power Report	Generates a scenario power report
	Cycle Accurate Power Report	Generates a cycle accurate power report
	Activity and Hazards Power Report	Generates an <u>activity and hazards power</u> report
Cycle Accurate Power Analysis	_	Generates a cycle-accurate power analysis

### **Simulation Menu**

Menu	Description
Import VCD File	Invokes the Import VCD Options dialog box
Remove VCD file	Removes the selected CVD file from the design
Audit files	Audits simulation files within the project

### **Help Menu**

Menu	Description
Help on <i>current tab</i>	Displays the help content for the current tab
Help Topics	Opens the help files for SmartPower
SmartPower User's Guide	Displays the SmartPower User's Guide
Data Change History	Displays the data change history report

### See Also

SmartPower preferences toolbar

# **Power - Settings Summary**

The Power - Settings Summary dialog box displays a summary of the power settings for the current design.

To open the Power - Settings Summary dialog box, from the File menu, choose Settings Summary or

click the **i** icon in the SmartPower toolbar.

Attribute	Value	
Design	SMALL_GATED	
Family	ProASIC3	
Die	A3P125	
Package	144 FBGA	
Temperature Range	COM	
Voltage Range	COM	
Operating Conditions	Typical	
Operating Mode	Active	

Figure 12 · Power - Settings Summary Dialog Box

The **Power - Settings Summary** dialog box displays the following information:

- Design: Displays the name of the design. •
- Family: Displays the device family used in the design. •
- Die: Displays the die. .
- Package: Displays the package. .
- Temperature Range: Displays the temperature range.
- Voltage Range: Displays the core supply voltage.
- Operating Condition: Displays the operating conditions that SmartPower uses to calculate static and . dynamic power contributions.
- Operating Mode: Displays the operating mode that SmartPower uses to calculate static and dynamic power contributions.

Note: The status bar also shows the ambient temperature, VCCA and speed grade.



# Initializing Frequencies and Probabilities

The **Initialize Frequencies and Probabilities** dialog box enables you to initialize the frequencies and probabilities for your design.

To open the Initialize Frequencies and

Probabilities dialog box, from the Tools menu, choose Initialize Frequencies and

**Probabilities**, or click the <sup>1</sup>/<sub>10</sub> icon in the SmartPower toolbar.

Note: This feature is only available in the Active operating mode or modes derived from the Active mode.

The dialog box is organized in the following panels: <u>General</u>, <u>Clocks</u>, <u>Register Outputs</u>, <u>Set/Reset Nets</u>, <u>Primary Inputs</u>, <u>Combinational Outputs</u>, <u>Enables Sets of Pins</u>, and <u>Other Sets of Pins</u>.

### General

SmartPower - Initialize Frequencies and Probabilities		
Select a Category:	General	
General Clocks Set/Register outputs Set/Reset nets Primary inputs Combinational outputs Set of pins Enables Others	Use this dialog box to initialize frequencies and probabilities for your design. Initialize mode: Active  To To For pins that have not been annotated, SmartPower can estimated their frequency and probability using a Vectorless analysis or fixed values. Use vectorless analysis Use vectorless analysis Use fixed values Remove Simulation file (VCD) if any.	
	Remove any manual annotations.	
Help	OK Cancel	

Figure 13 · Initialize Frequencies and Probabilities Dialog Box - General

Initialize mode - Select an active-based mode to initialize the frequencies and probabilities for.

For pins that have not been annotated, SmartPower can estimate their frequency and probability using <u>vectorless analysis</u> or fixed values:

**Use vectorless analysis** – SmartPower initializes frequencies and probabilities with vectorless analysis. **Use fixed values** – SmartPower initializes frequencies and probabilities (%) of all registers with a default toggle rate (available only when using toggle rates), frequency, and probability.

Based on the selected mode, a warning appears with information on the annotated pins. If the selected mode contains any annotations, you can remove annotations by selecting one or both options below:

**Remove simulation file (VCD) if any** – Select this option to remove the simulation file for the selected mode.

**Remove any manual annotations** – Select this option to remove all manual pin annotations for the selected mode.

### Clocks

SmartPower - Initialize Frequencies and Probabilities 🛛 🛛 🔀			
SmartPower - Initialize Frequenci Select a Category: General Clocks Register outputs Set/Reset nets Primary inputs Combinational outputs Set of pins Enables Others	Clocks          Initialize clock frequencies and duty cycles         with clock constraint if available in SmartTime         else, with default frequency         10,00		
Нер	and duty cycle 50.00 %		

Figure 14 · Frequencies and Probabilities Dialog Box – Clocks

**Initialize clock frequencies and duty cycles** – Select this option to initialize clock frequencies and duty cycles, with:

with clock constraint if available in SmartTime: When only this box is checked, SmartPower initializes all clock domains in SmartPower with clock constraints from SmartTime. If there is no frequency constraint set for this clock domain in SmartTime, the clock frequency of the domain will not be updated.

else, with default frequency (MHz) and duty cycle (%): When only this

box is checked, SmartPower initializes all clock domains in SmartPower with the specified default frequency and duty cycle.

Note: When both boxes (with clock constraint if available in SmartTime and with default frequency and duty cycle) are checked, SmartPower initializes all clock domains with clock constraints from SmartTime. If there is no frequency constraint set for a clock domain in SmartTime, it is initialized with the specified default frequency and duty cycle.



### **Register Outputs**

SmartPower - Initialize Frequencies and Probabilities 🛛 🛛 🔀			
Select a Category: General Clocks Sel/Reset nets Primary inputs Combinational outputs Set of pins Enables Others	✓ Initialize frequencies and probabilities         ✓ with Vectorless analysis         ✓ with fixed values         toggle rate       10.00         %         probability       \$0.00		
Help	OK Cancel		

Figure 15 · Frequencies and Probabilities Dialog Box – Registers

**Initialize frequencies and probabilities** – Select this option to initialize frequencies and probabilities for register outputs in your design.

With vectorless analysis – SmartPower initializes frequencies and probabilities using vectorless analysis.

**With fixed values**: SmartPower initializes frequencies and probabilities (%) of all register outputs with a default toggle rate (available only when using toggle rates) or frequency (when not using toggle rates), and a default probability.

### **Set/Reset Nets**

SmartPower - Initialize Frequenci	ies and Probabilities	
Select a Category: General Clocks Set/Register outputs Set/Reset nets Primary inputs Combinational outputs Set of pins Enables Others	Initialize frequencies and probabilities         with fixed toggle rate       0.00       %         with fixed probability       50.00       %	
Help	OK Cancel	

Figure 16 · Frequencies and Probabilities Dialog Box – Asynchronous

**Initialize frequencies and probabilities** – Select this option to initialize frequencies and probabilities for set/reset nets in your design.

With default toggle rate (%): SmartPower initializes frequencies and probabilities of all set/reset nets with the specified default toggle rate. This option is available only when using toggle rates.

With default frequency (MHz): SmartPower initializes all set/reset nets in SmartPower with the specified default frequency. This option is available only when not using toggle rates.

With default probability (%): SmartPower initializes probabilities of all set/reset nets with the specified default probability.

### **Primary Inputs**

SmartPower - Initialize Frequenci	ies and Probabilities	
Select a Category:	Primary inputs	
<ul> <li>General</li> <li>M Clocks</li> <li>Register outputs</li> <li>Set/Reset nets</li> <li>Primary inputs</li> <li>Combinational outputs</li> <li>Set of pins</li> <li>Enables</li> <li>Others</li> </ul>	✓ Initialize frequencies and probabilities with fixed toggle rate 10.00 % with fixed probability 50.00 %	
Help	OK Cancel	

Figure 17 · Frequencies and Probabilities Dialog Box – Primary Inputs

**Initialize frequencies and probabilities** – Select this option to initialize frequencies and probabilities for the primary inputs in your design.

With default toggle rate (%): SmartPower initializes frequencies and probabilities of all primary inputs with the specified default toggle rate. This option is available only when using toggle rates.

With default frequency (MHz): SmartPower initializes all primary inputs in SmartPower with the specified default frequency. This option is available only when not using toggle rates.

With default probability (%): SmartPower initializes probabilities of all primary inputs with the specified default probability.



### **Combinational Outputs**

SmartPower - Initialize Frequenci	ies and Probabilities	
Select a Category: General Clocks Clocks Set/Reset outputs Set/Reset nets Primary inputs Combinational outputs Set of pins Enables Others	Combinational outputs  Initialize frequencies and probabilities  with Vectorless analysis  with fixed values toggle rate 10.00 % probability 50.00 %	
Help	OK Cancel	

Figure 18 · Frequencies and Probabilities Dialog Box – Combinational

**Initialize frequencies and probabilities** – Select this option to initialize frequencies and probabilities for the combinational outputs in your design.

With vectorless analysis - SmartPower initializes frequencies and probabilities with vectorless analysis.

**With fixed values**: SmartPower initializes frequencies and probabilities (%) of all combinational outputs with a default toggle rate (available only when using <u>toggle rates</u>) or frequency (when not using toggle rates), and a default probability.

### **Enables**

SmartPower - Initialize Frequenci	es and Probabilitie	5			
Select a Category:	Enables				
💮 General					
UL Clocks					
Register outputs	🔽 Initializ	e frequencies and probabili	ties —		_
🚽 🥁 Set/Reset nets	C				
Primary inputs	• with	n Vectorless analysis			
↓ ↓ Combinational outputs	C with fixed values				
Set of pins			Frequency	Probability	
Enables		Domain	MHz	%	
Others	1	IOsEnableSet	0.00	12.50	
	2	MemoriesEnableSet	0.00	12.50	
Help		ОК	Cance	el 🔤	

Figure 19 · Frequencies and Probabilities Dialog Box – Enables

**Initialize frequencies and probabilities** – Select this option to initialize frequencies and probabilities for the enable sets of pins in your design.

With vectorless analysis - SmartPower initializes frequencies and probabilities with vectorless analysis.

**With fixed values**: SmartPower initializes frequencies and probabilities of all enables sets of pins with the specified default probability and frequency.

### Others

SmartPower - Initialize Frequenci	ies and Probabilities	×
Select a Category:	Others	
<ul> <li>General</li> <li>Clocks</li> <li>Register outputs</li> <li>Set/Reset nets</li> <li>Primary inputs</li> <li>Combinational outputs</li> <li>Set of pins</li> <li>Enables</li> <li>Others</li> </ul>	<ul> <li>Initialize frequencies and probabilities</li> <li>with Vectorless analysis         <ul> <li>primary inputs frequency</li> <li>primary inputs probability</li> <li>so.oo</li> <li>with fixed values</li> <li>frequency</li> <li>1.00</li> <li>MHz</li> <li>probability</li> <li>so.oo</li> <li>with fixed values</li> </ul> </li> </ul>	
Help	OK Cancel	

Figure 20 · Frequencies and Probabilities Dialog Box – Others

**Initialize frequencies and probabilities** – Select this option to initialize frequencies and probabilities for the other sets of pins in your design with default values.

**With vectorless analysis** – SmartPower initializes frequencies and probabilities with vectorless analysis as specified in the primary inputs frequency and probability.

With fixed values: SmartPower initializes frequencies and probabilities (%) of all other sets of pins with a default frequency and probability.

### See Also

Domains Tab Vectorless Analysis

## **Power Options**

Enables you to set options that affect the graphical and textual reports. To open the SmartPower **Power Options** dialog box:

- From the File menu choose Options
- Select the Options panel in the Power Report dialog box.
- Click the 
   icon in the SmartPower toolbar.



Power - Options	
Units Power: mW <b>v</b> Frequency MHz <b>v</b>	
Use toggle rates	
Help OK	Cancel

Figure 21 · SmartPower Preferences Dialog Box

There are two sections: Units and Use Toggle Rates.

- Units: Sets unit preferences for power (W, mW, vW) and frequency (Hz, KHz, MHz).
- Use Toggle Rates: When toggle rates are active (Use Toggle Rates box is checked), the data frequency of all the clock domains is defined as a function of the clock frequency. This updates the data frequency automatically when you update the clock frequency. Toggle rates enable you to specify the data frequency as a percentage of clock frequency, but you can no longer specify the data frequency as a number, only as a percentage of the clock frequency. To specify data frequencies, clear the Use Toggle Rates option in the Preferences window.

You can set the data frequency percentage when you <u>create a new clock domain</u> with toggle rates active. In addition, when toggle rates are active you can set the data frequency percentage in the <u>Domain</u> and <u>Frequencies</u> tabs.

Create Clock Domain	X
Potential Clock Pin CLK_pad/IOTILE:Y0	Create
Clock Frequency 10 MHz	Cancel
Data Frequency 20 %	

Figure 22 · Create Clock Domain – Toggle Rates Enabled

# **Operating Conditions**

The SmartPower Operating Conditions dialog box enables you to customize the operating conditions used in SmartPower for voltage and temperature.

Note: Changes will apply only to SmartPower and will not change the operating conditions set in Designer.

The General panel enables you to select the operating condition you want to apply to SmartPower: Best, Typical, or Worst.

SmartPower - Operating Condition	15	×
Select a Category:	General	
General Temperature settings Thermal resistance settings Voltage settings VCCA VCCI 2.5 VCCI 3.3 VCCI 1.8 VCCI 1.5	Use this dialog box to customize the operating conditions used in SmartPower. Changes will apply only to SmartPower and will not change the operating conditions set in Designer. Select an active operating condition for SmartPower from the options below:	
Help	OK Cancel	

Figure 23 · SmartPower Operating Conditions Dialog Box - General

You can customize temperature settings in the Temperature Settings panel, and the voltage settings in the Voltage Settings panels — each VCC voltage used in the design appears under Voltage settings.

SmartPower - Operating Condition	15	×
Select a Category: General Temperature settings Voltage settings VCCA VCCI 2.5 VCCI 3.3 VCCI 1.8 VCCI 1.5	Temperature settings         Use:       Design operating range (default)         SmartPower uses the operating range specified in the Device Selection Wizard:         This design uses "COM" settings.         Junction Temperature (in degrees Celsius)         Best:       Typical:       Worst:         0.00       25.00       70.00	
Help	OK Cancel	

Figure 24 · SmartPower Operating Conditions Dialog Box - Temperature Settings

Select one of three options to specify the temperature or voltage settings:

- Design operating range (default): sets the temperature or voltage operating range as specified in your <u>Project Settings</u>.
- Custom operating range: sets the temperature (junction or ambient) or voltage operating range for the current design in SmartPower only. You can enter temperature values in degrees Celsius and voltage values in volts for Best, Typical, and Worst.
- Mode by mode operating range: sets the temperature (junction or ambient) or voltage for each mode in SmartPower only. You can use the grid to enter temperature values in degrees Celsius and voltage values in volts for each mode, or select multiple modes in the grid, and click the **Set values for selected modes** button to enter the same values for all selected modes.



Select a Category:	Temperature settings				
General Temperature settings Thermal resistance settings Voltage settings Voltage settings VCCA VCCI 2.5 VCCI 2.5	Use: Mode by mode operating range SmartPower uses a different operating Operating ranges for each mode can b Specify (in Celcius degrees):	g range for each mo		nartPower only	у.
<ul> <li>VCCI 3.3</li> <li>VCCI 1.8</li> <li>VCCI 1.5</li> </ul>	Mode	Best	Typical	Worst	
VCCI 1.5	1 Active 2 Sleep	0.00	25.00 25.00	70.00 50.00	
	3 Static	0.00	25.00	50.00	
					all

 $\label{eq:Figure 25} Figure \ 25 \cdot SmartPower \ Operating \ Conditions \ Dialog \ Box \ - \ Mode-Specific \ Temperature \ Settings$ 

The junction temperature and static power are computed iteratively until they converge.

The formulas are:

$$T_{J} = T_{A} + \theta_{JA} \cdot (P_{dynamic} + P_{static})$$
$$P_{static} = f(T_{J}) = P_{0} + P_{1} \cdot T_{J}$$

If the computed junction temperature is outside the operating condition range (smaller than the best case value or greater than the worst case value), a violation warning will be reported.

Both T<sub>J</sub> and P<sub>static</sub> will be re-computed when any of the following parameters are changed:

- Ambient temperature
- Cooling style
- Custom thermal resistance,

or any parameters/options that affect the static or dynamic power values:

- Junction Temperature Display Mode
- Operating Condition (Affect dynamic power)
- Operating Mode (Affect dynamic power)
- Any of the clock domain frequencies (Affect dynamic power)

If you specified the Ambient temperature in the Temperature Settings panel, you can select the thermal characteristic for Theta $_{JA}$ .

SmartPower - Operating Condition	ıs 🔀
Select a Category:	Thermal resistance settings
General Temperature settings Thermal resistance settings Voltage settings VCCA VCCI 2.5 VCCI 3.3 VCCI 1.8 VCCI 1.5	Select the thermal characteristic for $\Theta_{7a}$ Pre-defined: 2.5 m/s 13.6 C/W Custom: 100.00 C/W
Help	OK Cancel

Figure 26 · SmartPower Operating Conditions Dialog Box - Thermal Resistance Settings

The thermal resistance is predefined for Still Air, 300 ft/min and Case Cooling. To enter a custom thermal resistance, select **Custom** from the **Cooling** field, and change the value.

SmartPower also reports the thermal resistance, Theta<sub>JA.</sub>

### See Also

SmartPower toolbar / menu commands SmartPower preferences toolbar

# **Custom Operating Modes**

SmartPower enables you to use pre-defined and custom operating modes. A pre-defined operating mode is an inherent mode of a family of devices that comes with a number of hard availability constraints on the FPGA resources. Custom operating modes are user-defined modes based on one of the pre-defined modes available for the family, where parameters such as clock, data, and toggle rate frequencies have been customized. A custom mode can also be linked to a VCD.

Custom modes can be used:

- To define additional modes where the chip is in the active pre-defined mode, but where the clock frequencies or the toggle rates are scaled up or down.
- To import multiple VCD files that capture individual steps that take place in different modes.
- To define a sequence of modes with a duration for each mode and get an estimate of the overall
  power consumption, from which extrapolate the battery life for the application. The <u>Scenario Power</u>
  report enables you to define a sequence of modes and estimate the weighted average of the power
  consumption of the chip over the whole sequence.
- To define additional modes where the chip is in a pre-defined mode, but the junction/ambient temperature or the rails' voltage modes are different.

#### To set the current mode:

From the **Edit** menu in SmartPower, choose **Modes and Scenarios > Use for Analysis >** *mode name*; or select the mode in the <u>Modes and Scenarios toolbar</u>.

#### To create a new custom mode:

 From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Modes > New Custom Mode; or click Custom Modes in the Modes and Scenarios toolbar, and select New custom mode. This brings up the New Custom Mode dialog box.



Power - New Custom	Mode 🛛 🔀
Name:	Mode3
Based on mode:	Active
Comment:	
Frequency 15 MHz	
Help	OK Cancel

Figure 27 · New Custom Mode Dialog Box

- 2. Enter the mode name, select the base mode, and enter comments that describe the mode. The base mode can be either a user-defined custom mode or the active mode. The new mode will inherit all clock and data frequencies and annotations of its base mode.
- 3. Click OK. The newly created operating mode is set as default in the Modes and Scenarios toolbar.

#### To edit a custom mode:

 From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Modes > Edit Custom Mode; or right-click the mode in the Modes and Scenarios toolbar, and select Edit custom mode. This brings up the Edit Custom Mode dialog box.

Power - Edit Custom Mode [custom_mode]		
Name:	custom_mode	
Comment:		
Copied from "Sleep"		
This mode is derived from the "Sleep" low power mode.		
Help	OK Cance	

Figure 28 · Edit Custom Mode Dialog Box

- 2. Edit the mode name and comments.
- 3. Click OK.
- Note: You can only use the Edit Mode dialog box to edit the name and comment of the current mode. To edit the mode properties such as clock and data frequencies, use the SmartPower tabs.

#### To copy a custom mode:

1. Right-click the mode in the Modes and Scenarios toolbar, and select **Create a copy of this mode**. This brings up the New Custom Mode dialog box.



Power - New Custom Mode		
Name:	Copy of Active	
Based on mode:	Active	
Comment:		
Copied from "Active"		
Help	OK Cancel	

Figure 29 · New Custom Mode Dialog Box

- 2. Edit the mode name and comments.
- 3. Click OK.

#### To delete a custom mode:

1. From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Modes > Delete Custom Mode; or right-click the mode in the Modes and Scenarios toolbar, and select Delete Mode. This brings up the Delete Custom Mode dialog box.

Power - Delete Custom Mode		
Choose th	ne custom mode to de	lete:
Mode3		<b>_</b>
Help	ОК	Cancel

Figure 30 · Delete Custom Mode Dialog Box

2. Select the mode from the pull down and click **OK**.

Note: You can only delete custom operating modes. Pre-defined modes cannot be deleted.

## Scenarios

A scenario is a sequence of previously defined <u>operating modes</u> with a specific duration for each mode. When you create a new design, SmartPower will automatically create some pre-defined scenarios that can be used as is, or copied to create a new scenario based on the pre-defined one.

Note: Pre-defined scenarios cannot be deleted or edited.

#### To set the current scenario for analysis:

From the **Edit** menu in SmartPower, choose **Modes and Scenarios > Use for Analysis >** <*scenario name*>; or select the scenario in the <u>Modes and Scenarios toolbar</u>.

Note: When a scenario is selected, only the Summary tab is available.

#### To create a new custom scenario

- 1. From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Scenarios > New Custom Scenario; or click Scenarios in the Modes and Scenarios toolbar, and select New custom scenario. This brings up the New Custom Scenario dialog box.
- 2. Enter the scenario name, enter a duration (total duration for the sequence must equal to 100%) and select previously defined <u>operating modes</u> for this sequence.
- 3. Click **OK**. The newly created scenario is set as default in the Modes and Scenarios toolbar.



### To edit a custom scenario:

 From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Scenarios > Edit Custom Scenario; or right-click the scenario in the Modes and Scenarios toolbar, and select Edit custom scenario. This brings up the Edit Custom Scenario dialog box.

Power - Edit Custom Scenario [Copy of 50% Flash*F 🔀				
I	Name: Copy of 50% Flash*Freeze			
		Duration (%)	Mode	^
	1	50	Active	
	2	50	Flash*Freeze	
	3			
	4			_
	5			
	6			
	8			
	9			~
	Total: 100 % Delete entry			
Comment:				
Copied from "50% Flash*Freeze"				
	Help OK Cancel			

Figure 31 · Edit Custom Scenario Dialog Box

- 2. Edit the information.
- 3. Click OK.

#### To copy a scenario:

1. Right-click the scenario in the Modes and Scenarios toolbar, and select **Create a copy of this scenario**. This brings up the New Custom Scenario dialog box.

Power - New Custom Scenario				
Name: Copy of scenario1				
		Duration (%)	Mode	<u>^</u>
	1	20	Active	
	2	80	Sleep	=
	3			
	4			
	5			
	6			
	7			
	8			
	9			<u> </u>
•	Total: 100 % Delete entry			
Comment:				
Copied from "scenario1"				
Help OK Cancel				

Figure 32 · New Custom Scenario Dialog Box

- 2. Edit the information.
- 3. Click OK.

#### To delete a custom scenario:

1. From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Scenarios > Delete Custom Scenario; or right-click the scenario in the Modes and Scenarios toolbar, and select Delete Scenario. This brings up the Delete Custom Scenario dialog box.

Power - Delete Custom Scenario 🛛 🛛 🔀		
Choose the	custom scenario to	delete:
scenario1	cascolin scenario co	■
Help	ОК	Cancel

Figure 33 · Delete Custom Scenario Dialog Box

2. Select the scenario from the pull down and click **OK**.

## **Power Reports**

The power report enables you to quickly determine if any power consumption problems exist in your design.

#### To generate a power report:

- 1. From the Designer **Tools** menu, choose **Reports > Power > Power**. The Power Report dialog box appears.
- 2. Select the options you want to include in the report, and then click **OK**. The power report appears in a separate window.

You can also generate the power report from within SmartPower. From the **Tools** menu, choose **Reports > Power Report**, or click the **Report** button to open the **Report** dialog box. By default, the report includes global design information and a power summary. Specify which results you want to display by selecting the categories and their options.



The power report dialog box is organized in the following panels: <u>General</u>, <u>Operating Conditions</u>, <u>Options</u>, <u>Breakdown by Instance</u>, <u>Frequency Summary</u>, and <u>Probability Summary</u>.

### General

The general panel enables you to select what to include in the report, the report format, and the mode that you want to generate the report for.

Power Report		
Select a Category: General Operating Conditions Options Breakdown by instance Frequency summary Probability summary	Include in the report         Power summary         Breakdown by rail         Breakdown by type         Breakdown by clock domain         Thermal summary         Battery life         Clock domain summary         Operating condition summary         Report format:         Text         Mode:         Active         1	
Help	OK Cancel	

Figure 34 · SmartPower Power Report Dialog Box - General Panel

### **Include in the Report**

Select the option(s) that you want to include in the Power Report:

Power summary – This section reports the static, dynamic and total power consumption of the design.

Breakdown by rail - This section shows the power consumption of each rail.

**Breakdown by type** – This section enables reporting on the power consumption according to: gates, nets, clocks, core static, IOs and memories.

Breakdown by clock domain – This section enables reporting on the power consumption of each clock domain.

**Thermal summary** – This section includes a thermal report. The ambient temperature can be defined by the operating conditions or defined by the ambient temperature.

When the first option is selected, the following characteristics are reported:

- Operating conditions
- Temperature range
- Junction temperature

When the second option is selected, the following characteristics are reported:

- Ambient temperature
- Cooling style
- Package
- Thermal resistance Theta-JA
- Junction temperature
- Temperature range
- Junction temperature range limits specification

Battery Life - This section reports the battery life.

Clock Domain Summary – This section reports the clock and data frequencies for each clock domain.

Operating Condition Summary – This section reports the operating conditions.

**Annotation Coverage** - This section reports the number and percentage of pins annotated by each source (VCD, manual annotation, SmartTime constraint, vectorless estimation, and fixed values) for all clocks, register outputs, combinational outputs, set/reset nets, primary inputs, enable pins, and other pins

### **Report Format**

Select Text or CSV (Comma Separated Value) as the desired export format.

#### Mode

Select a mode to generate the report for.

### **Operating Conditions**

The Operating Conditions panel enables you to select the operating conditions for the current report.

Power Report	
Select a Category: General Operating Conditions Options Breakdown by instance Frequency summary Probability summary	Operating Conditions Case: Typical
Help	OK Cancel

Figure 35 · SmartPower Power Report Dialog Box - Operating Conditions Panel

### **Options**

The Options panel enables you to select power and frequency units and to use toggle rates.



Power Report	
Select a Category: General Operating Conditions Difference Preakdown by instance Frequency summary Probability summary	Options Units Power: mW • Frequency: MHz •
Help	OK Cancel

Figure 36 · SmartPower Power Report Dialog Box - Options Panel

#### Units

Frequency: Sets unit preferences for frequency - Hz, KHz, MHz.

Power Units: Sets unit preferences for power - W, mW, or uW.

### **Use Toggle Rates**

When toggle rates are active (**Use Toggle Rates** box is checked), the data frequency of all the clock domains is defined as a function of the clock frequency. This updates the data frequency automatically when you update the clock frequency. Toggle rates enable you to specify the data frequency as a percentage of clock frequency, but you can no longer specify the data frequency as a number, only as a percentage of the clock frequency. To set the data frequency again, clear the **Use Toggle Rates** option.

### **Breakdown by Instance**

From this panel you can include the breakdown by instance in the report and set specific options.

Power Report		×
Select a Category: General Operating Conditions Options Breakdown by instance Frequency summary Probability summary	Include breakdown by instance         Include breakdown by instance         Limit the number of reported instances to         Report only instances with power greater than         Sort by:         Power Values         Sort order:         Descending	
Help	OK Cancel	

Figure 37 · SmartPower Power Report Dialog Box - Breakdown By Instance Panel

**Include breakdown by instance** – This section shows the power consumption of each element that has been instantiated in the design: gates, nets, memories, and IOs.

The breakdown by instance can be filtered by:

- Limit the number of reported instances to: will limit the number of instances reported to the specified number.
- Report only instances with power greater than: any instance with power consumption below the selected value will not be reported.

This section can be sorted by selecting the preferred method:

- Sort by: Name (alphabetical) or Power Values
- Sort Order: Ascending or Descending

Note: The filter reduces the number of lines in the report, one per instance.

### **Frequency Summary**

From this panel you can include the frequency summary in the report and set specific options.

Power Report		×
Select a Category: General Operating Conditions Options Breakdown by instance Frequency summary Probability summary	Include frequency summary         Limit the number of reported pins to         Report only pins with frequencies greater than         Sort by:         Frequency         Sort order:         Descending	z
Help	OK Cancel	

Figure 38 · SmartPower Power Report Dialog Box - Frequency Summary Panel

**Include frequency summary** – This section shows the frequency summary and reports the pin, net, domain, frequency, and frequency source for each pin.

The frequency summary can be filtered by:

- Limit the number of reported pins to: will limit the number of pins reported to the specified number.
- Report only pins with frequencies greater than: any pin with a frequency below the selected value will not be reported.

This section can be sorted by selecting the preferred method:

- Sort by: Pin Name, Net Name, Domain, Frequency, or Source
- Sort Order: Ascending or Descending

### **Probability Summary**

From this panel you can include the probability summary in the report and set specific options.



Power Report		×
Select a Category: General Operating Conditions Options Breakdown by instance Frequency summary Probability summary	Include probability summary         Sort by:         Pin Name         Sort order:         Descending	
Help	OK Cancel	

Figure 39 · SmartPower Power Report Dialog Box - Probability Summary Panel

**Include probability summary** – This section shows the probability summary and reports the driver, net, rate, source, and type for each pin.

This section can be sorted by selecting the preferred method:

- Sort by: Pin Name, Net Name, Rate, Source, or Type
- Sort Order: Ascending or Descending

Family:       IGLO         Die:       AGLE         Package:       484         Temperature Range:       COM         Voltage Range:       COM         Operating Conditions:       Typi         Operating Mode:       Acti         Data Source:       Adva         Power Summary	ftware, Releas 57 2008 _igloo 0 00V5 FBGA cal ve nced	e 8.4, Copyri		89-2008
Vendor:       Actel Corporation         Program:       Actel Designer Sc         Date:       Thu May 29 13:39:         Version:       3.0         Design:       fpgs         Family:       IGLO         Die:       AGL6         Package:       484         Temperature Range:       COM         Operating Conditions:       Typi         Operating Mode:       Acti         Data Source:       Adva         Power Summary	ftware, Releas 57 2008 _igloo 0 00V5 FBGA cal ve nced	e 8.4, Copyri		89-2008
Program:       Actel Designer Sc         Date:       Thu May 29 13:39:         Version:       3.0         Design:       fpga         Family:       IGLO         Die:       AGLA         Package:       484         Temperature Range:       COM         Voltage Range:       COM         Operating Conditions:       Typi         Operating Mode:       Acti         Data Source:       Adva         Power Summary	ftware, Releas 57 2008 0 0 00V5 FBGA cal ve nced +		.ght (C) 19	89-2008
Family:       IGLO         Die:       AGL6         Package:       484         Temperature Range:       COM         Voltage Range:       COM         Operating Conditions:       Typi         Operating Mode:       Acti         Data Source:       Adva         Power Summary	0 00V5 FBGA cal ve nced +			
+	Percentage   ++			
+	+			
Static Power   0.156   Dynamic Power   21.577 +	100.0% <sup> </sup>			
Breakdown by Instance 	0.7%     99.3%			
n445   Net   U44   I/C   U52   I/C	+	-+	I	
U44   I/C   U52   I/C		•	++	
U52   I/C	•	ADLIB:CLKE	UF	
1 n453 1 Mat		ADLIB:CLKE		
I maga l Mer	0.447	I	I	
U53   I/C		ADLIB:INBU	IF I	
LMDotIByteCtrLd   Net			I.	
PL/n_6   Net	•	•	I	
U100   I/C	1 0 200	ADLIB:OUTE		
U101   I/C		ADLIB:OUTE		
U104   I/C	0.209		10F	
	0.209   0.209	ADLIB:OUTE		
U106   I/C	0.209   0.209   0.209	ADLIB:OUTE   ADLIB:OUTE   ADLIB:OUTE		

Figure 40 · SmartPower Report

In addition to the information selected on the **Power Reports** dialog box, the report contains global design information.

**Global design information:** This section shows the target family, the package and the die. It also shows information about the operating conditions, speed grade, and power mode. This option is set by default.

#### See Also

Report (Power)

# Scenario Power Report

The scenario power report enables you to select a previously defined <u>scenario</u> and calculate the average power consumption and the battery life for this scenario.



#### To generate a scenario power report:

Note: In order to generate a scenario power report, your design must contain one or more scenarios.

- 1. From the Designer **Tools** menu, choose **Reports > Power > Power Scenario**. The Scenario Power Report dialog box appears.
- 2. Select the options you want to include in the report, and then click **OK**. The scenario power report appears in a separate window.

You can also generate the scenario power report from within SmartPower. From the **Tools** menu, choose **Reports > Scenario Power Report**, or click the **Scenario Power Report** button to open the Power Scenarios dialog box. By default, the report includes global design information and power sequencer summary. Specify which results you want to display by checking the boxes to be included in the report.

The power report dialog box is organized in the following panels: <u>General</u>, <u>Operating Conditions</u>, <u>Options</u>, and <u>Battery Life</u>.

### General

The general panel enables you to select what to include in the report, the report format, and the scenario you want to generate the report for.

Scenario Power Report		×
Select a Category: General Operating Conditions Options Battery life	Include in the report         Breakdown by rail         Breakdown by type         Breakdown by mode         Operating condition summary         Report format:         Text         Scenario:         scenario2	
Help	OK Cancel	

Figure 41 · SmartPower Scenario Power Report Dialog Box - General Panel

#### **Include in the Report**

Breakdown by Rail - This section shows the power consumption of each rail.

**Breakdown by Type** – This section enables reporting on the power consumption according to: gates, nets, clocks, core static, IOs, and memories.

Breakdown by Mode - This section enables reporting on the power consumption by mode.

Operating Condition Summary - This section reports the operating conditions.

#### **Report Format**

Select Text or CSV (Comma Separated Value) as the desired export format.

#### Scenario

Select a previously defined scenario to generate the report from.

### **Operating Conditions**

The Operating Conditions panel enables you to select the operating conditions case for the current design.



Scenario Power Report	
Select a Category: General Operating Conditions Options Battery life	Operating Conditions
Help	OK Cancel

Figure 42 · SmartPower Scenario Power Report Dialog Box - Operating Conditions Panel

### **Options**

The Options panel enables you to select power and frequency units and to use toggle rates.

Scenario Power Report	×
Select a Category: General Operating Conditions Diptions Battery life	Options Units Power: mW  Frequency: MHz Use toggle rates
Help	OK Cancel

Figure 43 · SmartPower Scenario Power Report Dialog Box – Options Panel

### Units

**Frequency:** Sets unit preferences for frequency – Hz, KHz, MHz. **Power Units:** Sets unit preferences for power – W, mW, or vW.

#### **Use Toggle Rates**

When toggle rates are active (**Use Toggle Rates** box is checked), the data frequency of all the clock domains is defined as a function of the clock frequency. This updates the data frequency automatically when you update the clock frequency. Toggle rates enable you to specify the data frequency as a percentage of clock frequency, but you can no longer specify the data frequency as a number, only as a percentage of the clock frequency. To set the data frequency again, clear the **Use Toggle Rates** option.



## **Battery Life**

The Battery Life panel enables reporting of the battery capacity and the battery life. Enter a battery capacity in MA/Hrs.

Scenario Power Report		×
Select a Category: General Operating Conditions Dotions Battery life	Battery life ✓ Include battery life Battery capacity: 1000.00 mA * Hrs	
Help	OK Cancel	

Figure 44 · SmartPower Scenario Power Report Dialog Box – Battery Life Panel

The SmartPower scenario power report returns the average power consumption and battery life for this sequence.

fpga_igloo - Powe	r_scenario Report				
e Actions Help					
Scenario Power	Report for de:	sign fpga_i	gloo with 1	the following settings:	
	el Designer Son May 29 13:42:3		ease 8.4, (	Copyright (C) 1989-2008	
Data Source:	IGLO AGL60 484 1 nge: COM COM itions: Typic	DOV5 FBGA cal nced			
Scenario Averag					
	Power (mW)	Percentag	e		
+   Total Power   Static Power   Dynamic Power +	10.926   0.138   10.788	100.0   1.3   98.7	*   *   *		
Battery Life +   Battery Capac +   Battery Life +	+ ity   1000.000 +	) mà*Hours Hours	+   + 		
Breakdown by mo				+	_4
Mode	Power in the 1	Mode (mW)	Duration	Power*Duration Weight	I
Mode Active     Mode Static     Mode Sleep		21.733   0.156   0.033	50.0% 35.0% 15.0%	0.5%   0.0%	 
++		+		+	-+

Figure 45 · SmartPower Scenario Power Report

In addition to the information selected on the **Scenario Power Reports** dialog box, the report contains global design information, a mode summary and the sequence average power.

**Global design information:** This section shows the target family, the package and the die. It also shows information about the operating conditions, speed grade and power mode. This option is set by default.

**Power Summary:** This section reports the power consumption of the sequence by mode. This option is set by default.

**Sequence Average Power:** This section reports the average power consumption of the sequence. This option is set by default.

#### See Also

Report (Sequencer)



# **Cycle-Accurate Power Reports**

Traditional power analysis based on a VCD simulation file reports an average power for the entire simulation time. Based on a VCD simulation file, the cycle-accurate power analysis will report one power value per clock period (or half-period) instead of an average power for the whole simulation. This feature allows to easily identify the worst cycle in terms of power performance; and helps to understand and further minimize power consumption by facilitating the analysis of data-dependent power variations, as well as dynamic power variations due to clock-gating, or even clock frequency variations.

#### To generate a cycle-accurate power report:

- 1. From the Designer **Tools** menu, choose **Reports > Power > Power Cycle Accurate**. The Cycle Accurate Power Report dialog box appears.
- 2. Select the options you want to include in the report, and then click **OK**. The cycle accurate power report appears in a separate window.

You can also generate the cycle accurate power report from within SmartPower. From the **Tools** menu, choose **Reports > Cycle Accurate Power Report** to open the cycle accurate power report dialog box; or select a vcd file from the Modes and Scenarios toolbar, and from the right-click menu, select **Tools > Power Cycle Accurate**.

The cycle-accurate power report dialog box is organized in the following panels: <u>General</u>, <u>Sampling Period</u>, <u>Partial Parsing</u>, <u>Top-Level Name</u>, <u>Glitch Filtering</u>, and <u>History Size Reduction</u>.

### General

Cycle Accurate Power Report		×
Select a Category: General Sampling period VCD parsing options Partial parsing Top level name Glitch filtering History size reduction	WCD file:       D:\work\code\design_vcd\BMotor.vcd         Report format:       Text         Use operating conditions from:       Active	
Help	OK Cancel	

Figure 46 · SmartPower Cycle Accurate Power Report Dialog Box – General **VCD file** - Select the VCD file you want to import.

**Report format** – Select **Text** or **CSV** (Comma Separated Value) as the desired export format. **Use operating conditions from** – Select the mode from which the operating conditions will be used.

## **Sampling Period**

**Partial Parsing** 

Cycle Accurate Power Report		$\mathbf{X}$
Select a Category: General Sampling period VCD parsing options Partial parsing Top level name Glitch filtering History size reduction	Sampling period            • Automatic detection from clock:         • PWM_clk         •         • Compute an average value per clock period         • Compute an average value per half clock period         • Compute an average value per half clock period         • Specify:         • Period:         • Offset:         • Offset:	
Help	OK Cancel	

Figure 47 · SmartPower Cycle Accurate Power Report Dialog Box – Sampling Period

Automatic detection from clock – This option automatically detects the sampling period from the fastest clock. You can also select any other clock in your design. You can specify whether the average value is computed per period or half-period.

Specify – Select this option to specify the period and offset used to calculate the sampling period.

Select a Category: General	Partial parsing	
Sampling period VCD parsing options Partial parsing Top level name Glitch filtering History size reduction	✓ Partially parse VCD         Start time:         End time:	0.00 ns 10000.00 ns
Help		OK Cancel

Figure 48 · SmartPower Cycle Accurate Power Report Dialog Box – Partial Parsing

**Partially parse VCD file** – Specify the Start and End times to partially parse the VCD file. This option can be used for large VCD files.



## **Top-Level Name**

Cycle Accurate Power Report	
Select a Category:	Top level name
General Sampling period VCD parsing options Partial parsing Top level name Glitch filtering History size reduction	Automatic detection     Specify:
Help	OK Cancel

Figure 49 · SmartPower Cycle Accurate Power Report Dialog Box – Top-Level Name

This option enables you to select how the top-level name is specified. Select **Automatic Detection** to let the VCD reader automatically detect the top-level name of the design, or select **Specify** to manually specify the top-level name.

### **Glitch Filtering**

Cycle Accurate Power Report	
Select a Category: General Sampling period VCD parsing options Partial parsing Top level name Glitch filtering History size reduction	Glitch filtering C Off Automatic glitch filtering Specify filtering threshold: 100 ps
Help	OK Cancel

Figure 50 · SmartPower Cycle Accurate Power Report Advanced Options Dialog Box – Glitch Filtering

This panel enables you to filter out pulses of short durations by selecting **Automatic Glitch Filtering** or by entering a value in the **Specify Filtering Threshold** field. The default glitch filtering option is **Automatic Glitch Filtering**.

## **History Size Reduction**

Cycle Accurate Power Report	
Select a Category: General Sampling period VCD parsing options Partial parsing Top level name Glitch filtering History size reduction	History size reduction ✓ Keep only local extrema ✓ Set power threshold: 0.00 mW
Help	OK Cancel

Figure 51 · SmartPower Cycle Accurate Power Report Advanced Options Dialog Box – History Size Reduction This panel enables you to limit the history size by keeping only local extrema or setting a power threshold. The results are displayed in the cycle accurate power report below.



		ccurate Report			
ile Actions	Help				
	rporation - Actel 1 t (c) 1989-2008	Designer Softwa	re Release 8	.4 (Version 8.4.0.0	)
Date: Thu	u May 29 13:53:58 2	2008			
Design : Family :	simple_PWM_8				
Die : AGI					
-	: 256 FBGA				
-	ure Range : COM				
-	Range : COM g Conditions : Typ:	icel			
	g Conditions : Typ. g Mode : Static	ICAI			
	rce : Advanced				
Vcd File:	: D:/work/code/des:	ign_vcd/BMotor.v	ved		
Max Power	r Report				
++	+				
	Start Time (ps) +				
	2000000 +		0.508 +	 +	
Cycle Bas	-	+	+	+	
Cycle Bas +	sed Power Report  Start Time (ps)	+   End Time(ps)	+	+	
Cycle Bas +	+ sed Power Report +   Start Time (ps) +	+   End Time(ps) +	+   Power(mW) +	+	
Cycle Bas +	sed Power Report  Start Time (ps) 	+   End Time(ps)   100000   200000	+	+	
+ Cycle Bas +   Cycle   +   1   2   1 1	sed Power Report 	+	+	+	
Cycle Bas 	sed Power Report    Start Time (ps)    0   100000   100000   1200000   1500000	<pre></pre>	+	+	
Cycle Bas +   Cycle   +   1     2     11     13     16     17	sed Power Report 	End Time(ps) 100000 200000 1100000 1300000 1600000 1700000	+   Power(mW) +   0.101   0.161   0.161   0.207   0.182   0.203	+	-
Cycle Bas 	sed Power Report   Start Time (ps)   0   100000   1200000   1200000   1500000   1600000   1700000	End Time(ps) 100000 200000 1100000 1300000 1300000 1600000 1700000	+	+	
Cycle Bas 	sed Power Report 	End Time(ps) 100000 200000 1100000 1300000 1600000 1700000 1800000 2100000	+   Power(mW) +   0.101   0.161   0.161   0.207   0.182   0.203   0.180   0.508	+	
Cycle Bas +	sed Power Report 	End Time(ps) 200000 100000 1100000 1300000 1600000 1700000 1200000 2200000 2200000	+	+	
Cycle Bas +	sed Power Report 	<pre>End Time(ps) 100000 200000 1100000 1300000 1300000 1700000 1800000 2200000 2200000 2300000</pre>	<pre> Power (mW)  O.101 O.161 O.161 O.207 O.182 O.203 O.180 O.508 O.180 O.180 O.180 O.180<o.180 o.180="" o.180<="" td=""><td>+</td><td></td></o.180></pre>	+	
Cycle Bas 	sed Power Report 	<pre>     End Time(ps)     100000     200000     1100000     1300000     1600000     1600000     1800000     2100000     2200000     2300000     2400000     2500000</pre>	+	+	
Cycle Bas 	sed Power Report 	End Time(ps) 100000 200000 1100000 1300000 1600000 1700000 2100000 2200000 2200000 2300000 2400000 2500000 2600000	<pre> Power(mW)  O.101 0.161 0.161 0.207 0.182 0.203 0.180 0.180 0.180 0.180 0.188 0.180 0.188 0.182 0.182 0.182 0.182 0.182 0.182&lt;0.182&lt;0.183 0.180 0.180 0.182&lt;0.182&lt;0.183 0.180 0</pre>	+	
Cycle Bas 	sed Power Report 	End Time(ps) 100000 200000 1100000 1300000 1600000 1700000 2100000 2200000 2300000 2400000 2400000 2400000 2400000 2900000	<pre> Power(mW)  0.101 0.161 0.161 0.207 0.182 0.203 0.180 0.180 0.180 0.180 0.188 0.188 0.182 0.182 0.182 0.182 0.199 0.180 0.238</pre>	+	
Cycle Bas 	sed Power Report 	End Time(ps) 100000 200000 1100000 1300000 1600000 1700000 1800000 2200000 2200000 2300000 2400000 2500000 2600000 3000000	<pre> Power (mW)  0.101 0.161 0.161 0.207 0.182 0.203 0.180 0.180 0.180 0.188 0.182 0.182 0.182 0.182 0.182 0.182 0.182 0.182 0.182 0.182 0.180 0.180 0.180 0.180 0.180 0.180</pre>	+	
Cycle Bas 	sed Power Report 	End Time(ps) 100000 200000 1100000 1300000 1300000 1700000 1700000 2200000 2200000 2400000 2400000 2600000 2600000 3000000 3000000 3100000	<pre> Power(mW)  0.101 0.161 0.161 0.207 0.182 0.203 0.180 0.180 0.180 0.180 0.188 0.188 0.182 0.182 0.182 0.182 0.199 0.180 0.238</pre>	+	

Figure 52 · SmartPower Cycle Accurate Power Report

# Activity and Hazards Reports

Traditional Power Analysis based on a VCD simulation file reports an average power value that will account for all nets switching in the design. This switching includes functional transitions and spurious transitions. Due to the delay of each gate, paths arriving at one internal gate may have different propagation delays. Therefore, a gate may exhibit multiple spurious transitions before settling to the correct logic level. The Activity and Hazards Power Report allows to quickly identify gates and nets of the design that consume power because of spurious transitions. This is helpful to understand and further minimize power consumption. The activity and hazards report reads a VCD file and reports transitions and hazards for each clock cycle of the VCD file.

#### To generate an activity and hazards power report:

1. From the Designer **Tools** menu, choose **Reports > Power > Power Activity and Hazards**. The Activity and Hazards Power Report dialog box appears.

2. Select the options you want to include in the report, and then click **OK**. The activity and hazards report appears in a separate window.

You can also generate the activity and hazards report from within SmartPower. From the **Tools** menu, choose **Reports > Activity and Hazards Report**; or select a vcd file from the Modes and Scenarios toolbar, and from the right-click menu, select **Tools > Power Activity and Hazards** 

The activity and hazards report dialog box is organized in the following panels: <u>General</u>, <u>Partial Parsing</u>, <u>Top-Level Name</u>, <u>Glitch Filtering</u>, and <u>Clock Domains</u>.

### General

Activity And Hazards Power Repor	t	×
Select a Category:	General	
General VCD parsing options — Partial parsing — Top level name — Glitch filtering Clock domains	VCD file: D:\work\code\design_vcd\BMotor.vcd   Report format: Text Use operating conditions from: Active  Report type: Report by Net - summary  For each net, report activity and power; sort by total power; sort order descending; Limit the number of reported nets to 40.	
Help	OK Cancel	

Figure 53 · SmartPower Activity and Hazards Report Dialog Box – General **VCD file** – Select the VCD file you want to import.

**Report format** – Select **Text** or **CSV** (Comma Separated Value) as the desired export format. **Use operating conditions from** – Select the mode from which the operating conditions will be used.

**Report type** – Select the report type:

- Report by net summary: summary report by net
- Report by net detailed: detailed report by cycle
- Report by cycle summary: summary report by net
- Report by cycle detailed: detailed report by cycle

The selected report type reports activity and power for each net sorted by power in descending order and limits the number of reported nets to 20 by default. To change these options, click each option and from the pop-up menu, select the desired option:

- Report: Select the query report type: activity, power, or activity and power.
- Sort by: Select the query sort by functional power, functional transitions, spurious power, spurious transitions, or total power.
- Sort order: Select the query sort order: ascending or descending.
- Limit the number of reported nets: Enter the query filter limit.



## **Partial Parsing**

Activity And Hazards Power Repo	rt	×
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Clock domains	✓ Partially parse VCD         Start time:       0.00         End time:       10000.00	
Help	OK Cancel	

Figure 54 · SmartPower Activity and Hazards Report Dialog Box – Partial Parsing

**Partially parse VCD file** – Specify the Start and End times to partially parse the VCD file. This option can be used for large VCD files.

### **Top-Level Name**

Activity And Hazards Power Repor	t	×
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Clock domains	Automatic detection     Specify:	
Help	OK Cancel	

Figure 55 · SmartPower Activity and Hazards Report Dialog Box – Top-Level Name

This option enables you to select how the top-level name is specified. Select **Automatic Detection** to let the VCD reader automatically detect the top-level name of the design, or select **Specify** to manually specify the top-level name.

### **Glitch Filtering**

Activity And Hazards Power Repor	t 🔀
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Clock domains	Glitch filtering         Automatic glitch filtering         Specify filtering threshold:         100
Help	OK Cancel

Figure 56 · SmartPower Activity and Hazards Report Advanced Options Dialog Box – Glitch Filtering

This option enables you to filter out pulses of short durations by selecting **Automatic Glitch Filtering** or by entering a value in the **Specify Filtering Threshold** field. The default glitch filtering option is **Automatic Glitch Filtering**.

## **Clock Domains**

Activity And Hazards Power Repor	t 🛛
Select a Category:	Clock domains
General VCD parsing options Partial parsing	Clock domain  • Automatic construction
Top level name Glitch filtering Clock domains	C Specify: Period: 10000.00 ps
	First edge: 0.00 ps
	Clock domain Active clock Active edge
	1 PWM_clk true ▼ rising ▼ 2 un1_dataa_int_NE true ▼ rising ▼
Help	OK Cancel

Figure 57 · SmartPower Activity and Hazards Report Advanced Options Dialog Box – Clock Domains The clock domain can be automatically constructed or it can be specified by the user.

Automatic construction – This option automatically constructs the clock domain. SmartPower automatically analyzes your design to assess if a clock is active and what is the active edge. **Specify** – Select this option to specify the period and first edge.

Use the clock domain table to set the active edge (rising, falling or both) and to set a clock as transparent. The results are displayed in the activity and hazards power report below.



Actions Help							
tivity map	report						
tel Cornore	tion - Actel Deg	igner Software Release	8 4 (176)	eion 8 4 0 0)			
pyright (c)		igner sorceare kerease	0.1 (70)	.5101 0.1.0.0)			
	06 10:43:59 200	8					
esign : simp	le_PWM_8						
amily : IGLO							
le : AGL600V							
ackage : 256 mperature R							
oltage Range							
	ditions : Typica	1					
erating Mod							
ata Source :	Advanced						
d file: D:/	work/code/design	_vcd/BMotor.vcd					
tivity Map		+					
		Dynamic Power (mW)					
		+					
Total	44184	0.155					
Functional	32364	0.128					
Spurious		0.027					
	11820   ++-						
	++-						
tivity Map:	Net Summary	÷					
tivity Map:	Net Summary	+			+		
tivity Map:	Net Summary	+	Type	Functional		Functional	Spurious
tivity Map:	Net Summary	+	Type	Functional	Spurious   Transitions	Functional   Power	
tivity Map: Net	Net Summary	Clock Domain   I	Type     	Functional Transitions	Spurious   Transitions	Functional   Power	Spurious     Power
tivity Map: Net PWM_clk_c	Net Summary		Type     	Functional Transitions 5999	Spurious   Transitions   +	Functional   Power   (mW) +	Spurious     Power     (mW)   ++   0.000
vivity Map: Net PWM_clk_c PWM_clk_c_0	Net Summary	<pre></pre>	Type         Clock   Clock	Functional Transitions 5999 5999	Spurious   Transitions   +   O   O	Functional   Power   (mW) +	Spurious     Power     (mW)   ++   0.000     0.000
PWM_clk_c Qaux[0]	Net Summary	/ Clock Domain         PWM_clk   PWM_clk   PWM_clk   unldata_int_NE:Y	Type       Clock   Clock   Data	Functional Transitions 5999 5999 1	Spurious   Transitions     0   0   2986	Functional   Power   (mW) +	Spurious     Power     (mW)   ++   0.000     0.000     0.013
Tivity Map: Net PWM_clk_c PWM_clk_c0 Qaux[0] PWM_clk_pad	Net Summary	<pre></pre>	Type       Clock   Clock   Data   Clock	Functional Transitions 5999 5999 1 5999	Spurious   Transitions   	Functional   Power   (mW) +	Spurious     Power     (mV)   +
PWM_clk_c PWM_clk_c Qaux[0] PWM_clk_pad Qaux[1]	<pre>Net Summoary ///UO/NET1</pre>	<pre>/ Clock Domain / / / PUM_clk / PUM_clk / unl_dataa_int_NE:Y / PUM_clk / unl_dataa_int_NE:Y</pre>	Type       Clock   Clock   Clock   Data   Clock   Data	Functional Transitions 5999 5999 1 5999 1	Spurious   Transitions      0   2986   0   1492	Functional   Power   (mW)   0.090   0.019   0.000   0.010   0.000	Spurious     Power     (mW)   ++   0.000     0.000     0.000     0.005
PWM_clk_c PWM_clk_c PWM_clk_c Qaux[0] PWM_clk_pad Qaux[1] uu3_qaux_U1	<pre>Net Summoary ///UO/NET1</pre>	<pre>/ Clock Domain / / / PUM_clk / PUM_clk / unl_dataa_int_NE:Y / PUM_clk / unl_dataa_int_NE:Y / unl_dataa_int_NE:Y / PUM_clk</pre>	Type       Clock   Clock   Data   Clock   Data   Data	Functional Transitions 5999 5999 1 5999 1 1 746	Spurious   Transitions      0   0   2986   0   1492   0	Functional   Power   (mW) +	Spurious     Power     (mV) + +
PWM_clk_c PWM_clk_c PWM_clk_c PWM_clk_c Qaux[0] PWM_clk_pad Qaux[1] un3_qqux_U1 Qaux[2]	<pre>Net Summoary ///UO/NET1</pre>	<pre>/ Clock Domain / / / / / / / / / / / / / / / / / / /</pre>	Type       Clock   Clock   Data   Clock   Data   Data   Data	Functional Transitions 5999 5999 1 5999 1 746 0	Spurious   Transitions   	Functional   Power   (mW) +	Spurious     Power     (mW)   ++   0.000     0.000     0.000     0.005
PWM_clk_c PWM_clk_c Qaux[0] PWM_clk_pad Qaux[1]	Net Summoary /UO/NET1 	<pre>/ Clock Domain / / / PUM_clk / PUM_clk / unl_dataa_int_NE:Y / PUM_clk / unl_dataa_int_NE:Y / unl_dataa_int_NE:Y / PUM_clk</pre>	Type     Clock   Clock   Data   Data   Data   Data	Functional Transitions 5999 5999 1 5999 1 746 0 23	Spurious   Transitions     0   0   2986   0   1492   0   746   350	Functional   Power   (mW) +	Spurious     Power     (mW)   +
Tivity Map: Net PUM_clk_c PUM_clk_c Qaux[0] PUM_clk_pad Qaux[1] un3_gaux_U1 Qaux[2] Qaux[3]	Net Summoary /UO/NET1 	<pre>/ Clock Domain / / Clock Domain / / / PWM_clk / PWM_clk / unl_dataa_int_NE:Y / PWM_clk / unl_dataa_int_NE:Y / PWM_clk / unl_dataa_int_NE:Y / unl_dataa_int_NE:Y / unl_dataa_int_NE:Y / unl_dataa_int_NE:Y</pre>	Type     Clock   Clock   Data   Data   Data   Data	Functional Transitions 5999 5999 1 5999 1 746 0 23 1	Spurious   Transitions   0   0   2986   0   1492   0   746   350   2986	Functional   Power   (mW)   0.090   0.019   0.000   0.000   0.000   0.000   0.000   0.000   0.000	Spurious     Power     (mW)     0.000     0.000     0.000     0.005     0.000     0.003     0.003
rtivity Map: Net PWM_clk_c PWM_clk_c_0 Qaux[0] PWM_clk_pad Qaux[1] un3_qaux_U1 Qaux[2] Qaux[3] un1_dataa_i I_4 I_5	Vet Summary /UO/NET1 _DWACT_FINC_E[0] nt_0_i	<pre>Clock Domain Clock Domain PFUM_clk Uni_dataa_int_NE:Y FUM_clk Uni_dataa_int_NE:Y FUM_clk Uni_dataa_int_NE:Y Uni_dataa_int_NE:Y Uni_dataa_int_NE:Y Uni_dataa_int_NE:Y Uni_dataa_int_NE:Y FUM_clk FUM_clk</pre>	Type     Clock   Clock   Data   Data   Data   Data   Data   Data   Data	Functional Transitions 5999 5999 1 5999 1 746 0 23 1 231 1 2987 1494	Spurious   Transitions     0   2986   0   1492   0   746   350   2986   0   0	Functional   Power   (mW)   0.090   0.019   0.000   0.000   0.000   0.000   0.000   0.000   0.000   0.001	Spurious     Power     (mW)     0.000     0.000     0.000     0.000     0.000     0.003     0.003     0.002     0.001
PUM_clk_c PUM_clk_c PUM_clk_cO Qaux[0] PUM_clk_pad Qaux[1] un3_qaux_U1 Qaux[2] Qaux[3] un1_dataa_i I_5 PUM_cout_pad	<pre>Net Summary /UO/NET1 _DWACT_FINC_E[0] nt_0_1 /UO/NET1</pre>	<pre>/ Clock Domain / / PUM_clk / PUM_clk / PUM_clk / uni_dataa_int_NE:Y / PUM_clk / uni_dataa_int_NE:Y / PUM_clk / uni_dataa_int_NE:Y / uni_dataa_int_NE:Y / uni_dataa_int_NE:Y / uni_dataa_int_NE:Y / PUM_clk / PUM_clk / PUM_clk / Uni_dataa_int_NE:Y / PUM_clk / Uni_dataa_int_NE:Y // Uni_dataa_int_N</pre>	Type Clock Clock Data Clock Data Data Data Data Data Data Data	Functional Transitions 5999 5999 1 5999 1 746 0 23 1 2387 1494 21	Spurious   Transitions   0 2986   0 1492   0 1492   0 1492   0 2866   2986   2986   0   0   0	Functional   Power   (mW)   0.090   0.019   0.000   0.000   0.000   0.000   0.000   0.000   0.000   0.001	Spurious     Power     (mW)     0.000
PWM_clk_c PWM_clk_c PWM_clk_c Qaux[0] PWM_clk_pad Qaux[1] un_qaux_U1 Qaux[2] Qaux[2] unl_dataa_i I_4 I_5 PWM_out_pad unl_dataa_i	<pre>Net Summary /UO/NET1 _DWACT_FINC_E[0] nt_0_1 /UO/NET1</pre>	<pre>Clock Domain  PWM_clk PWM_clk Unl_dataa_int_NE:Y PWM_clk Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y PWM_clk PUM_clk Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y</pre>	Type Clock Clock Clock Data Data Data Data Data Data Data Dat	Functional Transitions 5999 5999 1 5999 1 746 0 23 1 2987 1494 21 1	Spurious   Transitions     0   0   2986   0   1492   0   746   350   2986   0   0   0   0   1492	Functional   Power   (mW)   0.090   0.000   0.000   0.000   0.000   0.000   0.000   0.000   0.001   0.001   0.001   0.001	Spurious     Power     (nwU)   
Thirty Map: Net PWM_clk_c PWM_clk_c_0 Qaux[0] PWM_clk_pad Qaux[1] un3_qaux_U1 Qaux[2] Qaux[3] un1_dataa_i I_5 PWM_out_pad un1_dataa_i I_5	<pre>Net Summary /UO/NET1 _DWACT_FINC_E[0] nt_0_1 /UO/NET1</pre>	<pre>Clock Domain Clock Domain PPUM_clk PUM_clk Un1_dataa_int_NE:Y PUM_clk Un1_dataa_int_NE:Y PUM_clk Un1_dataa_int_NE:Y UN1_da</pre>	Type Clock Clock Data Clock Data Data Data Data Data Data Data Dat	Functional Transitions 5999 5999 1 5999 1 746 0 23 1 2987 1494 21 1 1 747	Spurious   Transitions     0   2986   0   1492   0   746   350   2986   0   0   0   1492   0	Functional   Power   (mW) +	Spurious     Power     (nw)   
PWM_clk_c PWM_clk_cO Qaux[0] PWM_clk_pad Qaux[1] un3_qaux_U1 Qaux[3] un1_dataa_i I_5 PWM_out_pad un1_dataa_i I_5 PWM_out_pad un1_dataa_i I_9 Qaux[4]	<pre>Net Summary /UO/NET1 _DWACT_FINC_E[0] nt_0_1 /UO/NET1</pre>	<pre>Clock Domain Clock Domain</pre>	Type Clock Clock Data Data Data Data Data Data Data Dat	Functional Transitions 5999 5999 1 5999 1 746 0 23 1 2987 1994 21 1 747 2	Spurious   Transitions   0   0   2986   0   1492   0   746   350   2986   0   0   0   0   1492   0   1492   0   184	Functional   Power   (mW)   0.090   0.019   0.000   0.000   0.000   0.000   0.000   0.000   0.001   0.001   0.001   0.001   0.000   0.000	Spurious     Power     (mW)     0.000     0.000     0.000     0.000     0.000     0.003     0.003     0.000
Net PWM_clk_c PWM_clk_c PWM_clk_c Qaux[0] PWM_clk_pad Qaux[1] unl_qaux_[1] Qaux[2] Qaux[2] Qaux[2] Qaux[2] PWM_out_pad unl_dataa_i I_9 Qaux[4] I_13 Qaux[4] Qau	<pre>Net Summary /UO/NET1 WACT_FINC_E[0] nt_0_i /UO/NET1 nt_1_i</pre>	<pre>Clock Domain  PUM_clk PUM_clk Unl_dataa_int_NE:Y PUM_clk Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y PUM_clk PUM_clk Unl_dataa_int_NE:Y PUM_clk Unl_dataa_int_NE:Y PUM_clk Unl_dataa_int_NE:Y PUM_clk Unl_dataa_int_NE:Y PUM_clk</pre>	Type     Clock   Clock   Data   Data	Functional Transitions 5999 5999 1 5999 1 746 0 23 1 2987 1494 21 1 747 2 373	Spurious   Transitions     0   0   2986   0   1492   0   746   350   2986   0   0   0   0   1492   0   1492   0   1492   374	<pre>Functional Power ( mW)</pre>	Spurious     Power     (nW)     .(nW)     .0.000     0.000     0.003     0.003     0.003     0.003     0.000     0.000
PWM_clk_c PWM_clk_cO Qaux[0] PWM_clk_pad Qaux[1] un3_qaux_U1 Qaux[3] un1_dataa_i I_5 PWM_out_pad un1_dataa_i I_5 PWM_out_pad un1_dataa_i I_9 Qaux[4]	<pre>Net Summary /UO/NET1 WACT_FINC_E[0] nt_0_i /UO/NET1 nt_1_i</pre>	<pre>Clock Domain  PUM_clk PUM_clk Unl_dataa_int_NE:Y PUM_clk Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y Unl_dataa_int_NE:Y PUM_clk PUM_clk Unl_dataa_int_NE:Y PUM_clk Unl_dataa_int_NE:Y PUM_clk Unl_dataa_int_NE:Y PUM_clk Unl_dataa_int_NE:Y PUM_clk</pre>	Type Clock Clock Data Data Data Data Data Data Data Dat	Functional Transitions 5999 5999 1 5999 1 746 0 23 1 2987 1494 21 1 1 747 2 373 746	Spurious   Transitions     0   2986   0   2986   0   1492   0   746   350   2986   0   0   1492   0   1492   0   184   374   0	Functional   Power   (mW)   0.090   0.019   0.000   0.000   0.000   0.000   0.000   0.001   0.001   0.001   0.001   0.001   0.001   0.000   0.000   0.000   0.000	Spurious     Power     (mW)     0.000     0.000     0.000     0.000     0.000     0.003     0.003     0.000

Figure 58 · SmartPower Activity and Hazards Report

# Cycle-Accurate Power Analysis

The Cycle-Accurate Power Analysis reports cycle-accurate power data in a graphical form. In the analysis window, you can specify ranges and compute averages for each range, define a list of watched blocks, obtain power usage of a single block or cycle, or obtain power usage of multiple blocks over several cycles.

#### To generate a cycle-accurate power analysis:

- From the SmartPower Tools menu, choose cycle-accurate Power Analysis; or select a vcd file from the Modes and Scenarios toolbar, and from the right-click menu, select Tools > cycle-accurate Power Analysis. The cycle-accurate Power Analysis dialog box appears.
- 2. Select the options you want to include in the report, and then click **OK**. The cycle-accurate power report appears in a separate window.

The cycle-accurate power analysis dialog box is organized in the following panels: <u>General</u>, <u>Sampling</u> <u>Period</u>, <u>Partial Parsing</u>, <u>Top-Level Name</u>, and <u>Glitch Filtering</u>.

## General

Cycle Accurate Power Analysis		×
Select a Category: General Sampling period VCD parsing options Partial parsing Top level name Glitch filtering	CD file:       de\for SmartPower\vishal_fpu_A3P1000.vcd          Use operating conditions from:       Active	
Help	OK Cancel	

Figure 59  $\cdot$  SmartPower cycle-accurate Power Analysis Dialog Box – General **VCD file** – Select the VCD file you want to import.

Use operating conditions from - Select the mode from which the operating conditions will be used.

## **Sampling Period**

Cycle Accurate Power Analysis		×
Select a Category: General Sampling period VCD parsing options Partial parsing Top level name Glitch filtering	Sampling period  Automatic detection from clock:  Carbon Compute an average value per clock period  Compute an average value per half clock period  Specify:  Period: 10000.00 Ps Offset: 0.00 Ps	
Help	OK Cancel	

Figure 60 · SmartPower cycle-accurate Power Analysis Dialog Box – Sampling Period

Automatic detection from clock – This option automatically detects the sampling period from the fastest clock. You can also select any other clock in your design. You can specify whether the average value is computed per period or half-period.

Specify – Select this option to specify the period and offset used to calculate the sampling period.



## **Partial Parsing**

Cycle Accurate Power Analysis		×
Select a Category: General Sampling period VCD parsing options Partial parsing Top level name Glitch filtering	✓ Partially parse VCD         Start time:       0.00         End time:       10000.00	
Help	OK Cancel	

Figure 61 · SmartPower cycle-accurate Power Analysis Dialog Box – Partial Parsing

**Partially parse VCD file** – Specify the Start and End times to partially parse the VCD file. This option can be used for large VCD files.

## **Top-Level Name**

Cycle Accurate Power Analysis		×
Select a Category: General Sampling period VCD parsing options Partial parsing Top level name Glitch filtering	• Automatic detection         • Specify:	
Help	OK Cancel	

Figure 62 · SmartPower cycle-accurate Power Analysis Dialog Box – Top-Level Name

This option enables you to select how the top-level name is specified. Select **Automatic Detection** to let the VCD reader automatically detect the top-level name of the design, or select **Specify** to manually specify the top-level name.

## **Glitch Filtering**

Cycle Accurate Power Analysis	
Select a Category: General Sampling period VCD parsing options Partial parsing Top level name Glitch filtering	Glitch filtering C Off Automatic glitch filtering Specify filtering threshold: 100 ps
Help	OK Cancel

Figure 63 · SmartPower cycle-accurate Power Analysis Advanced Options Dialog Box – Glitch Filtering

This option enables you to filter out pulses of short durations by selecting **Automatic Glitch Filtering** or by entering a value in the **Specify Filtering Threshold** field. The default glitch filtering option is **Automatic Glitch Filtering**.



### **Cycle-Accurate Power Analysis Window**

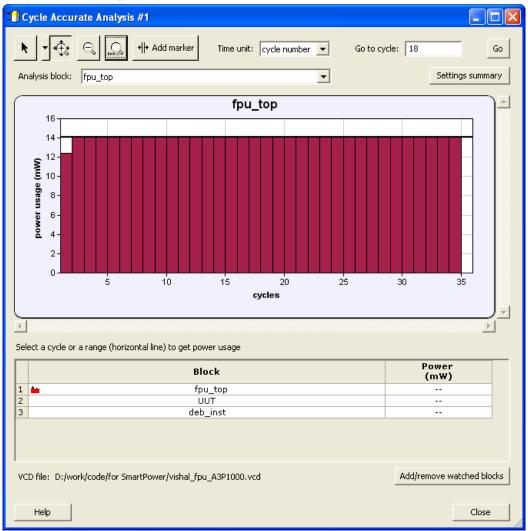


Figure 64 · cycle-accurate Power Analysis

Mouse over a cycle to obtain the cycle number, the start and end times, and the power usage for the selected cycle.

Use the **Select** button to select a cycle in the analysis, the grid displays the block name and power usage for the watched blocks.

Us the Add Marker button to create cycle ranges - intervals between markers and/or the simulation ends.

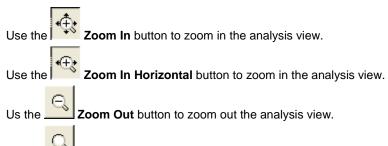
To select a range, mouse over the average power usage horizontal line. This will display the average power usage for the range.

To move to the beginning or end of a range, right-click the average power usage of the range and select **Go** to **Beginning of Range** or **Go to End of Range**.

To move the marker to another cycle, click and drag the marker to another cycle; or from the right-click menu, select **Move marker**, and enter a time value.

To delete the marker, right-click the marker, and select **Delete marker**.

To move to the previous or next markers, right-click the marker, and select **Go to previous marker** or **Go to** previous marker.



Us the **Zoom to Full View** button to zoom into full view.

To view the most power-consuming blocks for a cycle, right-click the cycle, and select **Show Most Consuming Blocks for this Cycle**. This opens the Biggest Power Contributors for Cycle window.

Bigge	est power contributors for cycle	8
	Block	Power (mW)
1	🛀 fpu_top	14.083
2	UUT	0.257
3	UUT/u6/II_0/U1	0.129
4	UUT/u6/II_0	0.129
5	UUT/u6	0.129
6	UUT/u4	0.033
7	UUT/u5	0.023
Help		

Figure 65 · Biggest Power Contributors for a Cycle Window

To view the analysis for a specific time, enter a time value in the **Go to time** box, select the time unit, and press the **Go** button.

To view the analysis for a specific block, select the block from the **Analysis Block** pull-down.

To export the cycle-accurate power analysis chart, right-click the chart, and select **Export Chart to File**. You can modify the blocks you want to watch during analysis, by pressing the **Add/Remove Watched** 

Blocks button.

If the operating conditions in SmartPower have been modified, a warning appears to indicate that the settings have been changed. Click the hyperlink to regenerate the Cycle-Accurate analysis view.

Click the View Settings Summary button to display the cycle-accurate settings.



Cycle Accurate Settings Summ	
Setting	Value
VCD file	D:/work/code/for SmartPower/vish
Operating conditions from mode	Active
Sampling period	autodetected from clock
Clock name	clk
Compute average per	period
Autodetect top level name	true
Partial parsing	true
Start time	0.000 ns
Stop time	10000.000 ns
Glitch filtering	auto
Glitch filtering threshold	300 ps
1	
	Close

Figure 66 · Cycle-Accurate Settings Summary

Click the **Add/Remove Watched Blocks** button to display a list of watched blocks . You can add or remove watched blocks by checking or unchecking the **Watch** checkbox for that particular block(s) or by selecting blocks in the grid and using the **Check** or **Uncheck Selected Blocks** buttons. You can use the filter options to hide or display the list of blocks based on the criteria entered.

Wate	:h blocks	×
	ck below the block(s) you want to watch during cycle accurate analysis: ck: * Show:	All Blocks
	Block	Watch 🔷
1	fpu_top	
2	UUT	
3	deb_inst	
4	UUT/u3	
5	UUT/u2	
6	UUT/u0	
7	UUT/u4	
8	UUT/u6	
9	UUT/u1	
10	UUT/u5	
11	UUT/u6/II_0	
Ch	eck selected blocks	Select All
	Help Of	Cancel

Figure 67 · Watched Blocks

# Importing a VCD File

The Value Change Dump (VCD) file is a simulation file. The format of this file is specified in the IEEE 1364 standard.

You can configure the Project Manager to automatically generate VCD files using Model Sim.

You can also generate a VCD file with a ModelSim simulator using the following commands:

```
vcd file example.vcd
vcd add -r /testbench/<top>_0/*
run 1 us
vcd flush
```

This example creates a VCD file example.vcd, adds all signals recursively, runs the simulation for one micro second, and quits. You must quit Model *Sim* in order to get an accurate result from SmartPower.

If you have not yet completed the layout of the design, the design software guides you through place-androute so that you can import the VCD file. In order to successfully annotate your VCD values to the design, Designer must complete place-and-route even if you generated your VCD file using timing simulation (prelayout).

Note: SmartPower has been validated with VCD files generated by Model*Sim*. However, you may use any Verilog/VHDL simulator that offers a VCD dump feature.

Refer to the user manual of your simulation tool for more information on how to generate a VCD file.

#### To import a VCD file:

1. From the Simulation menu, select Import VCD File. This opens the Import VCD Options dialog box.

Import VCD Options		×
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Remaining signals	General         VCD file:       D:\work\code\sub.vcd         Import in:         Existing mode:         New mode:	
Help	OK Cancel	

Figure 68 · Import VCD File Dialog Box

- 2. Select the VCD file you want to import and select a mode to import it in, or click **New Mode** and enter a mode name.
- 3. Select the options you want to specify:

**Partial Parsing** — Specify the **Start** and **End Times** to partially parse the VCD file. This option can be used for large VCD files.



Import VCD Options		$\mathbf{X}$
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Remaining signals	Partial parsing Partially parse VCD Start time: 0.00 ns End time: 10000.00 ns	
Help	OK Cancel	

Figure 69 · Import VCD File Dialog Box — Partial Parsing

**Top-Level Name** — This option enables you to select how the top-level name is specified. The **Top Level Name** is the instance name of your design instantiated in the simulation testbench. Select **Automatic Detection** to let the VCD reader automatically detect the top-level name of the design, or

select Specify to manually specify the top-level name.	
Import VCD Options	
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Remaining signals	Automatic detection     Specify:
Help	OK Cancel

Figure 70 · Import VCD File Dialog Box — Top-Level Name

**Glitch Filtering** — This option enables you to filter out pulses of short durations by selecting **Automatic Glitch Filtering** or by entering a value in the **Specify Filtering Threshold** field. The default option is **Automatic Glitch Filtering**.



Import VCD Options	
Select a Category: General VCD parsing options Partial parsing Top level name Glitch fikering Remaining signals	Clitch filtering C Off Automatic glitch filtering Specify filtering threshold: 100 ps
Help	OK Cancel

Figure 71 · Import VCD File Dialog Box — Glitch Filtering

**Remaining Signals** — Some signals may not be annotated by the VCD reader. This generally happens with VCD files created from a behavioral or a post-synthesis simulation. For those signals, you can either complete the annotation with the <u>vectorless analysis</u> or with the average values computed from the VCD file.

Import VCD Options		×
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Remaining signals	Image: Second state sta	
Help	OK Cancel	

Figure 72 · Import VCD File Dialog Box — Remaining Signals

- 4. Click OK.
- 5. When the vcd file is successfully imported, the file appears in the Modes and Scenarios toolbar, under the imported mode. The following messages appear in the Designer Log window:

Info: VCD:34 glitch(es) filtered with 1000 ps threshold The message above reports the number of glitches that have been filtered by the VCD reader. Info: VCD: Annotation Statistics Percentage of Annotated Pins:100.00 %

```
Percentage of Unannotated Pins:0.00 %
```



Percentage of Annotated Pins with Zero Frequency: 25.99 %

If the percentage of annotated pins is less than 50.00%, a warning message will be generated.

If the percentage of annotated pins is low, you may want to verify that signals at all levels of hierarchy were added recursively (for example using vcd add -r in ModelSim).

If you simulate a pre-synthesis netlist or a post-synthesis RTL netlist, it is possible to get a low percentage of annotated pins. This happens because not all logic elements are in the pre-synthesis netlist and the post-synthesis RTL netlist. For accurate power estimation, it is best to run post-layout simulation with a back-annotated netlist.

If you want to see exactly which pins are not annotated, open the SmartPower Frequencies tab. If your file was imported successfully, you will see a list of pins with annotated individual frequencies displayed with VCD Import as a source. The unannotated pins are displayed with Default Estimation as source. If your design has enable pins, open the SmartPower Probabilities tab.

After finishing the import VCD process, you can now create a <u>custom mode</u> based on the active mode. This custom mode will inherit all the clock and toggle frequencies of the active mode that have just been set through the VCD import. This final step is optional. It gives you the flexibility to modify the active mode frequencies while saving the VCD scenario in SmartPower. Refer to <u>Custom operating modes</u> for more details.

Note: If you generated the VCD file from Project Manager and if you are using Designer from Libero IDE, the list of generated VCD files appear in the unprocessed VCD file list. To import the VCD file, right-click and select Import VCD File.



Figure 73 · Unprocessed Simulation Files

## Importing a SAIF File in Designer

Use the following instructions to import a SAIF file.

#### To import a SAIF file:

1. From the **File** menu in **Designer**, select **Import Auxiliary Files**. Click **Add** to browse to your SAIF file and select it. When you have selected a SAIF file, click **OK** to continue.

If you have not yet completed the layout of the design, the design software guides you through placeand-route so that you can import the SAIF file. In order to successfully annotate your SAIF values to the design, Designer must complete place-and-route even if you generated your SAIF file using timing simulation (post-layout).

You may wish to import multiple SAIF files. If these files conflict (attempt to set a different frequency for the same net of your design, for example), the latest imported value takes precedence.

2. Specify your SAIF import options. Use the SAIF **Import Options** window to specify the instance name of your design in the simulation testbench (the instance name is the instance name of your design instantiated in the simulation testbench). You must include the hierarchy with the instance name. The example below shows how to identify the instance name of your design in the SAIF file. For example, the instance name of the design in the following SAIF file is "TEST\_BENCH/UUT".

```
(SAIFILE
(SAIFVERSION "1.1")
(DESIGN 2ff)
```

Click **OK** to continue.

.....

- Check the Log window for notification that you successfully imported the SAIF file ("The Import command succeeded..."). Even if the Import command succeeds, use SmartPower to verify which pins have been affected after you import the file.
- 4. Verify results of the imported file in the Frequencies tab screen in SmartPower. To view the results of your imported SAIF file, launch SmartPower and navigate to the Frequencies tab screen to view pins with annotated switching activities. If your file was imported successfully, you will see a list of pins with annotated switching frequencies and specific individual frequencies.

It may be that some pins of your design are not annotated by a SAIF import command. This sometimes happens if you simulate a pre-synthesis netlist. It is normal; not all logic elements are in the pre-synthesis netlist. Thus it is better to do a post-layout simulation with a back-annotated netlist for the most accurate power estimation.

# Removing a VCD File

The Value Change Dump (VCD) file is a simulation file. The format of this file is specified in the IEEE 1364 standard.

#### To remove a VCD file:

- Select the VCD file from Active mode or a custom mode, right-click the VCD file, and select Remove VCD File from <mode name> Mode; or
- From the Simulation menu, choose Remove VCD File > <file name>

Note: Any annotation will be removed when you remove the VCD file.

#### See Also

Importing a VCD File Modes and Scenarios Toolbar

# **Auditing Files**

SmartPower checks the time stamps of the VCD file and reports any missing or out-of-date files.

Audit is performed automatically when SmartPower is launched. You can trigger file audit at any time from the **Simulation** menu, by choosing **Audit Files**. An icon displaying the file status appears in the <u>Modes and</u> <u>Scenarios toolbar</u> next to the VCD file. Mouse over the icon to obtain more information.





#### Figure 74 · Audit Files Results

Table 4 · Audit Files Icons and Descriptions

lcon	Description
Δ	Indicates that the VCD file has been modified
8	Indicates that the VCD file is missing

To re-import the VCD file, right-click the VCD file and select **Re-import VCD File**, this will open the <u>Import VCD Options</u> dialog box.

# **Calculating Power**

## Steps to Calculate Power

Use the steps below to calculate the power consumption of your design. The list of screens and steps appear in the order in which you should view them to analyze your power accurately.

- 1. Summary tab View global power at the design level and view its impact on junction temperature.
- 2. <u>Domains tab</u> <u>Define clock domains</u> and specify a clock frequency and a data frequency for each clock domain.
- <u>Analysis tab</u> <u>View detailed hierarchical analysis</u> of your power consumption. This step is optional. But if your power consumption exceeds your budget, this step will help you to understand where there is room for improvement.
- Frequencies tab Specify individual pin frequencies, this step is optional, but gives you pin-by-pin control of the frequency.
- Probabilities tab Specify probabilities, this step is optional. You can use the default probabilities or set your own.

# Extracting Power Consumption of a Specific Clock Domain

To calculate the power consumption of a single clock domain (clock tree and data path) in a design:

- 1. Set SmartPower in toggle-rate mode. This is the default setting. To confirm that SmartPower is in toggle-rate mode, choose **Preferences** from **File** menu. Select the **Use Toggle Rates** check box
- 2. In the <u>Domains</u> tab, set all the **Clock Frequencies** to zero except for the clock domain for which you are calculating the power consumption.

The total power consumption of this clock domain is displayed in the <u>Summary</u> tab. This includes the contribution of the clock buffer, clock tree, and all clock input of the registers of this specific clock domain.

Note: In case you need to determine the power of the clock tree only, set the toggle rate of data on that clock domain to zero. The total power displayed is the power of that clock tree.

# Advanced Analysis of I/Os

SmartPower provides an easy way of estimating the power consumption related to I/Os. You can then analyze power consumption in detail.

#### To display I/O power consumption:

- In the Summary tab, select By Type from the Breakdown drop-down list. The grid displays the total power consumption of all I/Os in the design, as well as all other components. If you use different I/O standards, and different Vcci power rails, you can also display the power consumption for each rail by selecting By Rail from the Breakdown drop-down list. Breakdown By Rail shows the power consumption and current for each Vcci rail in the design.
- 2. In the Analysis tab, select the highest hierarchy level in the Hierarchy tree in the left pane. Select **By** Instance from the Breakdown drop-down list.
- 3. In the **Analysis** tab, unselect all categories under **Instances Contributions** except I/Os, and then click **Apply**. The table then displays a list of all I/Os in the design, along with the power contribution of each individual I/O. The columns display important I/O attributes: external port name, load, standard, drive-strength, slew, and macro.
- 4. In the **Probabilities** tab, you can control the output probability of each tri-state and bidirectional I/O. The probability is the percentage of time that the I/O is used as an output. The default value can be changed and a specific value can also be set for each bidirectional or tri-state I/O.



### See Also

Analyze results Analysis tab

# Define Clock Domains and Set of Pins

When you run SmartPower, it researches your existing clock domains and partitions your design automatically. You may wish to review the list of clock domains in the <u>Domains tab</u> to ensure that all the clocks of your design are included in the list. Add or remove clocks as necessary.

#### To add a new clock domain:

1. Click the **Domains** tab, and click the **Add Domain** button. Select **Clock Domain** from the drop-down list. This opens the **Create Clock Domain** dialog box.

Create Clock Domain	×
Potential Clock Pin CLK_pad/IOTILE:Y0	Create
	Cancel
Clock Frequency   10 MHz	
Data Frequency 1 MHz	

Figure 75 · Create Clock Domain Dialog Box – Toggle Rates Disabled

 To create a new clock, select a Potential Clock Pin, specify a clock and data frequency, and click Create. The new clock domain appears in the Domains window. If you select an existing clock pin from the drop-down list, the lists of clock pins and data pins of this new clock domain are computed automatically based on the netlist topology.

**Note:** Select Use Toggle Rates in the <u>SmartPower Preferences</u> to define your data frequency as a percentage of your clock frequency. If your data frequency is 20% of your clock frequency, type "20" in the Data Frequency text box.

Create Clock Domain	×
Potential Clock Pin CLK_pad/IOTILE:Y0	Create
Clock Frequency 10 MHz	Cancel
Data Frequency 20 %	

Figure 76 · Create Clock Domain Dialog Box – Toggle Rates Enabled

You may wish to create an empty clock domain and fill the lists of clock-pins and data pins manually. If so, do not select a clock pin, just type a new name for your clock domain.

Beyond the verification of the list of clock domains, you may also wish to verify that the lists of clock pins and data pins computed for each clock domain are correct.

To verify the lists of clock pins and data pins of a clock domain:

- 1. Click the **Domains** tab and select a specific **Domain** in the list.
- 2. **Display the list of clock pins or data pins of this Domain.** A drop-down list in the **Domains** tab enables you to select clock pins or data pins. SmartPower displays the list of pins corresponding to your selection below the drop-down list. You can add or remove clock pins and data pins as necessary.

- 3. **Remove a pin from a clock domain.** Highlight the selected pin and click the **Remove** button. The pin is removed from the clock domain and is made available in the list of pins that you can add in another clock domain.
- 4. Highlight the selected pin in the list of pins that are not yet in a domain and click the **Add** button to add a pin in a clock domain. This pin is added to the clock domain. It is a clock pin or a data pin, depending on the specification of the drop-down list when you click the **Add** button.
- Note: You cannot add a pin that exists in another domain until you free it from its existing domain. The pin is unavailable until you remove it from that domain.

After you have verified that all the clocks of your designs are correctly identified and constructed, you must specify the correct clock and data frequency for each clock domain.

#### To add a new set of pins:

1. Open the **Create Clock Domain** dialog box. Click the **Domains** tab, and click the **Add Domain** button. Select **Set of Pins** from the drop-down list.

Create Set of Pi	ns		×
Set Name	Output		Create
Frequency	1	MHz	Cancel

Figure 77 · Create Set of Pins Dialog Box

2. Create a Set of Pins. Name your new set of pins, specify a data frequency, and click Create. The new set of pins appears in the **Domains** window.

# Specify Clock and Data Frequencies in SmartPower

#### To specify a clock and data frequency:

- 1. Click the **Domains** tab
- 2. select the Clock/Data frequency cell and type in a new value

SmartPower defaults to 0 MHz for the clock frequency. Import your clock frequency from SmartTime by using the <u>Initialize Frequencies dialog box</u> in SmartPower or input your target for each clock frequency in the **Domains** tab. You must also specify a data frequency (5% of your clock frequency is a typical guideline for your data frequency – this corresponds to a toggle rate of 10 %.)

Not all the pins/gates/nets of your design are associated with a specific clock. For example, the frequency of a design input port is not always correlated to a clock frequency. By extension, all pins that are upstream of the first level of sequential elements are not associated with any clock. SmartPower creates an InputSet by default that it uses to group all the pins that are controlled by design inputs (instead of sequential elements). You may wish to <u>view and verify the InputSet</u> to further evaluate your design.

# Viewing and Verifying the InputSet in SmartPower

#### To verify the InputSet:

- 1. Click the **Domains** tab and select the domain named **InputSet** in the list.
- 2. Verify the list of pins of this domain. All the input ports of your design (except the clocks) belong in the **InputSet**. Also, all the pins that are between these input ports and the first level of sequential elements belong in the **InputSet**. You can add or remove pins as necessary.
- 3. Specify an average input frequency. SmartPower uses the same frequency for all pins of the InputSet. The default InputSet frequency is 1 MHz. Type in a new value to change it.

You may wish to split the InputSet into several sets in order to specify different frequencies. A classic example is to create a ResetSet, a reset tree with a very low frequency.



#### To split the InputSet into several sets:

- 1. Create a new set of pins: In the **Domains** tab, click the **New** button, and select **Set of Pins** from the drop-down menu. In the **Create Set Of Pins** dialog box, type a name and a frequency for the new set and click **Create**. The new set of pins appears in the **Domains** window. You can only create an empty set of pins, but it is possible to add pins to this domain later.
- 2. Remove a group of pins from the **InputSet**. Click the **Domains** tab and select the domain named **InputSet** in the list. Select the pins that you want to remove and click the **Remove** button.
- 3. Add this group of pins to the new set of pins. Click the **Domains** tab and select the newly created set of pins in the list. Highlight the pins in the list of pins that are not yet in a domain, and click the **Add** button. Repeat these three steps as necessary to create multiple input sets.

# **Specifying Individual Pin Frequencies**

The <u>Frequencies</u> tab enables you to specify an average clock and data frequency for each clock domain, and also an average frequency for each set of pins. This gives you an initial estimate of the power consumption of your design. However, if this estimate is not accurate enough, you may refine it with a pinby-pin annotation of the frequency.

#### To specify a frequency annotation for an individual pin:

- 1. Locate the pin in the **Frequencies** tab. You may need to select different clock domains from the dropdown list on the **Frequencies** tab. You can use filters to facilitate this search.
- 2. Select the pin(s) in the grid and click the **Set frequencies for selected pins** button, enter a new frequency value, and click **OK**. This specifies a new frequency for the selected pin(s).
- Note: This annotation procedure enables you to set the frequency of an individual pin, but this does not mean that the pin is removed from its clock domain. A frequency annotation just overrides the domain level frequency.

You may wish to change or remove a frequency annotation of an individual pin. This may be useful when you <u>import a VCD (value change-dump) file</u> or a <u>SAIF (Switching Activity Interchange Format)</u> file.

#### To change the frequency annotation of an individual pin:

- 1. Locate the pin in the **Frequencies** tab. You may need to select different clock domains from the dropdown list on the **Frequencies** tab. You can use filters to facilitate the search.
- 2. Select the pin(s) in the grid and click the **Set frequency for selected pins** button, enter a new frequency value, and click **OK**. This specifies a new frequency for the selected pin(s).

#### To remove the frequency annotation of an individual pin:

- 1. Locate the pin in the **Frequencies** tab. You may need to select different clock domains from the dropdown menu on the **Frequencies** tab. You can use filters to facilitate the search.
- 2. Select the pin(s) in the grid and click the **Reset frequencies for selected pins** button. This removes the specified frequency from the selected pins.

## Specifying Individual Pin Probabilities

The **Probabilities** tab enables you to specify the default output probability value for memory blocks, and tristate and bidirectional I/Os. In addition, you can increase the accuracy of the power estimation by annotating the probability of specific pins.

#### To specify or change the probability for one or multiple pins:

- 1. Locate the pin(s) in the Probabilities tab. You can use filters to facilitate this search.
- 2. Select the pin(s) and press the Set probabilities for selected pins button.
- 3. Enter a new probability value and press OK.

#### To reset the probability for one or multiple pins:

- 1. Locate the pin(s) in the Probabilities tab. You can use filters to facilitate this search.
- 2. Select the pin(s) and press the **Reset Probabilities for selected pins** button. This will reset the probability value.

# **Vectorless Estimation**

The Vectorless estimation method is an accurate method of annotating individual pins with frequencies and probabilities. It uses primary inputs, clock frequencies, and nets annotated with other methods as a starting point, and uses a Monte Carlo simulation to annotate all nets in the design with frequencies and probabilities.

Vectorless estimation is available and enabled by default for SmartFusion, IGLOO, ProASIC3 and Fusion families of devices.

Vectorless estimation can be enabled from the <u>Initialize Frequencies and Probabilities</u> dialog box or from the <u>VCD Import</u> dialog box.

Changes to probabilities or frequencies in the Probabilities, Frequencies, or Domains tabs result in an out-

of-date vectorless estimation. To update vectorless estimation, press the refresh vectorless 🧖 button.

# Viewing Results (Design Level)

Click the <u>Summary</u> tab to view global power consumption at the design level. The **Summary** tab shows your design's estimated power consumption and temperature information.

The power estimation reported in the **Summary** tab is the total static and dynamic power consumption of your design. For a more detailed view of this power consumption, click the <u>Analysis</u> tab.

#### To estimate the junction temperature:

- 1. Verify your package. You cannot change your package directly in SmartPower, because it may render your place-and-route information (and thus it may severely impact the total power consumption). If you wish to choose another package, you have to do it in **Designer > Tools > Device Selection**.
- 2. Click the **Summary** tab, and select a **Cooling** style in the list. Thermal resistance changes automatically when you update the cooling style.
- 3. Specify an ambient temperature. Enter an **ambient temperature** (default value is 25°C), and click the **Set** button.
- Note: The junction temperature value changes according to the package, cooling style, and ambient temperature values you choose.

# **Analyzing Results**

The **Analysis** tab displays the estimated power consumption of individual blocks, gates, nets, I/Os, and memory and enables you to make a hierarchical analysis of your power consumption. The **Analysis** tab may also help you to improve your power consumption by identifying the components that consume a significant amount of power.

#### To identify the components consuming the most power:

 Use the Analysis tab to expand the design hierarchy. The Analysis tab enables you to expand your design hierarchy and view a complete list of the blocks in your design. In the hierarchy window, click the + next to your design to view the items in the hierarchy. Click the + next to a sub-block to view its sub-elements.



	Power Consumption Block Name: WGT Static Power: 0 mW Dynamic Power: 0.014 Breakdown: By Type		Show C Chart 🕫 Grid
	_		
<ul> <li>€ CTRL</li> <li>€ BC</li> <li>€ SREG</li> <li>○ CLK</li> <li>○ CREG</li> </ul>	Type  1 Net 2 Gate	Power (m\/)	Percentage 20.3% 79.7%

Figure 78 · Analysis Tab Dialog Box

- 2. Click to select a block. By default, SmartPower selects the design-level block, but you can always select another block in the hierarchical tree. The **Report** window displays the list of sub-elements of the selected block. Initially, this list includes all sub-elements. The grid in the **Analysis** window displays a breakdown of the power of the selected block by type. This breakdown provides you a good overview of which areas of your design you should optimize for power.
- 3. To find the components that use a significant amount of power, choose **By Instance** from the **Breakdown** drop-down list.
- 4. Sort and filter the sub-elements to find the component that is using the most power. The Analysis window displays the list of sub-elements of the selected block. By default, this list includes all sub-elements. The grid contains columns for name, type, power, driver, fanout, macro, I/O standard, output load, output drive, slew, port, domain and frequency. You may limit the list of sub-elements to a list of sub-blocks, nets, gates, I/Os, memories, or any combination of these five classes of sub-elements. You can sort the list according to any column by double-clicking the column header.

#### See Also

Advanced Analysis of I/Os Analysis tab

## Cross-Probing in SmartPower

SmartPower supports cross probing with the other Designer tools. You must calculate your design's power consumption before you can cross probe effectively. See the <u>Calculating Power</u> section for more information.

#### To cross probe with the SmartPower tool:

- 1. View the detailed results of your power analysis in the Analysis tab of the SmartPower tool.
- 2. Select By Instance from the Breakdown drop-down list.
- 3. Open MultiView Navigator in Designer.
- 4. Select your component.
- 5. Click a sub-component in the grid to highlight the corresponding component in the **ChipPlanner** or **PinEditor** tool.

SmartPower for Libero SoC v11.8 User Guide

» Microsemi

🗞 Summary 🛛 🛍 Domains 🔎				· ·			
_}- ① fpga	Power Co	nsumption					
🚰 WGT			WOT				
🔁 🕄 PC	В	lock Name:	WGT				
⊕- <b>::</b> : ∨c	s	tatic Power:	0 mW				
Ė.∎ LMDC							
🔛 IG	Dyna	amic Power:	0.001 m	W			
in II PL							
	Breakdown	: By Instance		•			
in € IBC				<u> </u>			
SREG	Instances	Contributions-					
📲 ancu							
ST OLK	🛛 🔽 Blocks	s 🔽 Nets	✓	Gates 🔽	🚺 I/Os 🛛 🔽 Mem	iories	Apply
ELK	Blocks	s 🗹 Nets		Gates ∣⊻	/I/Us IM Mem	ories	Apply
EK CREG	P Blocks			Dynamic	'I/Us I¥ Mem Driver	ories Fanout	Apply
		Name	Туре	▲ Dynamic (m₩)	Driver	Fanout	Macro
	1 WGT.	Name /Q151_0	Type Net	▲ Dynamic (m₩) 0	Driver WGT/U46:Y	Fanout	Macro
	1 WGT. 2 WGT.	Name /Q151_0 /Q[0]	Type Net Net	▲ Dynamic (m₩) 0	Driver WGT/U46:Y WGT/Q_reg_0_:Q	Fanout 1	Macro
	1 WGT. 2 WGT. 3 WGT.	Name /Q151_0 /Q[0] /Q[1]	Type Net Net Net	Dynamic (mW) 0 0 0	Driver WGT/U46:Y WGT/Q_reg_0_:Q WGT/Q_reg_1_:Q	Fanout 1 1 3	Macro
	1 WGT. 2 WGT. 3 WGT. 4 WGT.	Name /Q151_0 /Q[0] /Q[1] /Q_reg_0_	Type Net Net Net Gate	Dynamic (mW) 0 0 0 0	Driver WGT/U46:Y WGT/Q_reg_0_:Q	Fanout 1	Macro 
	1 WGT. 2 WGT. 3 WGT. 4 WGT. 5 WGT.	Name /0151_0 /0[0] /0[1] /0_reg_0_ /0_reg_1_	Type Net Net Gate Gate	Dynamic (m\/) 0 0 0 0 0	Driver WGT/U46:Y WGT/Q_reg_O_:Q WGT/Q_reg_1_:Q 	Fanout 1 1 3 	Macro ADLIB:DFN1C ADLIB:DFN1C
	1 WGT. 2 WGT. 3 WGT. 4 WGT.	Name /0151_0 /0[0] /0[1] /0_reg_0_ /0_reg_1_ /U44	Type Net Net Net Gate	Dynamic (mW) 0 0 0 0	Driver WGT/U46:Y WGT/Q_reg_0_:Q WGT/Q_reg_1_:Q 	Fanout 1 1 3 	Macro 
	1 WGT. 2 WGT. 3 WGT. 5 WGT. 6 WGT.	Name           /Q151_0           /Q[0]           /Q[1]           /Q_reg_0_           /Q_reg_1_           /U44           /U45	Type Net Net Gate Gate Gate	► Dynamic (m₩) 0 0 0 0 0 0	Driver WGT/U46:Y WGT/0_reg_0_:Q WGT/0_reg_0_:Q   	Fanout 1 3  	ADLIB:DFN1C ADLIB:DFN1C ADLIB:ADI1D
	1 WGT. 2 WGT. 3 WGT. 4 WGT. 5 WGT. 6 WGT. 7 WGT.	Name           /Q151_0           /Q(0)           /Q(1)           /Q(1)<	Type Net Net Gate Gate Gate Gate	Dynamic (mW)     0     0     0     0     0     0     0     0     0     0     0     0     0     0     0     0     0     0	Driver WGT/U46:Y WGT/Q_reg_0_:Q WGT/Q_reg_1_:Q   	Fanout 1 3   	ADLIB:ADID ADLIB:ADID ADLIB:ADID
	1 WGT. 2 WGT. 3 WGT. 4 WGT. 5 WGT. 6 WGT. 8 WGT.	Name           /0151_0           /02           /03           /04           /04           /048	Type Net Net Gate Gate Gate Gate Gate Gate Gate	Dynamic (mW) 0	Driver WGT/U46:Y WGT/0_reg_0_:Q WGT/0_reg_1_:Q     	Fanout 1 3 	ADLIB:DFN1C ADLIB:DFN1C ADLIB:DFN1C ADLIB:ADI1D ADLIB:NV ADLIB:NV
	1 WGT. 2 WGT. 3 WGT. 4 WGT. 5 WGT. 6 WGT. 7 WGT. 8 WGT. 10 WGT. 11 WGT.	Name           /0151_0           /0[0]           /0[1]           /0]     <	Type Net Net Net Gate Gate Gate Gate Gate Gate Gate Ga	Dynamic (mW) 0	Driver WGT/U46:Y WGT/0_reg_0_:0 WGT/0_reg_1_:0        	Fanout 1 3 	ADLIB:DFN1C <sup>-</sup> ADLIB:DFN1C <sup>-</sup> ADLIB:AD11D ADLIB:AD12A ADLIB:AND2A ADLIB:MN2 ADLIB:MX2
	1 WGT. 2 WGT. 3 WGT. 4 WGT. 5 WGT. 6 WGT. 7 WGT. 8 WGT. 9 WGT. 10 WGT.	Name           /0151_0           /0[0]           /0[1]           /0]     <	Type Net Net Gate Gate Gate Gate Gate Gate Gate Ga	Dynamic (mW) 0	Driver WGT/U46:Y WGT/0_reg_0_:Q WGT/0_reg_1_:0           	Fanout 1 3 	Macro ADLIB:DFN1C ADLIB:DFN1C ADLIB:A011D ADLIB:AND2 ADLIB:AND2 ADLIB:AND2 ADLIB:MX2

Figure 79 · Cross-Probing with SmartPower: SmartPower Analysis View

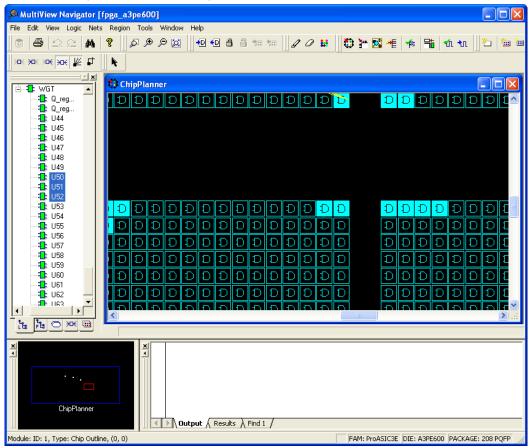


Figure 80 · Cross-Probing with SmartPower: ChipPlanner View



# SmartPower Calculation Equations

SmartPower calculates the static power and the dynamic power of your design, for given operating conditions and operating modes:

Static Power: This value is a summation of the static power consumed by each element of the design. SmartPower provides a static power consumption of the array. This value is die-dependent. This value is also a function of the operating mode. For some families, SmartPower also considers a static power contribution per I/O bank. For specific I/O technologies like voltage referenced I/Os or differential I/Os. SmartPower also considers a static power contribution per I/O.

Dynamic Power: This value is a summation of the dynamic power consumed by each element of the design (nets, modules, I/Os, RAMs, FIFOs, PLLs, etc.).

Operating Conditions: SmartPower calculates power consumption in Worst, Typical, or Best operating conditions. SmartPower uses the following as general guidelines:

- It applies a voltage derating to dynamic power contributions. Higher voltage typically leads to higher power consumption.
- It applies a temperature derating to static power contributions. Higher temperature typically leads to higher power consumption.
- It applies no radiation derating.

Operating Modes: SmartPower calculates power consumption in Active, Static, Flash\*Freeze, Sleep, and Shutdown operating modes, when applicable for your design.

#### **Sample Equations:**

The examples below are for general evaluation purposes only. They are not a precise representation of the actual calculations, since each calculation takes into account family-specific information.

- For a **net**.
  - $P = C \cdot V^2 \cdot F$

where C is the total capacitive loading of the net (extracted from the routing topology), V is the net's voltage swing, and F is the average switching frequency.

- Note: For the ProASIC<sup>PLUS</sup> family, SmartPower extracts the capacitive loading of a net from a Wire Load model.
- For a module, the power is computed using a characterized library (by family and die-size) describing a specific power model for each type of module. For example, the power model of a flip-flop is given by

 $P = P_{CK} \cdot F_{CK} + P_{DOUT} \cdot F_{DOUT} + P_{Din} \cdot F_{Din}$ where F<sub>CK</sub> is the average clock-input frequency for this flip-flop, F<sub>DOUT</sub> is its average data-output

frequency, and P<sub>CK</sub>, P<sub>DOUT</sub>, P<sub>Din</sub> are three constants estimated by electrical simulation and silicon characterization for this flip-flop module, and FDin is its average data-input frequency.

For an I/O, the formula used for computing the power consumption depends on the I/O technology and the family. For example, for a TTL output, the dynamic power is given by  $P = P_{INT} \cdot F + C \cdot V^2 \cdot F$ 

where C is the output load (derived from what you have set in the I/O Attribute Editor GUI, typically 35 pF for TTL), V is the output's voltage swing (3.3 V for TTL), and PINT represents an internal power contribution dissipated in the pad, and F is the average switching frequency of the I/O.

For a complex block, like a RAM, a FIFO, or a PLL, SmartPower uses a high-level power model that integrates design parameters.

SmartPower automatically computes all the constant parameters of these equations. However, the frequencies depend on the target frequencies of your design. Since it is impractical to enter each frequency manually, SmartPower has several flows that help you to estimate the frequencies and calculate the power consumption.

# **SmartPower Tcl Commands**

SmartPower supports the following Tcl scripting commands:

- set pin enable rate
- <u>set pin probability</u>
- smartpower add new custom mode
- <u>smartpower\_add\_new\_scenario</u>
- smartpower add pin in domain
- <u>smartpower\_battery\_settings</u>
- <u>smartpower\_change\_clock\_statistics</u>
- smartpower change setofpin statistics
- <u>smartpower\_commit</u>
- <u>smartpower\_create\_domain</u>
- <u>smartpower\_compute\_vectorless</u>
- <u>smartpower edit custom mode</u>
- smartpower edit scenario
- <u>smartpower\_import\_vcd</u>
- <u>smartpower\_initialize\_clock\_with\_constraints</u>
- <u>smartpower\_init\_do</u>
- <u>smartpower\_init\_set\_clocks\_options</u>
- smartpower init set combinational options
- <u>smartpower\_init\_set\_enables\_options</u>
- <u>smartpower\_init\_set\_othersets\_options</u>
- smartpower init set primaryinputs options
- smartpower init set registers options
- smartpower\_init\_set\_set\_reset\_options
- smartpower init setofpins values
- smartpower remove all annotations
- <u>smartpower\_remove\_custom\_mode</u>
- smartpower remove domain
- <u>smartpower\_remove\_file</u>
- smartpower\_remove\_pin\_enable\_rate
- smartpower\_remove\_pin\_frequency
- smartpower remove pin of domain
- <u>smartpower\_remove\_pin\_probability</u>
- <u>smartpower\_remove\_scenario</u>
- <u>smartpower\_restore</u>
- smartpower set cooling
- smartpower\_set\_mode\_for\_analysis
- smartpower set mode for pdpr
- <u>smartpower\_set\_operating\_condition</u>
- smartpower set pin probability
- smartpower set pin frequency



- <u>smartpower\_set\_preferences</u>
- smartpower set scenario for analysis
- <u>smartpower set temperature opcond</u>
- smartpower set thermalmode
- <u>smartpower set voltage opcond</u>
- smartpower temperature opcond set design wide
- smartpower\_temperature\_opcond\_set\_mode\_specific
- smartpower\_voltage\_opcond\_set\_design\_wide
- <u>smartpower\_voltage\_opcond\_set\_mode\_specific</u>

# smartpower\_add\_new\_custom\_mode

Tcl command; creates a new custom mode.

```
smartpower_add_new_custom_mode -name {mode_name} -base_mode {base_mode} -description
{mode_description}
```

#### **Arguments**

#### -name {mode\_name}

Specifies the name of the new custom mode.

-base\_mode {base\_mode}

Specifies the name of the base mode used to create the new custom mode. It must be one of the following: Active, Standby, or Flash\*Freeze.

-description {mode\_description}

Specifies the description of the new custom mode.

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Examples**

This example creates a new custom mode "Cust\_1" based on the Active mode:

smartpower\_add\_new\_custom\_mode -name {Cust\_1} -base\_mode {Active} -description {frequency 10 MHz}

#### See Also

smartpower\_remove\_custom\_mode
Designer Tcl Command Reference

# smartpower\_add\_new\_scenario

Tcl command; creates a new scenario.

```
smartpower_add_new_scenario -name {value} -description {value} -mode {value}
```

#### **Arguments**

-name {value}

Specifies the name of the new scenario. -description {value} Specifies the description of the new scenario.

```
-mode {<operating mode>:<duration>}+
```

Specifies the mode(s) and duration(s) for the specified scenario.

## **Supported Families**

See the Tcl Commands and Supported Families table for a list of supported families.

## **Examples**

#### This example creates a new scenario called myscenario:

smartpower\_add\_new\_scenario -name "MyScenario" -mode "Custom\_1:50.00"
"Custom\_2:25.00" -mode "Active:25.00"

#### See Also

Tcl documentation conventions Designer Tcl Command Reference

# smartpower\_add\_pin\_in\_domain

Tcl command; adds a pin into a clock or set domain.

```
smartpower_add_pin_in_domain -pin_name {pin_name} -pin_type {value} -domain_name
{domain_name} -domain_type {value}
```

## Arguments

-pin\_name {pin\_name}

Specifies the name of the pin to add to the domain.

-pin\_type {value}

Specifies the type of the pin to add. The following table shows the acceptable values for this argument:

Value	Description
clock	The pin to add is a clock pin
data	The pin to add is a data pin

-domain\_name {domain\_name}

Specifies the name of the domain in which to add the specified pin.

-domain\_type {value}

Specifies the type of domain in which to add the specified pin. The following table shows the acceptable values for this argument:

Value	Description
clock	The domain is a clock domain
set	The domain is a set domain

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for a list of supported families.





- The domain\_name must be a name of an existing domain.
- The pin\_name must be a name of a pin that exists in the design.

## **Examples**

#### The following example adds a clock pin to an existing Clock domain:

smartpower\_add\_pin\_in\_domain -pin\_name { XCMP3/U0/U1:Y } -pin\_type {clock} -domain\_name
{clk1} -domain\_type {clock}

#### The following example adds a data pin to an existing Set domain:

smartpower\_add\_pin\_in\_domain -pin\_name {XCMP3/U0/U1:Y} -pin\_type {data} -domain\_name
{myset} -domain\_type {set}

#### See Also

<u>Tcl documentation conventions</u> <u>Designer Tcl Command Reference</u> smartpower\_remove\_pin\_of\_domain

# smartpower\_battery\_settings

This SmartPower Tcl command sets the battery capacity in SmartPower. The battery capacity is used to compute the battery life of your design.

smartpower\_battery\_settings -capacity {decimal value}

## **Parameters**

-capacity {*decimal value*} Value must be a positive decimal. This parameter is mandatory.

## **Exceptions**

None

## Returns

This command does not return a value.

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## Usage

This section parameters for the command, their types, and the values they can be set to.

smartpower_battery_settings	Туре	Value	Description
capacity	Decimal	Positive decimal	Specify the battery capacity in mA*Hours

## Example

This example sets the battery capacity to 1800 mA \* Hours.

smartpower\_battery\_settings -capacity {1800}

# smartpower\_change\_clock\_statistics

Tcl command; changes the default frequencies and probabilities for a specific domain.

```
smartpower_change_clock_statistics -domain_name {value} -clocks_freq {value} -
clocks_proba {value} -registers_freq {value} -registers_proba {value} -set_reset_freq
{value} -set_reset_proba {value} -primaryinputs_freq {value} -primaryinputs_proba {value} -
combinational_freq {value} -combinational_proba {value}
```

#### **Arguments**

-domain\_name{value}

Specifies the domain name in which to initialize frequencies and probabilities.

```
-clocks_freq {value}
```

Specifies the user input frequency in Hz, KHz, or MHz for all clocks.

-clocks\_proba {value}

Specifies the user input probability in % for all clocks.

-registers\_freq {value}

Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

-registers\_proba {value}

Specifies the user input probability in % for all registers.

#### -set\_reset\_freq {value}

Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

```
-set_reset_proba {value}
```

Specifies the user input probability in % for all set/reset nets.

```
-primaryinputs_freq {value}
```

Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

```
-primaryinputs_proba {value}
```

Specifies the user input probability in % for all primary inputs.

-combinational\_freq {value}

Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

```
-combinational_proba {value}
```

Specifies the user input probability in % for all combinational combinational output.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.



## **Notes**

This command is associated with the functionality of Initialize frequencies and probabilities dialog box.

## **Examples**

The following example initializes all clocks withs:

```
smartpower_change_clock_statistics -domain_name {my_domain} -clocks_freq {10 MHz} -
clocks_proba {20} -registers_freq {10 MHz} -registers_proba {20} -set_reset_freq {10
MHz} -set_reset_proba {20} -primaryinputs_freq {10 MHz} -primaryinputs_proba {20} -
combinational_freq {10 MHz} -combinational_proba {20}
```

#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

# smartpower\_change\_setofpin\_statistics

Tcl command; changes the default frequencies and probabilities for a specific set.

```
smartpower_change_setofpin_statistics -domain_name {value} -data_freq {value} -
data_proba {value}
```

#### Arguments

-domain\_name{value}

Specifies the domain name in which to initialize data frequencies and probabilities. -data\_freq {value} Specifies the user input data frequency in Hz, KHz, or MHz for all sets of pins. -data\_proba {value} Specifies the user input data probability in % for all sets of pins.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### Notes

This command is associated with the functionality of Initialize frequencies and probabilities dialog box.

## Examples

The following example initializes all clocks withs:

<code>smartpower\_change\_setofpin\_statistics -domain\_name {my\_domain} -data\_freq {10 MHz} - data\_proba {20}</code>

#### See Also

<u>Tcl documentation conventions</u> <u>Designer Tcl Command Reference</u>

# smartpower\_commit

Tcl command; saves the changes to the design (.adb) file.

smartpower\_commit

## Arguments

None

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Examples**

smartpower\_commit

#### See Also

Tcl documentation conventions Designer Tcl Command Reference smartpower\_restore

# smartpower\_compute\_vectorless

This Tcl command executes a vectorless analysis of the current operating mode.

## Arguments

None

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## Example

smartpower\_compute\_vectorless

## See Also

Tcl Command Documentation Conventions Designer Tcl Command Reference

# smartpower\_create\_domain

Tcl command; creates a new clock or set domain.

```
smartpower_create_domain -domain_type {value} -domain_name {domain_name}
```

## **Arguments**

-domain\_type {value}

Specifies the type of domain to create. The following table shows the acceptable values for this argument:

Value	Description
clock	The domain is a clock domain
set	The domain is a set domain

-domain\_name {domain\_name}

Specifies the name of the new domain.



### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Notes**

The domain name cannot be the name of an existing domain. The domain type must be either clock or set.

#### **Examples**

The following example creates a new clock domain named "clk2": smartpower\_create\_domain -domain\_type {clock} -domain\_name {clk2}
The following example creates a new set domain named "myset":
smartpower\_create\_domain -domain\_type {set} -domain\_name {myset}

#### See Also

Tcl documentation conventions Designer Tcl Command Reference smartpower\_remove\_domain

# smartpower\_edit\_custom\_mode

Tcl command; edits a custom mode.

```
smartpower_edit_custom_mode -name {old_mode_name} new_name {new_mode_name} -description
{mode_description}
```

#### **Arguments**

-name {old\_mode\_name}
Specifies the name of the custom mode you want to edit.
-new\_name {new\_mode\_name}
Specifies the new name of the custom mode.
-description {mode\_description}
Specifies the description of the new custom mode.

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## **Examples**

#### This example edits custom mode "Cust\_1" and renames it "Cust\_2":

smartpower\_edit\_custom\_mode -name {Cust\_1} -new\_name {Cust\_2} -description {frequency 10 MHz}

#### See Also

Tcl documentation conventions Designer Tcl Command Reference smartpower\_remove\_custom\_mode smartpower\_add\_custom\_mode



# smartpower\_edit\_scenario

Tcl command; edits a scenario.

smartpower\_edit\_scenario -name {value} -description {value} -mode {value} -new\_name {value}

## Arguments

-name {value}
Specifies the name of the scenario.
-description {value}
Specifies the description of the scenario.
-mode {<operating mode>:<duration>}
Specifies the mode(s) and duration(s) for the specified scenario.
-new\_name {value}
Specifies the new name for the scenario

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Examples**

This example edits the name of myscenario to finalscenario:

smartpower\_edit\_scenario -name myscenario -new\_name finalscenario

#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

# smartpower\_import\_vcd

This SmartPower Tcl command imports into SmartPower a VCD file generated by a simulation tool. SmartPower extracts the frequency and probability information from the VCD.

```
import_vcd -file "VCD file" [-opmode "mode name"] [-with_vectorless "TRUE | FALSE"] [-
partial_parse\ "TRUE | FALSE"] [-start_time "decimal value"] [-end_time "decimal value"]
\
[-auto_detect_top_level_name "TRUE | FALSE"] [-top_level_name "top level name"] [-
glitch_filtering\ "false | auto | true"] [-glitch_threshold "integer value"] [-stop_time
"decimal value"]
```

#### **Parameters**

-file "VCD file"
Value must be a file path. This parameter is mandatory.
[-opmode "mode name"]
Value must be a string. This parameter is optional.
[-with\_vectorless "TRUE | FALSE"]
Value must be a boolean. This parameter is optional.
[-partial\_parse "TRUE | FALSE"]
Value must be a boolean. This parameter is optional.
[-start\_time "decimal value"]
Value must be a positive decimal. This parameter is optional.
[-end\_time "decimal value"]



Value must be a positive decimal. This parameter is optional.
[-auto\_detect\_top\_level\_name "TRUE | FALSE"]
Value must be a boolean. This parameter is optional.
[-top\_level\_name "top level name"]
Value must be a string. This parameter is optional.
[-glitch\_filtering "false | auto | true"]
Value must be one of false | auto | true. This parameter is optional.
[-glitch\_threshold "integer value"]
Value must be a positive integer. This parameter is optional.

## **Exceptions**

None

#### Returns

This command does not return a value.

#### Usage

This section lists all the parameters for the command, their types, and the values they can be set to. The default value is always listed first.

smartpower_import_vcd	Туре	Values	Description
file	String	Path to a VCD file	Path to a VCD file.
opmode	String	Operating mode name "Active" by default	Operating mode in which the VCD will be imported. If the mode doesn't exist, it will be created.
with_vectorless	Boolean	TRUE FALSE	Specify the method to set the frequency and probability information for signals not annotated by the VCD TRUE: use the vectorless analysis FALSE: use average value computed from the VCD.
partial_parse	Boolean	FALSE TRUE	Enable partial parsing of the VCD. Start time and end time need to be specified when TRUE.
start_time	Decimal value	positive decimal nanoseconds (ns)	Specify the starting timestamp of the VCD extraction in ns. It must be lower than the specified end_time. It must be lower than the last timestamp in the VCD file.

smartpower_import_vcd	Туре	Values	Description
end_time	Decimal value	positive decimal nanoseconds (ns)	Specify the end timestamp of the VCD extraction in ns. It must be higher than the specified start_time.
auto_detect_top_level_name	Boolean	TRUE FALSE	Enable the auto detection of the top level name in the VCD file. Top_level_name needs to be specified when FALSE.
top_level_name	Boolean	Full hierarchical name	Specify the full hierarchical name of the instance of the design in the VCD file.
glitch_filtering	Boolean	Auto FALSE TRUE	AUTO: Enable glitch filtering with predefined thereshold based on the family TRUE: Enable glitch filtering, glitch_threshold must be specified FALSE: Disable glitch filtering.
glitch_threshold	Integer	Positive integer	Specify the threshold in ps below which glitches are filtered out.

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Examples**

The Tcl command below imports the power.vcd file generated by the simulator into SmartPower:

smartpower\_import\_vcd -file "../../simulation/power.vcd"

The Tcl command below extracts information between 1ms and 2ms in the simulation, and stores the information into a custom mode:

smartpower\_import\_vcd -file "../../simulation/power.vcd" -partial\_parse TRUE -start\_time
1000000 -end\_time 2000000 -opmode "power\_1ms\_to\_2ms"

# smartpower\_init\_do

Tcl command; initializes the frequencies and probabilities for clocks, registers, set/reset nets, primary inputs, combinational outputs, enables and other sets of pins, and selects a mode for initialization.



```
\label{eq:value} $$ smartpower_init_do -with $$ value$ -opmode $$ value$ -clocks $$ value$ -registers $$ value$ - set_reset $$ value$ -primary inputs $$ value$ -combinational $$ value$ -enables $$ value$ -othersets $$ value$ -value$ -value$ -value$ -value$ -value$ -value$ -value$ -value} $$ value$ -value$ -
```

## **Arguments**

#### $-with{value}$

This sets the option of initializing frequencies and probabilities with vectorless analysis or with fixed values. The following table shows the acceptable values for this argument:

Value	Description
vectorless	Initializes frequencies and probabilities with vectorless analysis
fixed	Initializes frequencies and probabilities with fixed values

#### -opmode $\{value\}$

Optional; specifies the mode in which to initialize frequencies and probabilities. The value must be Active or Flash\*Freeze.

-clocks {value}

This sets the option of initializing frequencies and probabilities for all clocks. The following table shows the acceptable values for this argument:

Value	Description
true	Initializes frequencies and probabilities for all clocks
false	Does not initialize frequencies and probabilities for all clocks

#### -registers {value}

This sets the option of initializing frequencies and probabilities for all registers. The following table shows the acceptable values for this argument:

Value	Description
true	Initializes frequencies and probabilities for all registers
false	Does not initialize frequencies and probabilities for all registers

#### -set\_reset {value}

This sets the option of initializing frequencies and probabilities for all set/reset nets. The following table shows the acceptable values for this argument:

Value	Description
true	Initializes frequencies and probabilities for all set/reset nets
false	Does not initialize frequencies and probabilities for all set/reset nets

```
-primaryinputs{value}
```

This sets the option of initializing frequencies and probabilities for all primary inputs. The following table shows the acceptable values for this argument:

Value	Description
true	Initializes frequencies and probabilities for all primary inputs
false	Does not initialize frequencies and probabilities for all primary inputs

#### -combinational {value}

This sets the option of initializing frequencies and probabilities for all combinational outputs. The following table shows the acceptable values for this argument:

Value	Description
true	Initializes frequencies and probabilities for all combinational outputs
false	Does not initialize frequencies and probabilities for all combinational outputs

#### -enables {value}

This sets the option of initializing frequencies and probabilities for all enable sets of pins. The following table shows the acceptable values for this argument:

Value	Description
true	Initializes frequencies and probabilities for all enable sets of pins
false	Does not initialize frequencies and probabilities for all enable sets of pins

#### -othersets {value}

This sets the option of initializing frequencies and probabilities for all other sets of pins. The following table shows the acceptable values for this argument:

Value	Description
true	Initializes frequencies and probabilities for all other sets of pins
false	Does not initialize frequencies and probabilities for all other sets of pins

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Notes**

This command is associated with the functionality of <u>Initialize frequencies and probabilities</u> dialog box.

## **Examples**

The following example initializes all clocks with:



 $\label{eq:smartpower_init_do -with {vectorless} -opmode {my_mode} -clocks {true} -registers {true} -asynchronous {true} -primaryinputs {true} -combinational {true} -enables {true} - othersets {true} \\$ 

#### See Also

Tcl documentation conventions Designer Tcl Command Reference



# smartpower\_init\_set\_clocks\_options

Tcl command; initializes the clock frequency options of all clock domains.

```
smartpower_init_set_clocks_options -with_clock_constraints {value} -
with_default_values {value} -freq {value} -duty_cycle {value}
```

#### **Arguments**

-with\_clock\_constraints {value}

This sets the option of initializing the clock frequencies with frequency constraints from SmartTime. The following table shows the acceptable values for this argument:

Value	Description
true	Sets initialize clock frequencies with clock constraints ON
false	Sets initialize clock frequencies with clock constraints OFF

#### -with\_default\_values {value}

This sets the option of initializing the clock frequencies with a user input default value. The following table shows the acceptable values for this argument:

Value	Description
true	Sets initialize clock frequencies with default values ON
false	Sets initialize clock frequencies with default values OFF

-freq  $\{value\}$ 

Specifies the user input frequency in Hz, KHz, or MHz. -duty\_cycle {value} Specifies the user input duty cycles in %.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## Notes

This command is associated with the functionality of Initialize frequencies and probabilities dialog box.

#### **Examples**

The following example initializes all clocks after executing <u>smartpower\_init\_do</u> with -clocks {true}: smartpower\_init\_set\_clocks\_options -with\_clock\_constraints {true} -with\_default\_values {true} -freq {10 MHz} -duty\_cycle {20}

#### See Also

Tcl documentation conventions Designer Tcl Command Reference



# smartpower\_init\_set\_combinational\_options

Tcl commands; initializes the frequency and probability of all combinational outputs.

smartpower\_init\_set\_combinational\_options -freq {value} -proba {value}

## Arguments

-freq  $\{value\}$ 

Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

-proba {value}

Specifies the user input probability in %.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### Notes

This command is associated with the functionality of Initialize frequencies and probabilities dialog box.

#### **Examples**

The following example initializes all combinational signals after executing <u>smartpower\_init\_do</u> with - combinational {true}:

smartpower\_init\_set\_combinational\_options -freq {10 MHz} -proba {20}

#### See Also

<u>Tcl documentation conventions</u> <u>Designer Tcl Command Reference</u>

# smartpower\_init\_set\_enables\_options

Tcl command; initializes the clock frequency of all enable clocks with the initialization options.

smartpower\_init\_set\_enables\_options -freq {value} -proba {value}

#### Arguments

-freq {value}
Specifies the user input frequency (in Hz, KHz, or MHz).
-proba {value}
Specifies the user input probability in %.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### Notes

This command is associated with the functionality of Initialize frequencies and probabilities\_ dialog box.



## **Examples**

The following example initializes all clocks after executing smartpower\_init\_do with -enables
{true}:

smartpower\_init\_set\_enables\_options -freq {10 MHz} -proba {20}

#### See Also

Tcl documentation conventions Designer Tcl Command Reference

# smartpower\_init\_set\_othersets\_options

Tcl command; initializes the frequency and probability of all other sets.

```
smartpower_init_set_othersets_options [-freq "decimal value [ unit { Hz | KHz | MHz } ]"]
[-proba "decimal value"]
[-with "vectorless | default"]
[-input_freq "decimal value [ unit { Hz | KHz | MHz } ]"]
[-input_proba "decimal value"]
```

## Arguments

-freq "decimal value [unit {Hz | KHz| MHz}"
Specifies the default frequency and units.
-proba {decimal value}
Specifies the default probability.
-with "vectorless | default"
Specifies vectorless or default analysis.
-input\_freq "decimal value [unit {Hz | KHz| MHz}"
Specifies the input frequency and units.
-input\_proba {decimal value}
Specifies the input probability.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Notes**

This command is associated with the functionality of Initialize Frequencies and Probabilities dialog box.

#### **Examples**

The following example initializes all other sets after executing  $\underline{smartpower\_init\_do}$  with -othersets {true}:

 $martpower_init\_set_othersets_options -freq {10 MHz} -proba {20} [-with default]$ 

#### See Also

<u>Tcl documentation conventions</u> <u>Designer Tcl Command Reference</u>



# smartpower\_init\_set\_primaryinputs\_options

Tcl command; initializes the frequency and probability of all primary inputs.

```
smartpower_init_set_primaryinputs_options -freq {value} -proba {value}
```

### Arguments

-freq  $\{value\}$ 

Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

-proba {value}

Specifies the user input probability in %.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### Notes

This command is associated with the functionality of Initialize frequencies and probabilities dialog box.

#### **Examples**

The following example initializes all primary inputs after executing smartpower\_init\_do with primary inputs {true}:

smartpower\_init\_set\_primary inputs\_options -freq {10 MHz} -proba {20}

#### See Also

<u>Tcl documentation conventions</u> <u>Designer Tcl Command Reference</u>

# smartpower\_init\_set\_registers\_options

Tcl command; initializes the frequency and probability of all register outputs.

smartpower\_init\_set\_registers\_options -freq {value} -proba {value}

#### Arguments

#### -freq $\{value\}$

Specifies the user input frequency (in Hz, KHz, or MHz) or the toggle rate (in %). If the unit is not provided and toggle rate is active, the value is handled as a toggle rate; if toggle rate is not active, the value is handled as a frequency.

-proba {value} Specifies the user input probability in %.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### Notes

This command is associated with the functionality of Initialize frequencies and probabilities\_ dialog box.

## **Exceptions**

None

## **Examples**

The following example initializes all register outputs after executing <u>smartpower\_init\_do</u> with - registers {true}:

```
smartpower_init_set_registers_options -freq {10 MHz} -proba {20}
```

#### See Also

Tcl documentation conventions Designer Tcl Command Reference

# smartpower\_init\_setofpins\_values

Tcl command; initializes the frequency and probability of all sets of pins.

smartpower\_init\_setofpins\_values -domain\_name {name} -freq {value} -proba {value}

## Arguments

-domain\_name{name}

Specifies the set of pins that will be initialized. The following table shows the acceptable values for this argument:

Value	Description
IOsEnableSet	Specifies that the IOsEnableSet set of pins will be initialized
MemoriesEnableSet	Specifies that the MemoriesEnableSet set of pins will be initialized

-freq {value}
Specifies the user input frequency in Hz, MHz, or KHz.
-proba {value}
Specifies the user input probability in %.

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## **Notes**

This command is associated with the functionality of Initialize frequencies and probabilities dialog box.

## **Examples**

The following example initializes all primary inputs after executing <u>smartpower\_init\_do</u> with - othersets {true}: smartpower\_init\_setofpins\_values -domain\_name {IOsEnableSet} -freq {10 MHz} -proba {20}

#### See Also

<u>Tcl documentation conventions</u> <u>Designer Tcl Command Reference</u>



# smartpower\_remove\_all\_annotations

Tcl command; removes all initialization annotations for the specified mode.

smartpower\_remove\_all\_annotations -opmode {value}

#### Arguments

-opmode {value}

Removes all initialization annotations for the specified mode, where value must be Active or Flash\*Freeze.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### Notes

This command is associated with the functionality of Initialize frequencies and probabilities\_ dialog box.

#### **Examples**

The following example initializes all clocks with opmode Acitve: smartpower\_remove\_all\_annotations -opmode {Active}

#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

## smartpower\_remove\_custom\_mode

Tcl command; removes a custom mode.

smartpower\_remove\_custom\_mode -name {deleted\_mode\_name}

## Arguments

-name {deleted\_mode\_name}

Specifies the name of the custom mode you want to delete.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Examples**

This example delets custom mode "Cust\_1":

smartpower\_delete\_custom\_mode -name {Cust\_1}

#### See Also

Tcl documentation conventions Designer Tcl Command Reference sp\_add\_custom\_mode sp\_edit\_custom\_mode



# smartpower\_remove\_domain

Tcl command; removes an existing clock or set domain.

```
smartpower_remove_domain -domain_type {value} -domain_name {domain_name}
```

## Arguments

-domain\_type {value}

This specifies the type of domain to remove. The following table shows the acceptable values for this argument:

Value	Description
clock	The domain is a clock domain
set	The domain is a set domain

-domain\_name {domain\_name}

This specifies the name of the domain to remove

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### Notes

The domain name must be the name of an existing domain. The domain type must be either clock or set.

#### **Examples**

The following example removes the clock domain named "clk2": smartpower\_remove\_domain -domain\_type {clock} -domain\_name {clk2}
The following example removes the set domain named "myset":
smartpower\_remove\_domain -domain\_type {set} -domain\_name {myset}

#### See Also

Tcl documentation conventions Designer Tcl Command Reference smartpower\_create\_domain

## smartpower\_remove\_file

Tcl command; removes a VCD file from the specified mode or all operating mode. Frequency and probability information of signals annotated by the VCD are set back to the default value..

```
remove_file
-file {value} \
-format {value} \
-opmode {value} \
```

#### Arguments

-file {value}

Specifies the file to be removed. This is mandatory.



#### -format VCD

Specifies that the type to be removed is a VCD file. This is mandatory.

[-opmode {value}]

Specifies the operating mode. This is optional. The following table shows the acceptable values for this argument:

Value	Description
Active	The operating mode is set to active
Standby	The operating mode is set to static
Flash*Freeze	The operating mode is set to Flash*Freeze

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Examples**

This example removes the file test.vcd from the Active mode.

smartpower\_remove\_file -file "test.vcd" -format VCD -opmode "Active"
This example removes the VCD file power1.vcd from all operating modes:

smartpower\_remove\_file -file "powerl.vcd" -format VCD

#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

#### smartpower\_remove\_pin\_enable\_rate

# This command was obsoleted in SmartPower v8.5. Update your script to use smartpower\_remove\_pin\_probability to remove the pin probability.

Note: The information below is obsolete and should only be used as reference when executing previouslycreated scripts. Update your scripts to use smartpower\_remove\_pin\_probability.

Removes the probability value associated with a specific pin. This pin will have a default probability based on the domain set it belongs to.

smartpower\_remove\_pin\_enable\_rate -pin\_name {pin\_name}

## Arguments

-pin\_name {pin\_name}

Specifies the name of the pin with the probability to remove. This pin must be the direct driver of an enable pin.

## **Supported Families**

SmartFusion, IGLOO, ProASIC3, Fusion

## **Exceptions**

None

#### **Examples**

The following example removes the probability of the pin driving the enable pin of a bidirectional I/O: Smartpower\_remove\_pin\_enable\_rate -pin\_name mybibuf/U0/U1:EOUT

# smartpower\_remove\_pin\_frequency

Tcl command; removes the frequency associated with a specific pin. This pin will have a default frequency based on its domain.

smartpower\_remove\_pin\_frequency -pin\_name {pin\_name}

### **Arguments**

-pin\_name {pin\_name}

Specifies the name of the pin for which the frequency will be removed.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Notes**

The pin\_name must be the name of a pin that already exists in the design and already belongs to a domain.

#### **Examples**

The following example removes the frequency from the pin named "count8\_clock": smartpower\_remove\_pin\_frequency -pin\_name {count8\_clock}

#### See Also

Tcl documentation conventions Designer Tcl Command Reference smartpower\_set\_pin\_frequency

# smartpower\_remove\_pin\_of\_domain

Tcl command; removes a clock pin or a data pin from a clock or set domain, respectively.

```
smartpower_remove_pin_of_domain -pin_name {pin_name} -pin_type {value} -domain_name
{domain_name} -domain_type {value}
```

## Arguments

-pin\_name {pin\_name}

Specifies the name of the pin to remove from the domain.

```
-pin_type {value}
```

Specifies the type of the pin to remove. The following table shows the acceptable values for this argument:

Value	Description
clock	The pin to remove is a clock pin
data	The pinto remove is a data pin

-domain\_name {domain\_name}

Specifies the name of the domain from which to remove the pin.
-domain\_type {value}



Specifies the type of domain from which the pin is being removed. The following table shows the acceptable values for this argument:

Value	Description
clock	The domain is a clock domain
set	The domain is a set domain

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Notes**

The domain name must be the name of an existing domain. The pin name must be the name of an existing pin.

#### **Examples**

The following example removes the clock pin named "XCMP3/UO/U1:Y" from the clock domain named "clockh":

smartpower\_remove\_pin\_of\_domain -pin\_name {XCMP3/U0/U1:Y}

-pin\_type {clock} -domain\_name {clockh} -domain\_type {clock}

The following example removes the data pin named "count2\_en" from the set domain named "InputSet": smartpower\_remove\_pin\_of\_domain -pin\_name {count2\_en} -pin\_type {data} -domain\_name {InputSet} -domain\_type {set}

#### See Also

Tcl documentation conventions Designer Tcl Command Reference smartpower\_add\_pin\_in\_domain

# smartpower\_remove\_pin\_probability

Tcl command; removes the probability value associated with a specific pin. This pin will have a default probability based on the domain set it belongs to.

smartpower\_remove\_pin\_probability -pin\_name {pin\_name}

## **Arguments**

-pin\_name {pin\_name}

Specifies the name of the pin with the probability to remove. This pin must be the direct driver of an enable pin.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## **Examples**

The following example removes the probability of the pin driving the enable pin of a bidirectional I/O: Smartpower\_remove\_pin\_probability -pin\_name mybibuf/U0/U1:EOUT

#### See Also

Tcl documentation conventions Designer Tcl Command Reference smartpower\_set\_pin\_probability

# smartpower\_remove\_scenario

Tcl command; removes a scenario from the current design.

smartpower\_remove\_scenario -name {value}

#### **Arguments**

-name {value} Specifies the name of the scenario.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Examples**

This example removes a scenario from the current design: smartpower\_remove\_scenario -name myscenario

#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

## smartpower\_restore

Tcl command; restores all power information previously committed in SmartPower.

smartpower\_restore

## Arguments

None

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Examples**

smartpower\_restore

#### See Also

Tcl documentation conventions Designer Tcl Command Reference smartpower\_commit



# smartpower\_set\_mode\_for\_analysis

Tcl command; sets the mode for cycle-accurate power analysis.

```
smartpower_set_mode_for_analysis -mode {value}
```

## **Arguments**

-mode {value}

Specifies the mode for cycle-accurate power analysis.

Value	Description
Active	The operating mode is set to Active
Standby	The operating mode is set to Standby
Flash*Freeze	The operating mode is set to Flash*Freeze

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## **Examples**

The following example sets the mode for analysis to active:

smartpower\_set\_mode\_for\_analysis -mode {active}

#### See Also

<u>Tcl documentation conventions</u> <u>Designer Tcl Command Reference</u>

# smartpower\_set\_mode\_for\_pdpr

This SmartPower Tcl command sets the operating mode used by the Power Driven Place and Route (PDPR) tool during power optimization.

smartpower\_set\_mode\_for\_pdpr -opmode { value}

#### **Parameters**

-opmode {value}

Value must be a valid operating mode.

This parameter is mandatory.

Sets the operating mode for your power driven place and route.

#### **Exceptions**

None

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

## **Return Value**

This command does not return a value.

## **Examples**

This example sets the Active mode as the operating mode for Power Driven Place and Route. set\_mode\_for\_pdpr -opmode "Active"

This example creates a custom mode and set it to be used by Power Driven Place and Route (PDPR).

smartpower\_add\_new\_custom\_mode -name "MyCustomMode" \
-description "for PDPR" -base\_mode "Active"

smartpower\_set\_mode\_for\_pdpr -opmode "MyCustomMode

## See Also

Tcl Command Documentation Conventions

# smartpower\_set\_operating\_condition

Tcl command; sets the operating conditions used in SmartPower to one of the pre-defined types.

smartpower\_set\_operating\_condition -opcond {value}

## Arguments

-opcond  $\{\textit{value}\}$ 

Specifies the value of the operating condition. The following table shows the acceptable values for this argument:

Value	Description
best	Sets the operating conditions to best
typical	Sets the operating conditions to typical
worst	Sets the operating conditions to worst

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Examples**

This example sets the operating conditions to best:

smartpower\_set\_operating\_condition -opcond {best}

#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference



# smartpower\_set\_operating\_conditions

Tcl command; sets the operating conditions used in SmartPower.

```
smartpower_set_operating_conditions "still_air | 1.0_mps | 2.5_mps | custom" -heatsink
"None | custom | 10mm_Low_Profile | 15mm_Medium_Profile | 20mm_High_Profile" -boardmodel
"None_Conservative | JEDEC_2s2p" [-teta_ja "decimal value"] [-teta_sa "decimal value"]
```

#### Arguments

-still\_air {value}

Specifies the value for the still air operating condition. The following table shows the acceptable values for this argument:

Value	Description
1.0_mps	Sets the operating conditions to best
2.5_mps	Sets the operating conditions to typical
custom	Sets the operating conditions to worst

#### -heatsink {value}

Specifies the value of the operating condition. The following table shows the acceptable values for this argument:

Value	Description
none	No heat sink
custom	Sets a custom heat sink size
10mm_Low_Profile	10 mm heat sink
15mm_Low_Profile	15 mm heat sink
20mm_High_Profile	20 mm heat sink

#### -boardmodel {value}

Specifies your board model. The following table shows the acceptable values for this argument:

Value	Description
None_Conservative	No board model, conservative routing
JEDEC_2s2p	JEDEC 2s2p board model

```
-teta_ja {decimal_value}
```

Optional; sets your teta ja value; must be a positive decimal

```
-teta_sa {decimal_value}
```

Optional; sets your teta sa value; must be a positive decimal.

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Examples**

#### This example sets the operating conditions to best:

```
set_operating_conditions -airflow "still_air" -heatsink "None" -boardmodel
"None_Conservative "
```

#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

# smartpower\_set\_pin\_frequency

Tcl command; sets the frequency of a pin in megahertz (MHz). If you do not use this command, each pin will have default frequency based on its domain.

smartpower\_set\_pin\_frequency -pin\_name {pin\_name} -pin\_freq {value}

#### **Arguments**

-pin\_name {pin\_name}

Specifies the name of the pin for which the frequency will be set. -pin\_freq {value} Specifies the value of the frequency in MHz, which can be any positive decimal number.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### Notes

The *pin\_name* must be the name of a pin that already exists in the design and already belongs to a domain. When specifying the unit, a space must be between the frequency value and the unit.

#### **Examples**

This example sets the frequency of the pin named "count8\_clock" to 100 MHz: smartpower\_set\_pin\_frequency -pin\_name {count8\_clock} -pin\_freq {100}

#### See Also

Tcl documentation conventions Designer Tcl Command Reference smartpower\_remove\_pin\_frequency

# smartpower\_set\_pin\_probability

Enables you to set the probability value of a pin driving an enable pin. For I/Os, if you do not use this command, the probability of the IOEnableSet is used. For memories, if you do not use this command, the probability of the MemoriesEnableSet is used.

```
smartpower_set_pin_probability -pin_name {pin_name} -pin_enable_rate {value}
```

## Arguments

-pin\_name {pin\_name}

Specifies the name of a pin for which the probability will be set. This pin must be the direct driver of an enable pin.

-pin\_proba {value}



Specifies the value of the pin probability as a percentage, which can be any positive decimal between 0 and 100, inclusive.

#### **Supported Families**

SmartFusion, IGLOO, ProASIC3, Fusion

#### **Notes**

None

## **Exceptions**

None

## **Examples**

The following example sets the probability of the pin driving the enable pin of a bidirectional I/O smartpower\_set\_pin\_probability -pin\_name mybibuf/U0/U1:EOUT \
-pin\_proba 50.4

#### See Also

smartpower\_remove\_pin\_probability

## smartpower\_set\_process

Tcl command; sets the process used in SmartPower to one of the pre-defined types.

```
smartpower_set_process -process {value}
```

#### **Arguments**

#### -process {value}

Specifies the value of the operating condition. The following table shows the acceptable values for this argument:

Value	Description
Typical	Sets the process for SmartPower to typical
Maximum	Sets the process for SmartPower to maximum

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Examples**

This example sets the operating conditions to typical: smartpower\_set\_process -process {Typical}

#### See Also

Tcl documentation conventions



# smartpower\_set\_scenario\_for\_analysis

Tcl command; sets the scenario for cycle-accurate power analysis.

```
smartpower_set_scenario_for_analysis -scenario{value}
```

### Arguments

-scenario {value} Specifies the mode for cycle-accurate power analysis.

#### **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Examples**

The following example sets the scenario for analysis to my\_scenario: smartpower\_set\_scenario\_for\_analysis -scenario {my\_scenario}

#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

## smartpower\_set\_temperature\_opcond

Tcl command; sets the temperature in the operating conditions to one of the pre-defined types.

smartpower\_set\_temperature\_opcond -use{value}

#### Arguments

#### -use{value}

Specifies the temperature in the operating conditions. The following table shows the acceptable values for this argument:

Value	Description
oprange	Sets the temperature in the operating conditions as specified in your <u>Project Settings</u> .
design	Sets the temperature in the operating conditions as specified in the SmartPower design-wide operating range. Applies to SmartPower only.
mode	Sets the temperature in the operating conditions as specified in the SmartPower mode-specific operating range. Applies to SmartPower only.

## **Supported Families**

See the Tcl Commands and Supported Families table for the list of families that support this command.

#### **Examples**

This example sets the temperature in the operating conditions as specified in the custom mode-settings: smartpower\_set\_temperature\_opcond -use{mode}



#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

# smartpower\_set\_voltage\_opcond

Tcl command; sets the voltage in the operating conditions.

```
smartpower_set_voltage_opcond -voltage{value} -use{value}
```

## Arguments

#### $-voltage{value}$

Specifies the voltage supply in the operating conditions. The following table shows the acceptable values for this argument:

Value	Description
VDD	Sets the voltage operating conditions for VDD
VDDI 2.5	Sets the voltage operating conditions fo r VDDI 2.5
VPP	Sets the voltage operating conditions for VPP

#### $-use\{value\}$

Specifies the voltage in the operating conditions for each voltage supply. The following table shows the acceptable values for this argument:

Value	Description
oprange	Sets the voltage in the operating conditions as specified in your Project Settings.
design	Sets the voltage in the operating conditions as specified in the SmartPower design-wide operating range. Applies to SmartPower only.
mode	Sets the voltage in the operating conditions as specified in the SmartPower mode-specific operating range. Applies to SmartPower only.

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Examples**

This example sets the VCCA as specified in the SmartPower mode-specific settings: smartpower\_set\_voltage\_opcond -voltage{vcca} -use{mode}

#### See Also

Tcl documentation conventions Designer Tcl Command Reference



# smartpower\_temperature\_opcond\_set\_design\_wide

Tcl command; sets the temperature for SmartPower design-wide operating conditions.

```
smartpower_temperature_opcond_set_design_wide -best{value} -typical{value} -worst{value} -
thermal_mode{value}
```

### **Arguments**

 $-best{value}$ 

Specifies the best temperature (in degrees Celsius) used for design-wide operating conditions.

 $-typical\{value\}$ 

Specifies the typical temperature (in degrees Celsius) used for design-wide operating conditions. -worst{value}

Specifies the worst temperature (in degrees Celsius) used for design-wide operating conditions. -thermal\_mode{value}

Specifies the mode in which the junction temperature is computed. The following table shows the acceptable values for this argument:

Value	Description
ambient	The junction temperature will be iteratively computed with total static power
opcond	The junction temperature will be given as one of the operating condition range values specified in the device selection

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Examples**

This example sets the temperature for design-wide operating conditions to Best 20, Typical 30, and Worst 60:

smartpower\_temperature\_opcond\_set\_design\_wide -best{20} -typical{30} -worst{60}

#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

## smartpower\_temperature\_opcond\_set\_mode\_specific

Tcl command; sets the temperature for SmartPower mode-specific operating conditions.

```
smartpower_temperature_opcond_set_mode_specific -opmode{value} - thermal_mode{value} - best{value} -typical{value} -worst{value} -thermal_mode{value}
```

#### **Arguments**

-opmode  $\{value\}$ 

Specifies the operating mode. The following table shows the acceptable values for this argument:



Value	Description
Active	The operating mode is set to Active
Standby	The operating mode is set to Standby
Flash*Freeze	The operating mode is set to Flash*Freeze

#### -thermal\_mode{value}

Specifies the mode in which the junction temperature is computed. The following table shows the acceptable values for this argument:

Value	Description
ambient	The junction temperature will be iteratively computed with total static power
opcond	The junction temperature will be given as one of the operating condition range values specified in the device selection

#### -best{value}

Specifies the best temperature (in degrees Celsius) for the selected mode.

 $-typical\{value\}$ 

Specifies the typical temperature (in degrees Celsius) for the selected mode. -worst{value}

Specifies the worst temperature (in degrees Celsius) for the selected mode.

#### **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Examples**

This example sets the temperature for mode-specific operating conditions for mode1:

```
\label{eq:smartpower_temperature_opcond_set_mode_specific -mode{mode1} -best{20} -typical{30} -worst{60}
```

#### See Also

<u>Tcl documentation conventions</u> Designer Tcl Command Reference

# smartpower\_voltage\_opcond\_set\_design\_wide

Tcl command; sets the voltage settings for SmartPower design-wide operating conditions.

```
smartpower_voltage_opcond_set_design_wide -voltage{value} -best{value} -typical{value} -
worst{value}
```

#### **Arguments**

 $-voltage{value}$ 

Specifies the voltage supply in the operating conditions. The following table shows the acceptable values for this argument:

Value	Description
VDD	Sets the voltage operating conditions for VDD
VDDI 2.5	Sets the voltage operating conditions for VDDI 2.5
VPP	Sets the voltage operating conditions for VPP
VCCA	Sets the voltage operating conditions for VCCA
VCCI 3.3	Sets the voltage operating conditions for VCCI 3.3
VCCI 2.5	Sets the voltage operating conditions for VCCI 2.5
VCCI 1.8	Sets the voltage operating conditions for VCCI 1.8
VCCI 1.5	Sets the voltage operating conditions for VCCI 1.5
VCC33A	Sets the voltage operating conditions for VCC33A
VCCDA	Sets the voltage operating conditions for VCCDA

#### -best{value}

Specifies the best voltage used for design-wide operating conditions.
-typical{value}
Specifies the typical voltage used for design-wide operating conditions.
-worst{value}
Specifies the worst voltage used for design-wide operating conditions.

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

## **Examples**

This example sets VCCA for design-wide to best 20, typical 30 and worst 40: smartpower\_voltage\_opcond\_set\_design\_wide -voltage{VCCA} -best{20} -typical{30} worst{40}

#### See Also

Tcl documentation conventions Designer Tcl Command Reference

# smartpower\_voltage\_opcond\_set\_mode\_specific

Tcl command; sets the voltage settings for SmartPower mode-specific use operating conditions.

```
smartpower_voltage_opcond_set_mode_specific -opmode{value} -voltage{value} -best{value} -
typical{value} -worst{value}
```

#### Arguments

-opmode  $\{value\}$ 

Use this option to specify the mode from which the operating conditions are extracted to generate the report.



Value	Description
Active	The operating mode is set to Active
Standby	The operating mode is set to Standby
Flash*Freeze	The operating mode is set to Flash*Freeze

#### -voltage{value}

Specifies the voltage in the operating conditions. The following table shows the acceptable values for this argument:

Value	Description
VDD	Sets the voltage operating conditions for VDD
VDDI 2.5	Sets the voltage operating conditions for VDDI 2.5
VPP	Sets the voltage operating conditions for VPP
VCCA	Sets the voltage operating conditions for VCCA
VCCI 3.3	Sets the voltage operating conditions for VCCI 3.3
VCCI 2.5	Sets the voltage operating conditions for VCCI 2.5
VCCI 1.8	Sets the voltage operating conditions for VCCI 1.8
VCCI 1.5	Sets the voltage operating conditions for VCCI 1.5
VCC33A	Sets the voltage operating conditions for VCC33A
VCCDA	Sets the voltage operating conditions for VCCDA

-best{value}

Specifies the best voltage used for mode-specific operating conditions. -typical{value} Specifies the typical voltage used for mode-specific operating conditions. -worst{value} Specifies the worst voltage used for mode-specific operating conditions.

## **Supported Families**

See the <u>Tcl Commands and Supported Families</u> table for the list of families that support this command.

#### **Examples**

This example sets the voltage for the static mode and sets best to 20, typical to 30 and worst to 40: smartpower\_voltage\_opcond\_set\_mode\_specific -opmode{active} -voltage{VCCA} -best{20} - typical{30} -worst{40}

#### See Also

<u>Tcl documentation conventions</u> <u>Designer Tcl Command Reference</u>

# SmartPower Obsolete TCL Commands

# smartpower\_initialize\_allclocks

#### This command was obsoleted in SmartPower v8.5. Update your script to use:

<u>smartpower init set clocks options</u> to initialize the clock frequency options of all clock domains. <u>smartpower init set registers options</u> to initialize the frequency and probability of all register outputs. <u>smartpower\_init\_set\_set\_reset\_options</u> to initialize the frequency and probability of all set/reset nets. <u>smartpower\_init\_set\_primaryinputs\_options</u> to initialize the frequency and probability of all primary inputs. <u>smartpower\_init\_set\_combinational\_options</u> to initialize the frequency and probability of all primary inputs. <u>smartpower\_init\_set\_combinational\_options</u> to initialize the frequency and probability of all combinational outputs.

<u>smartpower init do</u> to initialize the frequencies and probabilities for clocks, register outputs, set/reset nets, primary inputs, combinational outputs, enables and other sets of pins, and selects a mode for initialization.

Note: The information below is obsolete and should only be used as reference. Update your scripts to use the TCL commands above.

Initializes the clock frequency and the data frequency of all clock domains with the initialization options.

smartpower\_initialize\_allclocks -with\_clock\_constraints {value} -with\_clock\_freq {value} clock\_freq {value} -with\_data\_freq {value} -data\_freq {value}

#### **Arguments**

-with\_clock\_constraints {value}

This sets the option of initializing the clock frequencies of all clock domains with frequency constraints from SmartTime. The following table shows the acceptable values for this argument:

Value	Description	
true	Sets initialize clock frequencies with clock constraints ON	
false	Sets initialize clock frequencies with clock constraints OFF	

#### -with\_clock\_freq {value}

This sets the option of initializing the clock frequencies with a user input frequency. The following table shows the acceptable values for this argument:

Value	Description
true	Sets initialize clock frequencies with fixed frequency ON
false	Sets initialize clock frequencies with fixed frequency OFF

#### -clock\_freq {value}

Specifies the user input clock frequency in MHz.

-with\_data\_freq {value}

Sets the option of initializing the data frequencies of all clock domains with a user input toggle rate or a user input frequency. The following table shows the acceptable values for this argument:

Value	Description	
true	Sets initialize data frequencies with fixed frequency ON	



Value	Description
false	Sets initialize data frequencies with fixed frequency OFF

#### -data\_freq {value}

Specifies the user input toggle rate or data frequency. If the value is a percentage number such as 20.0 %, it will be interpreted as a toggle rate. If the value is a decimal number in MHz such as 100.0 MHz, it will be interpreted as a fixed frequency value.

## **Supported Families**

SmartFusion, IGLOO, ProASIC3, Fusion

#### Notes

• This command is associated with the functionality of Initialize with SmartTime dialog box.

#### **Exceptions**

None

#### **Examples**

The following example initializes all clocks with clock constraints from SmartTime: smartpower\_initialize\_allclocks -with\_clock\_constraints {true}

# smartpower\_remove\_pin\_enable\_rate

# This command was obsoleted in SmartPower v8.5. Update your script to use smartpower\_remove\_pin\_probability to remove the pin probability.

Note: The information below is obsolete and should only be used as reference when executing previouslycreated scripts. Update your scripts to use smartpower\_remove\_pin\_probability.

Removes the probability value associated with a specific pin. This pin will have a default probability based on the domain set it belongs to.

smartpower\_remove\_pin\_enable\_rate -pin\_name {pin\_name}

#### **Arguments**

#### -pin\_name {pin\_name}

Specifies the name of the pin with the probability to remove. This pin must be the direct driver of an enable pin.

#### **Supported Families**

SmartFusion, IGLOO, ProASIC3, Fusion

#### **Exceptions**

None

#### **Examples**

The following example removes the probability of the pin driving the enable pin of a bidirectional I/O: Smartpower\_remove\_pin\_enable\_rate -pin\_name mybibuf/U0/U1:EOUT

# smartpower\_set\_default\_enable\_rate

This command was obsoleted in SmartPower v8.5. Update your script to use

smartpower\_change\_setofpin\_statistics to set the frequency and probability of the specified domain.

Note: The information below is obsolete and should only be used as reference when executing previouslycreated scripts. Update your scripts to use <u>smartpower\_change\_setofpin\_statistics</u>.

Sets the enable-rate of one of the enable set domains: IOEnableSet or MemoriesEnableSet.

smartpower\_set\_default\_enable\_rate -domain\_name {name} pin\_enable\_rate {value}

## Arguments

-domain\_name {name}

Specifies the name of the domain value of which you want to apply the enable rate value. The domain\_name can be IOsEnableSet or MemoriesEnableSet.

-pin\_enable\_rate {value}

Specifies the value of the pin enable rate as a percentage, which can be any positive decimal between 0 and 100, inclusive.

## **Supported Families**

SmartFusion, IGLOO, ProASIC3 and Fusion

## Notes

• None

## **Exceptions**

None

## **Examples**

The following example sets the enable rate for all the pins belonging to the domain set IOsEnableSet: smartpower\_set\_default\_enable\_rate -domain\_name IOsEnableSet -pin\_enable\_rate 52.2

# smartpower\_set\_domain\_frequency

#### This command was obsoleted in SmartPower v8.5. Update your script to use:

smartpower change setofpin statistics to change the frequencies and probabilities for all sets of pins in a specific domain

smartpower change clock statistics to change the frequencies and probabilities for all clocks in a specific domain

Note: The information below is obsolete and should only be used as reference when executing previouslycreated scripts. Update your scripts to use the TCL commands above.

Sets the frequency of a domain in megahertz (MHz).

```
smartpower_set_domain_frequency -domain_type {value} -domain_name {domain_name} -clock_freq
{value} -data_freq {value} -pin_freq {value}
```

## **Arguments**

-domain\_type {value}

Specifies the type of domain to set. The following table shows the acceptable values for this argument:



Value	Description
clock	The domain is a clock domain
set	The domain is a set domain

#### -domain\_name {domain\_name}

Specifies the name of the domain for which the frequency will be set.

-clock\_freq {value}

Specifies the clock frequency in megahertz (MHz), which can be any positive decimal number. This argument is available only for a clock domain.

-data\_freq {value}

Specifies the data frequency in megahertz (MHz), which can be any positive decimal number. This argument is available only for a clock domain.

-pin\_freq {value}

Specifies the value of the pin frequency in megahertz (MHz), which can be any positive decimal number, which can be any positive decimal number. This argument is available only for a set domain.

#### **Supported Families**

SmartFusion, IGLOO, ProASIC3, Fusion

#### **Notes**

- The domain type must be either clock or set.
- The domain name must be the name of an existing domain.
- The clock frequency must be a positive decimal number. Specifying the unit as part of the frequency value is optional. You must enter a space between the frequency value and the unit. You set the clock frequency only for clock domains.
- The data frequency must be a positive decimal number. Specifying the unit as part of the data frequency value is optional. You must enter a space between the data frequency value and the unit.

## **Exceptions**

None

#### **Examples**

The following example sets the clock and data frequency of a clock domain:

 $\label{eq:smartpower_set_domain_frequency -domain_type {clock} -domain_name {clk1} -clock_freq {32} or {30 MHz} -data_freq {3} or {3 MHz}$ 

The following example sets the data frequency of a set domain:

smartpower\_set\_domain\_frequency -domain\_type {set} -domain\_name {set1} -data\_freq {10}

# smartpower\_set\_pin\_enable\_rate

This command was obsoleted in SmartPower v8.5. Update your script to use smartpower\_set\_pin\_probability to set the pin probability.

Note: The information below is obsolete and should only be used as reference when executing previouslycreated scripts. Update your scripts to use <u>smartpower set pin probability</u>.

Enables you to set the probability value of a pin driving an enable pin. For I/Os, if you do not use this command, the probability of the IOEnableSet is used. For memories, if you do not use this command, the probability of the MemoriesEnableSet is used.

smartpower\_set\_pin\_enable\_rate -pin\_name {pin\_name} -pin\_enable\_rate {value}

#### Arguments

-pin\_name {pin\_name}

Specifies the name of a pin for which the probability will be set. This pin must be the direct driver of an enable pin.

-pin\_enable\_rate {value}

Specifies the value of the pin probability as a percentage, which can be any positive decimal between 0 and 100, inclusive.

#### **Supported Families**

SmartFusion, IGLOO, ProASIC3, Fusion

## **Exceptions**

None

#### **Examples**

The following example sets the probability of the pin driving the enable pin of a bidirectional I/O smartpower\_set\_pin\_enable\_rate -pin\_name mybibuf/U0/U1:EOUT \
-pin\_enable\_rate 50.4

# Data Change History - SmartPower

The data change history report lists power data updates up to the current release that may impact the power consumption of the design.



# **Product Support**

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

# **Customer Service**

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060** From the rest of the world, call **650.318.4460** Fax, from anywhere in the world **650. 318.8044** 

# **Customer Technical Support Center**

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

# **Technical Support**

For Microsemi SoC Products Support, visit http://www.microsemi.com/products/fpga-soc/designsupport/fpga-soc-support.

# Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

# Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

#### Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc\_tech@microsemi.com.

#### **My Cases**

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.



#### Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc\_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

# **ITAR Technical Support**

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc\_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.