# SpaceWire RMAP IP Cores

## Remote Memory Access Protocol (RMAP)

RMAP provides a standard mechanism for reading from, and writing to memory in a remote SpaceWire node. This simple but powerful capability is already designed into components like the SpW-10X router and missions like Bepi-Colombo and MMS. The RMAP standard document is an ECSS standard, ECSS-E-ST-50-52C.

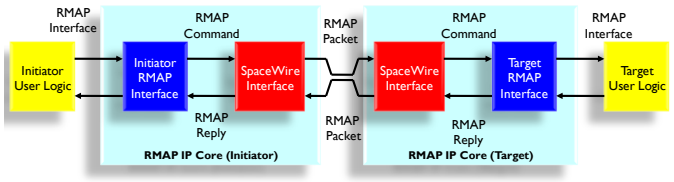
## IP Core Functionality

STAR-Dundee provide two independent SpaceWire RMAP IP Cores that together implement the RMAP standard:

- SpaceWire RMAP Initiator IP core
- SpaceWire RMAP Target IP core.

Both RMAP IP cores come supplied with STAR-Dundee SpaceWire Interface IP blocks to handle SpaceWire protocol point-to-point links.

The separation of the functionality of the RMAP Initiator IP core and the RMAP Target IP core and how, combined, they provide the full RMAP link is illustrated below.




### SpaceWire RMAP Initiator IP Core functionality

The command encoding function is provided by the RMAP Initiator: RMAP packets are initiated in the Initiator User Logic, encoded as RMAP packets in the Initiator Interface, passed to the SpaceWire Interface and then transmitted over the SpaceWire link as an RMAP packet.

The reply decoding function is decoded by the Initiator RMAP Interface and the reply data/information is passed to the Initiator User Logic.

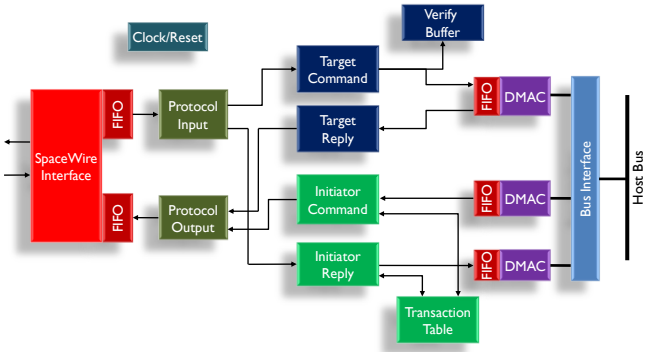
### SpaceWire RMAP Target IP Core functionality

The command decoding function is provided by the RMAP Target: RMAP packets are received by the SpaceWire Interface, decoded by the Target Interface and then the data or information is passed to the Target User Logic after authorisation of the command.

The Target RMAP Interface formats a RMAP reply packet which is sent over the SpaceWire interface.

## Architecture

The architecture of the RMAP cores is illustrated below. The SpaceWire Interface IP implements the SpaceWire serial point to point protocol, ECSS-E-ST-50-12C, and provides FIFO ports to the Protocol Input and Output blocks. The protocol input and output blocks determine the destination of packets dependent on the packet header. The RMAP Target units decode RMAP command packets, read or write data from the host bus and return RMAP reply packets. The RMAP Initiator units accept commands into the transaction table, encodes RMAP command packets, decodes reply RMAP packets and outputs status information. Target and Initiator units interact with the user memory space using DMA controllers.




## Memory Interface

The RMAP controller interface to memory is modelled on the AMBA AHB bus standard, part of the AMBA 2.0 specification. This provides a pipelined control/data bus transfer model. Data is transferred to and from the bus in bursts using internal burst FIFOs in the RMAP core. The bus can be configured for different bus size widths, byte order and bit swapping operations.

## Configuration

The RMAP IP cores are highly configurable using generics at the top level of the RTL port. The configuration options of the IP cores are:

- Host bus width, burst transfer depth, byte/bit order
- Watchdog timer on bus transfers
- Initiator maximum commands, transaction table size
- Internal FIFO sizes, verify buffers size

## Testing

The RMAP Target and RMAP Initiator IP cores have been extensively tested using an in-house testbench, covering many possible configurations and error conditions.

Both IP cores come with the testbench which can be configured to send and receive user specified data packets to and from the ports. The testbench reads the packets to be sent and received from a text command file which specifies the link, time to send the packet and the packet contents.

## Performance and Statistics

The IP cores are generic RTL code which can be synthesized for a range of ASIC and FPGA technologies including Actel and Xilinx.
The cores have been implemented at 200 Mbps in a Xilinx Spartan3E device and currently at 100 Mbps in an Actel AX2000 (with no optimisation). The results are obtained using the Mentor Graphics Precision toolkit (version 2008a.39).

| | Spartan3E1600 Slices | AX2000 Modules | ProASIC3E1500 Tiles |
|---|---|---|---|
| **Initiator** | 2306 (16%) | 7824 (25%) | 8088 (22%) |
| **Target** | 1134 (8%) | 4464 (14%) | 4576 (12%) |

## Licensing

STAR-Dundee SpaceWire IP is available under license, provided as complete VHDL source code.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