Libero® SoC v2021.1

PolarFire® SoC MSS Configurator User Guide

Introduction

The PolarFire SoC MSS Configurator provides a graphical user interface that allows embedded software engineers to quickly define the MSS startup state. It exports an XML file that is consumed by the embedded software flow that converts the XML into initialization constructs. Additionally, the tool outputs a CXZ file for inclusion into your Libero design flow. The CXZ file contains information about metadata and port needed by the FPGA designer to complete the connectivity between the MSS and the FPGA fabric.

MSS configurator is available as a standalone application and as part of the Libero® SoC design tool suite. The information in this user guide applies to both.

Attention: This document is updated for Libero® SoC v2021.1. For Libero SoC v12.6 related help information, refer PolarFire® SoC MSS Configurator User Guide v12.6.

References

See the following reference documents for further details:

- Configuration of the MSS clocks.
  - For detailed information about the MSS clocking features, see UG0913: PolarFire SoC FPGA Clocking Resources User Guide.
- Configuration of the MSS interfaces to the FPGA fabric.
  - For detailed information about the MSS Fabric Interface Controller (FIC) features, see UG0880: PolarFire SoC FPGA Microprocessor Subsystem (MSS) User Guide.
- Selection and assignment of the MSS peripherals to the MSS dedicated I/Os and/or the FPGA fabric dedicated peripheral interfaces.
  - For detailed information about the MSS Peripherals features, see UG0886: PolarFire SoC FPGA Peripherals User Guide.
- Configuration of the MSS Bank voltages and I/O standards and attributes.
  - For detailed information about the MSS Banks and I/Os features, see UG0916: PolarFire SoC FPGA I/O User Guide.
- Configuration of the MSS DDR memories (DDR3/L, DDR4, LPDDR3, and LPDDR4).
  - For detailed information about the MSS DDR4, DDR3, LPDDR3, and LPDDR4 features, see UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide.
- Configuration of the MSS debug features.
  - For detailed information about the MSS debug features, see UG0888: PolarFire SoC FPGA Trace and Debug User Guide.

Table of Contents

1. Installing the PolarFire SoC MSS Configurator

The PolarFire SoC MSS Configurator bundled with Libero is available at the following location in the Libero installation section:

- `Windows: <$Installation_Directory>\Microsemi\Libero_SoC_vX.X\Designer\bin64\pfsoc_mss.exe`
- `Linux: <$Installation_Directory>\Microsemi\Libero_SoC_vX.X\bin64\pfsoc_mss`

The PolarFire SoC MSS Configurator can also be installed as a standalone application.

For information about how to install Libero, see www.microsemi.com/product-directory/design-resources/1750-libero-soc#documents.

1.1 Input and Output Files

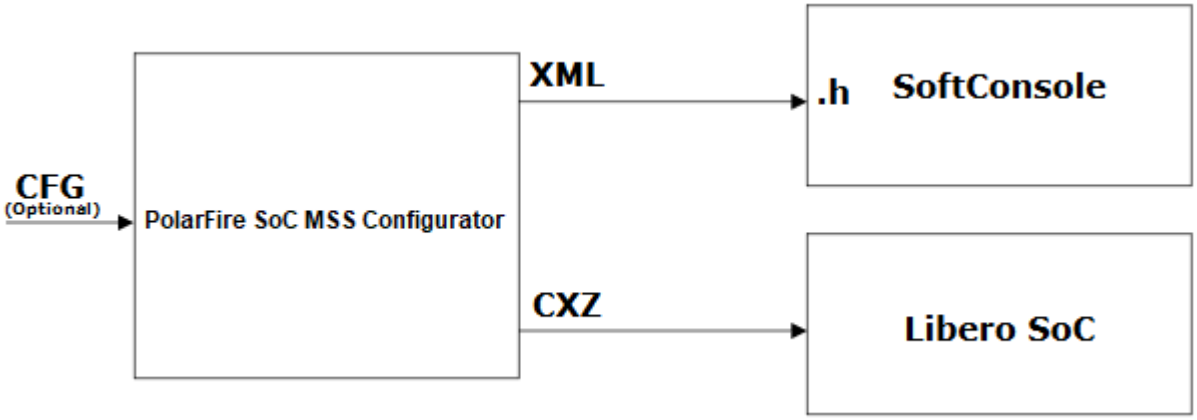
The following sections describe the PolarFire SoC MSS Configurator input and output files.

1.1.1 Output Files

The PolarFire SoC MSS Configurator generates the output file formats shown in the following figure.

- **XML Configuration File** — Contains the MSS memory map, clock, DDR memory controller, and peripheral configuration. The XML file is used to generate hardware files required for building the firmware project.
- **CXZ File** — Encapsulates the hardware design of the MSS block and can be imported into Libero SoC project.

Figure 1-1. PolarFire SoC MSS Configurator Block Diagram



1.1.2 Input files

The PolarFire SoC MSS Configurator can be invoked without any input files. A configuration file (.cfg) from an earlier MSS configurator session, can be optionally provided to the PolarFire SoC MSS Configurator.

Note: A .cfg file and a report file can also be generated from the PolarFire SoC MSS Configurator.

2. Running the PolarFire SoC MSS Configurator

You can run the PolarFire SoC MSS Configurator in Batch mode or Interactive mode.

2.1 Batch Mode

The PolarFire SoC MSS Configurator application can be executed in the Batch mode for scripted execution as follows:

- Windows:

```
 <Libero SoC or Standalone MSS Configurator installation area>\bin64\pfsoc_mss.exe
-CONFIGURATION_FILE:<absolute path for configuration file name (.cfg)>
-OUTPUT_DIR:<absolute path for output directory> -EXPORT_HDL:<true/false> -
LOGFILE:<absolute path for logfile file name>
```

  -EXPORT_HDL and -LOGFILE are optional arguments.

- Linux:

```
<Libero SoC or Standalone MSS Configurator installation area>/bin64/pfsoc_mss
-CONFIGURATION_FILE:<absolute path for configuration file name (.cfg)>
-OUTPUT_DIR:<absolute path for output directory> -EXPORT_HDL:<true/false> -
LOGFILE:<absolute path for logfile file name>
```

  -EXPORT_HDL and -LOGFILE are optional arguments.

Note: Relative path is not supported for PolarFire SoC MSS Configurator. Specify the complete path to execute PolarFire SoC MSS Configurator in Batch mode.

2.2 Interactive Mode

In the Interactive (GUI) mode, the PolarFire SoC MSS Configurator provides the following high-level options.

Table 2-1. Configurator-Project Menu Options

Option	Description
New	Starts configuring a new MSS subsystem.
Open	Opens a configuration (`.cfg`) file.
Save/Save As	Saves the current configuration of the MSS subsystem to a configuration (`.cfg`) file.
Generate	Generates MSS configuration (`.xml`) and component (`.cxz`) files after configuring the MSS subsystem.
Close	Closes the current configuration (`.cfg`) file.

2.3 Using the PolarFire SoC MSS Configurator GUI

The PolarFire SoC MSS Configurator GUI has the following tabs.

- Peripherals
- DDR Memory
- L2 Cache
- Crypto
- Fabric Interface Controllers
- Clocks
- MSS REFCLK I/O

- Bank 4 I/Os
- Bank 2 I/Os
- SGMII I/Os
- Misc
- Memory Partition and Protection

2.3.1 Clocks

Use the **Clocks** tab to configure the MSS PLL clock frequency and clock sources. For more information, see the UG0913: PolarFire SoC FPGA Clocking Resources User Guide.

There are three PLLs inside MSS, which generates the necessary clocks:

- MSS PLL
- DDR PLL
- SGMII PLL

Each PLL generates four output clocks from one input reference clock.

The actual output that can be achieved by the PLL Solver is shown in GUI next to the "Actual:" label. The color of the label is blue, if the requirement is met; it is red, if the requirement (from you) cannot be met.

In case of MSS PLL, you must specify the four output clock requirements.

- Output 0 (CPU Clock)
- Output 1 (Crypto Clock)
- Output 2 (eMMC Clock)
- Output 3 (CAN Clock)

The following conditions pose restrictions on PLL solver. Solver attempts to solve the fixed requirements first and then the ones without restriction.

1. When eMMC is enabled, the output clock requirement is fixed at 200 MHz.
2. When the CAN peripheral is enabled, the output clock requirement must be multiple of 8 (max 80 MHz).
3. Crypto can be at most 200 MHz.
4. CPU has the maximum frequency of 625 MHz.

In case of DDR PLL, the required output clock frequency is entered by you in DDR tab in Line Edit 'Memory clock frequency'. All four output clocks are generated by PLL that is the same frequency.

In case of SGMII PLL, output frequency requirement is fixed at 625 MHz for all four outputs. You do not have to enter this. Additionally, the output clocks are phase shifted by 90° (output 0 clock has 0° phase shift, output 1 clock has 90°, and so on).

The following table lists the option provided in MSS **Clocks** selection tab.

Table 2-2. MSS Clock Selection Tab

Option	Description
MSS Reference Clock Input Source	MSS can be clocked from dedicated I/O from Bank 5 (REFCLK) or North West PLL output.
MSS PLL clock frequency	You can set the frequency value of up to 625 MHz. All MSS clock frequencies are derived from this setting.
MSS CPU cores clock frequency Divider	The MSS CPU clock frequency is based on the MSS PLL clock frequency and is set using the divider values /1, /2, /4, or /8. The frequency must be greater or equal to the MSS AXI clock, and can have a maximum value of 625 MHz.

.....continued

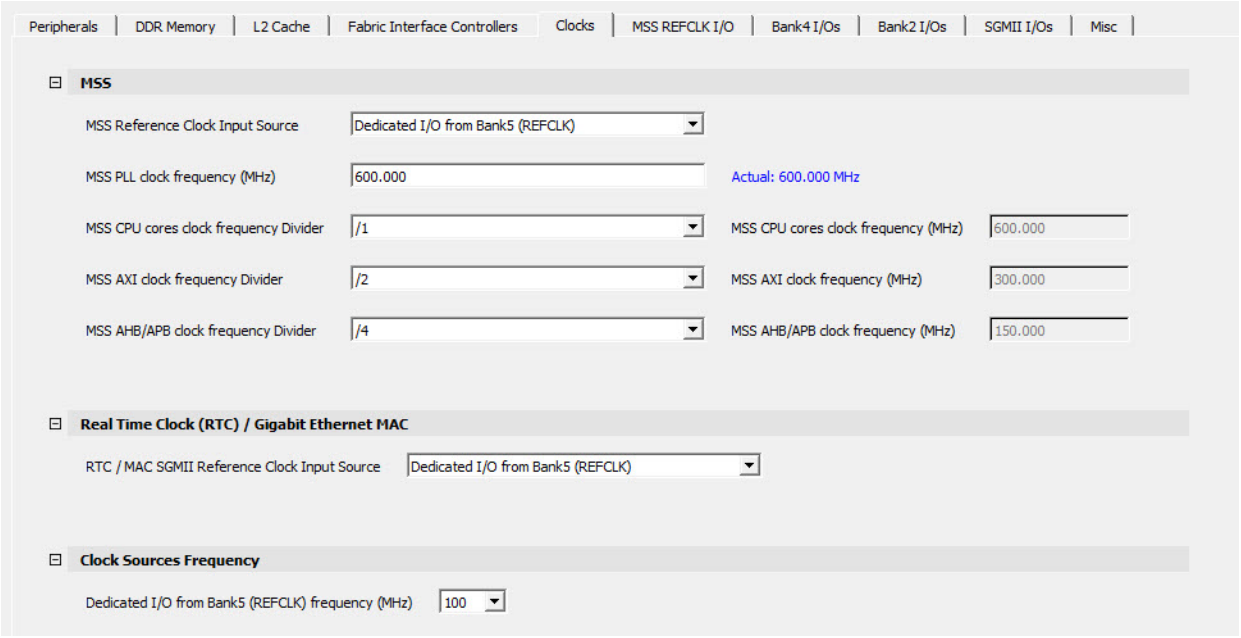
Option	Description
MSS AXI clock frequency Divider	The MSS AXI clock frequency is based on the MSS CPU clock frequency and is set using the divider values of /1, /2, /4, or /8. The frequency must be greater or equal to MSS AHB/APB clock, and can have a maximum value of 312.5 MHz.
MSS AHB/APB clock frequency Divider	The MSS AHB/APB clock frequency is based on the MSS CPU clock frequency and is set using the divider values /2, /4, or /8. The maximum supported frequency is 156.25 MHz.
DDR Reference Clock Input Source	You can select the NW PLL ports or I/Os from Bank 5.
RTC/MAC SGMII Reference Clock Input Source	You can select the NW PLL ports or I/Os from Bank 5.
Dedicated I/O from Bank5 (REFCLK) frequency	This is a dedicated I/O from Bank 5 to the MSS PLL. It can be either be 100 MHz or 125 MHz.
NW PLL (REF_0_PLL_NW) frequency (MHz)/ NW PLL (REF_1_PLL_NW) frequency (MHz)	This option is available when any peripheral is clocked from North West PLL output. It can be any value between 50 MHz to 125 MHz.
Crypto clock frequency from MSS (MHz)	You can set the reference clock frequency for Crypto between 1 MHz to 200 MHz.
MSS CAN clock frequency (MHz)	The MSS CPU clock frequency is based on the MSS PLL clock frequency. The supported frequencies in MHz are 8, 16, 24, 32, 40, 48, 56, 64, 72, and 80.

Note: The **DDR Reference Clock Input Source** option appears only when the DDR Memory type is selected from the **DDR Memory** tab.

The following figure shows the **Clocks** tab in the PolarFire SoC MSS Configurator. In this example, the following configuration is used:

- Dedicated I/Os from Bank 5 (REFCLK) are selected as the reference clock input source for the MSS. The MSS PLL clock frequency is set to 600 MHz.
- Dedicated I/Os from Bank 5 (REFCLK) are used to source the reference clock input frequency for the DDR subsystem.
- The DDR clock source and MSS clock source are set to 125 MHz.

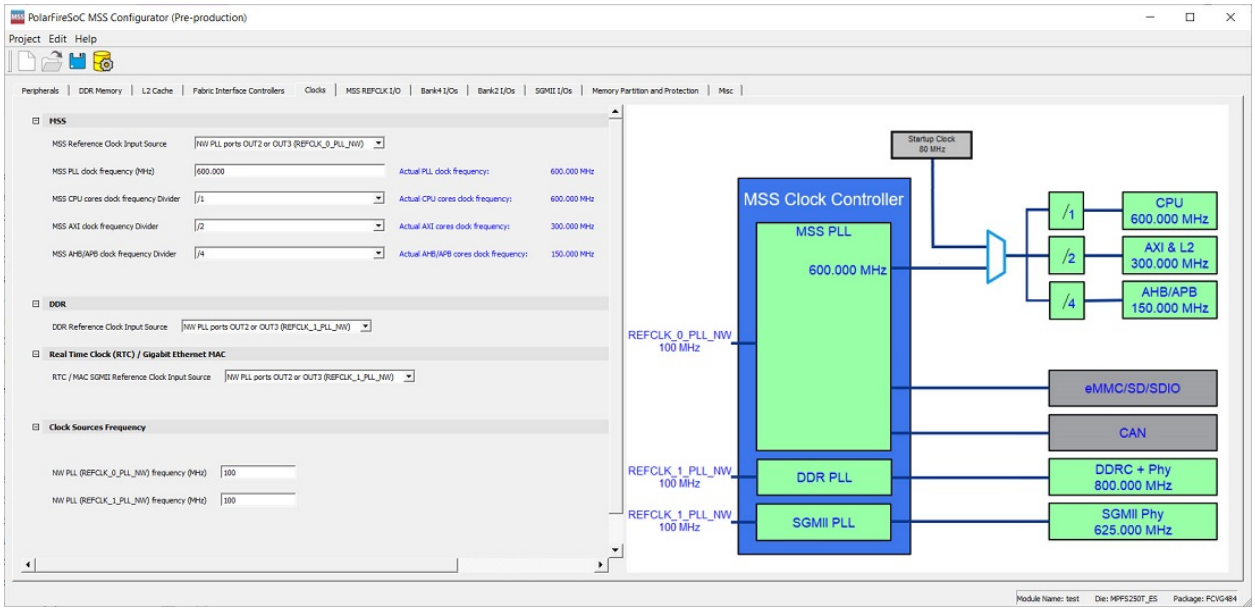
Figure 2-1. Clocks Tab



The following figure shows the **Clocks** tab with PLL in the PolarFire SoC MSS Configurator. In this example, the following configuration is used:

- NW PLL ports OUT2 or OUT3 (REFCLK_0_PLL_NW) are selected as the reference clock input source for the MSS. The MSS PLL clock frequency is set to 600.000 MHz.
- NW PLL ports OUT2 or OUT3 (REFCLK_1_PLL_NW) are used to source the reference clock input frequency for the DDR subsystem and Real Time Clock/Gigabit Ethernet MAC.
- The DDR Clock Source and MSS Clock Source are set to 100 MHz.

Figure 2-2. Clocks Tab with PLL



For more information about configuring the MSS DDR subsystem, see DDR Memory.

2.3.2 Fabric Interface Controllers

Using the **Fabric Interface Controllers** tab, any combination of **FIC_0**, **FIC_1**, **FIC_2**, **FIC_3** can be enabled and configured to support master and slave interfaces. For more information, see the UG0880: PolarFire SoC FPGA Microprocessor Subsystem (MSS) User Guide.

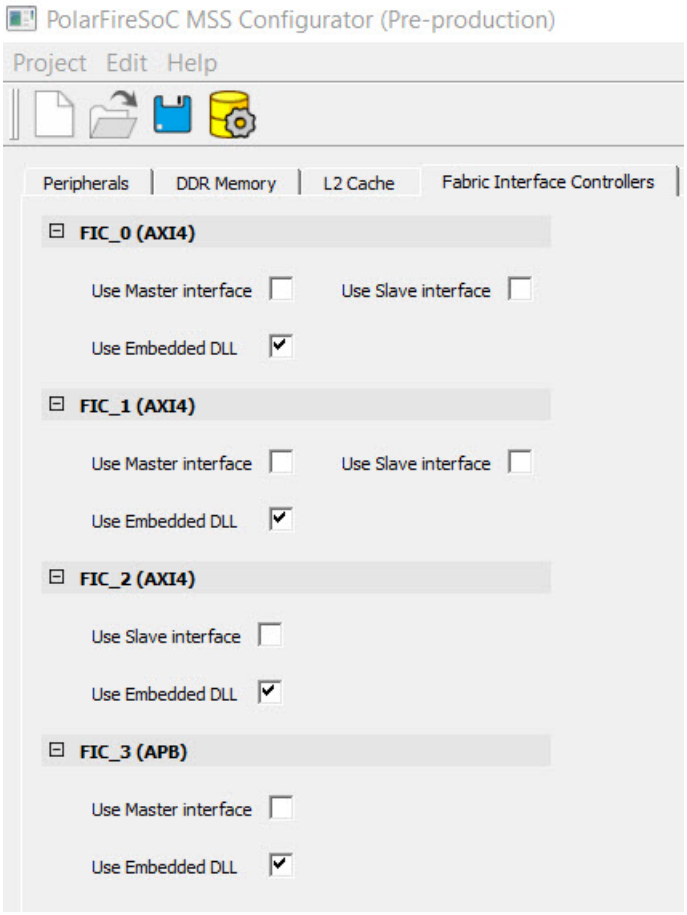
FIC_0, **FIC_1**, and **FIC_2** support AXI4 interfaces, while **FIC_3** supports APB.

For **FIC_0** and **FIC_1** interfaces, both master and slave interfaces can be enabled at the same time. **FIC_2** interface can support only slave interface and **FIC_3** interface can only support master interface. (MSS is master).

FIC_0 and **FIC_1** have both master and slave interfaces to and from the FPGA fabric, while **FIC_2** and **FIC_3** support slave or master interfaces, respectively.

The following figure shows all FIC options available and enabled. By default, the DLLs of all the FICs are enabled.

Figure 2-3. Fabric Interface Controllers Tab

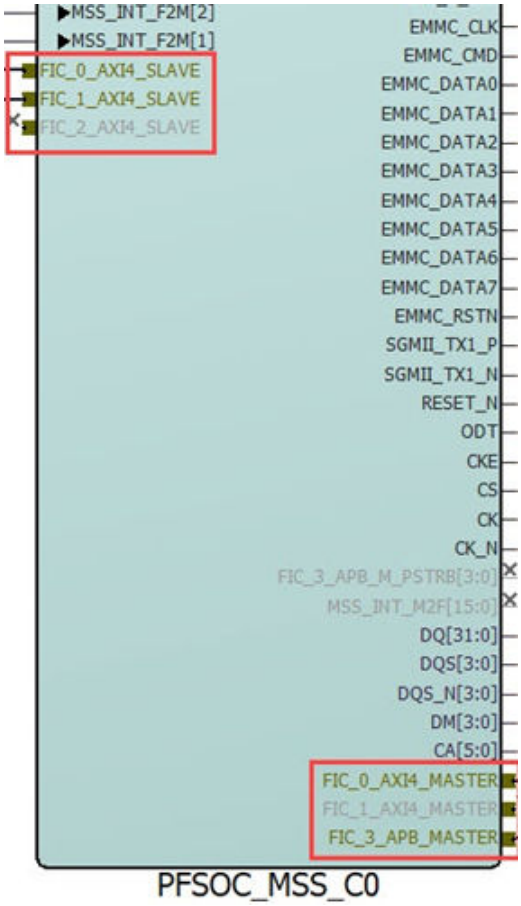


Note: The FIC interface can operate up to 250 MHz. The FIC clock is independent of the MSS clock. If the frequency of the FIC block is greater than or equal to 125 MHz, the embedded DLL must be enabled for removing clock insertion delay. If the frequency of the FIC block is less than 125 MHz, the embedded DLL must be bypassed.

When a master interface is enabled for a FIC, that master interface must be connected to a slave in the fabric. When a slave interface is enabled for a FIC, that slave interface must be connected to a master in the fabric.

There is clock domain crossing logic in the FIC block to address the asynchronous MSS and Fabric clocks and therefore user logic is not required to implement clock domain crossing synchronization for this interface.

Figure 2-4. FIC Interfaces Enabled



Note: The MSS SmartDesign component is visible only after importing the MSS CXZ file.

2.3.3 Peripherals

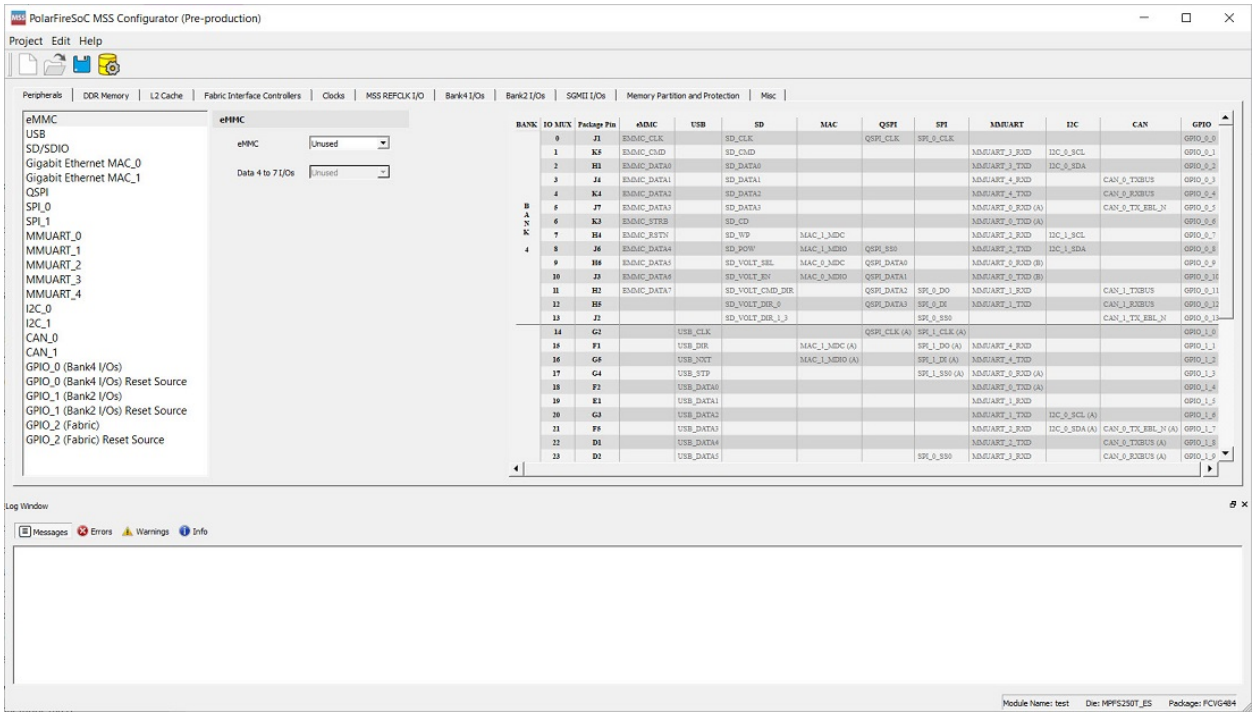
Select the following I/Os using the **Peripherals** tab:

- GPIOs from Bank 2 and Bank 4, which are dedicated to the MSS.
- Fabric I/Os, if the dedicated I/Os from Bank 2 and Bank 4 are not available.
- GPIOs from Bank 5 are dedicated to SGMII but can be routed to GMII or MII fabric I/Os. GPIO from Bank 5 are displayed only when Gigabit Ethernet MAC_0 or Gigabit Ethernet MAC_1 is selected.

Note: I/Os from the DDR bank are dedicated to the DDR Controller in the MSS.

For more information, see UG0880: PolarFire SoC FPGA Microprocessor Subsystem (MSS) User Guide . The following figure shows the **Peripherals** tab on the PolarFire SoC MSS Configurator.

Figure 2-5. Peripherals Tab



By default, all peripherals are marked as unused. To include peripherals that are required in the design, select the peripheral from the left-hand side of the window and use the corresponding drop-down to assign MSS I/Os or fabric I/Os.

The I/Os associated with the following peripherals are dedicated and cannot be assigned to fabric I/Os:

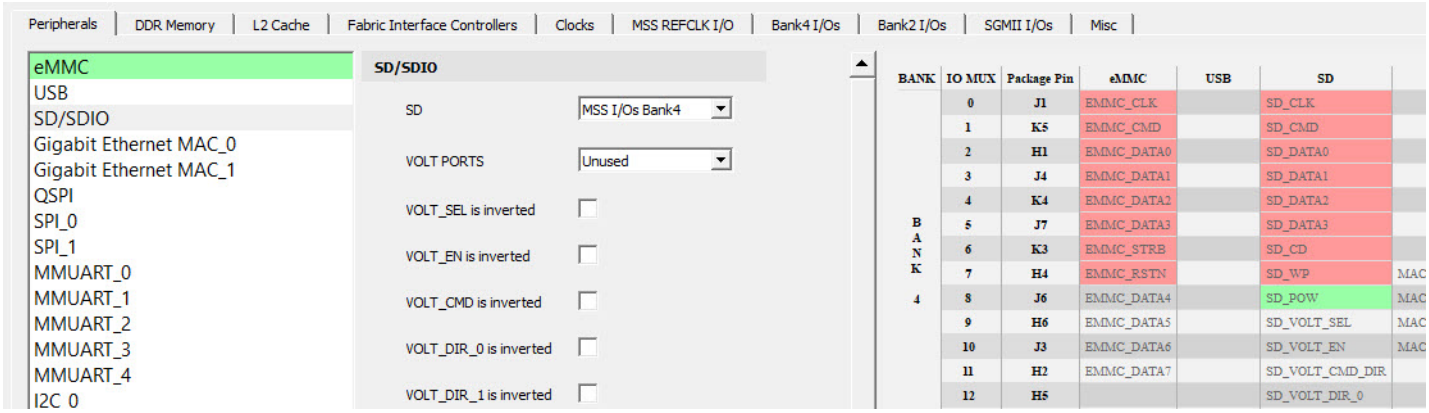
- USB peripherals are dedicated in Bank 2.
- eMMC peripherals are dedicated in Bank 4.
- Ports SD_POW and SD_WP can be disabled when not in use and can be used for other interfaces.
- SD/SDIO peripherals are dedicated in Bank 4.

Note: If the I/Os for a peripheral are selected in a bank, you cannot select the same I/Os for another peripheral from the same bank. If you try, the tool generates the following warning message in the log window.

Figure 2-6. Error Message

For example, eMMC and SD cannot be used simultaneously as shown in the following figure.

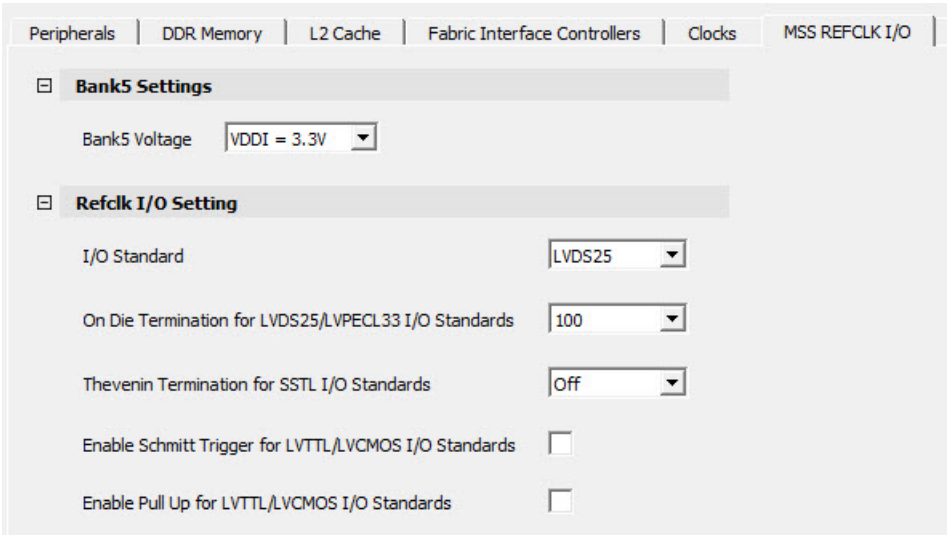
Figure 2-7. Overlapping I/O Warning



2.3.4 MSS REFCLK I/O

Using the **MSS REFCLK I/O** tab, you can select electrical characteristics of the Bank 5 I/Os, as shown in the following figure. The tool generates a warning in the log window for unsupported selections.

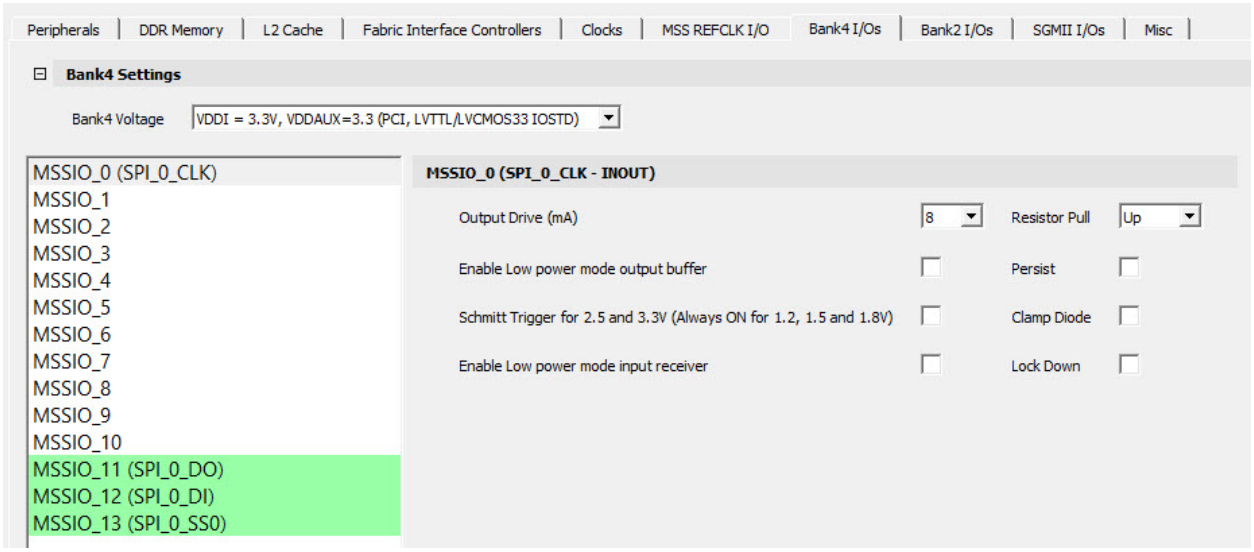
Figure 2-8. MSS REFCLK I/O Tab



2.3.5 Bank4 and Bank2 I/Os

The MSS I/Os are available across Bank 4 and Bank 2. The **Bank4 I/Os and Bank2 I/Os** tabs allow you to select the electrical characteristics of the MSS I/Os. Each MSS I/O along with the settings must be enabled one by one.

Figure 2-9. Bank 4 I/Os Tab



2.3.6 DDR Memory

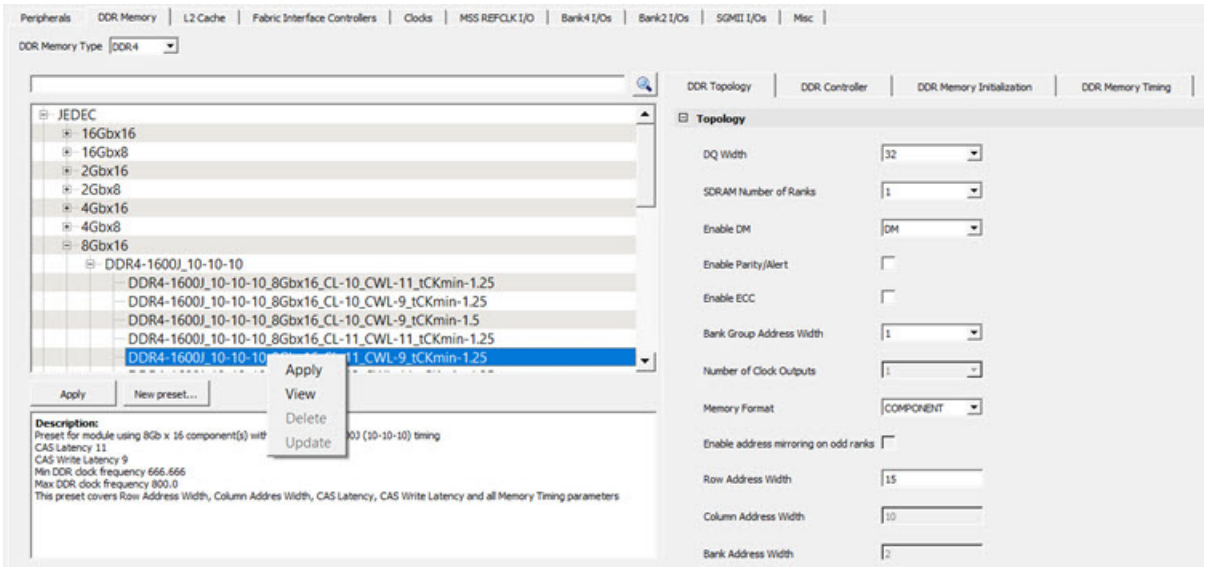
Select the required DDR type from the **DDR Memory Type** pulldown. The DDR configuration options are available on the **DDR Topology**, **DDR Controller**, **DDR Memory Initialization**, and **DDR Memory Timing** tabs (see the following figure).

For more information, see the UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide.

The **DDR Topology** tab, in the following figure, controls the physical aspects of the memory, such as data and address widths, enabling of ECC and DM, and setting the clock frequency.

- For DDR3 and DDR4, the COMPONENT, UDIMM, RDIMM, LRDIMM, and SODIMM memory formats are supported.
- For LPDDR3/4, only the COMPONENT memory format is supported.

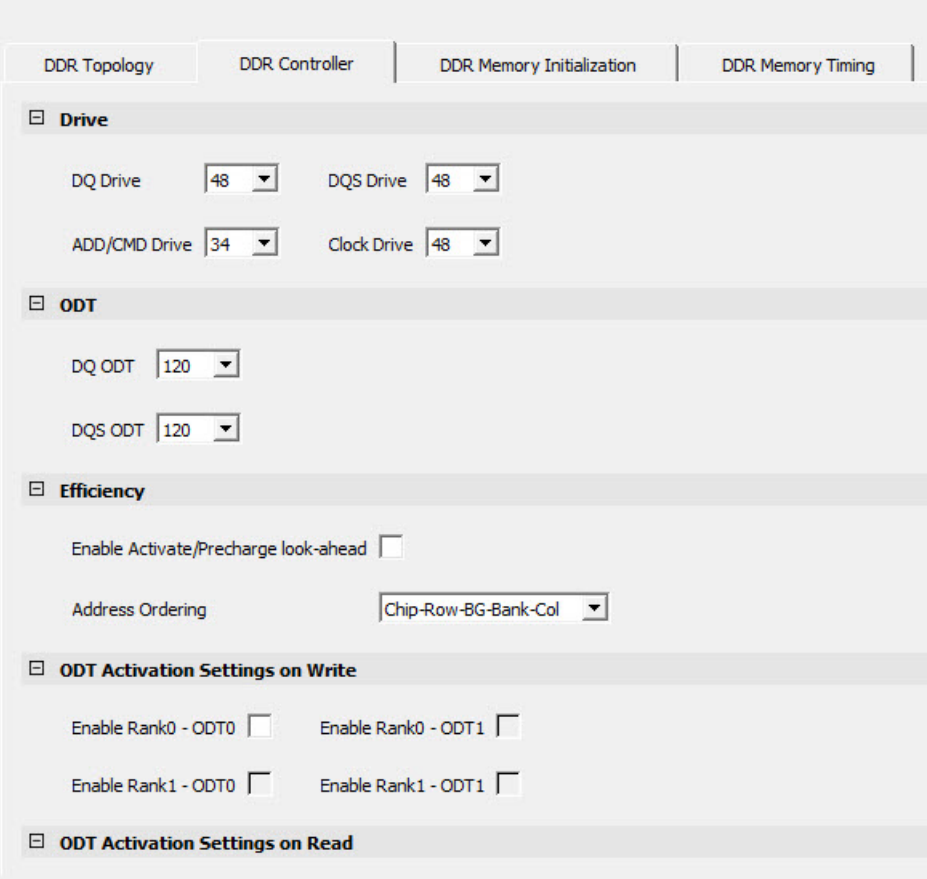
Figure 2-10. DDR Memory Tab



Note: Configure the DDR parameters according to the datasheet from the DDR vendor.

The **DDR Controller** tab controls the DQS Drive, ODT, Precharge look-ahead, and Address Ordering.

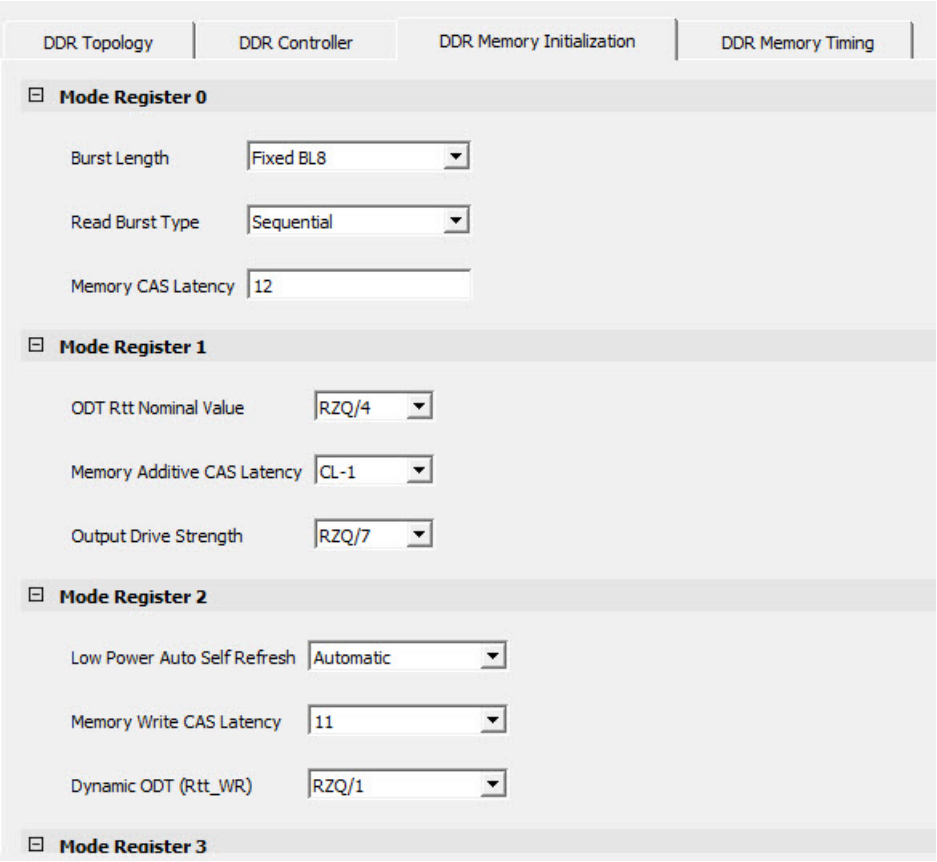
Figure 2-11. DDR Controller Tab



The **DDR Memory Initialization** tab controls the DDR mode register configuration according to the JEDEC specification. In the PolarFire SoC FPGA DDR architecture, these parameters are passed to the start-up code running on the E51 monitor core, which then performs the DDR initialization sequence and configures the mode registers.

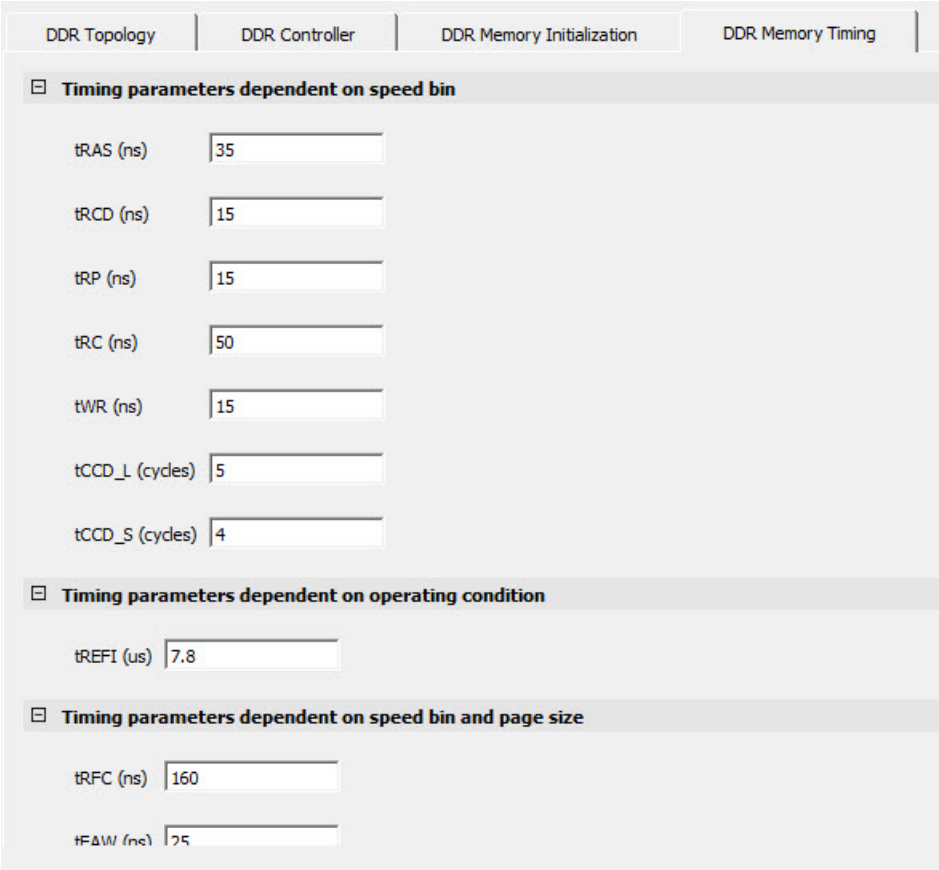
The following figure shows the memory initialization configuration.

Figure 2-12. DDR Memory Initialization



The **DDR Memory Timing** tab controls the timing parameters, which are translated to the appropriate configuration values for the DDR subsystem IP.

Figure 2-13. DDR Memory Timing Tab



2.3.7 Misc

Use the **Misc** tab to enable the following options:

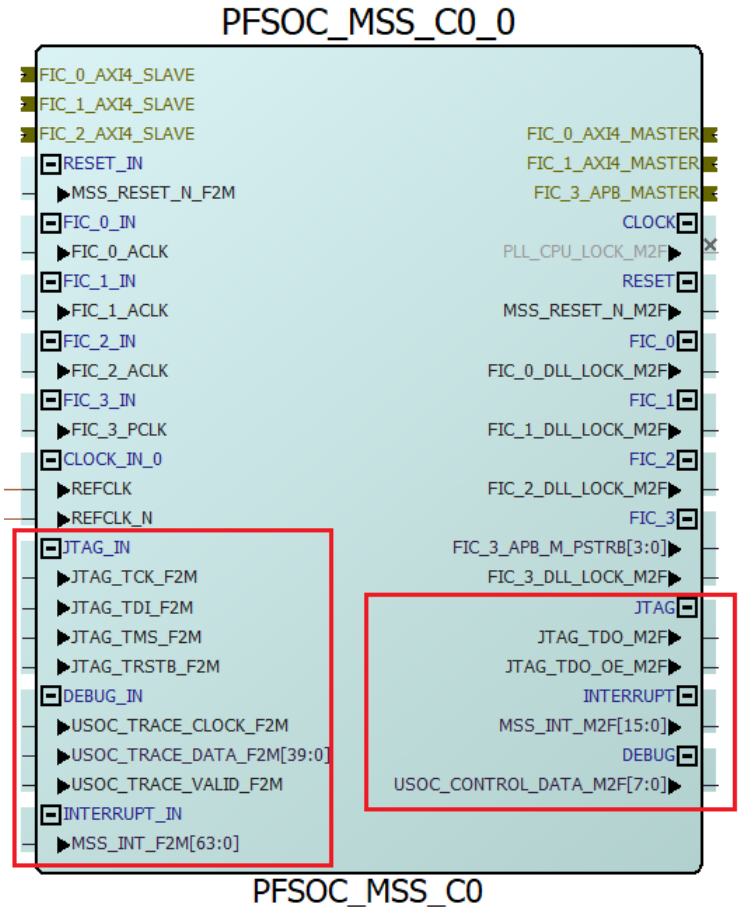
- Trace functionality
- JTAG (Debug) functionality
- Interrupts to/from MSS
- Lock down of Bank 2 and Bank 4 I/Os
- Lock down of DDR and SGMII I/Os

Figure 2-14. Misc Tab

For more information, see UG0888: PolarFire SoC FPGA Trace and Debug User Guide.

By default, these options are marked as unused. When any of the options are enabled, the corresponding ports are exposed on the MSS block (see the following figure).

Figure 2-15. PFSOC_MSS_C0_0 Jtag Trace Enabled

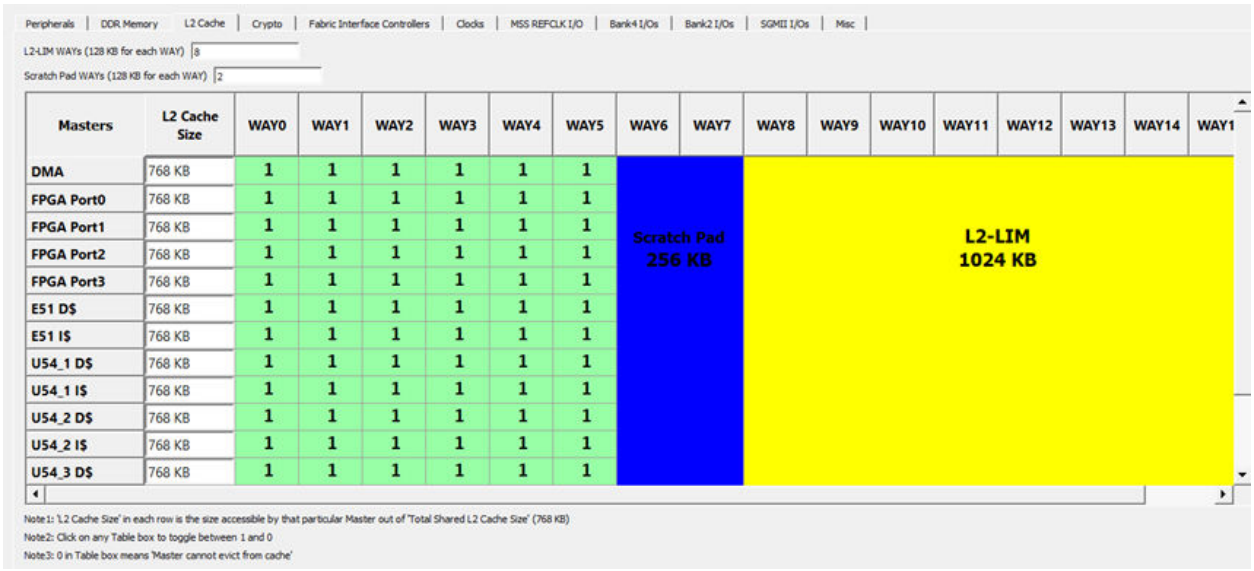


2.3.8 L2 Cache

Level2 memory subsystem has three operating modes – Cache, Loosely-Integrated-Memory (LIM), and Scratchpad. These modes can be configured in MSS configurator using the options in the L2 Cache tab based on user needs. The goal is to make the configuration options easier to use and understand for the users.

Users can allocate L2 memory for the processor or peripheral using the L2 Cache tab as shown in the following table:

Figure 2-16. L2 Cache



In the L2 Cache tab:

- There are 16 WAYs. WAY0 is always allocated for Cache.
- In the GUI, the default L2-LIM size will be set at 15 (WAY1 – WAY15). This means that 1 WAY (128 Kbytes) is configured as L2 cache and 1920 Kbytes is configured as LIM. User can increase or decrease the L2-LIM size to configure the LIM as Cache memory for various processors and peripherals.
- In the GUI, all the WAYs are enabled for Cache by default. The user can disable the selection to allocate it for Scratchpad.
- Cache size shows the amount of memory available and is shared among all processors and peripherals.

2.3.9 SGMII

PolarFire SoC supports two full-duplex SGMII channels (Channel0 and Channel1). Each channel has one RX and one TX. There are two input and two output I/Os that need to be configured for SGMII, and all I/Os are differential.

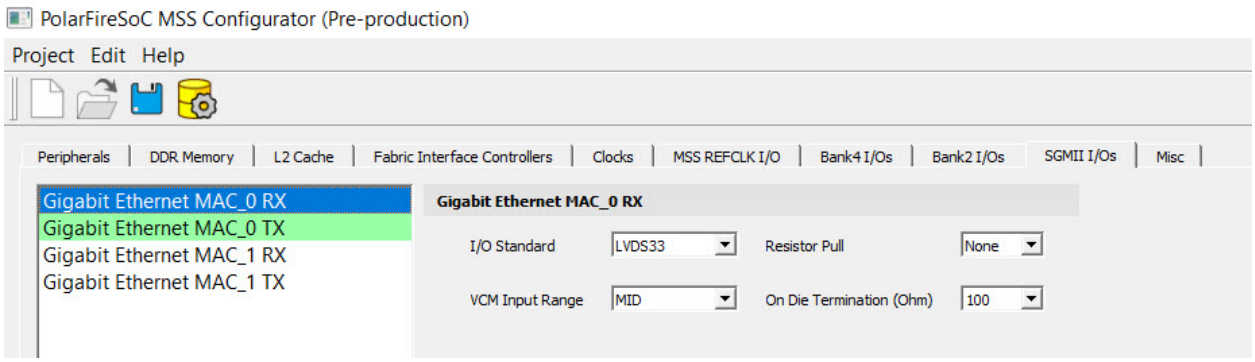
SGMII Inputs

MAC_0 (Channel0) RX and MAC_1 (Channel1) RX are inputs and have the following options:

- I/O Standard
  Note: The IOSTD must match the bank voltage in the **MSS REFCLK I/O** tab. For example, if the bank 5 voltage VDDI is 3.3 V, you cannot set SGMII I/Os to any IOSTD, which is 2.5 V such as LVDS25, RSDS25, MINILVDS25, SUBLVDS25, PPDS25, and LCMDS25.
- Resistor Pull
- VCM Range
- On Die Termination (Ohm)

The following figure shows the SGMII RX.

Figure 2-17. SGMII RX



SGMII RX Register Settings

The following table lists the Channel0/Channel1 RX register settings.

Table 2-3. Channel0/1 RX Register Settings

GUI Labels/Parameter Name	Options
I/O Standard	LVDS33, LVDS25, RSDS33, RSDS25, MINILVDS33, MINILVDS25, SUBLVDS33, SUBLVDS25, PPDS33, PPDS25, LCMDS33, LCMDS25
Resistor Pull	None, Up, Down
VCM Input Range	MID, LOW
On Die Termination (Ohm)	OFF, 100

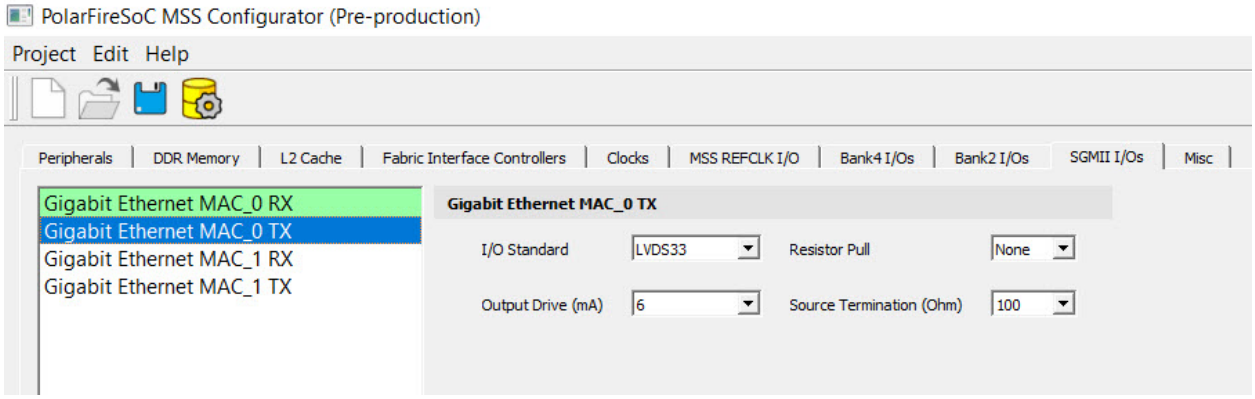
SGMII Outputs

MAC_0 (Channel0) TX and MAC_1 (Channel1) TX are outputs and have the following options:

- I/O Standard
- Resistor Pull
- Output Drive
- Source Termination (Ohm)

The following figure shows the SGMII TX.

Figure 2-18. SGMII TX



SGMII TX Register Settings

The following table lists the Channel0/Channel1 TX register settings.

Table 2-4. Channel0/1 TX Register Settings

GUI Labels/Parameter Name	Options
I/O Standard	LVDS33, LVDS25, RSDS33, RSDS25, MINILVDS33, MINILVDS25, SUBLVDS33, SUBLVDS25, PPDS33, PPDS25, LCMDS33, LCMDS25
Resistor Pull	None, Up, Down
Output Drive (mA)	1.5, 2, 3, 3.5, 4, 6
Source Termination (Ohm)	OFF, 100

SGMII Output I/O Standard Settings

Based on the selection of the I/O standard the user needs to enforce the following DRC checks:

Table 2-5. SGMII Output DRC Check

I/O_TYPE	Direction	Legal Output DRIVE Settings (mA)
LVDS33	Output	6, 4, 3.5, 3
LVDS25	Output	6, 4, 3.5, 3
RSDS33	Output	4, 3, 2, 1.5
RSDS25	Output	4, 3, 2, 1.5
MINILVDS33	Output	6, 4, 3.5, 3
MINILVDS25	Output	6, 4, 3.5, 3
SUBLVDS33	Output	3, 2, 1.5, 1
SUBLVDS25	Output	3, 2, 1.5, 1
PPDS33	Output	4, 3, 2, 1.5
PPDS25	Output	4, 3, 2, 1.5
LCMDS33	Output	6, 4, 3.5, 3
LCMDS25	Output	6, 4, 3.5, 3

I/O Standard and Supported Output Drive

Voltage selection for Bank5 should match the I/O Standard selected for TX and RX in both channels.

Example 2-1.

Bank5 Voltage selection -> VDDI = 3.3v -> LVDS33 is legal but not LVDS25

Table 2-6. Legal Values/Settings for I/O_TYPE/Output Drive Combination

I/O_TYPE	Legal Output DRIVE Settings (mA)
LVDS33	6, 4, 3.5, 3
LVDS25	6, 4, 3.5, 3
RSDS33	4, 3, 2, 1.5

.....continued	
I/O_TYPE	**Legal Output DRIVE Settings (mA)**
RSDS25	4, 3, 2, 1.5
MINILVDS33	6, 4, 3.5, 3
MINILVDS25	6, 4, 3.5, 3
SUBLVDS33	3, 2, 1.5, 1
SUBLVDS25	3, 2, 1.5, 1
PPDS33	4, 3, 2, 1.5
PPDS25	4, 3, 2, 1.5
LCMDS33	6, 4, 3.5, 3
LCMDS25	6, 4, 3.5, 3

2.3.10 Crypto

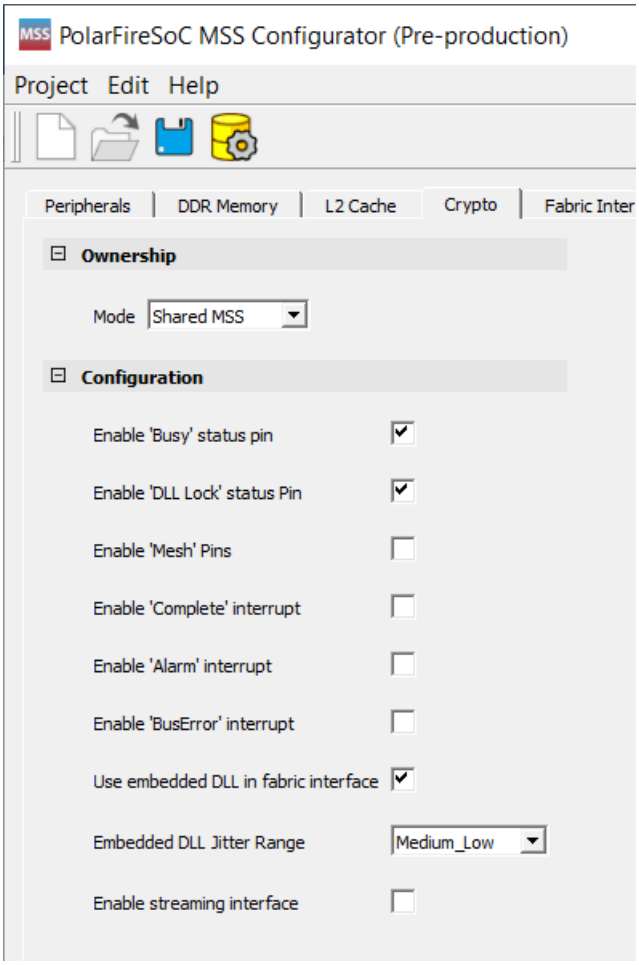
The following table lists the crypto ownership modes.

Table 2-7. Crypto Ownership Modes

Owner	Description
MSS	The MSS owns the crypto.
Fabric	The Fabric owns the crypto and ports are exposed to the fabric.
Shared MSS	This is shared between the MSS and the Fabric. The MSS is the first owner. There are regular ports and other ports for handshaking to switch the ownership.
Shared Fabric	This is shared between the MSS and the Fabric. The Fabric is the first owner. There are regular ports and other ports for handshaking and to switch ownership.

Note: Streaming Interface is not available for Fabric mode.

Figure 2-19. Crypto Tab



In the crypto modes:

- The status pins and interrupt pins are available as configuration options in all the ownership modes except the MSS ownership mode.
- There are three options that expose the DLL lock, Busy, and Mesh ports. The Busy and DLL Lock are ON by default, while the Mesh input pin connects to 0 when not used.
- The **Use embedded DLL in fabric interface** is always provided in all modes and is enabled by default when the **Enable streaming interface** option is selected.

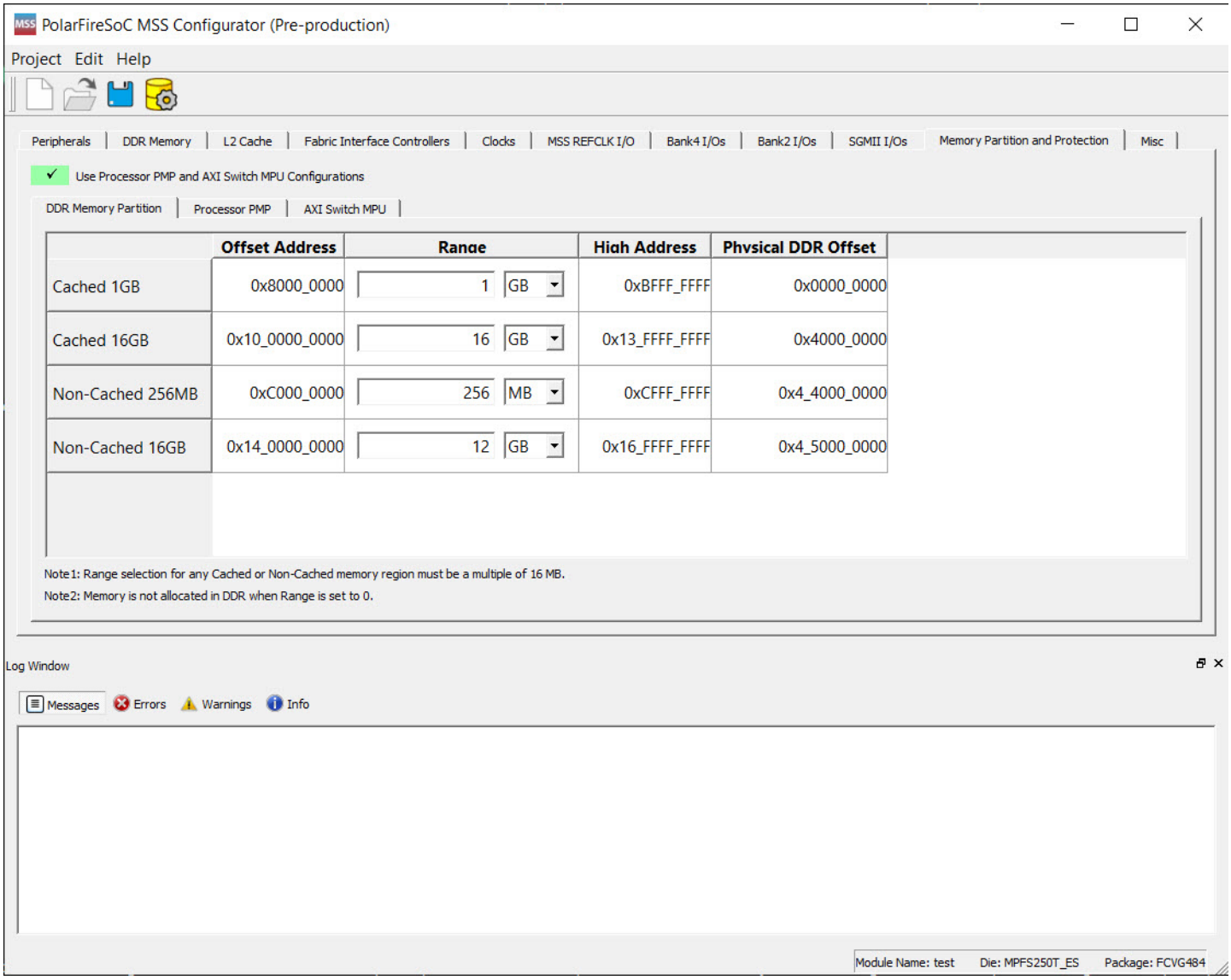
2.3.11 Memory Partition and Protection

The Physical Memory Protection (PMP) prevents a process (running on a RISC-V Processor) or a master (FPGA Fabric) from accessing memory that has not been allocated to it. RISC-V system has PMP unit which provides control registers for each processor to allow physical memory access privileges (read, write, execute) to be specified for each physical memory region. Similarly, the AXI Switch has Memory Protection Unit (MPU) block which provides register control to setup memory access regions for FPGA masters.

DDR Memory Partition

The DDR Memory Partition tab allows the DDR memory to be allocated to cached, non-cached regions depending on the amount of DDR memory physically connected.

Figure 2-20. DDR Memory Partition Tab

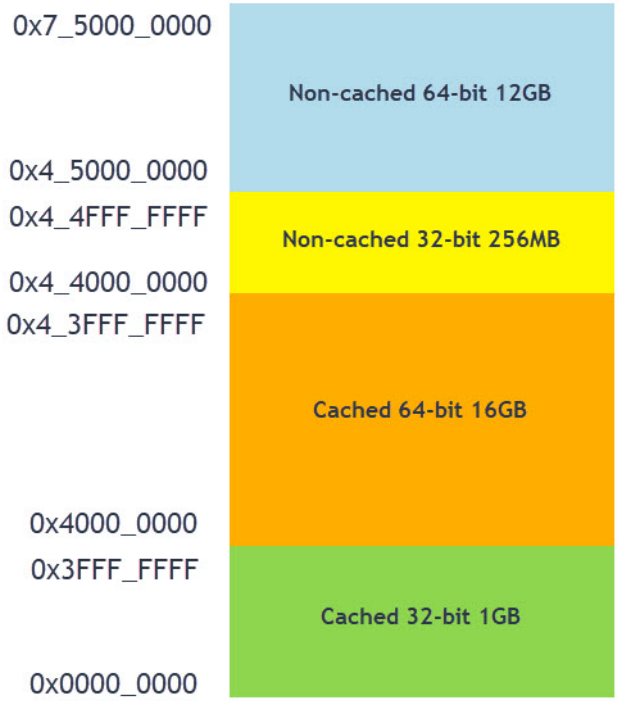


In the DDR Memory Partition:

- The Offset Address (Base Address) for both cached and non-cached regions is fixed.
- High Address is the End Address based on the size.
- Users are expected to enter the Range. Based on the Range selection, High Address and Physical DDR Offset is updated.
  - When Range is set to zero, memory is not allocated in DDR.
  - When Range is set to a non-zero value, it must be a multiple of 16 MB.
- Physical DDR Offset is allocation of DDR memory (connected to the FPGA system) based on the non-zero Range value.
- Range is allocated sequentially starting with 0x0000_0000 in the following order:
  - Cached 32-Bit
  - Cached 64-Bit
  - Non-Cached 32-Bit
  - Non-Cached 64-Bit

The following figure shows the graphical representation of how the Physical DDR Offset allocation is done based on the above ranges:

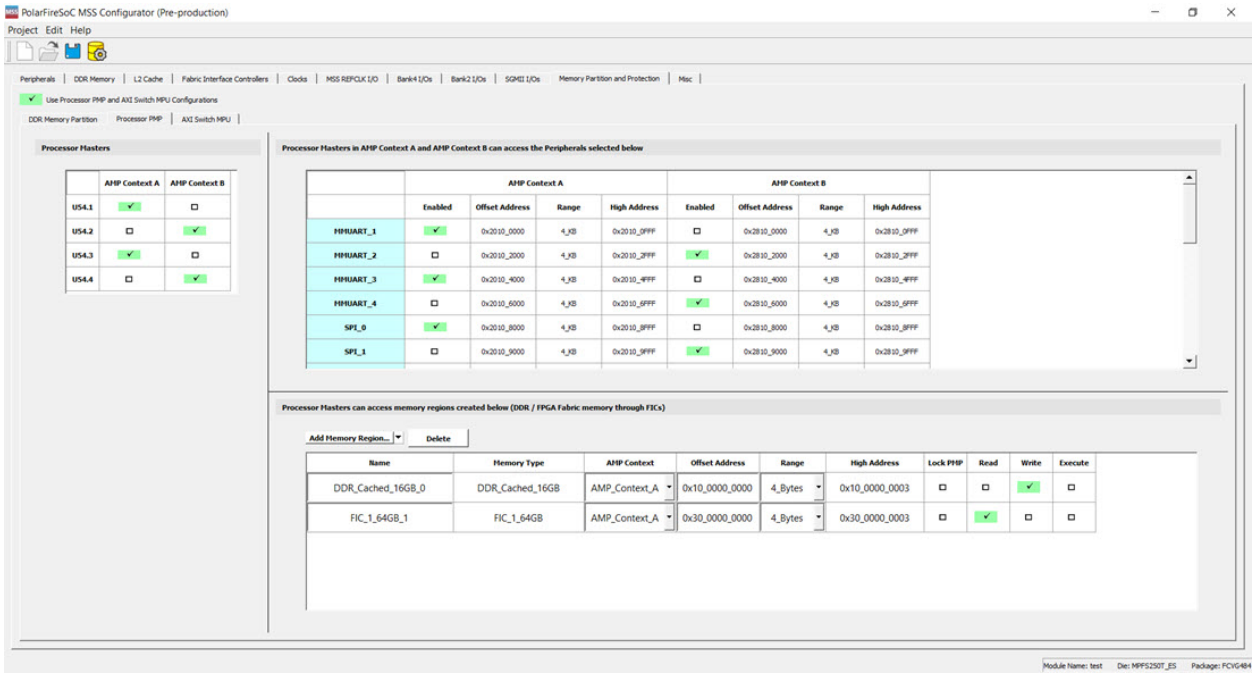
Figure 2-21. Physical DDR Offset - Graphical Representation



Processor PMP

The following figure shows the Processor PMP tab.

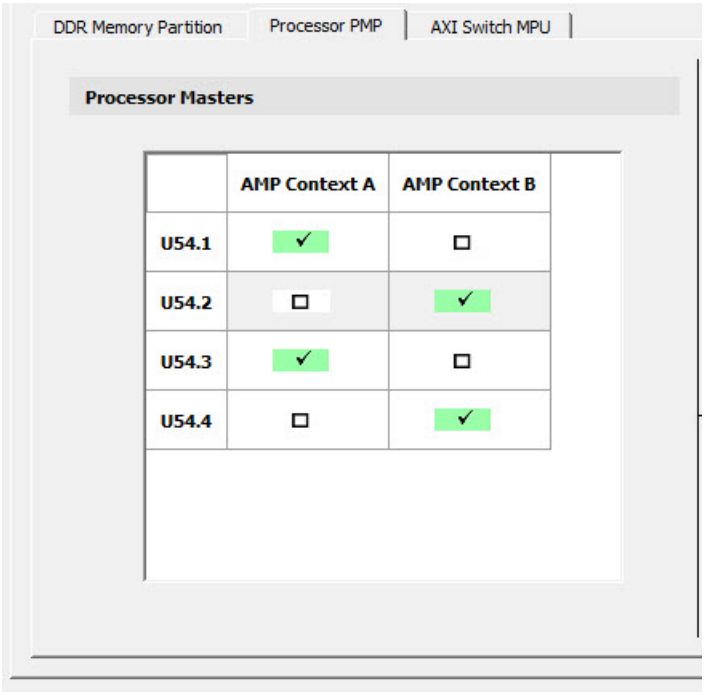
Figure 2-22. Processor PMP Tab



Processor Masters

Four CPU masters can be enabled in one of the two Asymmetric Multi Processing (AMP) contexts. CPU masters can access both CPU and Peripherals.

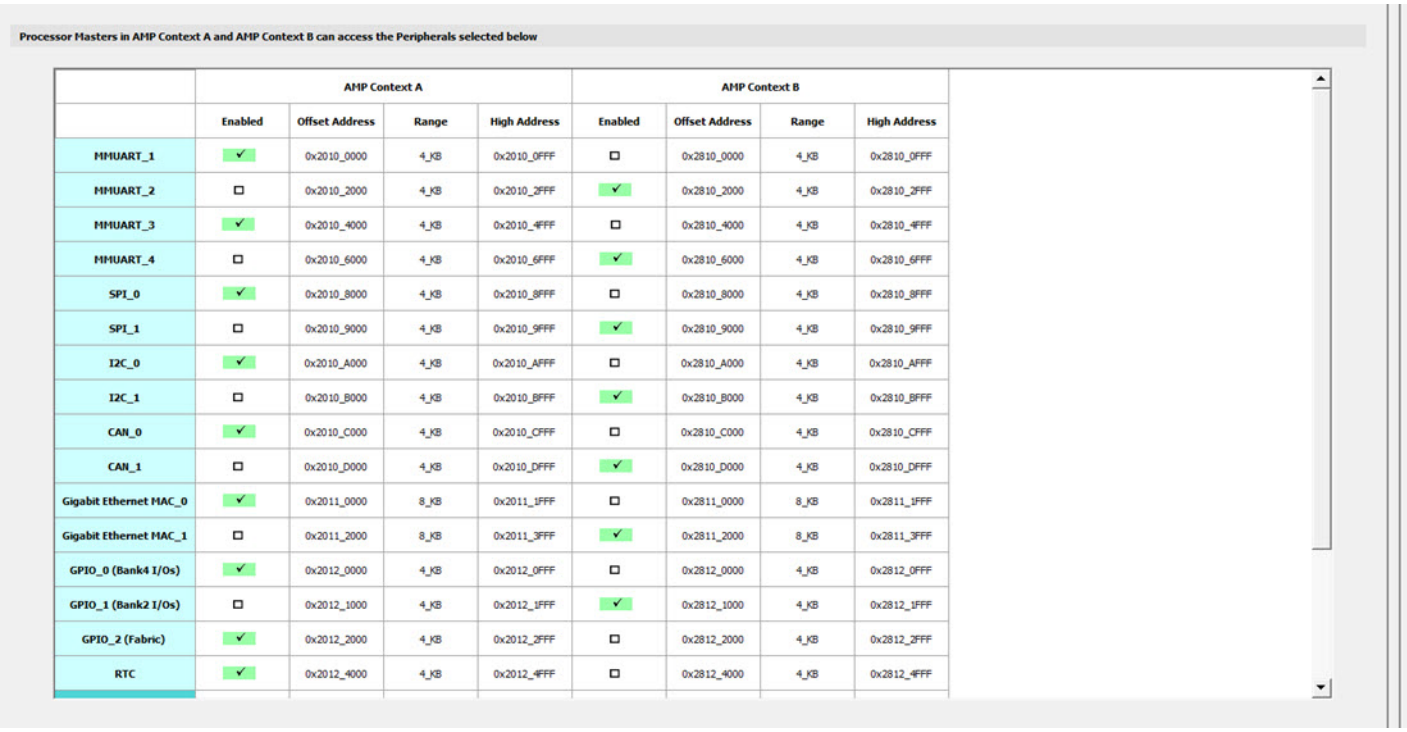
Figure 2-23. Processor Masters



Processor Masters in Context A and Context B can access the Peripherals selected below

The AMP Context A is assigned to AHB0 bus interface and AMP Context B is assigned to AHB1 bus interface. Peripherals can be enabled in either Context A or in Context B. The range and base address for the peripherals are populated in Graphical User Interface and are not editable. The base address will be different for peripherals that are on dual AHB bus interfaces for Context A and Context B.

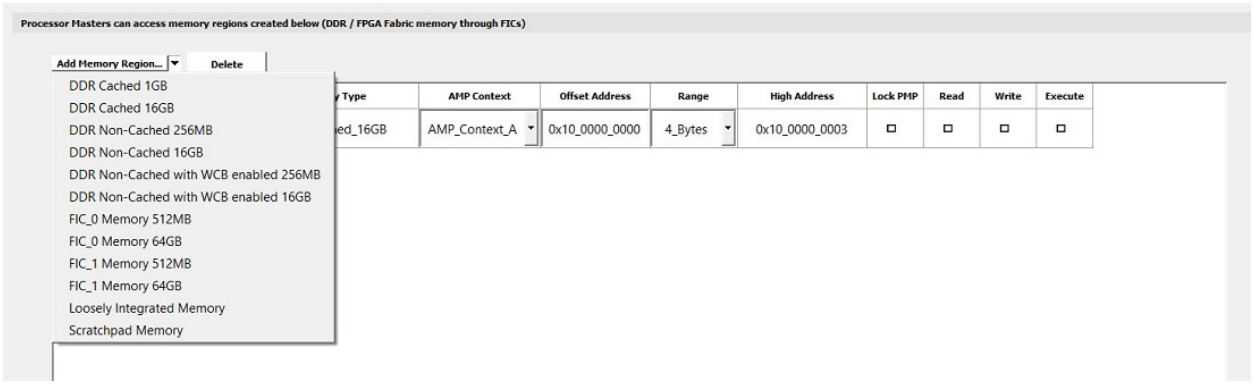
Figure 2-24. Processor Masters in Context A and Context B Accessing the Peripherals



	AMP Context A				AMP Context B			
	Enabled	Offset Address	Range	High Address	Enabled	Offset Address	Range	High Address
MMUART_1	✓	0x2010_0000	4_KB	0x2010_0FFF	☐	0x2810_0000	4_KB	0x2810_0FFF
MMUART_2	☐	0x2010_2000	4_KB	0x2010_2FFF	✓	0x2810_2000	4_KB	0x2810_2FFF
MMUART_3	✓	0x2010_4000	4_KB	0x2010_4FFF	☐	0x2810_4000	4_KB	0x2810_4FFF
MMUART_4	☐	0x2010_6000	4_KB	0x2010_6FFF	✓	0x2810_6000	4_KB	0x2810_6FFF
SPI_0	✓	0x2010_8000	4_KB	0x2010_8FFF	☐	0x2810_8000	4_KB	0x2810_8FFF
SPI_1	☐	0x2010_9000	4_KB	0x2010_9FFF	✓	0x2810_9000	4_KB	0x2810_9FFF
I2C_0	✓	0x2010_A000	4_KB	0x2010_AFFF	☐	0x2810_A000	4_KB	0x2810_AFFF
I2C_1	☐	0x2010_B000	4_KB	0x2010_BFFF	✓	0x2810_B000	4_KB	0x2810_BFFF
CAN_0	✓	0x2010_C000	4_KB	0x2010_CFFF	☐	0x2810_C000	4_KB	0x2810_CFFF
CAN_1	☐	0x2010_D000	4_KB	0x2010_DFFF	✓	0x2810_D000	4_KB	0x2810_DFFF
Gigabit Ethernet MAC_0	✓	0x2011_0000	8_KB	0x2011_1FFF	☐	0x2811_0000	8_KB	0x2811_1FFF
Gigabit Ethernet MAC_1	☐	0x2011_2000	8_KB	0x2011_3FFF	✓	0x2811_2000	8_KB	0x2811_3FFF
GPIO_0 (Bank4 I/Os)	✓	0x2012_0000	4_KB	0x2012_0FFF	☐	0x2812_0000	4_KB	0x2812_0FFF
GPIO_1 (Bank2 I/Os)	☐	0x2012_1000	4_KB	0x2012_1FFF	✓	0x2812_1000	4_KB	0x2812_1FFF
GPIO_2 (Fabric)	✓	0x2012_2000	4_KB	0x2012_2FFF	☐	0x2812_2000	4_KB	0x2812_2FFF
RTC	✓	0x2012_4000	4_KB	0x2012_4FFF	☐	0x2812_4000	4_KB	0x2812_4FFF

Processor Masters can access memory regions created below (DDR/FPGA Fabric memory through FICs)
DDR memory appears at several address ranges depending on whether it is cached, non-cached or access through a Write Combine Buffer (WCB). WCB improves performance (by combining multiple writes to the same address into a single write) for sequential accesses. Each AMP context needs to specify how much DDR memory of each type it needs. Some DDR memories may be shared between AMP Context to pass data. User can create protection for memory region accessed by processors by clicking on the **Add Memory Region...** button. User can delete any memory region by selecting the memory region and clicking **Delete** button. The following figure shows the memory regions available to Processor Masters.

Figure 2-25. Memory Regions Available to Processor Masters



The following table lists different types of memory regions that user can create.

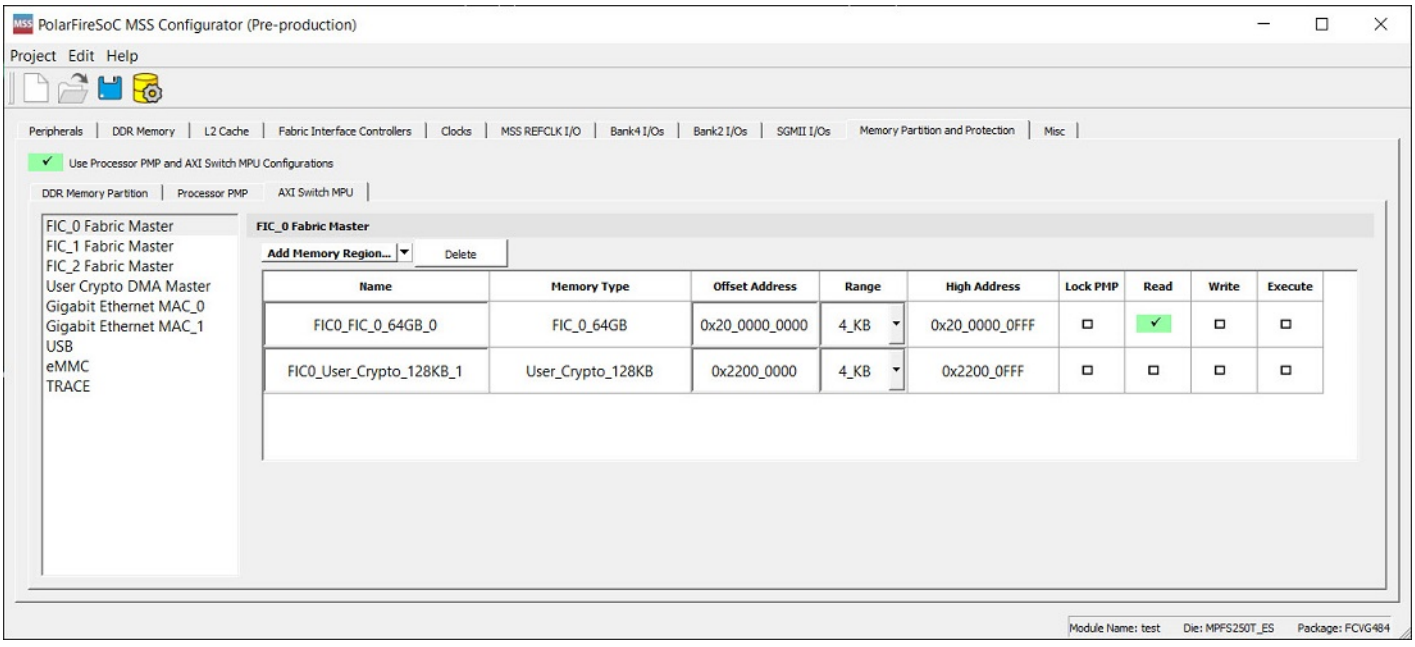
Table 2-8. Available Memory Region

Memory Type	Memory Size	Address Size	Address Range
DDR Cached	512 MB	32-bit	0x80000000 - 0xBFFFFFFF
	16 GB	64-bit	0x10_00000000 - 0x13_FFFFFFFF
DDR Non-Cached	256 MB	32-bit	0xC0000000 - 0xCFFFFFFF
	16 GB	64-bit	0x14_00000000 - 0x17_FFFFFFFF
DDR Non-Cached with WCB enabled	256 MB	32-bit	0xC0000000 - 0xCFFFFFFF
	16 GB	64-bit	0x14_00000000 - 0x17_FFFFFFFF
FIC_0 Memory	512 MB	32-bit	0x60000000 - 0x7FFFFFFF
	64 GB	64-bit	0x20_00000000 - 0x2F_FFFFFFFF
FIC_1 Memory	512 MB	32-bit	0xE0000000 - 0xFFFFFFFF
	64 GB	64-bit	0x30_00000000 - 0x3F_FFFFFFFF
Loosely Integrated Memory	—	—	Start Address is 0x0800_0000
Scratch	—	—	Start Address is 0x0A00_0000

AXI Switch MPU

AXI switch Memory Protection Unit (MPU) provides FPGA (Non-CPU) Masters read/write/execute access to the Memory subsystem and Fabric Memory. Users can create protection for memory regions accessed by FPGA Masters by clicking any one of the FPGA Masters and clicking the **Add Memory Region...** button. User can delete any memory region by selecting the memory region and clicking **Delete** button.

Figure 2-26. AXI Switch MPU Tab



The following table lists the different types of memory regions that user can create.

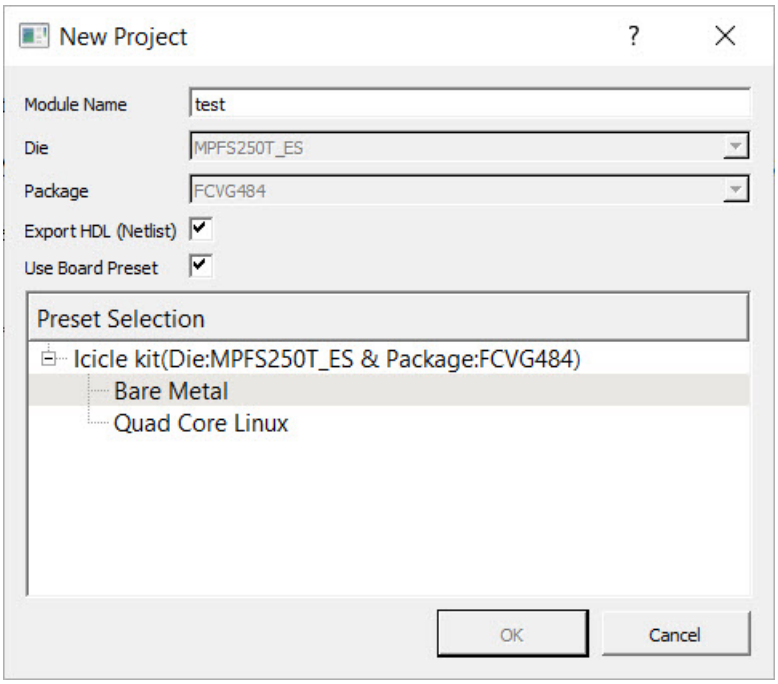
Memory Type	Memory Size	Address Size	Address Range
DDR Non-Cached	256 MB	32-bit	0xC0000000 - 0xCFFFFFFF
	16 GB	64-bit	0x14_00000000 - 0x17_FFFFFFFF
FIC_0 Memory	512 MB	32-bit	0x60000000 - 0x7FFFFFFF
	64 GB	64-bit	0x20_00000000 - 0x2F_FFFFFFFF
FIC_1 Memory	512 MB	32-bit	0xE0000000 - 0xFFFFFFFF
	64 GB	64-bit	0x30_00000000 - 0x3F_FFFFFFFF
FIC_3 Memory	512 MB	32-bit	0x40000000 - 0x5FFFFFFF
User Crypto Memory	128 KB	32-bit	0x22000000 - 0x2201FFFF

3. Creating a Project and Configuring MSS

To create a project and configure MSS:

1. Launch the PolarFire SoC MSS Configurator (`pfsoc_mss`) using one of the following ways:
   – Libero SoC installation directory
   – Standalone MSS installation area
   – Windows Start menu
2. Create a new project using **Project > New**.
3. Enter a module name (for example `PFSOC_MSS_C0`), and then select the appropriate die and package. The module name you enter appears in the following places:
   – File names of the PolarFire SoC MSS Configurator generated outputs at the specified output/generation directory
   – MSS component file (`<module_name>.cxz`)
   – MSS XML configuration file (`<module_name>_mss_cfg.xml`)
   – MSS configuration file corresponding to the current MSS configuration that is generated (`<module_name>.cfg`)
   – MSS configuration report file (`<module_name>_Report.html`)
   – Component/module name of the MSS component (`cxz`) that can be imported to a Libero SoC project

Figure 3-1. MSS - Module Name Dialog Box



Presets for Icicle Kit

When users create a ‘New Project,’ they can import one of the available presets for Icicle kit. These presets will be staged in data folder and will be in ‘CFG’ format. All the parameter/values from the CFG file will be loaded, except for the following three parameters:

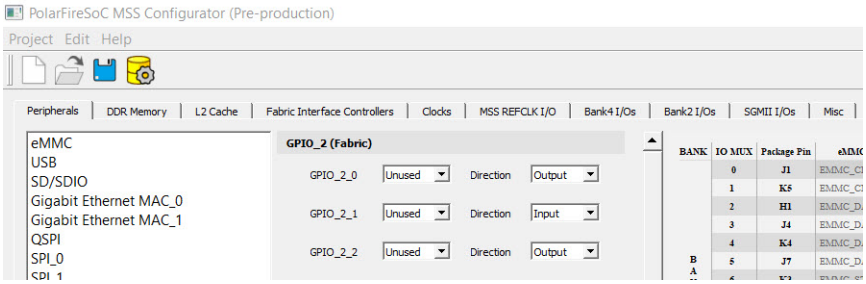
- Module Name
- Die
- Package

User-selected values will be used for Module Name, Die, and Package parameters in the GUI. This is done to facilitate changing Module Name/Die/Package (from the Icicle kit preset) to meet users need.

The list of presets will be shown using a tree widget. By default, 'Default Configuration' preset is selected in GUI and user must explicitly select one of the presets for Icicle kit to load them. Once a preset is selected, users will not be able to edit them using **Edit Settings** option as the preset tree widget will not be shown in 'Edit Settings' dialog.

The following figure shows the MSS configurator tabs.

Figure 3-2. MSS Configurator Tabs



4. Configure **Clocks**, **Fabric Interface Controllers**, **I/O Configuration**, **DDR Memory**, and **Misc settings**.
5. Click the **Save** option to save the MSS configuration to a `.cfg` file.
6. From the Save MSS Configuration dialog box:
   - Browse to a directory and create a folder. For example, create `C:\Microsemi\PFSOC_MSS_Configuration`.
   - Enter a file name (for example `PFSOC_MSS_C0)` and click **Save**.
     Note: The file name you enter is for the standalone MSS project only and is not used as the component name.

The MSS Configuration is created and saved to the file specified and the Log window shows the following message: `INFO: Successfully saved MSS configuration in C:/Microsemi/PFSOC_MSS_Configuration/PFSOC_MSS_C0.cfg file.`

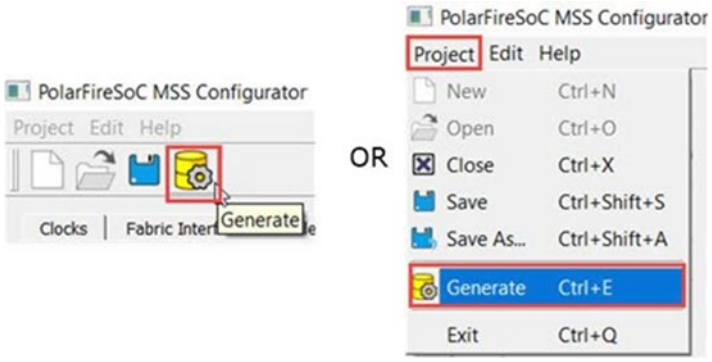
4. Generating, Importing, and Exporting the MSS Component

The following sections describe the steps for generating, importing, and exporting the MSS component.

4.1 Generating the MSS Component and Report

To generate the MSS component, use the **Generate** option (see the following figure).

Figure 4-1. Generate Option



The configuration file (`module_name.xml`) required for the firmware project and the configuration report file (`module_name.html`) are also generated at this time.

The Log window shows the following messages indicating the generated files:

```
INFO: Successfully generated MSS configuration report to 'C:/Microsemi/
PFSOC_MSS_Configuration\PFSOC_MSS_C0_Report.html'
```

```
INFO: Successfully generated MSS component file to 'C:/Microsemi/PFSOC_MSS_Configuration/
PFSOC_MSS_C0.cxz'
```

The report file `module_name.html` consists of following sections:

- Design Information – This section consists of design parameters like device family name, die, package, configurator version, and the date the report was generated.
- FPGA Fabric – This section mentions whether FPGA Fabric programming is required or not.
- Fabric Interface Controllers – Consists information about status of the interface controllers.
- Peripherals – Contains information about which peripherals are being used or unused.
- DDR Memory – Shows the memory type.
- List of Ports – Depicts information about all the ports with direction.
- I/O REFCLK Port Settings – Shows all the information about Reference clock ports.
- MSSIO Port Settings – Shows all the information about MSSIO ports.
- DDRIO Port Settings – Shows all the information about DDRIO ports.
- SGMII I/O Port Settings – Shows all the information about SGMII ports.

Figure 4-2. Configuration Report for PolarFire SoC MSS Configurator (Pre-production)

Design Information

Design Parameter Name	Design Parameter Value
Family	PolarFireSoC
Die	MPFS460TS
Package	FCG1152_Eval
Version	2.0
Date	Wed Oct 28 15:39:08 2020

FPGA Fabric

FPGA Fabric Programming	Required

Fabric Interface Controllers

Interface Controller Name	Enabled
FIC_0 AXI4 Master Interface	false
FIC_0 AXI4 Slave Interface	false
FIC_1 AXI4 Master Interface	false
FIC_1 AXI4 Slave Interface	false
FIC_2 AXI4 Slave Interface	false
FIC_3 APB Master Interface	false

Peripherals

Peripheral Name	Enabled
eMMC	UNUSED
USB	UNUSED
SD/SDIO	UNUSED
Gigabit Ethernet MAC_0	SGMII_IO_B5
Gigabit Ethernet MAC_1	GMII_MII_FABRIC
QSPI	UNUSED
SPI_0	UNUSED
SPI_1	UNUSED
SD/SDIO	UNUSED
MMUART_0	MSSIO_B2_A
MMUART_1	UNUSED
MMUART_2	UNUSED
MMUART_3	UNUSED
MMUART_4	UNUSED
I2C_0	UNUSED
I2C_1	UNUSED
CAN_0	MSSIO_B2_A
CAN_1	UNUSED

DDR Memory

DDR	Protocol
Memory Type	DDR4

List of Ports

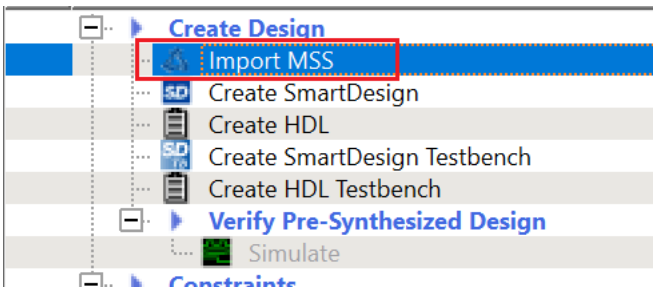
Port Name	Direction
MSS_RESET_N_F2M	INPUT

4.2 Importing the MSS CXZ File to Libero SoC

To import the `PFSOC_MSS_C0.cxz` file:

1. Use the **Import MSS** option shown in the following figure.

Figure 4-3. Import MSS to Libero



2. From Design Hierarchy, drag the MSS component to SmartDesign canvas.
3. Build the hierarchy.

Note: Any changes required in the MSS configuration must be performed in the PolarFire SoC MSS Configurator, and the updated `MSS CXZ` file must be re-imported and used in Libero SmartDesign.

4.3 Importing the MSS XML File to SoftConsole

Copy the XML file from:

```
<$Directory>:/Microsemi/PFSOC_MSS_Configuration/PFSOC_MSS_C0_mss_cfg.xml
```

to:

```
<$Installation
Directory>:\Microchip\<$SoftConsole_Workspace>\Project_Name\src\platform\config\xml
```

Note: This step can also be performed using the **Import** option from SoftConsole.

4.4 Exporting the FPGA Design Hardware Platform Information

When using PolarFire SoC, the overall application runs an embedded software application on the RISC-V cores that may use the FPGA fabric to expand the number of I/O peripherals, accelerate software functions using FPGA logic, or control FPGA fabric functions. In these cases, the processor communicates with the FPGA fabric via the MSS Fabric Interface Controllers (FIC) and interrupt ports. The embedded software application must contain the following information to establish this communication properly:

- Fabric blocks like LSRAM, DMA Controller, and PCIe are connected to the AXI interconnect IP on the Fabric side. MSS communicates with these fabric blocks via Fabric Interface Controllers, which connects to the AXI Interconnect IP. The memory addresses of these fabric blocks are specified in the AXI Interconnect IP Configurator. These memory addresses must be specified in the software application.
- In the Libero SoC design, the user must drive the required MSS interrupt ports and other interrupts can be grounded. The corresponding Interrupt Request (IRQ) handler routines must be invoked in the software application for interrupt handling.

Libero SoC v12.5 does not export the FPGA fabric peripheral memory map, interrupt mapping, or peripheral clock frequencies. Therefore, add this information manually in your embedded software projects. For example, if fabric blocks such as LSRAM and DMA Controller are used in the design and interfaced with the MSS through a FIC, then the memory addresses of these fabric blocks must be specified in the user application code for accessing them from MSS.

5. Simulating an FPGA Design Interacting with MSS

The MSS simulation model has been designed to verify that the connectivity to the MSS has been properly established with the FPGA fabric logic.

The MSS simulation model can be used to verify:

- The Fabric—MSS connectivity using the Fabric Interface Controllers (FICs).
- The Fabric—MSS interrupt (M2F and F2M) interface.

For information about how to set up and run the simulation for the PolarFire SoC MSS, see UG0926 User Guide PolarFire SoC FPGA MSS Simulation.

6. Programming the Application Bitstream

To program the application bitstream:

1. Use Libero SoC or FlashProExpress to program the FPGA fabric array, sNVM, eNVM and any security settings.
2. Use Libero SoC to program any eNVM client.

Note: SoftConsole must be used to program the Boot mode.

Alternatively, you can also perform the following steps:

1. Use SoftConsole to program the eNVM with the First Stage Boot image.
    1.1. Select the project you want programmed to eNVM in SoftConsole's **Project Explorer** pane.
    1.2. Click the **PolarFire SoC Boot Mode 1** external tool.

Programming progress messages appear in the Console.

For more information, see PolarFire SoC Software Development and Tool Flow User Guide.

7. Sample Project

For PolarFire SoC Icicle Kit reference design and supporting files, see PolarFire SoC Icicle Kit Reference Design GitHub repository.

8. Revision History

Revision	Date	Description
C	04/2021	The following list of changes are made in this revision. • Peripherals: Added note related to the availability of SD pins. • Crypto: Updated the section with Streaming Interface Option details. • Memory Partition and Protection: Added this section.
B	12/2020	Revision B is released in December 2020. Following is a list of changes made in this revision: • Updated the Using the PolarFire SoC MSS Configurator GUI section. • Updated the Creating a Project and Configuring MSS section. • Updated the Generating the MSS Component and Report section. • Updated the Clocks section. • Added a note in the SGMII section.
A	9/2020	Initial Revision

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