Libero® SoC v2021.1

SmartDesign User Guide

Introduction

SmartDesign is a visual block-based design creation and entry tool for the instantiation, configuration, and connection of Microchip IPs, user-generated IPs, and custom and glue-logic HDL modules. This tool provides a canvas, which is analogous to a breadboard, for stitching together the various design components. The final result from SmartDesign is a design-rule-checked and automatically abstracted synthesis-ready HDL file. A generated SmartDesign can be the entire FPGA design or a component subsystem to be reused in a larger design.

The following design objects can be instantiated in the SmartDesign Canvas:

- Microchip IP Cores
- User-generated or third-party IP Cores
- HDL design files
- HDL + design files
- Basic macros
- Other SmartDesign components (`*.cxf` files) generated from SmartDesign in the current Libero® SoC project or imported from other Libero SoC projects
- Reusable design blocks (`*.cxz` files) published from Libero SoC

SmartDesign supports SmartFusion®2, IGLOO®2, RTG4™, PolarFire® and PolarFire® SoC devices.

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1. About SmartDesign

This section provides an overview of SmartDesign.

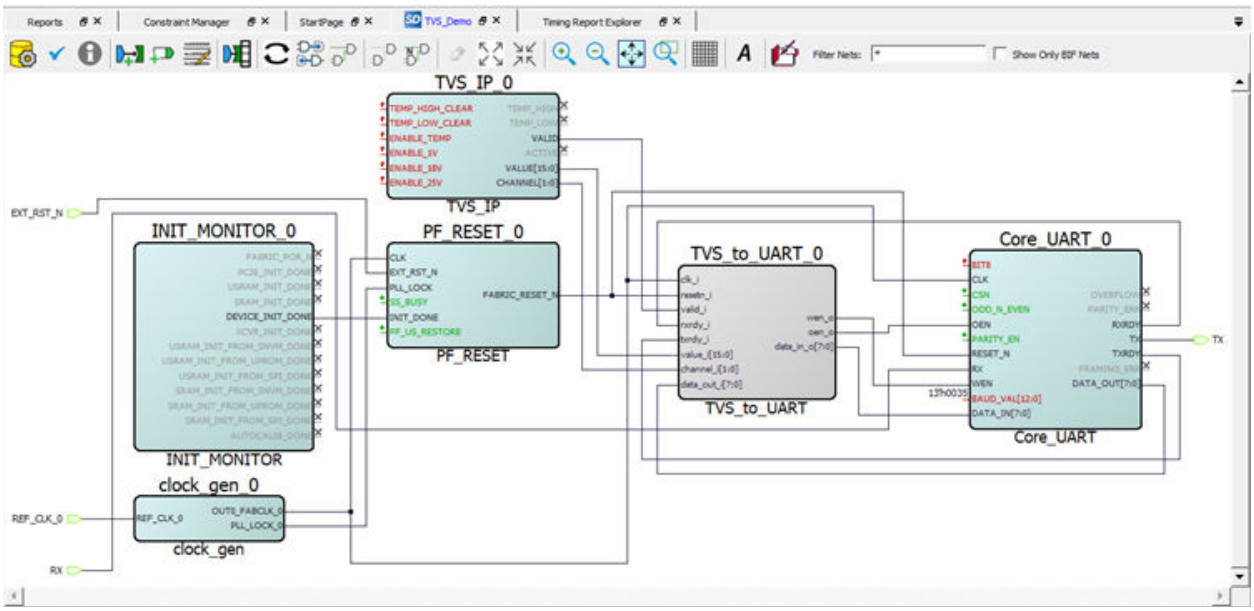
1.1 Canvas Layout

The SmartDesign canvas places all components in columns, with the nets vertically routed in the space between columns. Top-level input ports are placed in the leftmost column. Top-level output ports and inout ports are placed in the rightmost column.

Components can be moved up and down the columns. When components are instantiated in SmartDesign, they are placed in an existing column or a new column created for them. When components are moved up and down, the column boundaries are shown. When components are moved horizontally, the instance can be moved to a different column, the column it is in can be moved, or a new column can be created at the new location for the instance.

The following figure shows the SmartDesign canvas.

Figure 1-1. SmartDesign Canvas



1.2 SmartDesign in the Libero SoC Design Flow

SmartDesign allows you to stitch together HDL, IPs, re-usable design blocks, lower level SmartDesign blocks, and other design blocks of different types, and generate a top-level design. The **Files** tab lists your SmartDesign files in alphabetical order.

To build your design, perform the following procedure:

1. **Instantiating components:** This step is analogous to inserting design components onto the breadboard. In this step you add one or more building blocks, HDL modules, components, and schematic modules from the Project Manager to your design. The components can be design blocks, IP cores from the Catalog, basic macros, design blocks (*.cxz), and other SmartDesign components (.cxf) file imported into the Libero SoC project.
2. **Connecting bus interfaces:** In this step, you can add connectivity via standard bus interfaces to your design. This step is optional and can be skipped if you prefer manual connections. Components generated from the Catalog may include predefined interfaces that allow for automatic connectivity and design rule checking when used in a design.

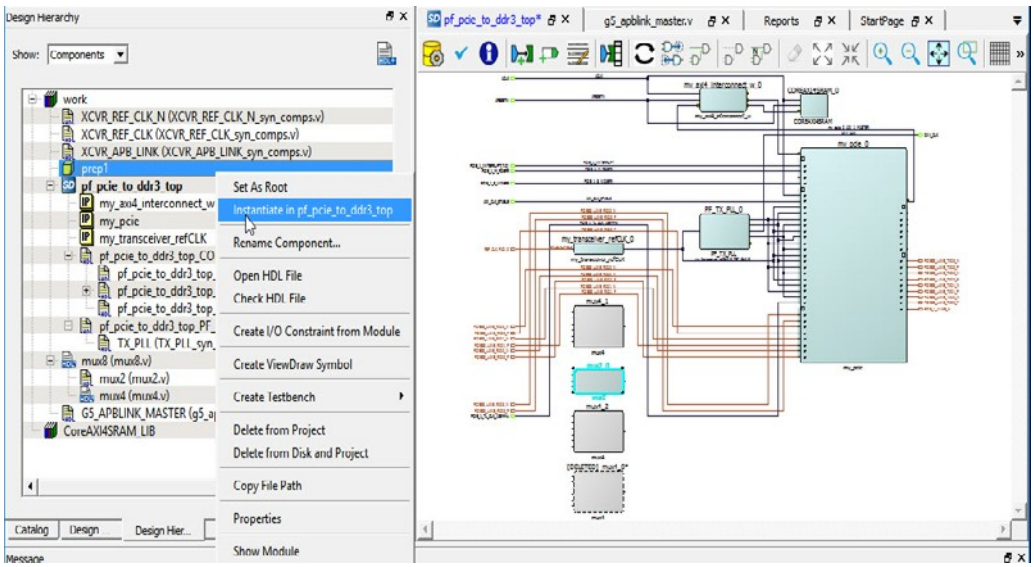
3. **Connecting instances:** The Canvas allows you to create manual connections between ports of the instances in your design. Unused ports can be tied off to GND or VCC (disabled); input buses can be tied to a constant, and you can leave an output open by marking it as unused.
4. **Generating the SmartDesign component:** In this step, you generate a top-level (Top) component and its corresponding HDL file. This component can be used by downstream processes, such as synthesis and simulation, or you can add your SmartDesign HDL into another SmartDesign. When you generate your SmartDesign, the tool invokes the Design Rules Checker to verify the connectivity of your design. Undriven and floating ports, along with other Design Rule Check (DRC) violations, are reported in the Log/Message window. Any error messages must be addressed before a component can be generated successfully. The design flow cannot proceed if component generation fails.

1.3 Instantiating Components into SmartDesign Canvas

For all the following design objects, drag-and-drop or right-click **object > Instantiate** to instantiate the design objects:

- IP cores—To instantiate IP cores, drag the IP core from the Catalog into the SmartDesign Canvas. Configure the IP cores in the IP Core Configurator before it can be dropped in the SmartDesign Canvas. IP cores displayed in the Catalog as italics are cores that are available in Microchip IP Core Repositories, but are not yet downloaded to the vault (the disk location where downloaded cores are stored). Download the IP core prior to configuration and instantiation.
- HDL files—To instantiate HDL design blocks, drag the HDL design file from the Design Hierarchy into the SmartDesign Canvas.
- HDL+ cores—HDL+ cores are HDL files where the parameters and generics are used and a core has been generated out of it (right-click **HDL file > Create Core from HDL**). Drag and drop the HDL+ module into the SmartDesign canvas. The HDL core becomes configurable inside the SmartDesign canvas. Open the configurator to set the values for the parameters and generics. An interface bus may also be added to the HDL+ core, and it will show up in the SmartDesign with a bus interface pin that can be used to easily connect to the appropriate bus IP Core inside SmartDesign Canvas.
- Re-usable Design Blocks (*.cxz) file—Drag and drop the design blocks (*.cxz) from the Design Hierarchy into the SmartDesign canvas. Design blocks are components that may have completed layout in a different Libero SoC project and exported/published, to be ready for re-use in a higher level design as a component. The design blocks must be imported into the current Libero SoC project to be instantiated in SmartDesign. The following figure shows how to instantiate a design block.

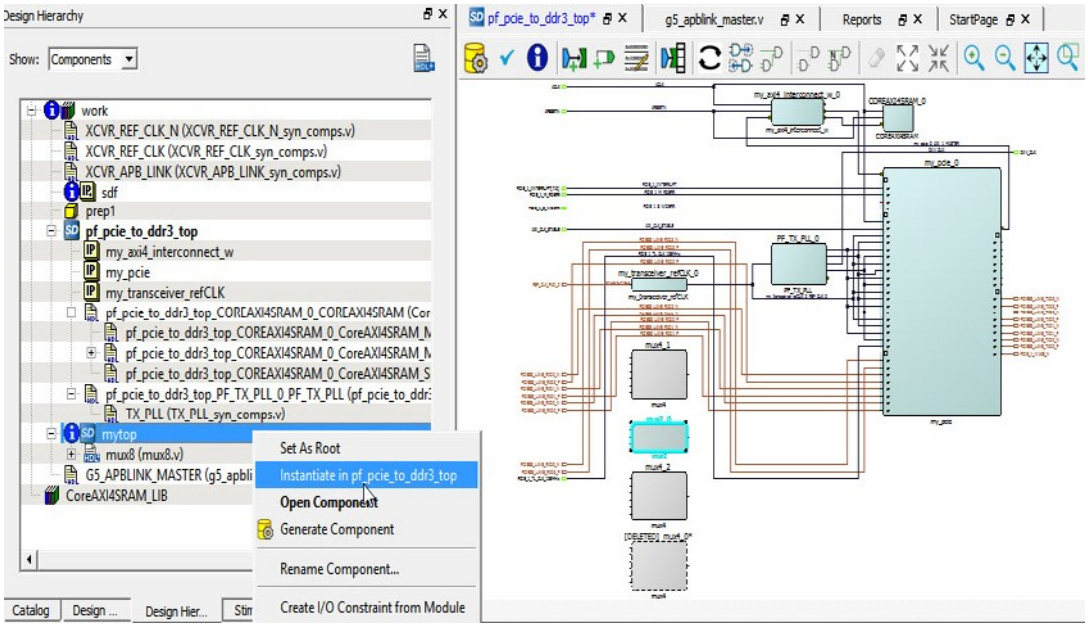
Figure 1-2. Design Block (*.cxz) Instantiation



- SmartDesign Components—Another SmartDesign component (*.cxf) can be instantiated in the SmartDesign. Drag and drop the Smart Design component (*.cxf) from the Design Hierarchy into the SmartDesign canvas. Instantiation can also be done by right-clicking the (top) module name in the Design Hierarchy and choosing

Instantiate. The component (*.cxf) and its corresponding HDL files and IP cores must be imported into the current project and configured before instantiating in the new SmartDesign project.

Figure 1-3. SmartDesign Component (*.cxf) Instantiation

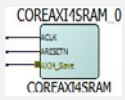
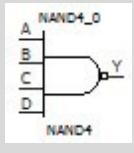
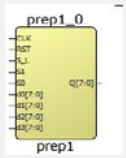


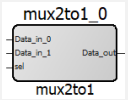
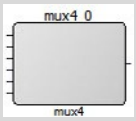
1.4 SmartDesign Canvas and Component Display

The SmartDesign Canvas window can be docked/undocked by clicking the icon. The canvas displays different component types with different colors. When the mouse is hovered over the component, a tooltip displays the type and name of the component. For IP Cores, the core version is also displayed.

The following table lists the component types and their appearance in the SmartDesign canvas.

Table 1-1. Component Type and Name in Canvas

Graphic Display	Component Type	Tooltip Information
	IP Cores from Catalog	Core: COREAXI4SRAM 2.1.105
	Basic Macros/Macro Library from Catalog	Macro: NAND4
	Re-usable Design Blocks (*.cxz file) imported into Libero SoC project	Block: prep1
	SmartDesign Components (*.cxf file) imported into Libero SoC project	SmartDesign: adder_shift32

.....continued		
Graphic Display	**Component Type**	**Tooltip Information**
	Design HDL file imported into Libero SoC project	HDL: mux2
	Core generated from HDL	HDL+: mux4

1.5 SmartDesign Tcl Commands

For details about the Tcl commands supported by SmartDesign, refer to the SmartFusion2, IGLOO2, RTG4 Tcl Commands Reference Guide or the PolarFire FPGA Tcl Commands Reference Guide.

2. SmartDesign Icons, Hotkeys, and Menu Items

This section describes the SmartDesign icons, hotkeys, and menu items.

2.1 SmartDesign Icons

Across the top of the SmartDesign canvas is a list of icons. Use the icons to:

- Make connections
- Control the canvas display
- Invoke Design Rule Check
- Generate the HDL for the component
- Adding Text
- Save the SmartDesign to PDF

The following table lists the SmartDesign icons. Tooltips are provided for each icon. Hover the mouse over the icon to display the tool-tips.

Table 2-1. SmartDesign Icons

Icon	Action/Tooltip	Description
	Generate Component	Generates the design. Converts the visual design you create into an HDL file for use in the project if there are no errors in the design. This action implicitly and automatically invokes the Design Rule check. DRC Error messages are generated in the Log/Message window. A DRC report is also generated (Design > Reports > <top_level_smart_design_name>_DRC.xml).Clicking this button affects the design state.
	Design Rule Check	Invokes the Design Rule Checker (DRC). If the design is not valid (DRC violations), then errors appear in the Log/Message window. A DRC report is also generated (Design > Reports > <top_level_smart_design_name>_DRC.xml). No HDL file is generated even if the DRC check passes. Clicking this button does not affect the design state. To generate the HDL for the component, click the **Generate Component** button.
	Toggle Highlighting Instances with Status Message	Click this icon to highlight any instances on the canvas that have status information for the instance (for example, “A new version is available”). Hovering the mouse over an instance opens a tooltip to display the info/message (for example, “A new version is available”). Click this icon if you have made any changes to a component, reconfigured a core or have downloaded newer versions of the core used in the design.
	Add Port	Add a new top-level port to the design. A pop-up window appears for you to enter the name of the port and the directions (Input/Output/Inout). Input Ports are added in the leftmost column of the canvas. Output and Inout ports are added in the rightmost column. After the port is added, hover the mouse over the input port to display the port name, direction and fanout. Hover the mouse over the output port to display the port name, direction and drivers of output port. Bus ports can also be added. For example: myInputBus[7:0] Alternatively, right-click on empty space inside the canvas and choose **Add Port**. A port is added in the canvas and is anchored at the Y coordinates of cursor. See the figure below.

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Icon	Action/Tooltip	Description
	View Memory Map	Click this icon to open the **View Memory Map** dialog which shows the memory map corresponding to various masters in the SmartDesign component in a hierarchical tree format. This dialog box shows the memory map starting from a master in the design to peripherals connected through bus and bridge cores hierarchically. Each peripheral in the memory map is shown with a Start Address, Range and DRC.
	QuickConnect	Opens a dialog that helps you make connections more quickly. This dialog lists the pins in the design, and allows you to select multiple pins and make a connection directly.
	Reset Layout	Click to reset the layout view. Clicking this button removes all presentation information (position, size, highlights, modified pin orders).
	Auto-arrange Layout	Click to redo the layout of where components are placed on the screen. Only the location (x-y coordinates) of the instances and ports are changed. All presentation information remains intact.
	Compress Layout	Click to push the instances and ports towards each other in order to remove extra white space between them on the screen. The relative positions of the instances on the screen are preserved. The result is a more compact display of the design.
	Hide Nets	Toggle button. Click to hide nets and make them invisible on the canvas. All nets on the canvas are hidden. This button has precedence over net filtering and over-rides all net filters. To hide some but not all nets, do not use this button. Use the **Filter Net** widget at the rightmost of the toolbar. Hiding nets also hides the net names (if present). When a net is hidden, the net stubs that the hidden net is connected to are still visible. Selecting the net stubs shows the RATS net connection of the net.
	Show Nets	Toggle button. Click to show/hide nets. All nets on the canvas are shown/hidden. If nets are shown, all nets matching the net filter (at the far right of toolbar) are shown.
	Show/Hide Net Names	Toggle button. Click to show net name displayed alongside the net. Hiding net names makes the canvas less cluttered for big designs. Net names are always displayed in a tooltip when the mouse is hovered above the net.
	Unhighlighted All	Remove all highlighting of all design objects (nets, pins, ports, instances) on the canvas. This option is highlighted only if design objects are already highlighted.
	Expand All Instances	Expand (display the hierarchy to the lowest level) in place of all instances in the canvas.
	Fold All Instances	Collapse the hierarchy of all expanded instances into the top-level hierarchy.

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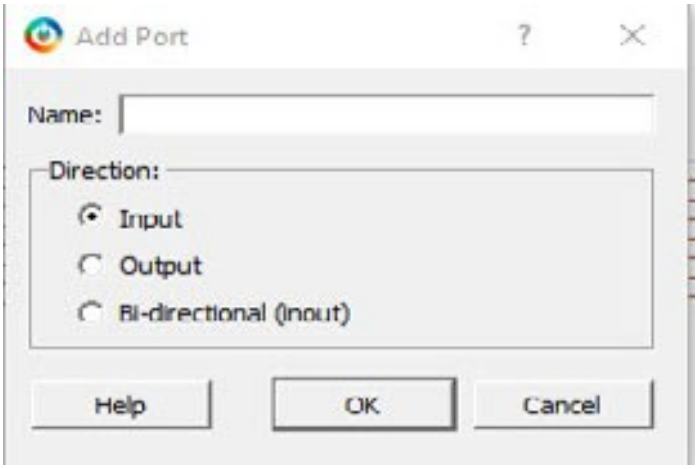
Icon	Action/Tooltip	Description
	Zoom In	Zoom in on the canvas.
	Zoom Out	Zoom out off the canvas.
	Zoom to Fit	Adjust the zoom so that everything on the canvas just fits inside of the visible viewport with no extra empty space around the design.
	Zoom to Selection	Click this icon and drag the mouse to draw a rectangle which when released causes a zoom in so that the visible viewport area is approximately the size of the drawn rectangle.
	Show Grid	Click to show a background grid behind the items on the canvas. If the grid does not appear when the button is clicked, zoom in until the grid shows. The grid pattern may not show if the canvas is zoomed too far out.
	Add Note	Click to enter the Add Note mode. The next mouse click on the canvas opens a dialog box for entering the text and font size for the text (anchored at the mouse click location).
	Save to PDF	Click this icon to bring display a dialog that allows you to save a picture of all/part of the design to a PDF document.

Figure 2-1. Add Port Dialog Box



2.2 SmartDesign Hotkeys

The following table lists the Hotkeys available in the SmartDesign canvas.

Table 2-2. SmartDesign Hotkeys

Hotkey	Description
CTRL + w	Maximize the canvas work area.
CTRL + f	Open the Find dialog box.

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Hotkey	Description
CTRL + +/CTRL + = scroll wheel up	Zoom in (same as clicking the Zoom In button in toolbar or pressing CTRL+ mouse)
CTRL + -	Zoom out (same as clicking the Zoom Out button in toolbar or pressing CTRL + mouse scroll wheel down)
CTRL + c	Clear the clipboard. If a single instance is selected before the Hotkey, it is added to the clipboard. The display name of the design object is also copied.
CTRL + v	If the copy information of a single instance is in the clipboard then call clone instance on it. For details, see Help.
CTRL + z	Undoes the last operation.
CTRL + y	Redoes the last operation.
SHIFT + click	Click one item and SHIFT + click another item. The first clicked item, the second clicked item and all items of the same type between the first and second clicks are selected. This command is helpful when multiple items needed to be selected for the same command (promotion to top-level/Add to group).
CTRL + click	Control + click is a toggle switch that selects or de-selects an item under the mouse cursor.
CTRL+SHIFT+click and then drag	Selects a pin of an instance and drag the mouse to a new location to move the pin of the instance. This is not available for macros and expanded in place instances.

2.3 Click-and-Drag Operations

The following table lists the mouse click-and-drag operations available in the SmartDesign canvas.

Table 2-3. Mouse Click-and-Drag Actions

Mouse Actions	Description
Left-click and drag towards the top-left corner, and then release.	Zoom in. The distance of the mouse travel determines the magnitude of the zoom-in and is indicated by a positive integer in red. See the figure below.
Left-click and drag towards the top-right corner, and then release.	Zoom out. The distance of the mouse travel determines the magnitude of the zoom- out and is indicated by a negative integer in red. See the figure below.
Left-click and drag towards bottom left, and then release	Zoom to fit. Change the display to fit the canvas view area snugly.
Left-click and drag toward bottom right, and then release	Draw a rectangle on the canvas. Instances, pins and ports must be fully contained inside the rectangle to be selected. Nets partially inside the rectangle are selected.

Figure 2-2. Example of Zoom In

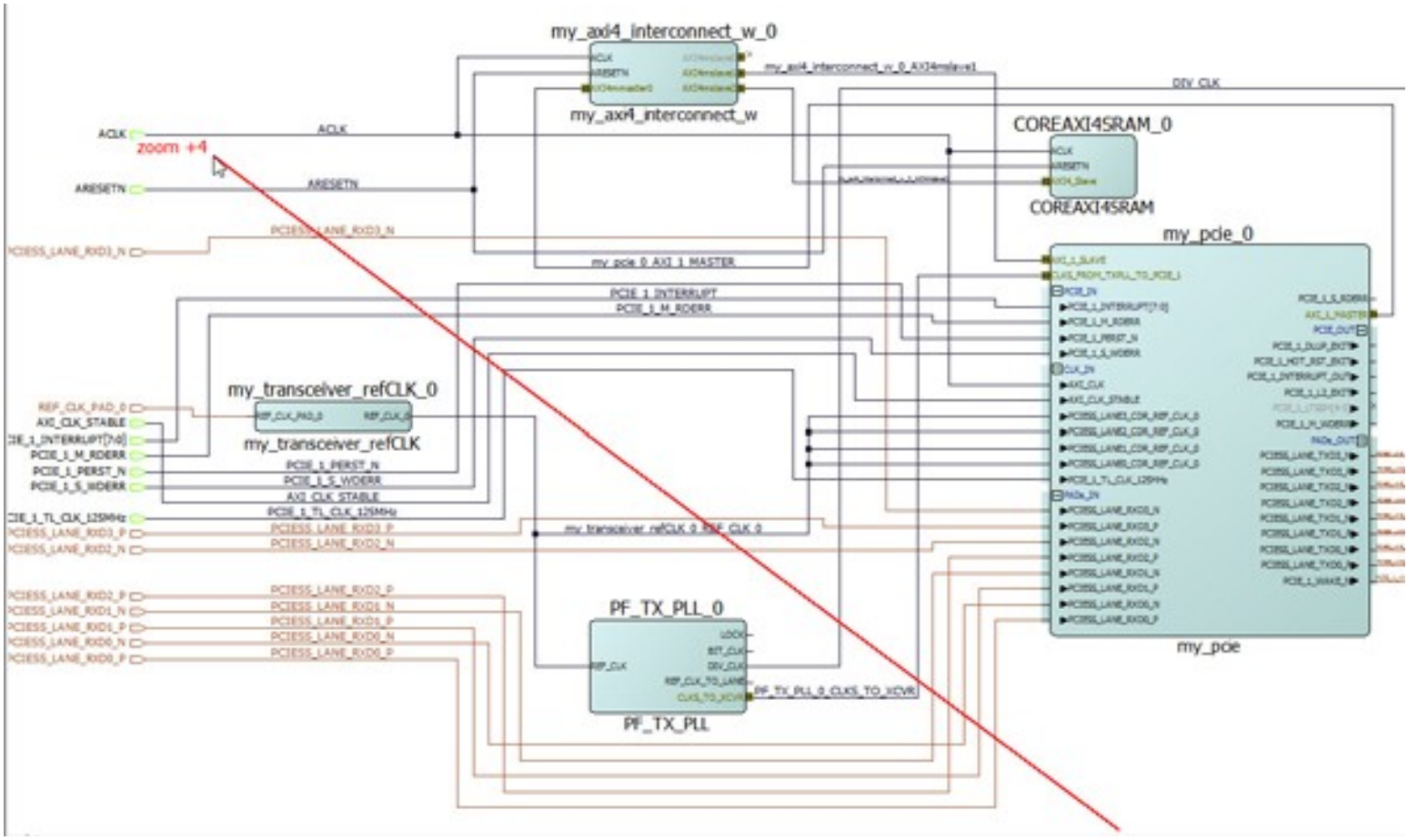
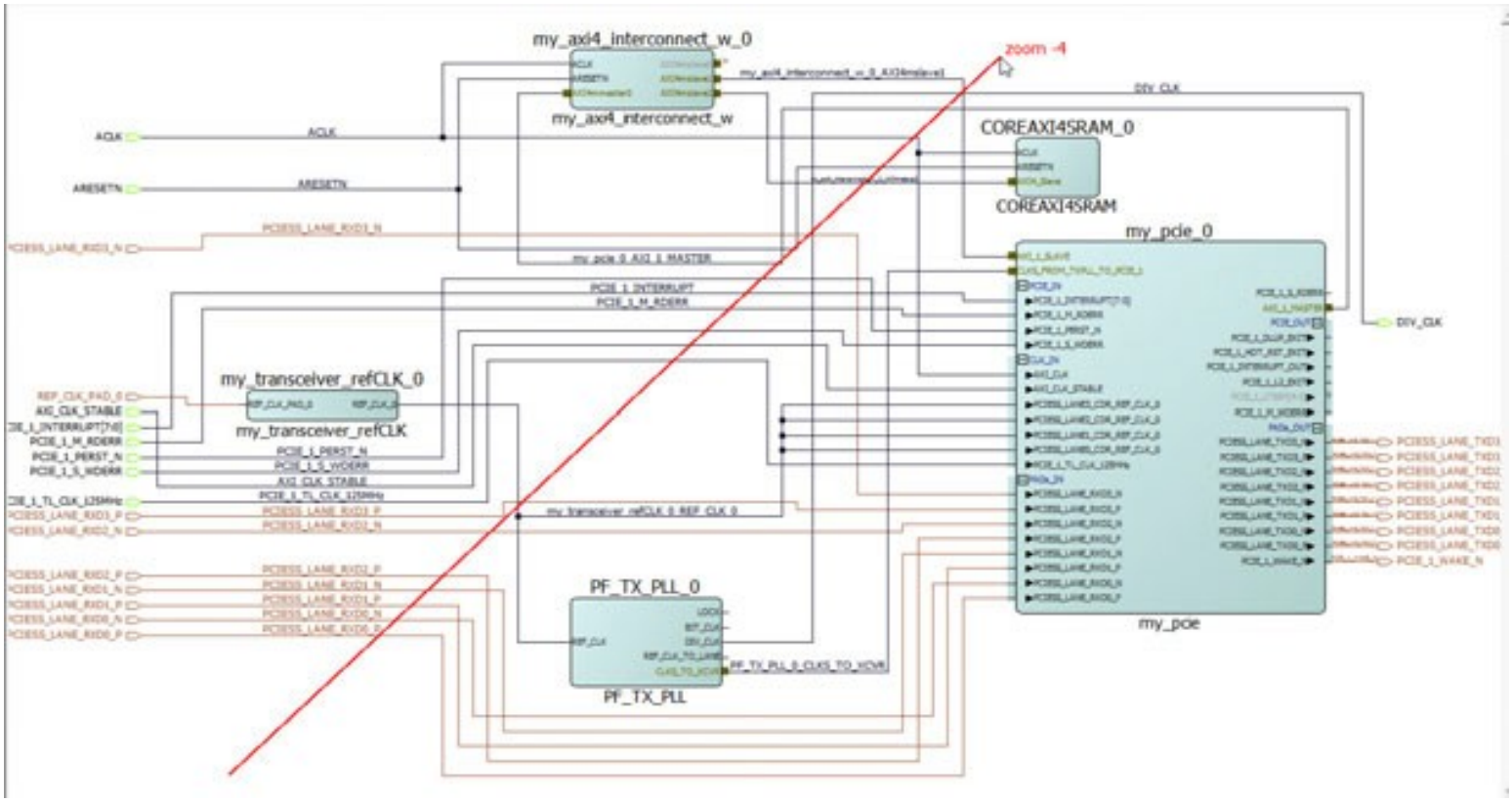


Figure 2-3. Example of Zoom Out



3. SmartDesign User Actions

The SmartDesign tool has a rich set of menu items, accessible from the right-click menu of a selected design object, for you to:

- Make connections between design objects
- Rename design objects
- Highlight design objects
- Traverse up/down the hierarchy of instances
- Assign attributes of pins/nets/buses.

The list of available user actions varies with the design object. Some actions are common to all objects, while other actions are unique to a design object (net/instances/pins/ports).

3.1 Net Actions

When a net or multiple nets are selected, the following actions are available in the right-click menu item.

3.1.1 Connect

This action combines with all selected pins/ports to form a connection. Selecting a net is functionally equivalent to selecting all pins and ports to which this net is connected. This action can also be used to connect a net to another net if one of the net is not driven.

3.1.2 Go to Driver

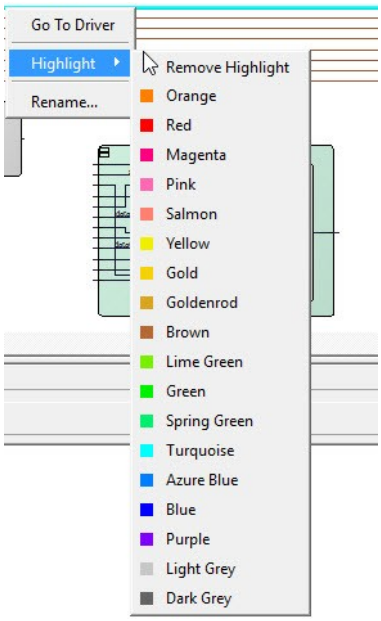
When a net is selected, the Go to Driver action centers the view on the net's driver pin/port, zooms away, and then selects the net driver. The driver must be an input port/output pin. It cannot be an inout pin/port. This action is not available when multiple nets are selected or the selected net has no driver. Go to Driver traces the net to the driver at the local level of hierarchy. It does not traverse hierarchy.

3.1.3 Highlight

Right-clicking a design object (nets/pins/ports/bus interface/instance) menu opens a menu of colors for highlighting. Clicking a color selects that color to highlight the selected design objects. If any design objects are already highlighted then highlighting a different color will overwrite the previous highlight color. The highlight action is available when a single or multiple design objects are selected.

Note: Highlighting a net highlights the net and all the pins/ports (through the hierarchy) connected to the net.

Figure 3-1. Highlight Colors



To remove the highlight on a single design object, right click the design object and select **Remove Highlight**.

To remove all highlighted design objects, click the **Unhighlighted All** icon in the toolbar.

3.1.4 Rename

The rename action opens a dialog for a new net name to be entered to replace the old name. Clicking OK changes the net name to the new net name if it is valid (e.g., not already used). Clicking OK prints an error in the Log window and the dialog does not close if the name already exists or is invalid.

3.1.5 Delete

Deletes the net. Net names, if shown, are also deleted.

3.2 Instance Actions

When one or more instances are selected, the following actions are available in the right-click menu.

3.2.1 Configure

If the instance is a SmartDesign component, the Configure action opens the SmartDesign canvas for edits. If the selected instance is an IP Core, the **Configure** button opens the Configurator dialog for the core to be configured. If the selected instance is an HDL, the configure action opens the HDL file in the text editor. This action is equivalent to double-clicking the instance. This action is available only when one single instances is selected.

This action is also available in the right-click menu of low-level instances in the Expanded Inplace view.

3.2.2 Modify HDL

This action opens the instance's HDL source file in the text editor. Available only when an instance of an HDL+ component is selected.

Note: If the component is an HDL file, this option is not available. To open an HDL file, double-click the HDL component on the SmartDesign canvas or right-click the HDL component and choose **Configure**.

3.2.3 Highlight

This action opens a menu with multiple highlight color selections. Clicking that color selects that color to highlight the selected items. If any items are already highlighted then highlighting a different color will overwrite the previous highlight color. The action is available when a single or multiple nets are selected.

Highlighting an instance automatically highlights the non-highlighted pins of the instance as well. Clicking the **Unhighlight all** icon  in the toolbar removes the highlight color of all highlighted design objects, including highlighted nets.

This action is also available in the right-click menu of low-level instances in the Expanded Inplace view.

3.2.4 Rename

This action opens the rename dialog for a new instance name to be entered. If the instance name is valid, clicking **OK** changes the instance to this name, and then closes the dialog.

If the instance name is not valid or already exists, clicking **OK** prints an error in the Log window, displays a warning message, and will not close.

3.2.5 Copy and Paste

Copy and Paste are used to copy instance to the clipboard and paste the copied instance on the canvas.

The copy action is also available in the right-click menu of low-level instances in the Expanded Inplace view.

Copying an IP Core on the canvas copies into the clipboard the following:

- The configuration of the core
- Pin attributes (Tie high/low/Mark Unused/Inverted)
- Name of the instance
- The input pin connections are available only if pasted inside the same SmartDesign component
- Presentation Information (e.g., Highlighting, size, pin order) is available only if pasted inside the same SmartDesign component.

Note: If a change is made to the instance after the copy, but before the paste command, the paste command uses the most current version of the instance, not the version at the time of copy. Copying from another Libero SoC project is not supported.

3.2.6 Delete

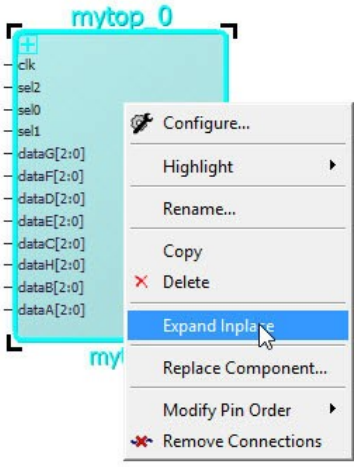
This action deletes the selected item. When multiple items are selected, all are deleted.

Note: Not all design objects can be deleted. Pad ports cannot be deleted.

3.2.7 Expand Inplace and Fold Instance

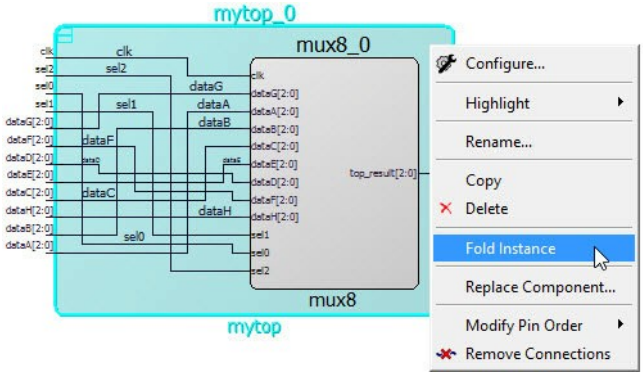
The Expand Inplace action is equivalent to clicking the **+** (Expand) sign in the top-left corner of the instance. It causes the selected instance to expand (to expose all levels of hierarchy) in place if not expanded. It is available to all instances at all levels of hierarchy except the lowest level. If only one instance is selected, the viewport will zoom to the instance after the expand or fold is completed. This action is for SmartDesign components and is read-only. No changes can be made to the expanded hierarchy. Changes to the components at the lower level of hierarchy must be made by opening the low-level component directly. For more information, see Expand and Fold Instance.

Figure 3-2. Expand Inplace



The Fold Instance action is a toggle switch. It is equivalent to clicking the **-** (Fold) sign of an expanded instance. It causes the expanded hierarchy of the instance to collapse to the top level.

Figure 3-3. Fold Instance

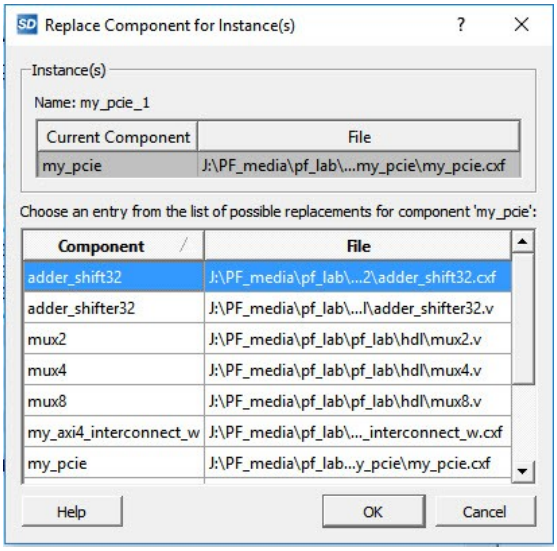


3.2.8 Replace Component

This action displays the Replace Component for Instance(s) dialog. Selecting an instance and then clicking **OK** replaces every instance of that component in the current design with an instance of the new component if that component is valid. All pins that have the same name on the new component will keep their connections, whereas pins that no longer exist will lose their connection and a warning will be printed in the Log window. The dialog will then close.

Selecting an instance and then clicking **OK** for a non-valid component will close the dialog and print an error in the Log window

Figure 3-4. Replace Component Dialog



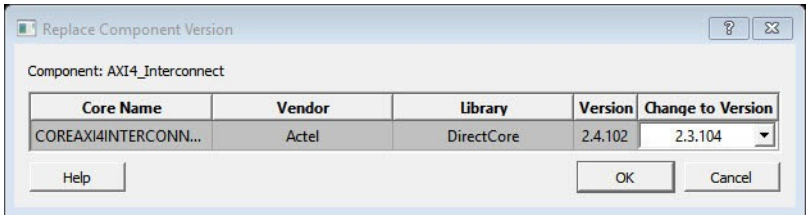
3.2.9 Update Component

This action updates all instances of that component in the current SmartDesign with the newest version of that component. This is available only when the port list has changed. Changing the port list of an instance causes it to return to a new default size.

3.2.10 Replace Component Version

This action exists for IP cores. Under **Design Hierarchy**, select an IP core, right-click, and choose **Replace Component Version**. The Replace Component Version dialog appears.

Figure 3-5. Replace Component Version Dialog

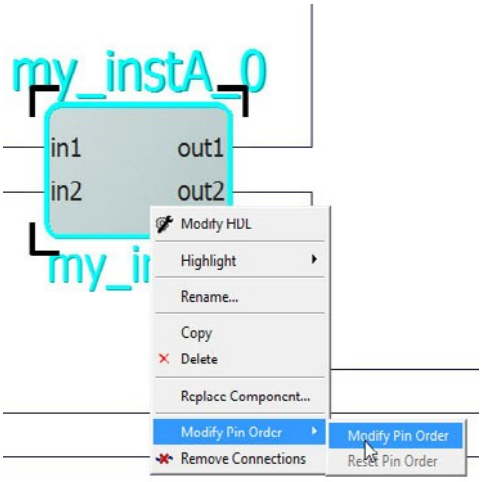


Changing the version in the dialog and then clicking **OK** changes all instances of that component in the current SmartDesign canvas to the specified version of that component.

3.2.11 Modify Pin Order

This a toggle switch. Right-click an instance to open the drop-down menu. Select **Modify Pin Order**. A pop-up window provides instructions on how to reset pin order. Press CTRL+SHIFT and click to select the pin you want to move.

Figure 3-6. Modify Pin Order



Drag the mouse to a new location and release the mouse. The pin is moved to a new location. By default, input pins are on the left of the instance while output pins/inout pins are on the right. **Modify Pin Order** allows you to place the pins on any one of the four sides of the instance. A pin that has been moved away from default locations is identified by a bold arrow head. An inward-pointing arrow head indicates an input pin and an outward-pointing arrow head indicates an output pin. Inout pins do not have an arrow head when they are moved away from the default locations (right side of instance).

Note: If there are two instances on the canvas that communicate with each other in a way where the outputs of one component instance A communicates with the inputs of another component instance B and vice versa, modifying the pin order gives a less cluttered view of the SmartDesign component. See Modify Pin Order Before Connections for details.

Note: **Modify Pin Order** is disabled when the instance is expanded in place. The modified pin order may not be preserved when an instance is expanded but will retain the set order when folded.

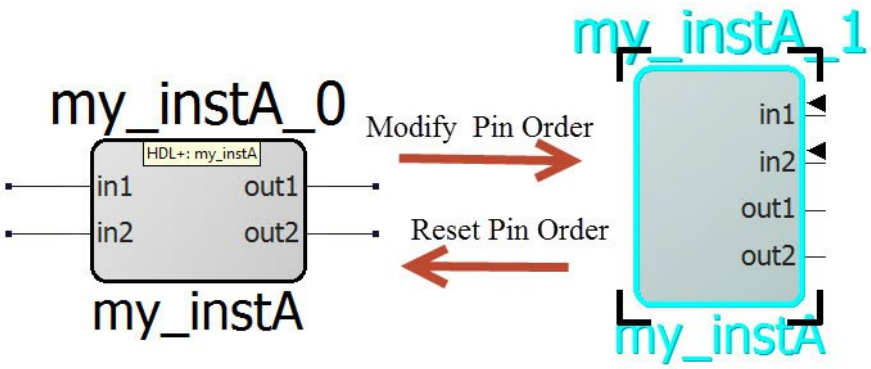
3.2.12 Reset Pin Order

This is a toggle switch. Reset pin order reverses modifications and resets the pins to the default location.

If you moved an instances pin order, this action unresizes the instance and reloads the order from the SmartDesign model.

Note: If you move a pin, and then move it back to its original position, reset pin order will be enabled, but will only resize.

Figure 3-7. Modify/Reset Pin Order



3.2.13 Remove Connections

This action disconnects all pins that can be disconnected. Pins that cannot be disconnected (for example pins connected to pads) are logged in the Log window.

3.2.14 Help

Opens the handbook, release notes, or configuration user guides for the core.

3.3 Pin/Port Actions

Right-click a pin or a port and the drop-down menu appears. Not all actions appear for every port/pin.

3.3.1 Connect

The Connect action adds a net to the design that connects the selected pins/ports. This is the only pin/port action that takes selected nets into account. Selecting a net works as if you selected all of the nets connected pins/ports.

3.3.2 Disconnect

This action disconnects all selected non-pad pins/ports from their attached net if it is allowed (not violating the DRC rules).

3.3.3 Promote to Top Level

This option is available to input/output/inout pins (scalar and bus), slices, and Bus Interfaces (BIF). It creates a top-level port and a net connecting the top-level port to the pin or slices. If a port with that name already exists, a new unique port name is created.

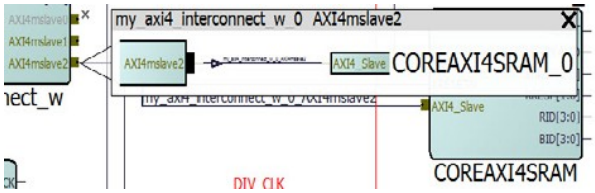
3.3.4 Go to Driver

This action centers on, zoom around, and selects the driver of the pin/port. This action is not available for output pins and top-level input ports. The driver cannot be an inout.

3.3.5 Magnify Pin

This action opens the Magnify window to display connection information (driver/load) about the pin. It is equivalent to double-clicking the pin.

Figure 3-8. Magnify Pin Window



See Magnify Pin for details.

3.3.6 Highlight

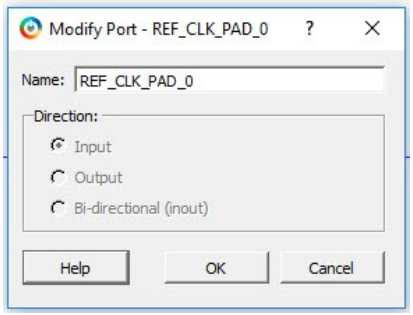
This action opens a menu with multiple highlight color selections. Clicking that color selects that color to highlight the selected items. If any items are already highlighted then highlighting a different color will overwrite the previous highlight color. The action is available when a single or multiple pins/ports are selected.

Clicking the **Unhighlight all** icon in the toolbar removes the highlight color of all highlighted design objects, including highlighted pin/ports.

3.3.7 Modify and Rename

This action opens a Modify Port dialog. It allows the top-level port name and the range to be changed.

Figure 3-9. Modify/Rename Dialog



3.3.8 Delete

This action deletes all selected items that can be deleted: slices, groups, group members, top-level ports.

The delete action deletes all items selected, even if the selected items are of different types. When a group member is deleted, the member is deleted from the group only. The actual pin is not deleted.

3.3.9 Expanding and Collapsing Bus

Expanding a bus displays the slices of the bus and collapsing the bus hides the slices. Slices with net connections cannot be hidden and cannot be collapsed into the bus.

3.3.10 Flip Bit Order

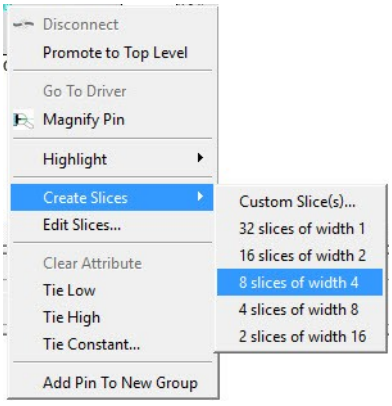
This option is available only to slices. It allows you to flip the upper range (MSB) and lower range (LSB) of the slice. All connection/tieoff information and presentation information are retained.

3.3.11 Create Slices

Open a menu of slice options that can be created from the bus pin/ports. A custom slice option to create any slice/bit combination of your choice and the more common possible combinations of slices are available. For example, using a 32-bit bus with the Custom Slices option allows the creation of any slice/bit combinations (e.g., a slice of 10 bits and another slice of 22 bits). To make it convenient to create slices, common, off-the-shelf bus slices are listed in the drop-down menu; for example:

- 32 slices of width 1
- 16 slices of width 2
- 8 slices of width 4
- 4 slices of width 8
- 2 slices of width 16

Figure 3-10. Slice Creation for a 32-bit Bus



On a components bus pin the slices will be expanded by default.

The directions of the slices (input/out) are indicated by an arrow head.

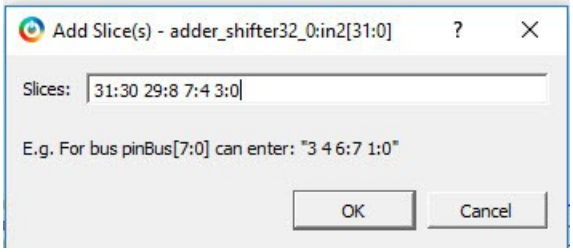
On a top-level bus port the slices will be placed in a column below the bus port.

Note: If slices exist before new off-the-shelf slices are created, the existing slices are deleted first before new ones are created.

3.3.12 Custom Slices

This option opens a dialog for entering a list of slices. If these slices are all valid then they are added to the bus. If the slices are not valid (e.g., slice bits already exist and used in an existing slice), the error is reported in the Log window. The dialog supports any separator character except colon because the colon is used to specify a range. No characters other than the colon is allowed adjacent to the two range indices.
Note: Creating a custom slice does not delete pre-existing slices.

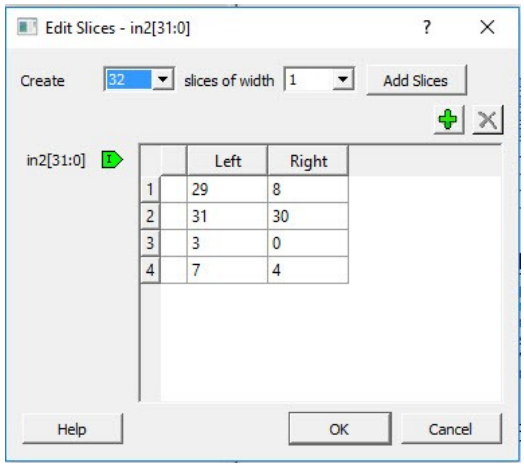
Figure 3-11. Custom Slices Dialog



3.3.13 Edit Slices

The Edit Slice option opens the Edit Slices dialog. It allows existing slices to be modified.

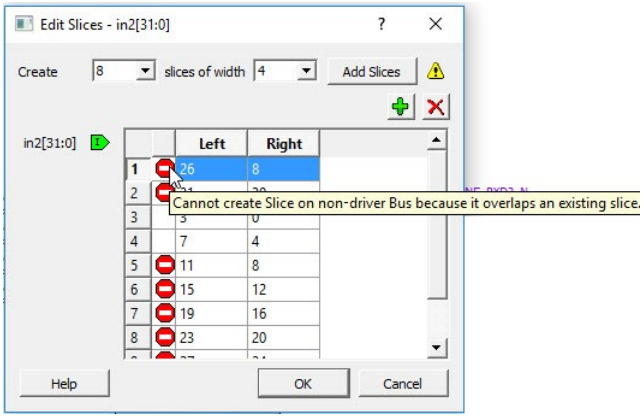
Figure 3-12. Edit Slices Dialog



Use the dialog to change the range of the bits, add a slice or delete a slice. Modifying the slices and clicking **OK** initiates the changes if they are valid and closes the dialog.

Modifying the slices and clicking **OK** prints an error in the Log and closes the dialog if the changes are not valid. Some error messages may be reported in the Edit Slice dialog. Hover the mouse over the error icon to display details of the error.

Figure 3-13. Tooltip and Error Message



3.3.14 Clear Attributes

This action clears the pin attributes (Tie to High/Low/Constant, Inversion/Marked Unused).

3.3.15 Mark Unused

This is available to the output pins (scalar and bus) of a component instance. This action specifies the pin/port as unused so it can pass DRC check without being connected.

3.3.16 Invert

This action inverts the input/output scalar pin and port. A bubble is added to indicate inversion.

3.3.17 Tie High and Tie Low

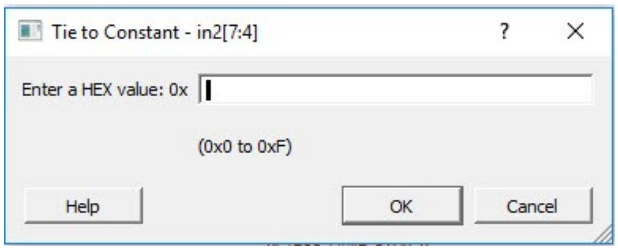
The Tie High action connects the pin (scalar and bus) to VCC. For a bus pin this action deletes all slices. For a group this action is applied to all non-output member pins in the group.

The Tie Low action connects the pin (scalar and bus) to Ground. For a bus pin this action deletes all slices. For a group this action is applied to all non-output member pins in the group.

3.3.18 Tie Constant

This action is available only to bus pins and slices (except single-bit slice). It opens the Tie to Constant dialog box for a constant value in HEX to be entered for the bus pins and slices. Only valid values entered in HEX within parenthesis are allowed.

Figure 3-14. Tie to Constant Dialog



3.3.19 Add Pin to New Group and Add Pin to Group

This menu item is available to instance pins. If a group is selected first, right-click a pin and choose **Add Pin to Group** to add the pin to the selected group. If no group is selected first, the menu item is called **Add Pin to New Group**, a new group with the default group name Group/Group_1/Group_2/Group_3/ and so on is created, and all selected pins are added to the newly created group.

A pin group can be expanded to display the member pins or collapsed to hide the member pins. Member pins connected to nets cannot be hidden and cannot be collapsed into the group. Only member pins (in a pin group) with Pin Attributes (Tie high/low/marked unused) can be hidden and collapsed into the pin group.

3.3.20 Rename (Group)

This is available only to group pins. It opens the Rename Group dialog for the group name to be changed. If a valid name is entered then clicking **OK** renames the group. The new name field defaults to the current group name if no new name is entered in the dialog.

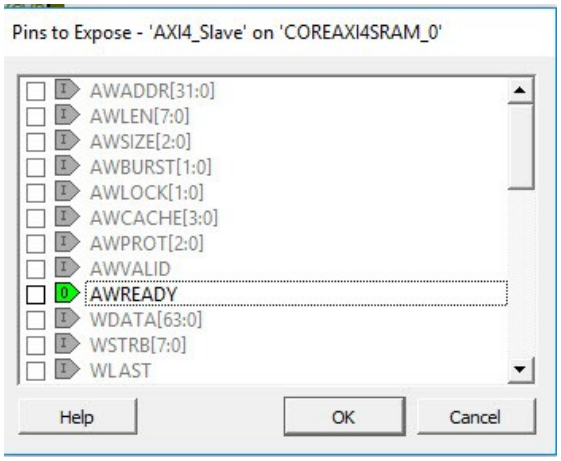
If an invalid name is entered or a pin with that name already exists then clicking **OK** prints an error in the Log and closes the dialog.

3.3.21 Show and Hide BIF Pins

This opens the Show Pins to Expose dialog to display all the Bus Interface Pins available to be exposed or hidden from the instance. Check the pins in the BIF you want to expose and uncheck the pins you want to hide. Hidden pins will not be exposed on the interface.

Note: Not all pins can be exposed. The pins that can be exposed depends on the BIF. If the BIF is connected already, then none of the input pins can be exposed. If the BIF is not connected, every item in the menu can be exposed.

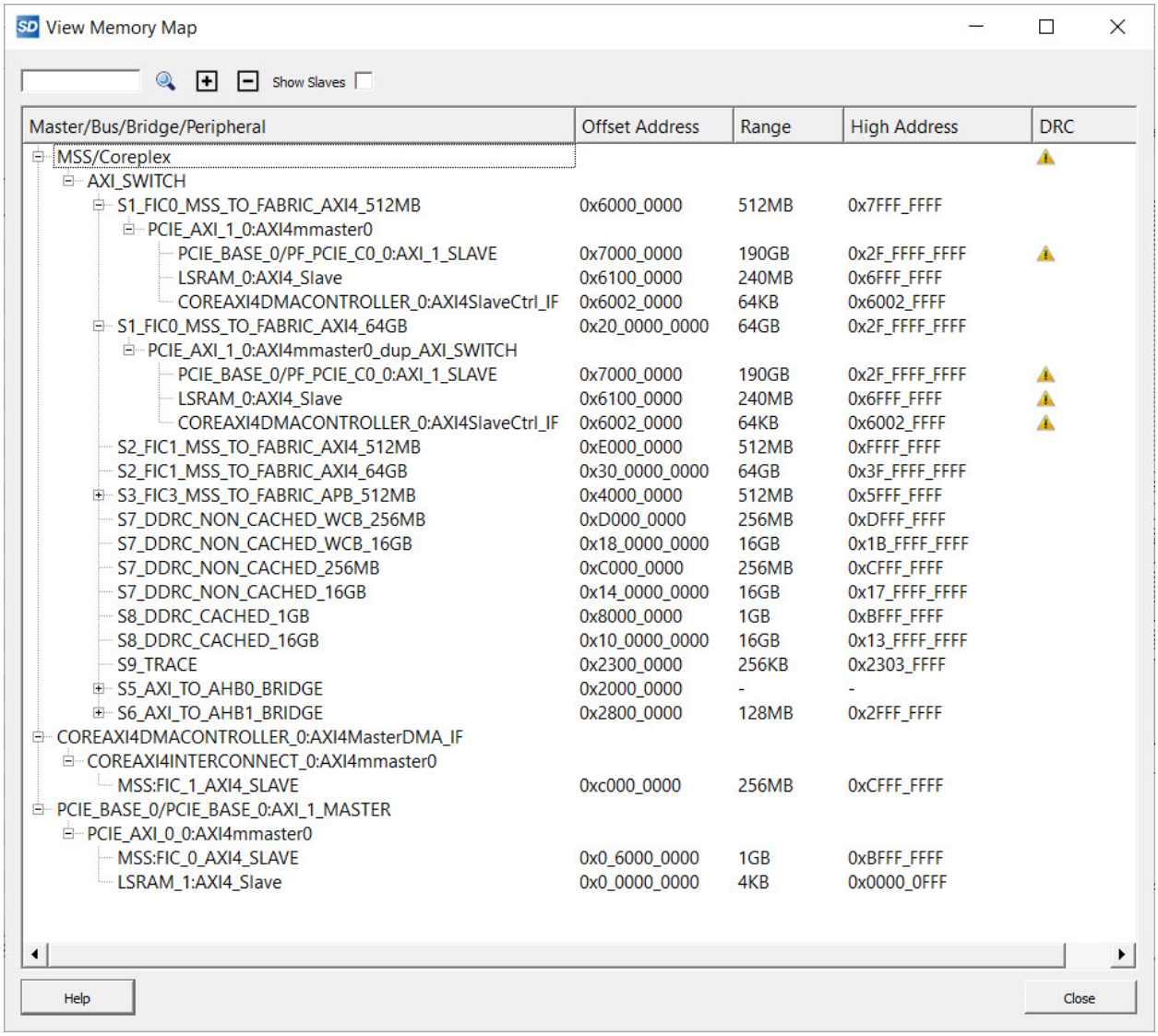
Figure 3-15. Show to Expose Dialog



3.4 View Memory Map

The View Memory Map dialog constructs the memory map corresponding to various masters in the SmartDesign component and displays the hierarchy in a tree format. To open the dialog box, right-click anywhere on the SmartDesign canvas and select **View Memory Map**. Alternatively, right-click on any bus core instance in the canvas and select **View Memory Map**, or click the **View Memory Map** icon in the toolbar at the top of the canvas  .

Figure 3-16. View Memory Map Dialog Box



This dialog box shows the memory map starting from a master in the design to peripherals connected through bus and bridge cores hierarchically. There can be various types of bus and bridge cores in the hierarchy between the master and the peripherals.

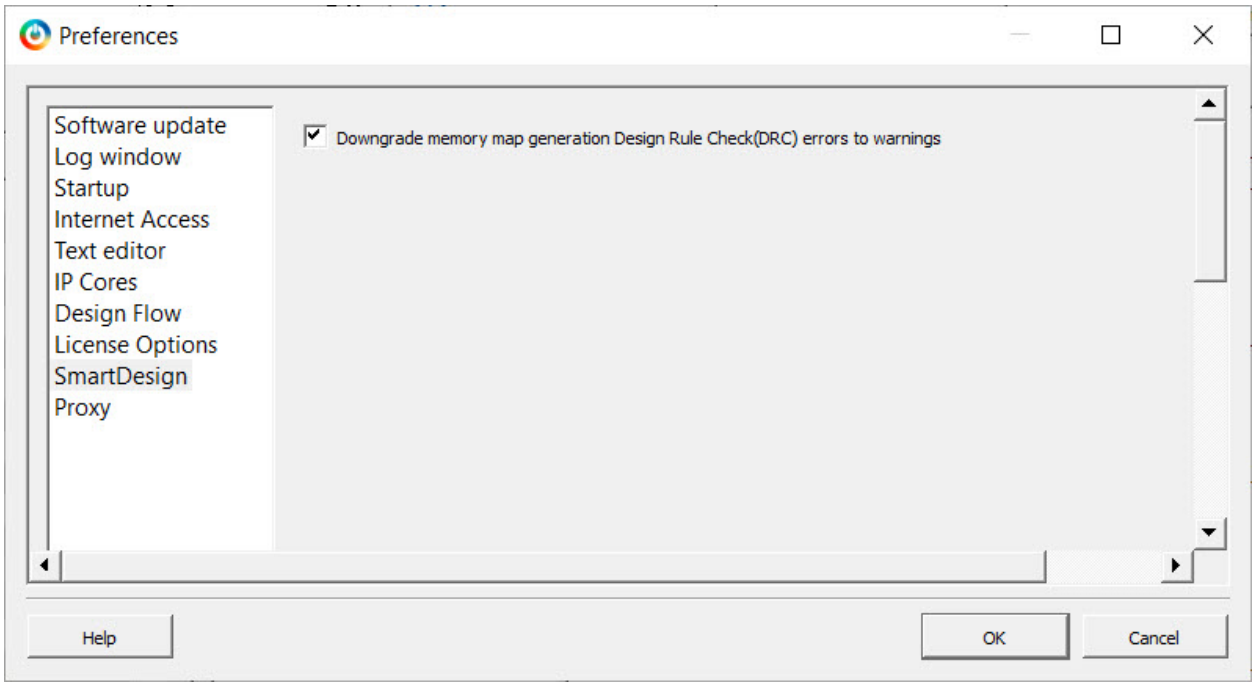
- Master Node -> Parent Bus -> Bridge -> Child Bus -> Peripherals
- Master Node - > Bus -> Peripherals

Note: The memory map dialog box also considers masters, bus and bridge cores, and peripherals that are present in other SmartDesign components, which are instantiated under the current SmartDesign's hierarchy.

Each peripheral in the memory map is shown with an Offset Address, Range, High Address and DRC. If DRC exists, an Error/Warning icon with a tooltip message will be shown. DRC is flagged if a peripheral cannot be accessed completely or partially by the master's address space.

Downgrade memory map generation Design Rule Check(DRC) errors to warnings Option has been added to downgrade DRC errors to warnings while generating a Memory Map report. You can access this option by clicking on **Project > Preferences > SmartDesign**.

Figure 3-17. Downgrade memory map generation Design Rule Check(DRC) errors to warnings option in Preferences Dialog Box

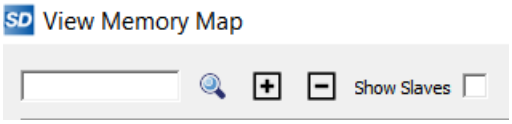


Note:
In PolarFire SoC MSS based designs, the Fabric Interface Controllers(FICs) FIC_0 and FIC_1 have two regions each, 64GB and 512MB. A peripheral accessible by the Coreplex via one FIC region may not be accessible in the other FIC region based on the address spaces and bus configurations. This is a valid design scenario and should not be flagged as an error in the Memory Map DRC section. So a Memory Map DRC error that is seen in both the regions (64GB and 512MB regions) of a FIC will stay as an error, and if the DRC error is seen only in one of the two regions of the FIC, then it will be automatically downgraded to a DRC warning, both in the Memory Map and SmartDesign component generation.

Navigation buttons and filters

The **View Memory Map** dialog also provides new buttons and filters at the top of the dialog box for easy navigation and ease of use.

Figure 3-18. View Memory Map Dialog Buttons and Filters



- Search button

  You can search for a specific master/bus/bridge/peripheral in the memory map by specifying a full or partial name in the search text box.

- Expand all button

  Expands and shows the full hierarchy of all masters in the memory map starting from the master to the peripherals.

- Collapse all button

  Collapses the full hierarchy of all masters in the memory map and only shows the top-level masters in the dialog.

- Show Slaves filter

  Shows all the masters and the peripherals under them in the design in a flat hierarchy with their start addresses, ranges and DRCs if any. The bus and bridge cores will not be shown.

Exporting Memory Map Report

The View Memory Map dialog contents can be exported to a memory map report file of .json or .html format. Select the **Memory Map Report** option from Libero File -> Export. In the Export Memory Map Report dialog, you can specify the SmartDesign component for which you want to export the memory report. Click on the **Browse** button in the dialog to specify the memory map report file name, type (.json or .html) and location on disk. A .json or .html format memory map report file (which can be opened in a web browser or a json viewer in a text editor) will be created when you click the **Save** button.

Figure 3-19. Libero Option to Export Memory Map Report

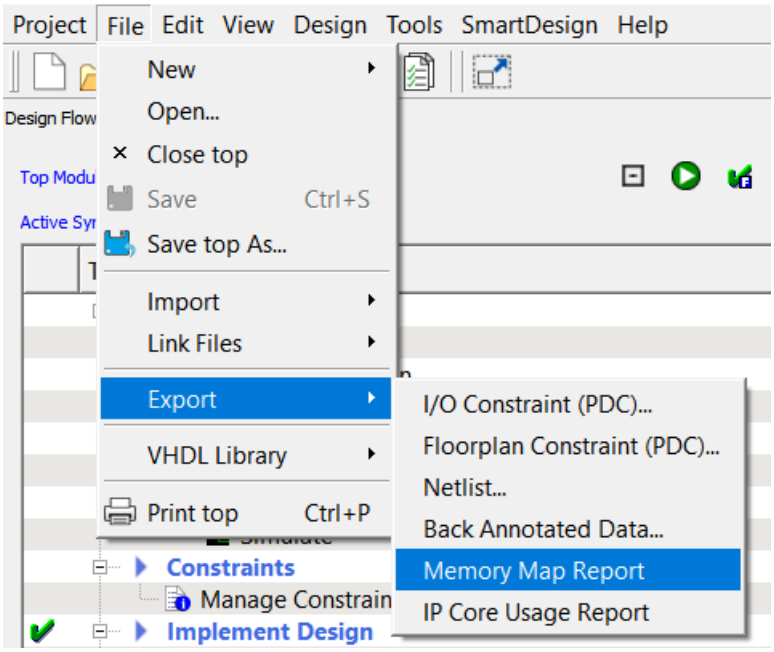


Figure 3-20. Export Memory Map Dialog Box (.json format)

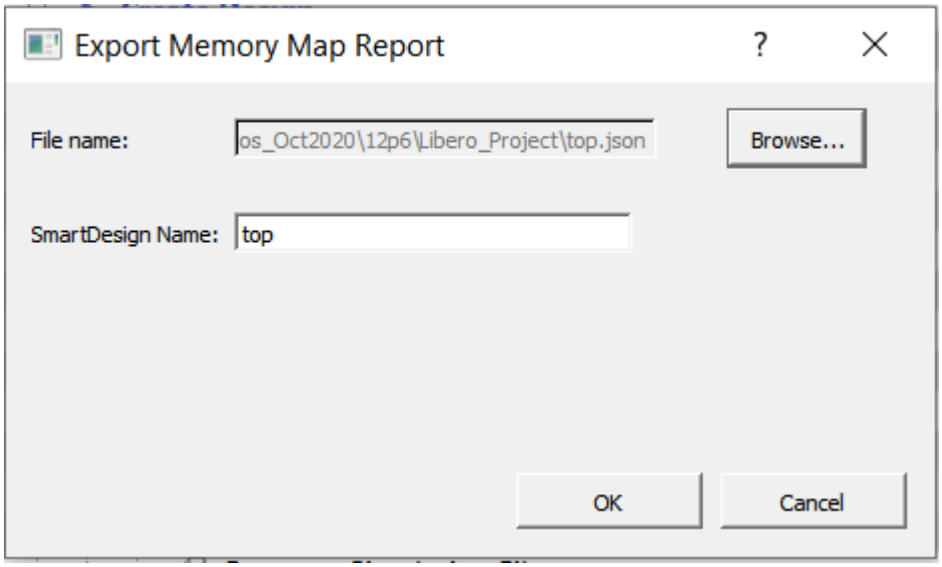


Figure 3-21. Export Memory Map Dialog Box (.html format)

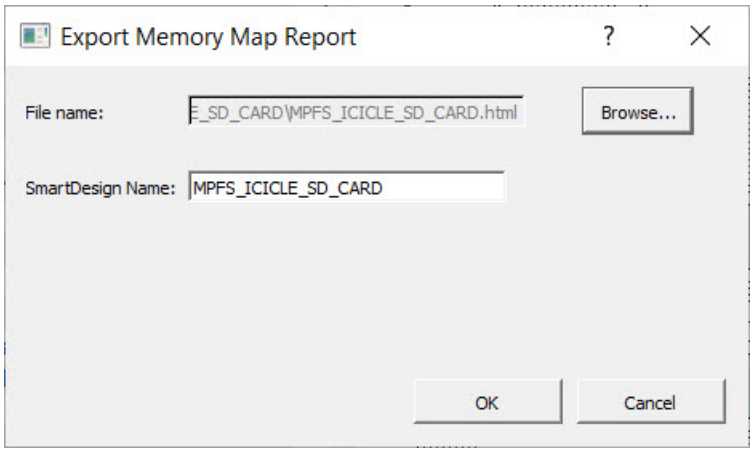


Figure 3-22. Sample Memory Map Report (.json format)


```
{
	"title": "Memory Map Report",
	"date": "Mon Feb 15 15:01:56 2021",
	"project_name": "MPFS_ICICLE_SD_CARD",
	"project_location": "C:\\Users\\C51990\\Desktop\\convert_to_word\\MPFS_ICICLE_SD_CARD",
	"SmartDesign name": "MPFS_ICICLE_SD_CARD",
	"Master/Bus/Bridge/Peripheral OffsetAddress Range HighAddress":[
	{"Node name":"COREAXI4DMACONTROLLER_0:AXI4MasterDMA_IF",
	"Type":"Master",
		"Connected Node":[
			{"Node name":"COREAXI4INTERCONNECT_0:AXI4mmaster0",
			"Type":"Bus",
				"Connected Node":[
			{"Node name":"MSS:FIC_1_AXI4_SLAVE",
			"Offset Address":"0xc000_0000",
			"Range":"256MB",
			"High Address":"0xCFFF_FFFF",
			"Type":"Peripheral"
			}                              ]                    }            ]
	}
,
	{"Node name":"MSS/Coreplex",
	"Type":"Master",
		"Connected Node":[
			{"Node name":"AXI_SWITCH",
			"Type":"Bus",
				"Connected Node":[
			{"Node name":"S1_FIC0_MSS_TO_FABRIC_AXI4_512MB",
			"Offset Address":"0x6000_0000",
			"Range":"512MB",
			"High Address":"0x7FFF_FFFF",
			"Type":"Bridge",
				"Connected Node":[
			{"Node name":"PCIE_AXI_1_0:AXI4mmaster0",
			"Type":"Bus",
				"Connected Node":[
			{"Node name":"PCIE_BASE_0/PF_PCIE_C0_0:AXI_1_SLAVE",
			"Offset Address":"0x7000_0000",
			"Range":"190GB",
			"High Address":"0x2F_FFFF_FFFF",
			"DRC":"Warning: Peripheral 'PCIE_BASE_0/PF_PCIE_C0_0:AXI_1_SLAVE' with address space 0x7000_0000 - 0x2F_FFFF_FFFF can be accessed partially by Master address space 0x6000_0000 -
0x7FFF_FFFF",
			"Type":"Peripheral"
			},
			{"Node name":"LSRAM_0:AXI4_Slave",
			"Offset Address":"0x6100_0000",
			"Range":"240MB",
			"High Address":"0x6FFF_FFFF",
```


Figure 3-23. Sample Memory Map Report (.html format)

Memory Map Report: MPFS_ICICLE_SD_CARD

Design Details

FAM: PolarFireSoC
Die: MPFS250T_ES
Package: FCVG484
Speed Grade: STD
Voltage: 1.0
date: Fri Feb 12 13:53:16 2021
project_name: MPFS_ICICLE_SD_CARD
project_location: C:\\Users\\C51990\\Desktop\\MPFS_ICICLE_SD_CARD
SmartDesign name: MPFS_ICICLE_SD_CARD

Memory Map

The SmartDesign MPFS_ICICLE_SD_CARD contains the following Masters under its hierarchy

- Coreplex
- COREAXI4DMACONTROLLER_0:AXI4MasterDMA_IF
- PCIE_BASE_0:AXI_1_MASTER

top of page

Coreplex

Peripheral	Offset Address	Range	High Address	DRC
PCIE_BASE_0/PF_PCIE_C0_0:AXI_1_SLAVE	0x7000_0000	190GB	0x2F_FFFF_FFFF	Warning: Peripheral 'PCIE_BASE_0/PF_PCIE_C0_0:AXI_1_SLAVE' with address space 0x7000_0000 - 0x2F_FFFF_FFFF can be accessed partially by Master address space 0x6000_0000 - 0x7FFF_FFFF
LSRAM_0:AXI4_Slave	0x6100_0000	240MB	0x6FFF_FFFF	
COREAXI4DMACONTROLLER_0:AXI4SlaveCtrl_IF	0x6002_0000	64KB	0x6002_FFFF	
PCIE_BASE_0/PF_PCIE_C0_0:AXI_1_SLAVE	0x7000_0000	190GB	0x2F_FFFF_FFFF	Warning: Peripheral 'PCIE_BASE_0/PF_PCIE_C0_0:AXI_1_SLAVE' with address space 0x7000_0000 - 0x2F_FFFF_FFFF can be accessed partially by Master address space 0x20_0000_0000 - 0x2F_FFFF_FFFF
LSRAM_0:AXI4_Slave	0x6100_0000	240MB	0x6FFF_FFFF	Warning: Peripheral 'LSRAM_0:AXI4_Slave' with address space 0x6100_0000 - 0x6FFF_FFFF cannot be accessed by Master address space 0x20_0000_0000 - 0x2F_FFFF_FFFF
				Warning: Peripheral

Masters, Bus and Bridge cores available in Libero SoC Catalog

Various types of cores recognized as masters, and bus and bridge cores are available in the Libero SoC Catalog window that can be used in a design. There are a few limitations on some of the core versions that can be used in a design for the memory map to be constructed correctly in the **View Memory Map** dialog. The below consolidated table of all the available masters, and bus and bridge cores highlights those limitations/exceptions on the cores and core versions w.r.t memory map.

Table 3-1. Masters, Bus and Bridge cores available in Libero SoC Catalog

Classification	Core	Core Type	Minimum core version supported in Libero SoC v2021.1 for Memory Map generation	Latest core version available in Libero SoC v2021.1
Masters	MIV_RV32IMC	AXI, AHBLite and APB3 Masters	NA. All available production versions will work.	2.1.100
	MIV_RV32	AXI, AHBLite and APB3 Masters	NA. All available production versions will work.	3.0.100
	MIV_RV32IMA_L1_AXI	AXI Master	NA. All available production versions will work.	2.1.100
	MIV_RV32IMA_L1_AHB	AHBLite Master	NA. All available production versions will work.	2.3.100
	MIV_RV32IMAF_L1_AHB	AHBLite Master	NA. All available production versions will work.	2.1.100
	CORERISCV_AXI4	AXI4 Master	NA. All available production versions will work.	2.0.102
	COREAXI4DMACONTROLLER	AXI4 Master	NA. All available production versions will work.	2.0.100
	COREABC	APB3 Master	NA. All available production versions will work.	3.8.102

Family specific Master cores	PolarFireSoC Standalone MSS (PolarFireSoC only)	AXI4 Master	NA. All available production versions will work.	v2.0
	System Builder and SmartFusion2 MSS (SmartFusion2 and IGLOO2)	AHBLite and APB3 Masters	NA. All available production versions will work.	1.1.500
	CORECORTEXM1(PolarFire, PolarFireSoC and RTG4)	AHBLite Master	NA. All available production versions will work.	3.0.100 and 2.0.100
	PF_PCIE (PolarFire only)	AXI Master	NA. All available production versions will work.	2.0.104
	SERDES_IF, SERDES_IF2, SERDES_IF3 (SmartFusion2 and IGLOO2)	AXI and AHBLite Masters	NA. All available production versions will work.	1.2.210, 1.2.212, 1.2.212 respectively
	PCIE_SERDES_IF (RTG4 only)	AXI and AHBLite Masters	NA. All available production versions will work.	2.0.100
	COREHPDMACTRL (SmartFusion2 and IGLOO2)	AHBLite Master	NA. All available production versions will work.	2.1.103
	CORESYSSERVICES (SmartFusion2 and IGLOO2)	AHBLite Master	NA. All available production versions will work.	3.2.102
	CoreConfigMaster (SmartFusion2 and IGLOO2)	AHBLite Master	NA. All available production versions will work.	2.1.102
Bus cores	COREAXI4INTERCONNECT	AXI bus	2.5.100	2.8.103
	CoreAHBLite	AHBLite bus	NA. All available production versions will work	5.4.102
	CoreAPB3	APB3 bus	NA. All available production versions will work	4.1.100
	CoreAXI	AXI bus	NA. All available production versions will work	3.2.101

Family specific bus type cores	PF_DRI (PolarFire and PolarFireSoC)	APB bus	This core is not supported for Memory Map generation. Correct addresses and/or hierarchy will not be shown for this core in the Memory Map of Libero SoC v2021.1. Will be supported in a future release	1.1.100
	CoreConfigP (SmartFusion2 and IGLOO2)	APB bus	NA. All available production versions will work	7.1.100
Bridge cores	COREAXITOAHBL	AXI to AHBLite bridge	Must use v3.5.100 for proper Memory Map generation in Libero SoC v2021.1	3.5.100
	COREAHBL2AHBL_BRIDGE	AHBLite to AHBLite bridge	This core is not supported for Memory Map generation. Correct addresses and/or hierarchy will not be shown for this core in the Memory Map of Libero SoC v2021.1. Will be supported in a future release	2.1.108
	COREAHBLTOAXI	AHBLite to AXI bridge	NA. All available production versions will work	2.1.101
	COREAHBTOAPB3	AHBLite to APB bridge	NA. All available production versions will work	3.1.100
	COREAXITOAXICONNECT	AXI to AXI bridge	This core is not supported for Memory Map generation. Correct addresses and/or hierarchy will not be shown for this core in the Memory Map of Libero SoC v2021.1. Will be supported in a future release	2.0.101

4. Designing with SmartDesign

SmartDesign is a GUI-driven block-based design entry tool for the instantiation, configuration, and connection of various types design blocks.

The SmartDesign canvas is similar to a breadboard, where the components of different types are assembled (instantiated), stitched together (connections made via nets) to create a design-rule-checked synthesis-ready HDL file for the complete FPGA design process.
To design with SmartDesign:

1. Create a top-level SmartDesign component (analogous to the breadboard).
2. Configure/Instantiate components on the top-level SmartDesign.
3. Make the connections (analogous to making wire connections to the different components).
4. Add top-level ports.
5. Invoke a DRC on the design.
6. Generate the top-level component.

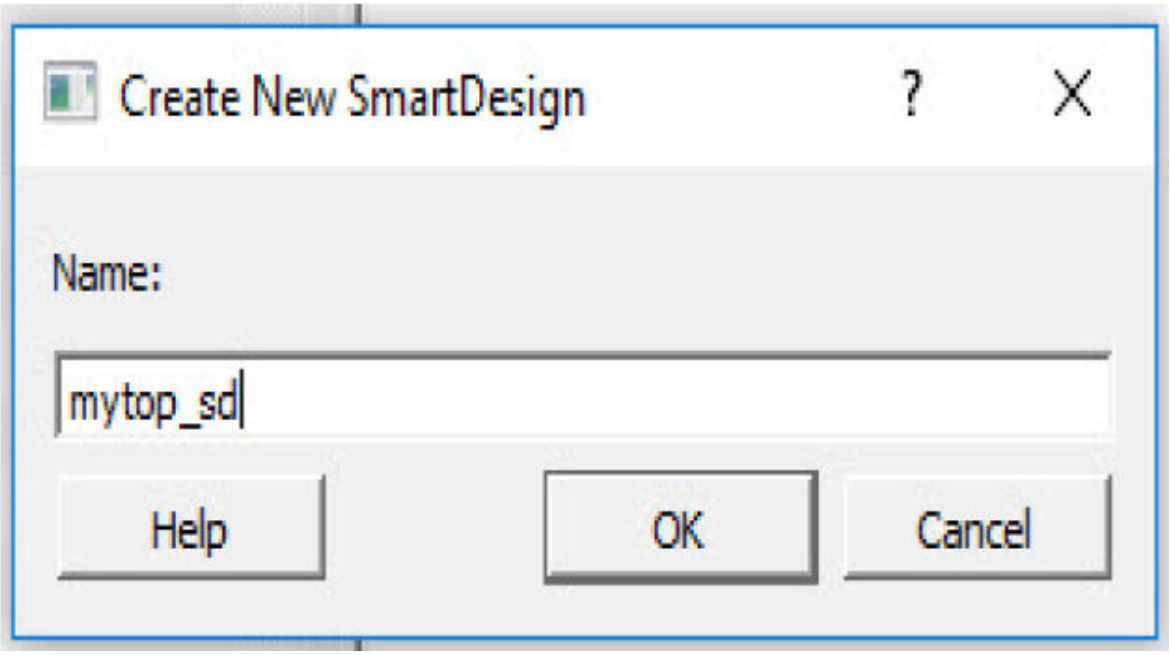
4.1 Create a Top-Level SmartDesign Component

A SmartDesign Component must be first created. This SmartDesign component may be the top level of the design or it may be used as a lower level SmartDesign component (after successful generation) in another design.

To create a SmartDesign Component:

1. From the **File** menu, choose **New > SmartDesign**, or double-click **Create SmartDesign** in the Design Flow window. The Create New SmartDesign dialog box opens.

   Figure 4-1. Create New SmartDesign Dialog Box



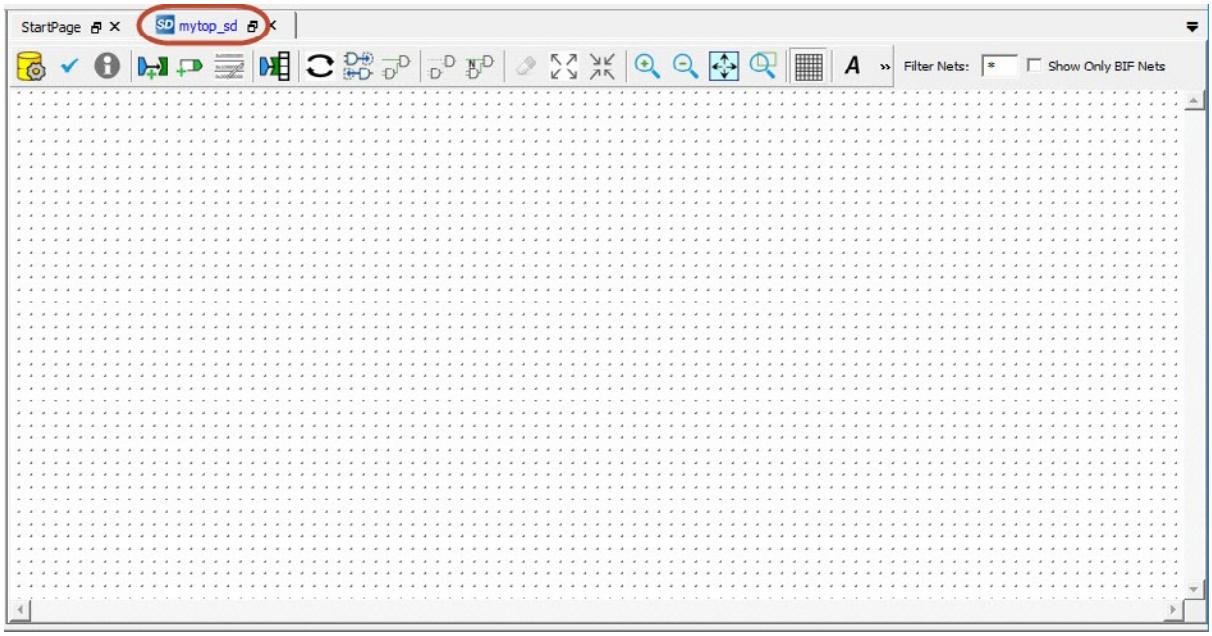
2. Enter a name and click **OK**. The component appears in the **Design Hierarchy** tab of the Design Explorer.

Note: The component name must be unique in your project.

The main window displays the SmartDesign canvas (the breadboard) with the component name you have entered displayed in a tab across the window.

The following figure shows the SmartDesign Canvas with the Grid turned on. By default, the grid is turned off.

Figure 4-2. SmartDesign Canvas with Grid Turned On



4.2 Configure/Instantiate Components

4.2.1 Configure

This step is required for IP cores such as Clock Conditioning Circuitry (CCC), DDR3/4 Memory Controllers, SRAMs, AMBA Bus Interface cores, and Transceiver Interface cores. These cores are available in the Catalog of the Design Explorer. If the core name appears in italics, double-click the core to download the core from the Microchip IP Core Repository to your hard disk (the vault) first. Double-click the core in the catalog to open the Core's Configurator to configure the core. For details, refer to the respective configuration user guides.

4.2.2 Instantiate

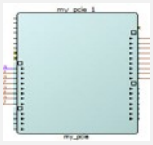
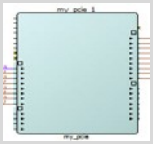
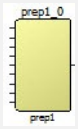
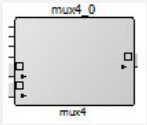
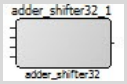
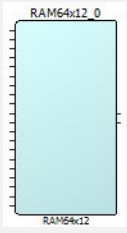
The SmartDesign canvas accepts the following component types for instantiation:

- Configured Microchip IP Cores
  - Drag and drop from the Catalog
  - IP cores must first be configured before they can be instantiated. If the IP core is not configured before instantiation, the drag-and-drop operation invokes the Core Configurator for the core to be configured.
- User-generated or third-party IP Cores
  - Drag and drop from the Catalog
- HDL design files
  - Drag and drop from the Design Hierarchy
- HDL + design files (from the Design Hierarchy)
  - HDL+ design files are parameterized HDL design files or HDL files with Buses attached
  - Drag and drop from the Design Hierarchy
- Basic macros
  - Drag and drop from Macro Library section in the Catalog
- Other SmartDesign components
  - These are *.cxf files generated from SmartDesign in the current Libero SoC project or imported from other Libero SoC projects.
  - Drag and drop from the Design Hierarchy

- Re-usable design blocks
  - These are *.cxz files published from Libero SoC and used as design blocks
  - Drag and drop from the Design Hierarchy

Each of these design components, after instantiation, is identified by different colors in the Design Canvas A tooltip pops up to provide details of the component when the mouse is hovered over the component.

Table 4-1. Component Types in the SmartDesign Canvas and Tooltip

Icon	Type of Design Components	Tooltip Information
	Configured IP Core Component	Component: my_pcie Core: PF_PCIE 1.0.217
	IP Core directly instantiated from the Catalog	Core: PF_PCIE 1.0.217
	Block (*.cxz) file	Block: prep1
	SmartDesign component (*.cxf) file	SmartDesign: mytop
	HDL+	HDL+: mux4
	HDL	HDL:adder_shifter32
	Macro	Macro: RAM64x12

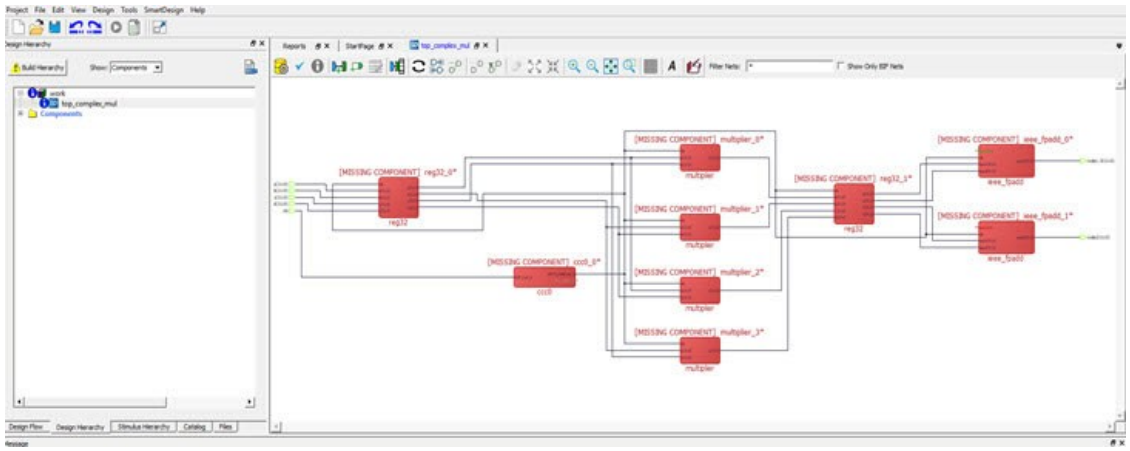
The tooltip displays the following information about the component:

- Type of component
- Name of component
- Version of Core (for IP cores only)

4.2.3 Importance of .cxf Files in SmartDesign

SmartDesign components can be instantiated in another SmartDesign component by dragging and dropping them into the SmartDesign canvas. The low-level SmartDesign components in the hierarchy must be imported before instantiating in a new project. This is done by selecting **Import > Components** in the **File** menu. The HDL and corresponding cores associated with these components must also be imported and configured before instantiating in the new SmartDesign component. If you just import the .cxf file and do not import files corresponding to the low-level instances, you will see those instances highlighted in red and you will be informed of missing components. See the following example figure.

Figure 4-3. Errors While Importing SmartDesign Components with HDL Files and IP Cores



Using .cxf files is important in the following cases:

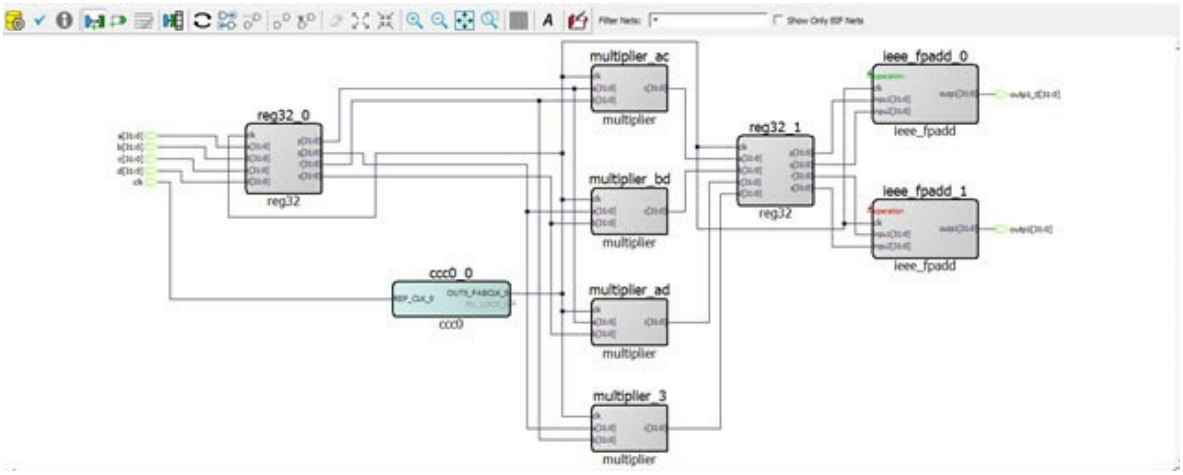
- When working on multiple designs with very few changes in the original design blocks.
- When dividing a large design into smaller designs with very few additional blocks.

Using .cxf files provides the following advantages:

- Significant time savings (decreased generation time)
- Reduces errors in manual connections

See the following design example.

Figure 4-4. SmartDesign Example for Complex Multiplication



The example design above has clocking blocks, multiplier blocks, and adder blocks. You could separate this design into two separate designs— complex_real and complex_imaginary— in either of the following ways:

- Without using .cxf files— create two new projects, import and configure all necessary HDL files and IP cores, and make the connections manually.

- Using .cxf files—From the **Project** menu, save the original project with a new name using the **Save As** option. Make the necessary changes in the new project by deleting the blocks and ports you no longer need and adding additional blocks (if necessary), restoring the connections between existing blocks from original design. This saves time while dividing large designs into smaller designs, without the need to make all the connections manually.

To save the original project with a new name, from the **Project** menu, select the **Save As** option. Click **OK** after entering the new project name.

To change the name of the SmartDesign component, right-click the component in the Design Hierarchy and choose **Rename Component**.

To create a SmartDesign component for calculating the real part of a complex multiplication, remove the blocks that are not necessary for calculating real part, and also remove the unused ports. This eliminates many of the manual connections and decreases generation time. Real designs may not be as simple as this, but this type of dividing saves time while preserving the connections between existing blocks.

See the following example figures.

Figure 4-5. SmartDesign Component for Real Part Calculation of Complex Multiplication

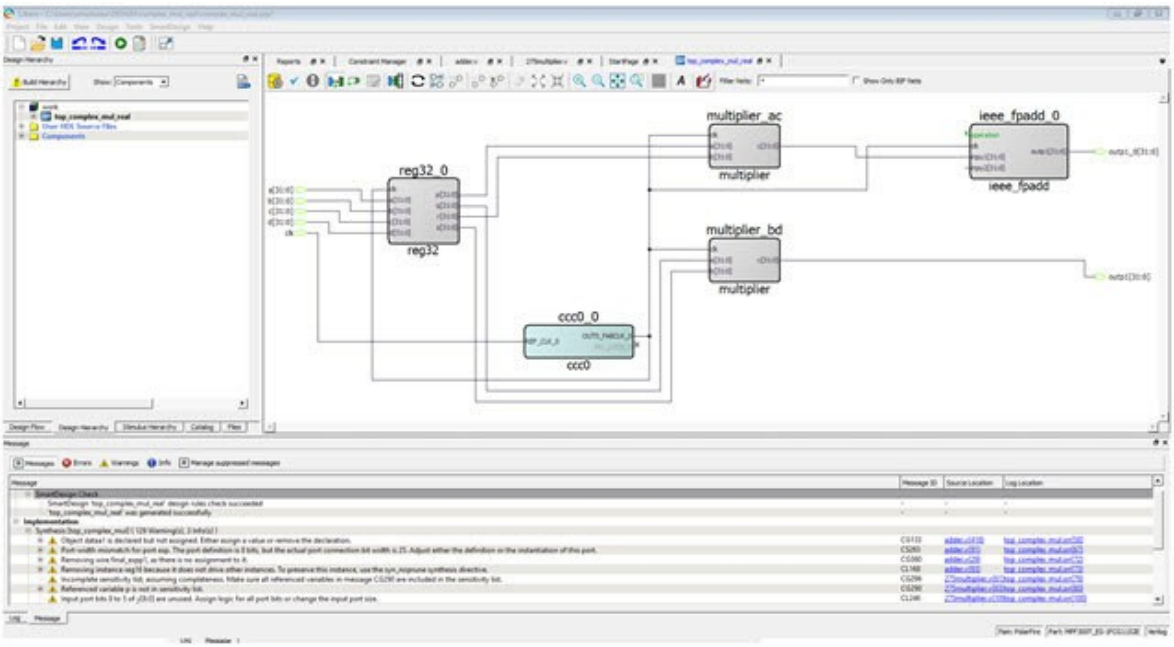
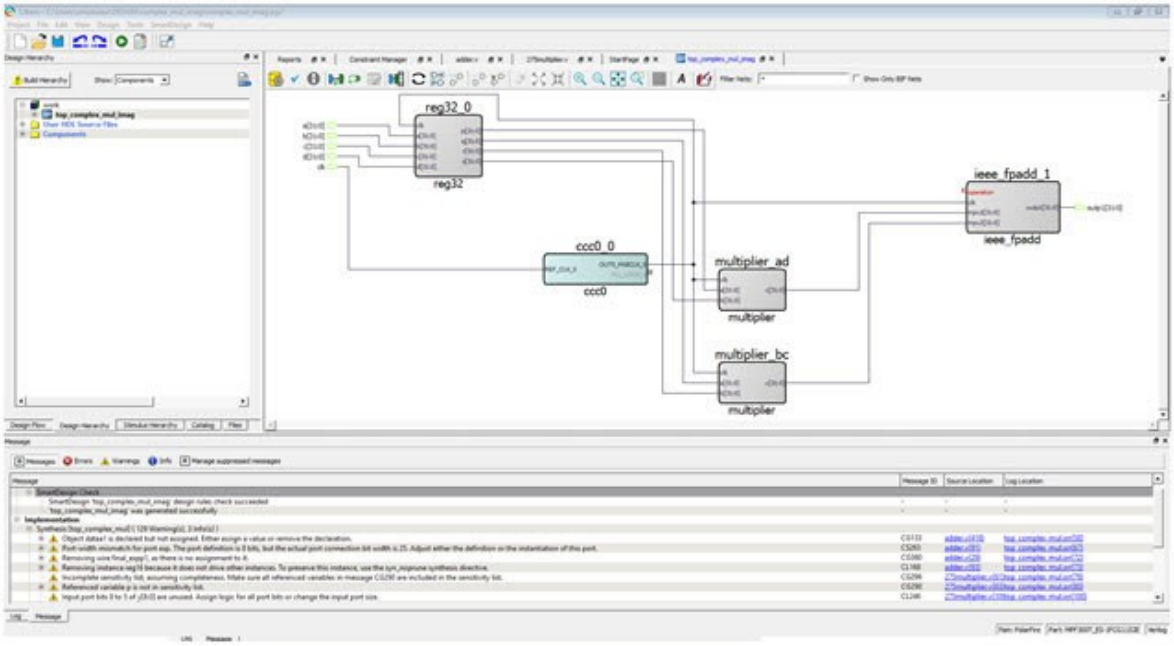


Figure 4-6. SmartDesign Component for Imaginary Part Calculation of Complex Multiplication



4.3 Make the Connections

There are several ways to make net connections in the SmartDesign Canvas.

4.3.1 QuickConnect

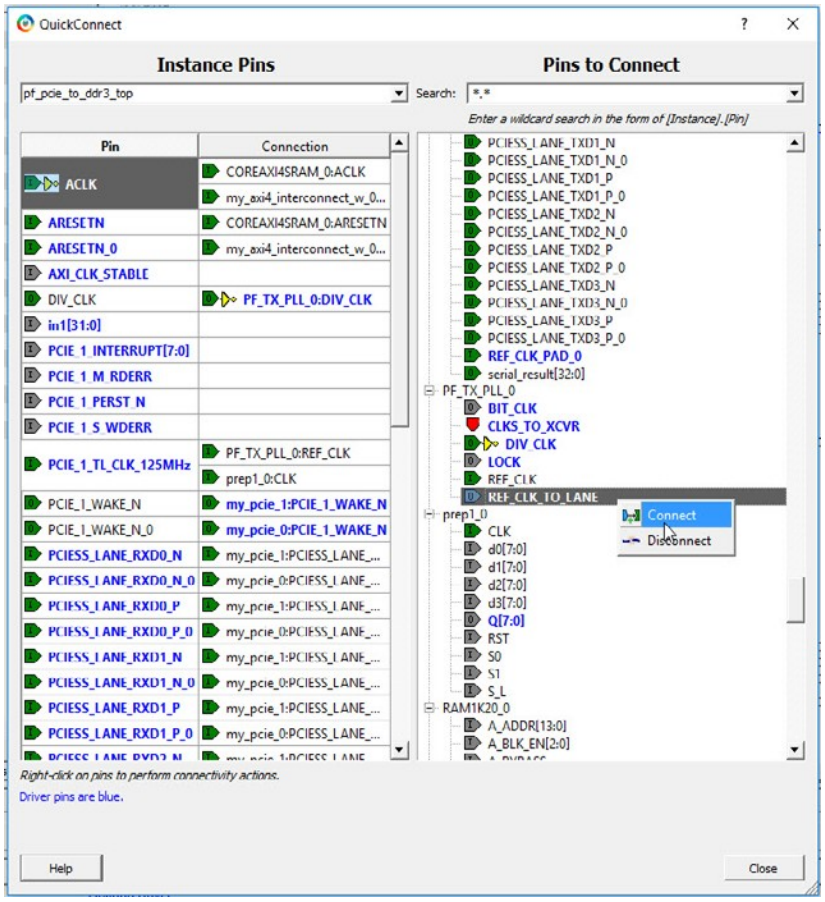
Click the **QuickConnect** icon to open the QuickConnect dialog box. QuickConnect is useful if you have a large design with many pins to connect and know the names of the pins you wish to connect without looking at the SmartDesign canvas. Connections are reflected in the Canvas as you make them in the dialog box. Error messages appear in the Log window immediately. It may be useful to resize the QuickConnect dialog box so that you can view the Log window or SmartDesign Canvas while you make the connections.

To connect pins using QuickConnect:

1. Find the Instance Pin you want to connect and click to select it.
2. In **Pins to Connect**, find the pin to which you want to connect, right-click, and choose **Connect**. If necessary, use the **Search** field to narrow down the list of pins displayed in Pins to Connect.
   Note: This dialog box enforces DRC checks. If the connection is invalid then the **Connect** menu item is grayed out.

Connections can also be made by selecting pins in the same column.

Figure 4-7. QuickConnect Dialog



4.3.2 Control + Click Connection

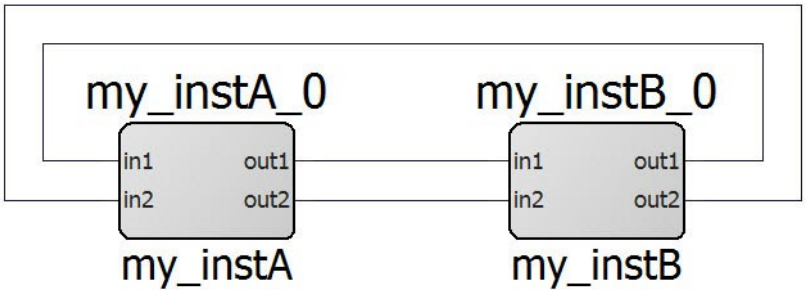
Use Control + Click to connect two pins on the canvas:

1. Left-click one pin.
2. Control and left-click another pin.
3. Right-click the second pin and select **Connect**.

4.3.3 Modify Pin Order Before Connections

When two instances on the Canvas need to communicate with each other such that the output pins of one instance drive the input pins of another instance and vice versa, some of the nets between the two instances may have to go around the instance to make the connections.

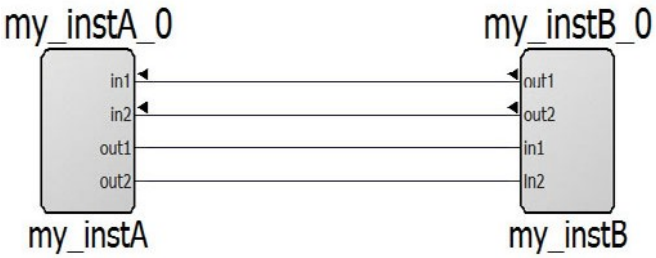
Figure 4-8. Connections between Two Instances with Regular Pin Order



However, if the pin order is modified such that the output pins of my_instance B are put on the left side and the input pins of Instance A are put on the right side of the instance, the net connection between the two instances are direct straight lines. The nets do not need to go around the instance.

See Modify Pin Order for details on how to modify the pin order.

Figure 4-9. Connections between Two Instances with Modified Pin Order



After the pin order is modified, input pins are identified by inward-pointing arrow heads and output pins are identified by outward pointing arrow heads. The arrow head helps you identify at a glance the direction of the pins (input/output) when they are not in the default locations. You can always hover the mouse over the pin to open the tooltip message to see the direction.

Note: Inout pins, by default, are put on the right side of the instance. They do not have arrow heads when their location is modified. Hover the mouse over the pin to open the tooltip message to see the direction of the pin (input/output/inout).

4.3.4 Splitting the Bus Before Connections

Before connections are made to a bus, the bus may need to be split for the following reasons:

- Different bits of the bus go to different parts of the design.
- Some bits of the bus need not to be connected and have attributes on them (output pins mark unused, tie to high/low or tie to constant).

The bus pin can be split into standard or custom slices:

- Standard slices are common, off-the-shelf slices available in the right-click menu of a selected bus pin or port.
- Custom slices are various slice/width combinations that are possible for the given bus width but not available from the off-the-shelf listings in the right-click drop-down menu. A special dialog is available to customize the slices.

Refer to Custom Slices.for details.

4.3.5 Search Design Objects to Connect

For a large design with many instances and pins, it may be difficult to find the pin/port/instance/net to make connections.

Two different ways are available for addressing this issue:

- Find window
- Net Filter in SmartDesign Canvas

4.3.5.1 Find Window

The Find window is outside the SmartDesign canvas, but can be used to easily find design objects to make net connections.

1. Open the SmartDesign component in the canvas.
2. Click **Edit > Find** in the Libero SoC menu to open the Find window at the bottom of the Libero main window. You can also press CTRL+F to open the Find window.
3. Select **Current Open SmartDesign** in the **Search** in drop-down menu.
4. Enter the type of design objects (Instance/Net/Pin) in the **Type** drop-down menu.
5. Enter the string of characters in the **Find** field.

6. Click **Find All**.
7. If there are matches, click the item in the **Search Results**.

The SmartDesign canvas will zoom in and highlight the design object. Zoom out far enough, with the design object still selected, to see the rest of the design and make the net connections.

4.3.5.2 Net Filter in SmartDesign Canvas

Use net filters in the SmartDesign Canvas to filter nets. Net filtering will filter out any nets that do not match the filter and make the SmartDesign Canvas less cluttered.

1. Open the SmartDesign component.
2. Enter a string in the **Filter Nets** field. By default, the filter field has the "* "character, which means all nets are shown (no filtering). Enter the net name or parts of the net name to filter the net you are interested in. To find all clock nets, you may want to put in *clk* in the field. Valid characters to enter in the field are:
   - "*" - a wild card that matches any number of characters
   - "?"- matches only one single character
   - [a-z, A-Z, 0-9] - matches any character inside the bracket
   - The comma "," character or the space character is used to delimit multiple matches. A filter field with the entry "clk,reset" or "clk reset" matches any net names with the "clk" or "reset" string.

Note: For any term entered in the filter field that contains no "*" ,"?", "[", "]", the tool adds the wild-card match "*" before and after each term. "clk reset" and "*clk* *reset*" give the same matches. Net filtering is case-insensitive.

To narrow down the filter, click the **Show Only BIF Nets** check box. Only Bus Interface (BIF) nets that match the filter are shown. BIF nets that do not match the filter and non-BIF nets are hidden.

BIF pins are identified by the  icon on the instance. BIF nets are nets connected to BIF pins.

4.4 Add or Modify Top-Level Ports

You can add ports to ports in your SmartDesign and rename the ports.

4.4.1 Add Prefixes to Bus Interface and Group Names on Top-level Ports

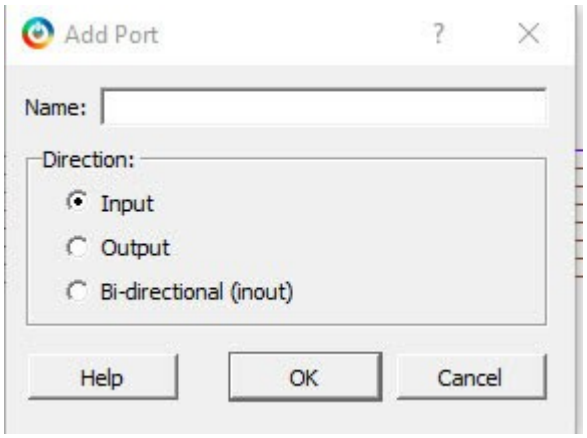
Bus Interfaces and Groups are comprised of other ports. On the top level, you can add prefixes to the group or bus interface port name to the sub-port names. To do so, right-click the group or bus interface port and choose **Prefix <name> to Port Names**.

4.4.2 Adding and Removing Ports

To add ports:

1. From the **SmartDesign** menu, choose **Add Port**. The Add Port dialog box appears (as shown in the following figure).

Figure 4-10. Add New Port Dialog Box



2. Specify the name of the port you want to add. You can specify a bus port by indicating the bus width directly into the name using brackets [ ], such as mybus[3:0].
3. Select the direction of the port.

To remove a port from the top level, right-click the port and choose **Delete**.

4.4.3 Modify Port

To rename a top-level port, right-click the top-level port and choose **Modify Top Level Port**. You can rename the port, change the bus width (if the port is a bus), and change the port direction.

Right-click a top-level port and choose **Modify Port** to change the name and/or direction (if available).

4.5 Invoke DRC on the Design

The DRC runs automatically when you generate your SmartDesign; the results appear in the **Reports** tab. You can also initiate a DRC by clicking on the **Design Rule Check** icon of the SmartDesign Canvas Icons.

For more information about running and understanding DRC results, see DRC Check.

4.6 Generate the Top-Level Component

The SmartDesign that has been created must now be generated. Generating a SmartDesign component may fail if there are any DRC errors. DRC errors must be corrected before you generate your SmartDesign top-level component.

If the ports of a sub-design have changed, then the parent SmartDesign component will be annotated with the icon  in the **Design Hierarchy** tab of the Design Explorer. This issue must also be corrected before you generate your SmartDesign top-level component.

Once there are no further DRC errors, the top-level component can be generated either recursively or non-recursively. Non-Recursive generation is enabled by default.

4.6.1 Recursive Generation

In recursive generation mode, the **Generate** button will try to generate all sub-design SmartDesigns, starting with depth. The parent SmartDesign will only be generated if all the sub-designs are generated successfully. To enable recursive generation, from the **Project** menu, choose **< Project > Preferences > Design Flow > Generate Recursively**.

4.6.2 Non-Recursive Generation

In the "non-recursive generation" mode, the **Generate** button will only attempt to generate the specified SmartDesign. This generation can be marked as successful even if a sub-design is ungenerated (either never attempted or unsuccessfully attempted). An ungenerated component will be annotated with the  icon in the **Design Hierarchy** tab of the Design Explorer.

5. Design Navigation Features

The SmartDesign Canvas provides the following navigational features:

- Expand/Fold Instance
- Magnified window

5.1 Expand and Fold Instance

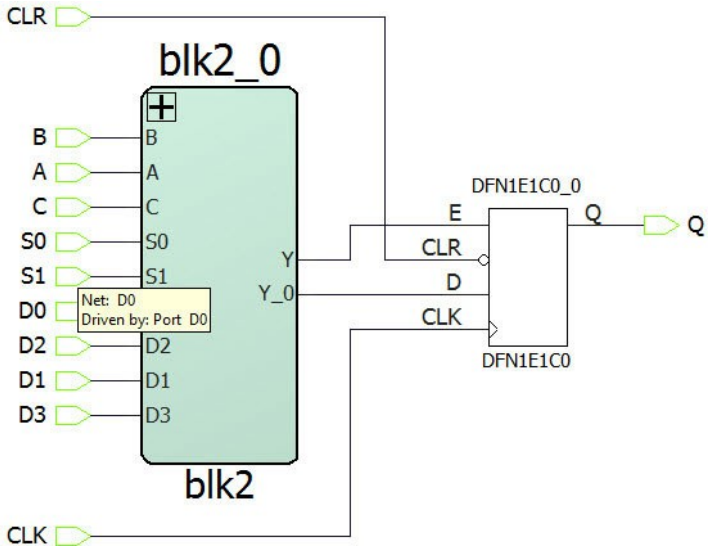
The Expand and Fold instance feature allow you to traverse up (Fold Instance) and down (Expand Instance) the design hierarchy of a SmartDesign component.

An instance of a SmartDesign component which contains lower level hierarchies can be expanded or folded in place. Expanded means traversing one level of hierarchy for viewing. Fold means the design is collapsed to the next higher level. The expand/fold instance is a read-only view of the component.

The Expand and Fold actions are executed in place. The result of the Expand and Fold Instance appears in the same location, relative to the rest of the design in the same window. No new window is opened.

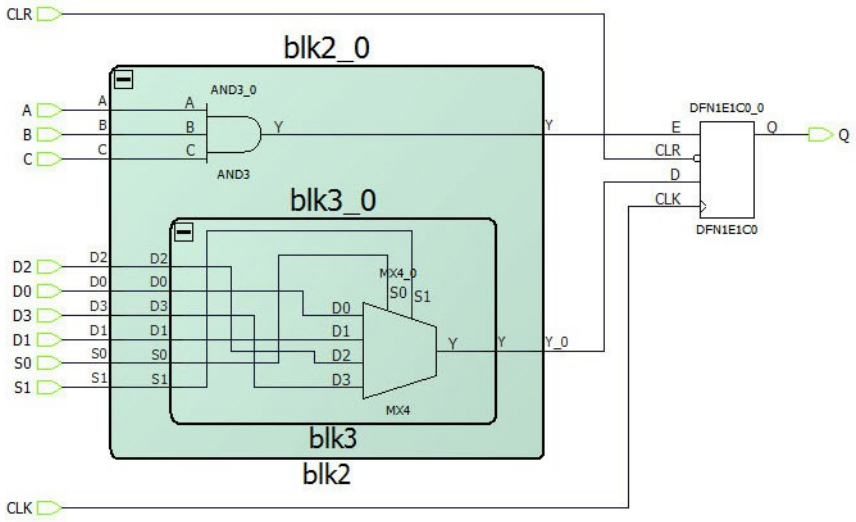
A folded design is indicated by a **+** sign at the top-left corner of the design. Clicking the **+** sign expands the folded design to the next lower levels of hierarchy. Alternatively, right-click the instance and select **Expand Inplace**.

Figure 5-1. Top-Level Design - Folded



An expanded design is indicated by a**-** sign at the top-left corner of the design. Clicking the **-** sign collapses the design hierarchy to the next higher level of hierarchy. Alternatively, right-click the instance and select **Fold Instance**.

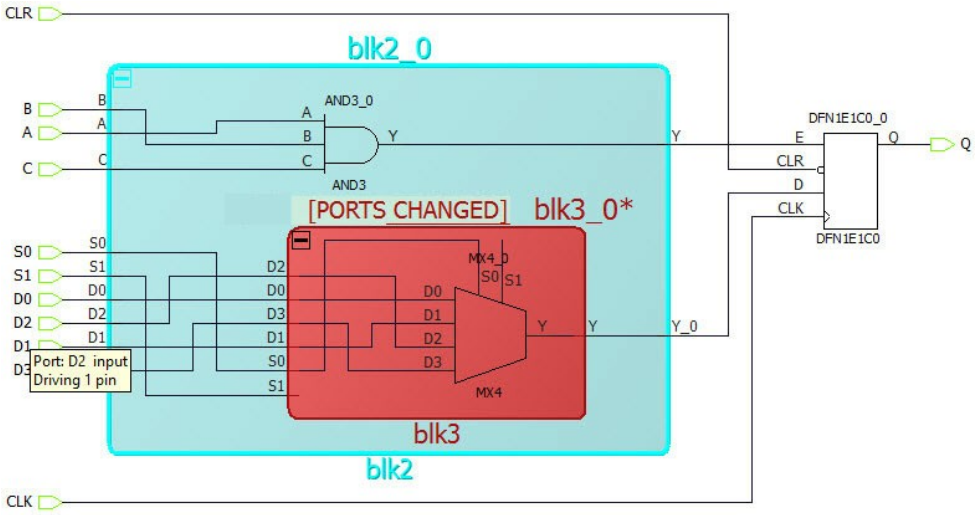
Figure 5-2. Top-Level Design - Expanded



When a lower level of the design hierarchy is modified, the parent block that instantiates the modified lower level is indicated by the asterisk (*) next to the name in the **SmartDesign Component Name** tab to indicate a change. If the modified block is two levels of hierarchy down, the design blocks of the next two higher levels have the asterisk (*) next to their names (in the **SmartDesign** tab) to indicate that the design component has changed. The modified block is highlighted in red and clearly identified as [PORTS CHANGED].

Note: The red highlight and the [PORTS CHANGED] identification appears only after the higher level block(s) is folded and expanded again to expose the changed lower level block.

Figure 5-3. Red Highlight and Changed_Module Identification



Note: Instead of [PORTS CHANGED], the error becomes [MISSING MODULE] if any one of the following conditions occurs:

- A lower level SmartDesign component instantiated in a higher level module/block has been deleted from the Project (Design Flow window > right-click **SmartDesign Component** and select **Delete from Project**).
- An IP core instantiated in a higher level module/blocks is not found or has been removed from the vault.

If the changed or missing module/block is at the lowest level of hierarchy, the **Update Component** and **Generate Components** steps must be repeated at every level of hierarchy above the changed module/block until the top-level hierarchy is reached, updated, and regenerated.

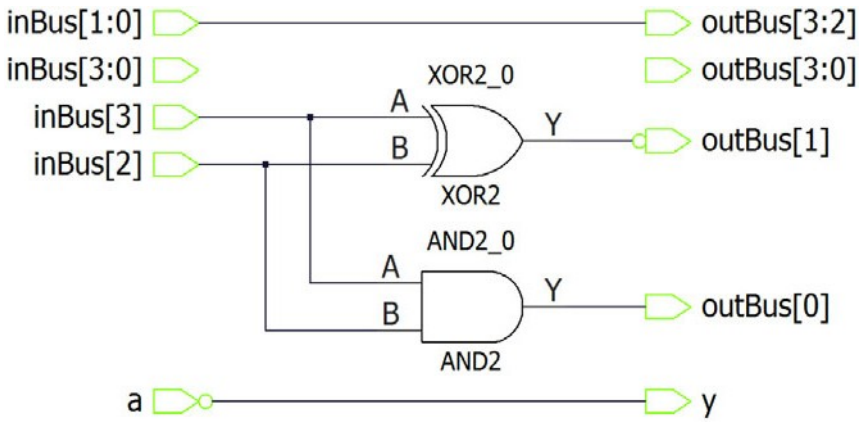
5.1.1 Expand Inplace and Low-Level Blocks

When a design component is expanded any place, SmartDesign reads in the current state of the low-level blocks after it expands. If changes are made to the low-level blocks (e.g., name changes, connectivity changes, addition or deletion of instances, pin order changes), the Expand Inplace view must be folded and expanded again before the Expanded Inplace view shows the update.

The top-level ports in the low-level blocks are shown differently in the Expanded Inplace view if these top- level ports are:

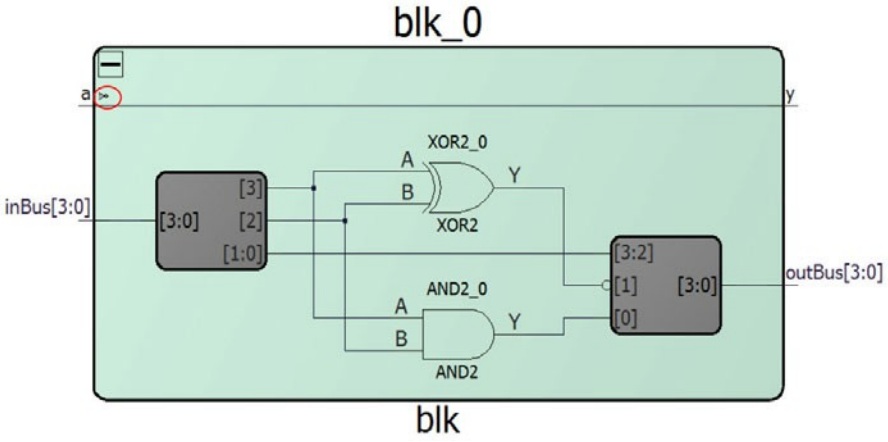
- Inverted
- Sliced

Figure 5-4. Low-Level Block View with Inverted Port and Sliced Port



At the Expanded Inplace view, for inverted ports, an inverter symbol is displayed next to the port (circled in the following figure). For the slice ports in this view, a slicer instance is inserted for each sliced bus.

Figure 5-5. Expanded Inplace View with Inverter Symbol and Slicer Ports



5.1.2 Component Regeneration

When the port list of the lower level block has changed, you need to:

1. Go to next higher level of the design hierarchy.
2. Right-click the lower level component and select **Update Component**.
3. Generate the higher level component.

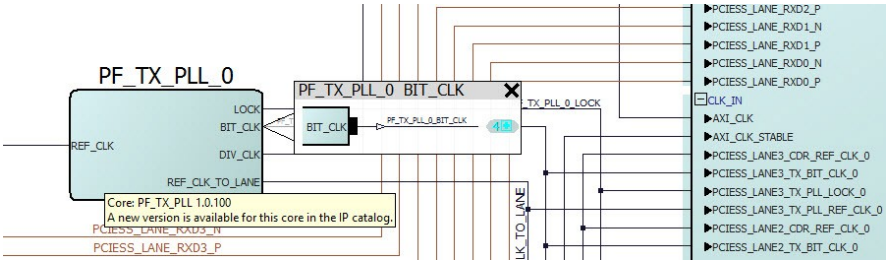
The red highlight and the [PORTS CHANGED] text disappear when the component update is successful.

5.2 Magnify Pin

This option is available to pins and ports only. Double-click a pin or a port or right-click and select **Magnify Pin** to access this option. The Magnify Pin window shows the specified pin/port's connections.

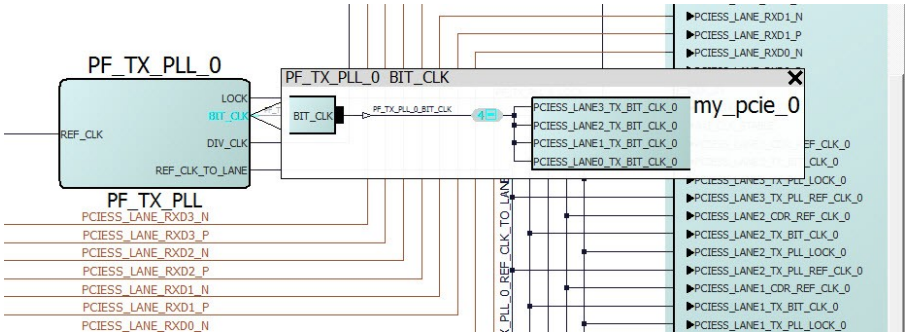
If the pin has a fanout of more than 1, the number 4 beside the + sign in the following figure shows the total fanout.

Figure 5-6. Magnify Pin Window



Click the + sign to see all the fanouts of the pin (see the following figure).

Figure 5-7. Magnify Pin Window with Fanout Expanded



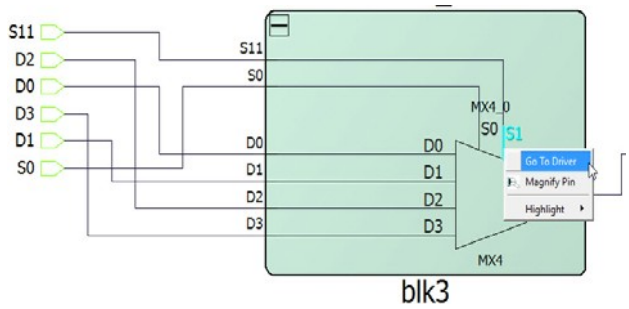
Double-clicking the net/pin/port/instance inside the Magnify window zooms into and selects the item. This makes it easy to navigate inside large designs.

To close the Magnify window, click the **Delete** (**X**) button on the Magnify window or press ESC on the keyboard.

5.3 Go To Driver

Right-click a net/pin/port and select **Go To Driver**. SmartDesign zooms in and selects the driver of the net/pin/port at the current level of hierarchy.

Figure 5-8. Go To Driver



6. Appendix A - FAQ

The collection of SmartDesign Frequently Asked Questions are useful for anyone new to SmartDesign. The questions are grouped as follows:

6.1 General Questions

1. What is SmartDesign?
2. How do I create my first SmartDesign?
3. What are the differences between the Old and New SmartDesign Canvas?
4. What do I need to do with my existing SmartDesign component when I switch to the new SmartDesign?

6.2 Instantiating into your SmartDesign

1. Instantiating Into Your SmartDesign
2. How do I create my first SmartDesign?
3. I have a block that I wrote in VHDL (or Verilog), can I use that in my SmartDesign?
4. My HDL module has Verilog parameters or VHDL generics declared, how can I configure those in SmartDesign?

6.3 Working in SmartDesign

1. How do I make manual connections?
2. How do I connect a pin to the top level?
3. Oops, I just made a connection mistake. How do I disconnect two pins?
4. I need to apply some simple 'glue' logic between my cores. How do I do that?
5. My logic is a bit more complex than inversion and tie offs - what else can I do?
6. How do I create a new top-level port for my design?
7. How do I rename one of my instances?
8. How do I rename my group pins?
9. I need to reconfigure one of my Cores, can I just double-click the instance?
10. I want more Canvas space to work with!

6.4 Working With Processor-Based Designs in SmartDesign

1. I need my peripheral at a specific address or slot.
2. How do I view the Memory Map of my design?
3. 6.11.3 How can I connect my own HDL block as a peripheral on the AMBA bus?
4. How do I start writing my application code for my design?
5. How do I simulate my processor design?

6.5 VHDL Construct Support in SmartDesign

1. What VHDL constructs do you support?
2. How can I import files with VHDL Special Types into SmartDesign?
3. What is the purpose of the mapping file?
4. Where will the mapping file meta.out be generated?
5. What are the VHDL special types that are not generated automatically?
6. What do I do if I am using VHDL types that are not generated automatically?

7. What is the meta.out file format?

6.6 Making the Design Look Nice

1. Can the tool automatically place my instances on the Canvas to make it look nice?
2. My design has a lot of connections, and the nets are making my design hard to read. What do I do?
3. My instance has too many pins on it; how can I minimize that?
4. Oops, I missed one pin that needs to be part of that group? How do I add a pin after I already have the group?
5. I have a pin that I don't want inside the group, how do I remove it?
6. How can I better see my design on the Canvas?

6.7 Generating the Design

1. Ok, I'm done connecting my design, how do I 'finish' it so that I can proceed to synthesis?
2. I get a message saying it's unable to generate my SmartDesign due to errors, what do I do? What is the Design Rules Check?
3. What does this error mean? How do I fix it?

6.8 General Questions

6.8.1 What is SmartDesign?

SmartDesign is a design entry tool. It is the first tool in the industry that can be used for designing System on a Chip designs, custom FPGA designs or a mixture of both types in the same design. A SmartDesign can be the entire FPGA design, part of a larger SmartDesign, or a user created IP that can be stored and reused multiple times. It is a simple, intuitive tool with powerful features that enables you to work at the abstraction level at which you are most comfortable.

It can connect blocks together from a variety of sources, verify your design for errors, manage your mem- ory map, and generate all the necessary files to allow you to simulate, synthesize, and compile your design.

6.8.2 How do I create my first SmartDesign?

In the Libero SoC Project Manager Design Flow window, under Create Design, double-click **Create SmartDesign**.

6.8.3 What are the differences between the old and new SmartDesign Canvas?

There are no major differences between the old and new SmartDesign canvas. The layout and features are similar.

6.8.4 What must I do with my current SmartDesign component when I switch to the new SmartDesign?

If you want to import SmartDesign components generated in the old canvas into a new SmartDesign canvas, import the .cxf file and the associated HDL files and IP cores and configure them. However, if you want to open a project in the new version, you must update project data.

6.9 Instantiating Into Your SmartDesign

6.9.1 Where is the list of cores that I can instantiate into my SmartDesign?

The list of available cores is displayed in the Catalog. This catalog contains all DirectCore IP, Design Block cores, and macros.

Drag and drop the core from the Catalog onto your SmartDesign Canvas. The Core Configurator opens. Configure the core and an instance of your Core appears on the Canvas.

6.9.2 Can I use a block that I wrote in VHDL (or Verilog) in my SmartDesign?

Yes, import your HDL file into the Project Manager (**File > Import Files**) to have your HDL module appear in the Project Manager Hierarchy. Then drag-and-drop it from the Design Hierarchy onto your SmartDesign Canvas.

6.9.3 My HDL module has Verilog parameters or VHDL Generics declared, how can I configure those in SmartDesign?

If your HDL module contains configurable parameters, you must create a 'core' from your HDL before using it in SmartDesign. Once your HDL module is in the Project Manager Design Hierarchy, right-click and choose **Create Core from HDL**. You can then add bus interfaces to your module if necessary. Once this is complete, you can drag your new HDL+ into the SmartDesign Canvas and configure your parameters by double-clicking it.

6.10 Working in SmartDesign

6.10.1 How do I make manual connections?

Connection tool is automatically activated and cross icon is displayed when hovering over port icon. When cross icon is displayed, you can left click and start dragging to the target.

- For the pins, connection tool is activated when hovering over pin icon or pin name.
- For the nets, connections tool is activated when hovering over any part of the net.

The connection tool will not activate when hovering over pin/port/net for the following cases:

- For the hierarchy views.
- Inside the configurator window.
- When "Zoom to Selected Area" mode is activated.
- When "Add Note" mode is activated.

6.10.2 How do I connect a pin to the top level?

Right-click the pin and choose **Promote to Top Level**.

For multiple pins, select all the pins you want to promote, right-click one of the pins, and choose **Promote to Top Level**. All your selected pins will be promoted to the top level.

6.10.3 I made a connection mistake. How do I disconnect two pins?

Use CTRL+Z to undo your last action. If you want to undo your 'undo', use redo (CTRL+Y). To disconnect pins you can:

- Right-click the pin you want to disconnect and choose **Disconnect**.
- Select the net and press the delete key.

6.10.4 How can I apply simple 'glue' logic between cores?

For basic inversion of pins, you can right-click a pin and choose **Invert**. An inverter will be placed at this pin when the design is generated. You can also right-click a pin and choose **Tie Low** or **Tie High** if you want to connect the pin to either GND or VCC.

To tie an input bus to a constant, right-click the bus and choose **Tie to Constant**. To mark an output pin as unused, right-click the pin and choose **Mark as Unused**.

To clear these, just right-click on the pin again and choose **Clear Attribute**.

6.10.5 My logic is more complex than inversion and tie offs - what else can I do?

You have full access to the library macros, including AND, OR, and XOR logic functions. These are located in the Catalog, listed under Macro Library. Drag the logic function onto your SmartDesign Canvas.

6.10.6 How do I create a new top-level port for my design?

Click the **Add Port** button in the Canvas toolbar

6.10.7 How do I rename one of my instances?

Right-click the instance on the Canvas and a dialog opens for you to rename the instance. The instance name is located directly above the instance on the Canvas.

6.10.8 How do I rename my top-level port?

Right-click the port you want to rename and choose **Modify/Rename**.

6.10.9 How do I rename my group pins?

Right-click the group pin you want to rename and choose **Rename**.

6.10.10 I need to reconfigure one of my Cores, can I just double-click the instance?

Yes.

6.10.11 I want more Canvas space to work with!

Maximize your workspace (CTRL+W), and your Canvas will maximize within the Project Manager. Press CTRL+W again if you need to see your Hierarchy or Catalog.

6.11 Working with Processor-Based/AMBA-Bus Designs

6.11.1 I need my peripheral at a specific address or slot

Right-click the Canvas and choose **View Memory Map** to invoke the View Memory Map dialog that enables you to set a peripheral to a specific address on the bus.

The bus core will show the slot numbers on the bus interface pins. These slot numbers correspond to a memory address on the bus.

Verify that your peripheral is mapped to the right bus address by viewing the Memory Map.

6.11.2 How do I view the Memory Map of my design?

Generate your project and open datasheet in Report View.

The memory map section will also show the memory details of each peripheral, including any memory mapped registers.

6.11.3 How can I connect my own HDL block as a peripheral on the AMBA bus?

SmartDesign supports automatic creation of data driven configurators based on HDL generics/parameters.

If your block has all the necessary signals to interface with the AMBA bus protocol (ex: address, data, control signals):

1. Right-click your custom HDL block and choose **Create Core from HDL**. The Libero SoC creates your core and asks if you want to add bus interfaces.
2. Click **Yes** to open the Edit Core Definition dialog box and add bus interfaces. Add the bus interfaces as necessary.
3. Click **OK** to continue.
   Now your instance has a proper AMBA bus interface on it. You can manually connect it to the bus or let Auto Connect find a compatible connection.

6.11.4 How do I start writing my application code for my design?

Libero SoC simplifies the embedded development process by automatically creating the workspace and project files for the Software IDE that you specify in the Tools profile.

Once you have generated your design, the firmware and workspace files will automatically be created. Click **Write Application Code** in the **Design Flow** tab and the Software IDE tool will open your design's workspace files.

6.11.5 How do I simulate my processor design?

SmartDesign automatically generates the necessary Bus Functional Model (BFM) scripts required to simulate your processor based design. A top-level testbench for your SmartDesign is generated automatically as well.

Create your processor design, generate it, and you will be able to simulate it in ModelSim.

6.12 VHDL Construct Support in SmartDesign

6.12.1 What VHDL constructs are supported?

VHDL types Record, Array, Array of Arrays, Integer, and Unsigned are supported on entity ports of imported VHDL files and treated as special types in Libero SoC.

6.12.2 How can I import files with VHDL Special Types into SmartDesign?

To work with a VHDL file with Special Types, you must:

1. Drag and drop the entity into SmartDesign and connect it just as you would with any other SmartDesign instance.
2. Generate the Mapping File (meta.out):
   - Navigate to the Design Hierarchy view, under the current SmartDesign.
   - Right-click every VHDL file or every top hierarchical file and choose **Create Mapping File** (VHDL).
3. Generate the SmartDesign.
4. Continue with the Libero SoC Design Flow steps (Synthesis, Simulation, etc.).
   If you try to Generate your SmartDesign without generating the Mapping File, the following error appears in the log window:

   ```
   Error: Select the HDL file in the Design Hierarchy and right-click the HDL file and
   choose Create Mapping File(VHDL) because at least one entity port is of type Array or
   Record.
   ```

   The above is reported only if the entity port is of type Record, Array, Array of Array, or Unsigned.

6.12.3 What is the purpose of the mapping file?

The mapping file contains the mapping information between the SmartDesign ports and original user-specified data types of ports in design files, and is used for type casting of signals during design generation.

6.12.4 Where will the mapping file meta.out be generated?

The file is generated in your $project_dir/hdl folder. This file will be used during SmartDesign generation.

6.12.5 What are the VHDL special types that are not generated automatically?

The following types are not automatically generated from the right-click menu option **Create Mapping File (VHDL)**:

- Array of array is not supported
- Array of record is not supported
- Enum in range of array is not supported.
- Constants are not supported.
- Buffer output ports are not supported

6.12.6 What do I do if I am using VHDL types that are not generated automatically?

You must manually write the mapping information in the meta.out file for unsupported types (types which are not generated automatically) in the prescribed format.

- Integer
- Unsigned
- Array and Array of Arrays
- Record

6.12.7 What is the meta.out file format?

6.12.7.1 meta.out File Format

MetaFile: MetaLibraryItem | MetaPackageList | MetaEntityList MetaLibraryItem: library <lib_name>

MetaPackageList: MetaPackageItem MetaPackageList

MetaPackageItem: package <package_name> MetaItemDeclarationList end
MetaItemDeclarationList: MetaItem MetaItemDeclarationList

MetaItem: (MetaRecordItem | MetaArrayOfArrayItem | MetaIntegerType | MetaArrayItem)
MetaIntegerItem: (MetaIntegerType | MetaIntegerWithoutType)

MetaIntegerType: integer <integer_name> NumericRange MetaIntegerWithoutType: integer NumericRange MetaUnsignedItem: unsigned <name> NumericRange

MetaArrayOfArrayItem: array_of_array < MetaArrayOfArrayName> Range [MetaArrayItem] end
MetaRecordItem: record <record_name> RecordItemList end

RecordItemList: RecordItem RecordItemList

RecordItem: <Inst_name> (MetaArrayOfArrayName | MetaIntegerItem | MetaUnsignedItem | MetaSim- pleArray)

MetaEnumuratedItem: enum <enum_name> (Item_name{,Item_name}) Range: [NumericRange | MetaEnumuratedItem]

NumericRange: lsd: msd

MetaArrayItem:array <array_name> [<record_name>] end MetaEntityList: entity <entity_name> MetaEntityItemList end MetaEntityItemList: MetaEntityItem MetaEntityItemList

MetaEntityItem: (RecordEntityItemList | IntegerEntityItemList | ArrayEntityItemList | ArrayOfArrayEntity- ItemList | UnsignedEntityItemList | BufferPortItemList)

RecordEntityItemList: RecordEntityItem RecordEntityItemList RecordEntityItem: (RecordNormalItem | RecordArrayOfArrayItemList)

RecordNormalItem: <user_port_name>. RecordItem <record_name>
RecordArrayOfArrayItemList: <record_port_name>[index]. RecordItem <record_name>
BufferPortItemList: BufferPortItem BufferPortItemList

BufferPortItem: buffer <buffer_name>

IntegerEntityItemList: IntegerEntityItem IntegerEntityItemList

IntegerEntityItem: <user_port_name> (MetaIntegerType | MetaIntegerWithoutType)
ArrayEntityItemList: ArrayEntityItem ArrayEntityItemList

ArrayEntityItem: <user_port_name> MetaArrayItem ArrayOfArrayEntityItemList: ArrayOfArrayEntityItem ArrayOfArrayEntityItemList ArrayOfArrayEntityItem: <port_name> < MetaArrayOfArrayName> UnsignedEntityItemList: UnsignedEntityItem UnsignedEntityItemList UnsignedEntityItem: <user_port_name> MetaUnsignedItem

6.12.7.2 Meta.out file Example

```
package record_pkg array array1

end

array_of_array array2 [3:0] end

record test

test_integer integer [0:127] test_array array1 test_array_of_array array2
test_unsigned unsigned [2:0] end

end

entity MUX mux_in1.test_std_logic test
```

```
mux_in1.test_std_logic_vector test mux_in1.test_integer test mux_in1.test_array
test mux_in1.test_array_of_array[0] test mux_in1.test_array_of_array[1]
test mux_in1.test_array_of_array[2] test mux_in1.test_array_of_array[3] test
mux_in1.test_unsigned test mux_in2.test_std_logic test mux_in2.test_std_logic_vector
test mux_in2.test_integer test mux_in2.test_array test mux_in2.test_array_of_array[0]
test mux_in2.test_array_of_array[1] test mux_in2.test_array_of_array[2] test
mux_in2.test_array_of_array[3] test mux_in2.test_unsigned test mux_out.test_std_logic
test mux_out.test_std_logic_vector test

mux_out.test_integer test mux_out.test_array test mux_out.test_array_of_array[0]
test mux_out.test_array_of_array[1] test mux_out.test_array_of_array[2] test
mux_out.test_array_of_array[3] test mux_out.test_unsigned test mux_array array1

end
```

6.13 Making the Design Look Nice

6.13.1 Can the tool automatically place my instances on the Canvas to make it look nice?

Yes. Right-click the Canvas white space and choose **Auto Arrange Instances**.

6.13.2 My design has a lot of connections, which make my design hard to read. What do I do?

You can disable the display of the nets in the toolbar (**Hide Nets**). This hides all the nets in your design automatically.

You can still see how pins are connected by selecting a net stub, the net will automatically be visible again as a RAST net. The tooltip also shows the drivers of the pin.

To show BIF Nets only, check the box at the far right of the SmartDesign Canvas window.

6.13.3 My instance has too many pins on it; how can I minimize that?

Group functional or unused pins together. For example, on the CoreInterrupt there are 8 FIQ- Source* and 32 IRQSource* pins, group these together since they are similar in functionality.

To group pins, select all the pins you want to group, then right-click one of the pins and choose **Add pins to group**.

If a pin is in a group, you are still able to use it and form connections with it. Expand the group to gain access to the pin. All Member pins of the group are shown.

Pins in a group can be hidden and collapsed into the group. If a pin (in a group) is connected to a net, then the pin cannot be hidden and collapsed into the group. Pins (in a group) can be hidden and col- lapsed if the pins are tie-off/marked unused/disconnected.

6.13.4 I missed one pin that needs to be part of that group? How do I add a pin after I already have the group?

Select the group, right-click the pin you want to add and select **Add Pin to Group**.

6.13.5 How do I remove a pin that I don't want inside the group?

Right-click the pin and choose **Ungroup Pin** or select the pin and press the Delete key on the keyboard.

6.13.6 How can I improve the readability of my design on the Canvas?

Use the zoom icons in the Canvas toolbar zoom in, zoom out, zoom to fit, and Zoom selection. You can also maximize your workspace with CTRL+W.

6.14 Generating the Design

6.14.1 Now that I am done connecting my design, how do I finish it so that I can proceed to synthesis?

In the SmartDesign Canvas toolbar, click the **Generate Component** icon.

6.14.2 I get a message that my SmarDesign cannot be generated due to errors. What do I do and what is the Design Rules Check?

The Design Rules Check is included in your Report View. It lists all the errors and warnings in your design, including unconnected input pins, required pin connections, configuration incompatibilities between cores, etc.

Errors are shown with a small red stop sign and must be corrected before you can generate. Warnings can be ignored.

For details Appendix C - DRC Check.

6.14.3 What does this error mean and how do I fix it?

Review the errors in Appendix C - DRC Check to correct DRC violations.

7. Appendix B - Glossary

Table 7-1. SmartDesign Glossary

Term	Description
BIF	Abbreviation for bus interface. Logical grouping of ports or pins that represent a single functional purpose. May contain both input and output, scalars, or buses. A bus interface is a specific mapping of a bus definition onto a component instance.
Bus	An array of scalar ports or pins, where all scalars have a common base name and have unique indexes in the bus.
Bus Definition	Defines the signals that comprise a bus interface. Includes which signals are present on a master, slave, or system interface, signal direction, width, default value, etc. A bus definition is not specific to a logic or design component but is a type or protocol.
Bus Interface Net	A connection between two or more compatible bus interfaces Canvas A visual representation of the breadboard for placing components and stitching the components to create a working design.
Driver	A driver is the origin of a signal on a net. The input and slave BIF ports of the top-level or the output and Master BIF ports from instances are drivers.
Instance	A block-like item with pins on either side of it. These are connected together to create designs. You may have multiple instances of a single component in your design. For each specific instance, you usually will have custom connections that differ from other instances of the same component.
Net	A wire that connects pins/ports in a design PAD The property of a port that must be connected to a design's top- level port. PAD ports will eventually be assigned to a package pin. In SmartDesign, these ports are automatically promoted to the top-level and cannot be modified.
Pins	Pins are the inputs/outputs/inouts of an instance that a net can be attached to for connection with other components in the design. By default, pins are placed on either the left (inputs) or the right side (outputs and inouts) of the instance. Pin order can be modified for a cleaner, less cluttered connection.
Port	A port is like a pin, but it is not attached to an instance. It acts as a way of letting a net connect to the outside world. A port has a direction (input, output, bi-directional) and may be referred to as a 'scalar port' to indicate that only a single unit-level signal is involved. In contrast, a bus interface on an instance may be considered as a non-scalar, composite port.
Macro	A type of very basic instance that typically has a special well- known shape associated with it. Inside of more complicated instances will be connected macros to do a more complicated function. Macros are specific to the technology family. Macros are listed in the Basic Macro group in the Catalog.
HDL File	A specially formatted text-file that describes the designs you create in a standard way.
Viewport	The rectangular view area of the canvas that is visible to you. You can move the viewport around on the canvas or zoom in/out to view your design. Showing the whole canvas would be too large in most cases.
Master BIF	Master Bus Interface. The bus interface that initiates a transaction (such as a read or write request) on a bus.
Slave BIF	Slave Bus Interface. The bus interface that responds to a transaction (such as a read or write request) on a bus.

.....continued

Term	Description
System Bus Interface	Interface that is neither master nor slave; enables specialized connections to a bus.
Slice	A slice is created from a bus. It is a portion of the bus and it contains some but not all scalar members of the bus.
Top-Level Port	An external interface connection to the outside world. Scalar if a 1-bit port, bus if a multiple-bit port or a Bus Interface (BIF). These are connected to the pad/package pins of the FPGA device.
Pin Group	A grouping of pins (scalar or bus) you create for easy connection or identification.

8. Appendix C - DRC Check

When SmartDesign components are generated, the tool automatically enforces DRCs. The component is generated if the check passes.

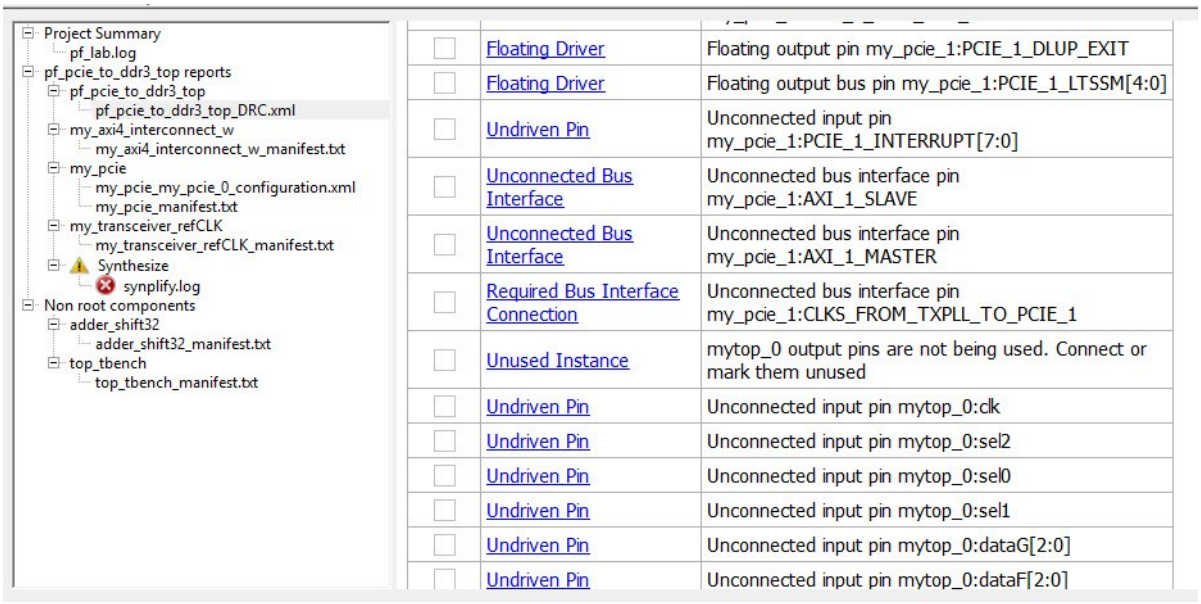
Alternatively, to invoke DRC checks without generating the component, click the **DRC check** icon in the toolbar.

To view the results of the DRC check, from the **Design** menu, choose **Reports**. The Report is named `<Design component>_DRC_xml` in the **Reports** tab. DRC errors are also reported in the Log/Message window.

Click the links on the DRC report. SmartDesign zooms in and highlights the design object that is the subject of the DRC violation.

You must correct all DRC errors before you can generate the SmartDesign component and continue with the design flow.

Figure 8-1. DRC Report



8.1 Message Types and Corrective Actions

The following are the more common DRC errors and the corrective actions you need to take.

Table 8-1. DRC Errors and Corrective Actions

DRC Error	Description
Unused Instance	You must remove this instance or connect at least one output pin to the rest of the design.
Out-of-date Instance	You must update the instance to reflect a change in the component referenced by this instance.
Undriven Pin	To correct the error you must connect the pin to a driver or change the state, i.e., tie low (GND), tie high (VCC), tie to Constant or marked unused.

.....continued

DRC Error	Description
Floating Driver	You can mark the pin unused if it is not going to be used in the current design. Pins marked unused are ignored by the Design Rules Check.
Unconnected Bus Interface	You must connect this bus interface to a compatible port because it is required connection.
Required Bus Interface Connection	You must connect this bus interface before you can generate the design. These are typically silicon connection rules.
Exceeded Allowable Instances for Core	Some IP cores can only be instantiated a certain number of times for legal design. For example, there can only be one CortexM1 or CoreMP7 in a design because of silicon limitations. You must remove the extra instances. This check is technology-dependent.
Incompatible Family Configuration	The instance is not configured to work with this project's Family setting. Either it is not supported by this family or you need to re-instantiate the core. This DRC check is family/technology-dependent.
No RTL License, No Obfuscated License, No Evaluation License	You do not have the proper license to generate this core. Contact Microchip SoC to obtain the necessary license.
No Top level Ports	There are no ports on the top level. To auto-connect top-level ports, right-click the Canvas and choose Auto-connect
Self-Instantiation	A component cannot instantiate itself-This is reported only in the Log/Message window.

9. Revision History

Revision	Date	Description
B	04/2021	The following changes are made in this revision: 3.4 View Memory Map: Updated the View Memory Map dialog box, added note, added information related to Downgrade option in Preferences window. 2.1 SmartDesign Icons:Updated section since Connection Mode icon is removed from the tool. 4.3 Make the Connections: Removed Section Connection Mode since it has been converted to inbuilt Connection Tool. 6.10.1 How do I make manual connections?: Updated the section with information related to the Connection Tool.
A	11/2020	Document converted to Microchip template. Initial Revision.

10. Microchip FPGA Technical Support

Microchip FPGA Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. This section provides information about contacting Microchip FPGA Products Group and using these support services.

10.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

10.2 Customer Technical Support

Microchip FPGA Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microchip FPGA Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

You can communicate your technical questions through our Web portal and receive answers back by email, fax, or phone. Also, if you have design problems, you can upload your design files to receive assistance. We constantly monitor the cases created from the web portal throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

Technical support can be reached at soc.microsemi.com/Portal/Default.aspx.

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), log in at soc.microsemi.com/Portal/Default.aspx, go to the **My Cases** tab, and select **Yes** in the ITAR drop-down list when creating a new case. For a complete list of ITAR-regulated Microchip FPGAs, visit the ITAR web page.

You can track technical cases online by going to My Cases.

10.3 Website

You can browse a variety of technical and non-technical information on the Microchip FPGA Products Group home page, at www.microsemi.com/soc.

10.4 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support at (https://soc.microsemi.com/Portal/Default.aspx) or contact a local sales office.

Visit About Us for sales office listings and corporate contacts.

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

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