Libero® SoC v2021.1

SmartTime Static Timing Analyzer (STA) User Guide

Introduction

SmartTime is a Libero® SoC interactive gate-level static timing analysis tool that allows you to visualize and identify timing issues in your designs. Using this tool, you can evaluate how close you are to meeting your timing requirements, create custom sets to track, set timing exceptions to obtain timing closure, and define cross-probe paths with other tools.

SmartTime is supported in SmartFusion®2, IGLOO®2, RTG4™, PolarFire®, and PolarFire SoC families.

Key SmartTime features allow you to:

- Perform complete timing analysis of your design to ensure that your designs meet all timing constraints and operate at the desired speed, with the appropriate amount of margin across all operating conditions.
- Browse through your design's various clock domains to examine the timing paths and identify those that violate your timing requirements.
- Create customizable timing reports.
- Navigate directly to the paths responsible for violating your timing requirements.

Note: Creating and editing timing constraints are handled in a separate Timing Constraints Editor. For more information, see the Timing Constraints Editor User Guide.

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1. About SmartTime

The following sections describe SmartTime functions.

1.1 Static Timing Analysis (STA)

Static timing analysis (STA) offers an efficient technique for identifying timing violations in your design and ensuring that it meets all your timing requirements. You can communicate timing requirements and timing exceptions to the system by setting timing constraints. A static timing analysis tool will then check and report setup and hold violations as well as violations on specific path requirements.

STA is particularly well suited for traditional synchronous designs. The main advantage of STA is that unlike dynamic simulation, it does not require input vectors. It covers all possible paths in the design and does all the above with relatively low run-time requirements.

The major disadvantage of STA is that the STA tools do not automatically detect false paths in their algorithms as it reports all possible paths, including false paths, in the design. False paths are timing paths in the design that do not propagate a signal. To get a true and useful timing analysis, you need to identify those false paths, if any, as false path constraints to the STA tool and exclude them from timing considerations.

The SmartTime user interface provides efficient, user-friendly ways to define these critical false paths.

1.2 Timing Constraints

SmartTime supports a range of timing constraints to provide useful analysis and efficient timing-driven layout.

1.3 Timing Analysis

SmartTime provides a selection of analysis types that allow you to:

- Find the minimum clock period/highest frequency that does not result in a timing violations
- Identify paths with timing violations
- Analyze delays of paths that have no timing constraints
- Perform inter-clock domain timing verification
- Perform maximum and minimum delay analysis for setup and hold checks

To improve the accuracy of the results, SmartTime evaluates clock skew during timing analysis by computing individual clock insertion delays for each register.

SmartTime checks the timing requirements for violations while evaluating timing exceptions such as multicycle or false paths.

1.4 SmartTime and Place and Route

Libero SoC Place and Route uses SmartTime STA during timing-driven place-and-route operations run in the background. As a result, your analysis and place and route constraints are always consistent.

1.5 Timing Reports

SmartTime provides robust reporting capabilities that allow you to generate the following report files:

- Timing Report for Max and Min Delay Analysis
- Timing Violations Report for Max and Min Delay Analysis
- Bottleneck Report
- Constraints Coverage Report

- Combinational Loop Report

1.6 Cross-probing into Chip Planner

From SmartTime, you can select a design object and cross-probe the same design object in Chip Planner.

Design objects that can be cross-probed from SmartTime to Chip Planner include:

- Ports
- Macros
- Timing paths

1.7 Cross-probing into Constraints Editor

From SmartTime, you can cross-probe into the Constraints Editor. The Constraints Editor must be running for cross-probing to work.

For more information, see 9.9.3 Cross-probing from SmartTime to Chip Planner.

2. Design Flows with SmartTime

You can access SmartTime in Libero SoC during the following design implementation phases:

- During Place and Route – when you select timing-driven place-and-route, SmartTime runs in the background to provide accurate timing information.
- After Place and Route – run SmartTime to perform post-layout timing analysis and adjust timing constraints. In the Libero SoC Design Flow window, expand **Implement Design > Verify Post-Layout Implementation** and then either:
  - Double-click **Verify Timing** to generate Timing Reports.
  - Right-click **Open SmartTime > Open Interactively** to run SmartTime.
- During Back-Annotation – SmartTime runs in the background to generate the SDF file for timing simulation.

You can also run SmartTime to generate Timing Reports, regardless of which design implementation phase you are in.

For more information about Place and Route and Back-Annotation, see the Libero SoC User Guide.

3. Starting and Closing SmartTime

You must complete Place and Route for your design before using SmartTime interactively. Otherwise, Libero SoC completes that phase before starting SmartTime.
To open SmartTime interactively:

1. Select **Implement Design > Verify Post Layout Implementation**.
2. Right-click **Open SmartTime** and select **Open Interactively**.
   SmartTime reads your design and displays post- or pre-layout timing information.
   To close SmartTime, choose **Exit** from the **File** menu.

4. Configuring SmartTime Settings

The SmartTime Options dialog box allows you to change general, analysis, and advanced settings.

4.1 Configuring SmartTime General Settings

To configure **General** settings in the SmartTime Options dialog box:

1. From the SmartTime Maximum/Minimum Delay Analysis View window, choose **Tools > Options**. The SmartTime Options dialog box appears.

Figure 4-1. SmartTime Options Dialog Box - General Settings for SmartFusion®2, IGLOO®2, and RTG4™

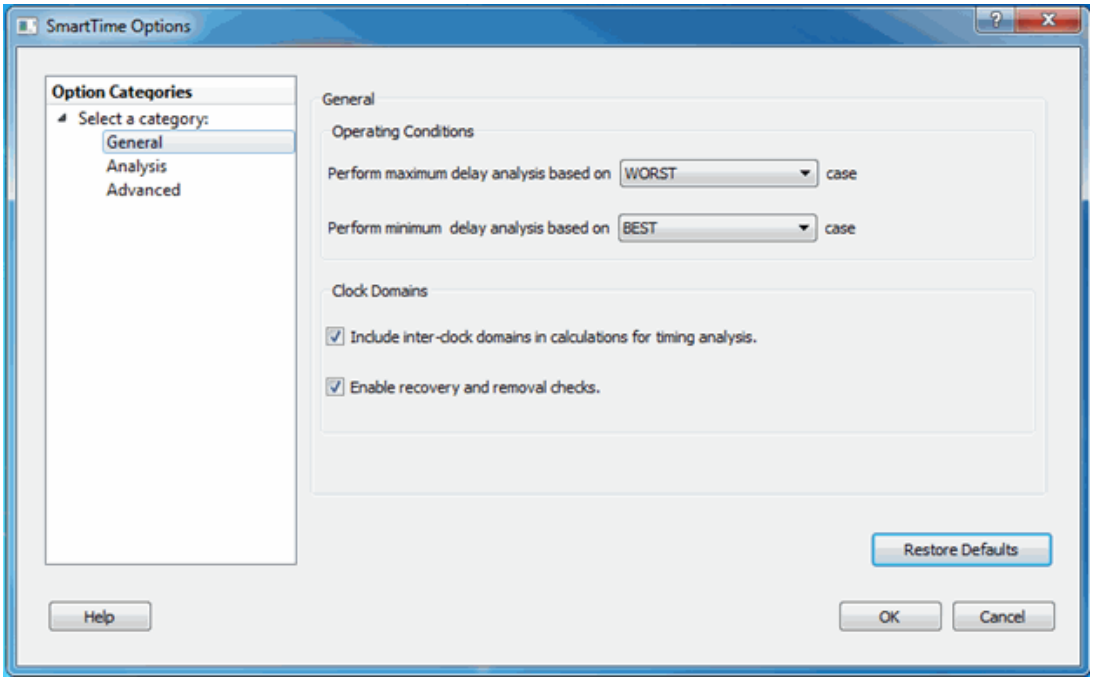
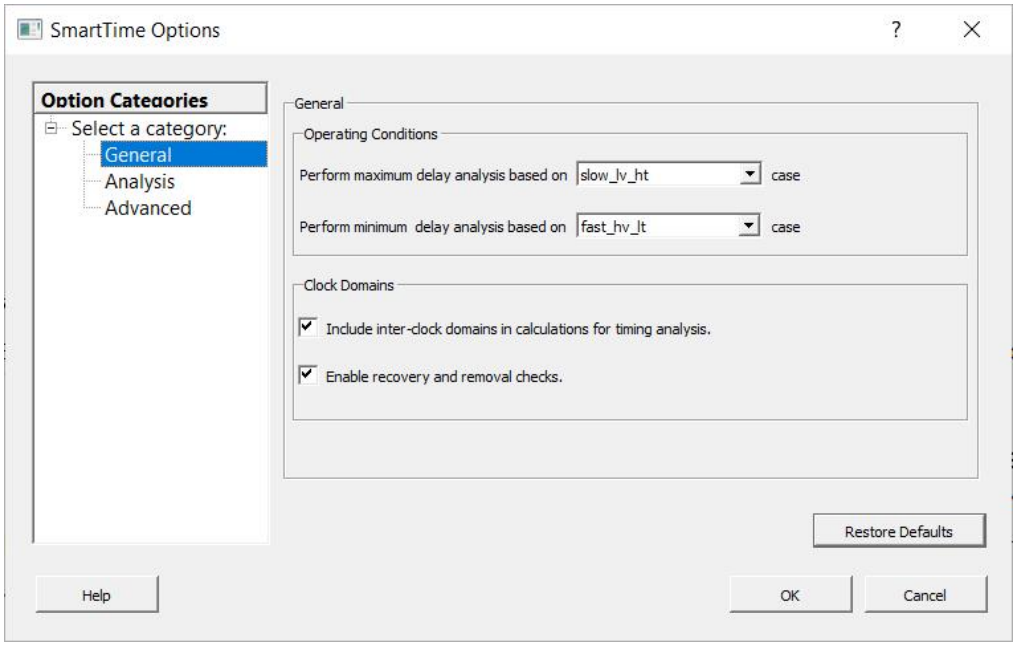


Figure 4-2. SmartTime Options Dialog Box - General Settings for PolarFire



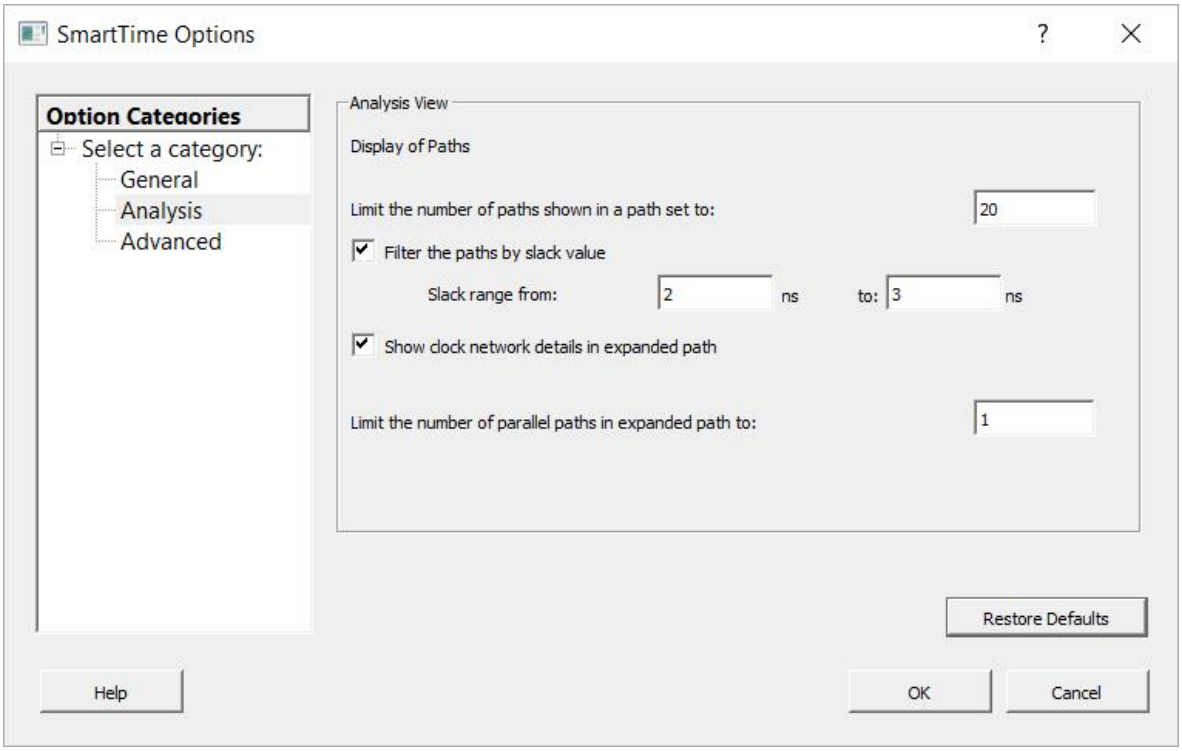
2. In the **General** category, select the settings for the operating conditions. SmartTime performs maximum or minimum delay analysis based on the best, typical, or worst case.
3. Specify whether you want SmartTime to use inter-clock domains in calculations for timing analysis.
4. To revert the **General** settings to their default value, click **Restore Defaults**.
5. Change **Analysis** and **Advanced** settings as necessary.
6. When finished, click **OK**.

4.2 Configuring SmartTime Analysis Settings

To configure **Analysis** settings in the SmartTime Options dialog box:

1. From the SmartTime Maximum/Minimum Delay Analysis View window, choose **Tools > Options**. The SmartTime Options dialog box appears.
2. In the left pane, click **Analysis**.

Figure 4-3. SmartTime Options Dialog Box - Analysis Settings



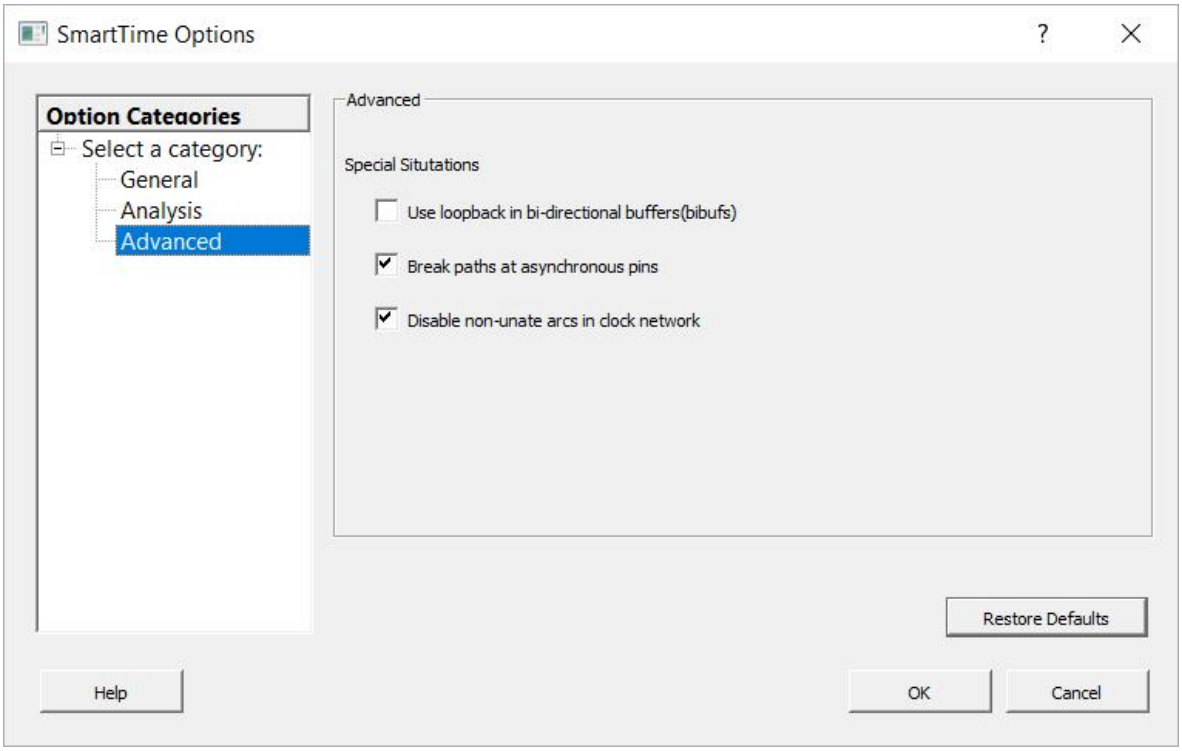
3. Enter a number greater than 1 to specify the maximum number of paths to include in a path set during timing analysis.
4. Check or uncheck whether to filter the paths by slack value. If you check this box, specify the slack range between the minimum slack and maximum slack.
5. Check or uncheck whether to include clock network details.
6. To specify the number of parallel paths in the expanded path, enter a number greater than 1.
7. To revert the **Analysis** settings to their default value, click **Restore Defaults**.
8. Change **General** and **Advanced** settings as necessary.
9. When finished, click **OK**.

4.3 Configuring SmartTime Advanced Settings

To configure **Advanced** settings in the SmartTime Options dialog box:

1. From the SmartTime Maximum/Minimum Delay Analysis View window, choose **Tools > Options**. The SmartTime Options dialog box appears.
2. In the left pane, click **Advanced**.

Figure 4-4. SmartTime Options Dialog Box - Advanced Settings



3. Specify whether to use loopback in bidirectional buffers (bibufs) and/or break paths at asynchronous pins. The specify whether to disable non-unate arcs in the clockpath.
4. To revert the **Advanced** settings to their default value, click **Restore Defaults**.
5. Change **General** and **Analysis** settings as necessary.
6. When finished, click **OK**.

5. SmartTime Toolbar

The SmartTime toolbar contains icons for constraining or analyzing designs. Tool tips are available for each icon.

Table 5-1. SmartTime Toolbar Icons

Icon	Description
	Saves the changes.
	Undoes previous changes.
	Redoes previous changes.
	Opens the maximum delay analysis view.
	Opens the minimum delay analysis view.
	Opens the manage clock domains manager.
	Opens the path set manager.
	Recalculates all analyses.

6. SmartTime Timing Analyzer

The following sections describe the SmartTime Timing Analyzer functions.

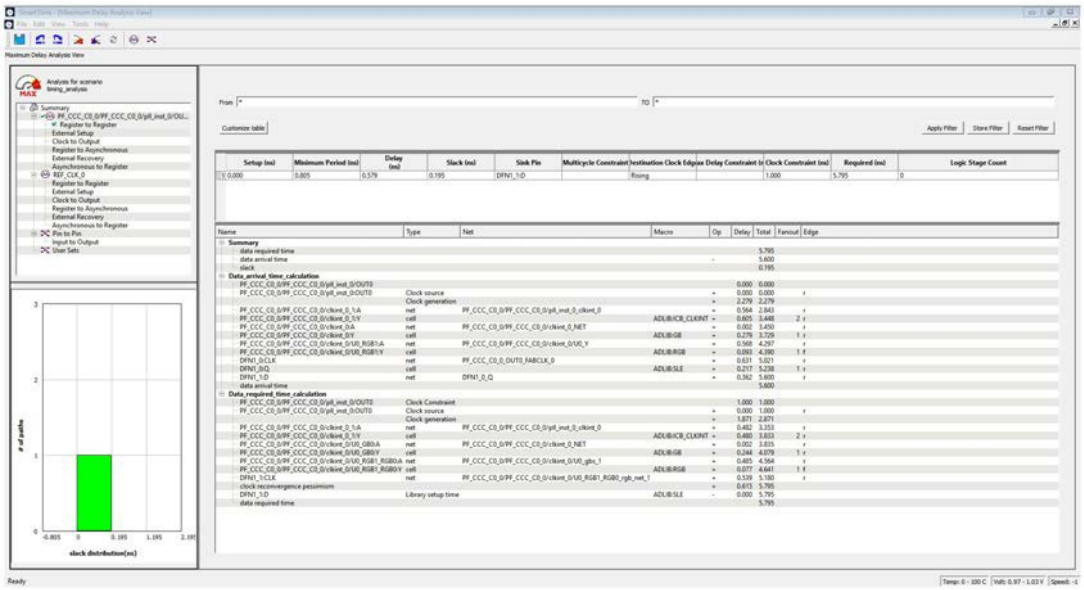
6.1 SmartTime Analyzer Components

SmartTime Timing Analyzer consists of the following components:

- Domain Browser: allows you to perform your timing analysis on a per domain basis.
- Path List: shows paths in a specific set within a given domain sorted by slack.
- Path Details: shows detailed timing analysis of a selected path in the paths list.
- Analysis View Filter: allows you to filter the content of the paths list.
- Path Slack Histogram: when a set is selected in the Domain Browser, Path Slack Histogram shows a distribution of the path slacks for that set. Selecting one or multiple bars in the Path Slack Histogram filters the paths shown in the Path List.

The following figure shows the SmartTime Timing Analyzer Components. You can copy and change the resolution and number of bars of the chart from the right-click menu.

Figure 6-1. SmartTime Timing Analyzer Components



6.2 Analyzing Your Design

The timing engine uses the following priorities when analyzing paths and calculating slack:

1. False path
2. Max/Min delay
3. Multi-cycle path
4. Clock

If multiple constraints of the same priority apply to a path, the timing engine uses the tightest constraint.

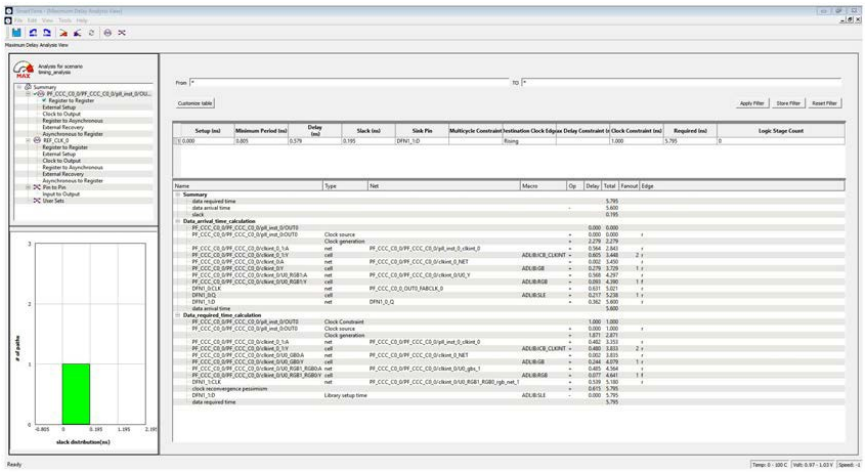
You can perform two types of timing analysis:

- Maximum Delay Analysis
- Minimum Delay Analysis

To perform the basic timing analysis, use one of the following methods to open the Timing Analysis View:

- From the SmartTime **Tools** menu, choose **Timing Maximum Delay Analysis** or **Minimum Delay Analysis**.
- From the SmartTime window, click the  icon for Maximum Delay Analysis or the  icon for Minimum Delay Analysis.

Note: When you open the Timing Analyzer from Designer, the Maximum Delay Analysis window appears by default.



6.3 Maximum Delay Analysis View

To enter Maximum Delay Analysis View:

1. In the Domain Browser, select the clock domain. Clock domains with a ✔ indicate that the timing requirements in these domains were met. Clock domains with an x indicate that there are violations within these domains. **Paths List** shows the timing paths sorted by slack. The path with the lowest slack (biggest violation) is at the top of the list.
2. Select the path you want to view.
   Path Details below the **Paths List** shows detailed information about how the slack was computed by detailing the arrival time and required time calculation. If a path is violated, the slack is negative and shown in red.
3. To display a separate view that includes the path details and schematic, double-click the path.
4. Repeat this procedure as necessary.

   Note: If the minimum pulse width of one element on the critical path limits the maximum frequency for the clock, an icon for the clock name appears in the **Summary List**. Clicking the icon displays the name of the pin that limits the clock frequency.

6.4 Managing Clock Domains

In SmartTime, timing paths are organized by clock domains.

By default, SmartTime displays domains with explicit clocks. Each clock domain includes at least three path sets:

- Register to Register
- External Setup (in the Maximum Analysis View) or External Hold (in the Minimum Analysis View)
- Clock to Out

You must select a path set to display a list of paths in that specific set.

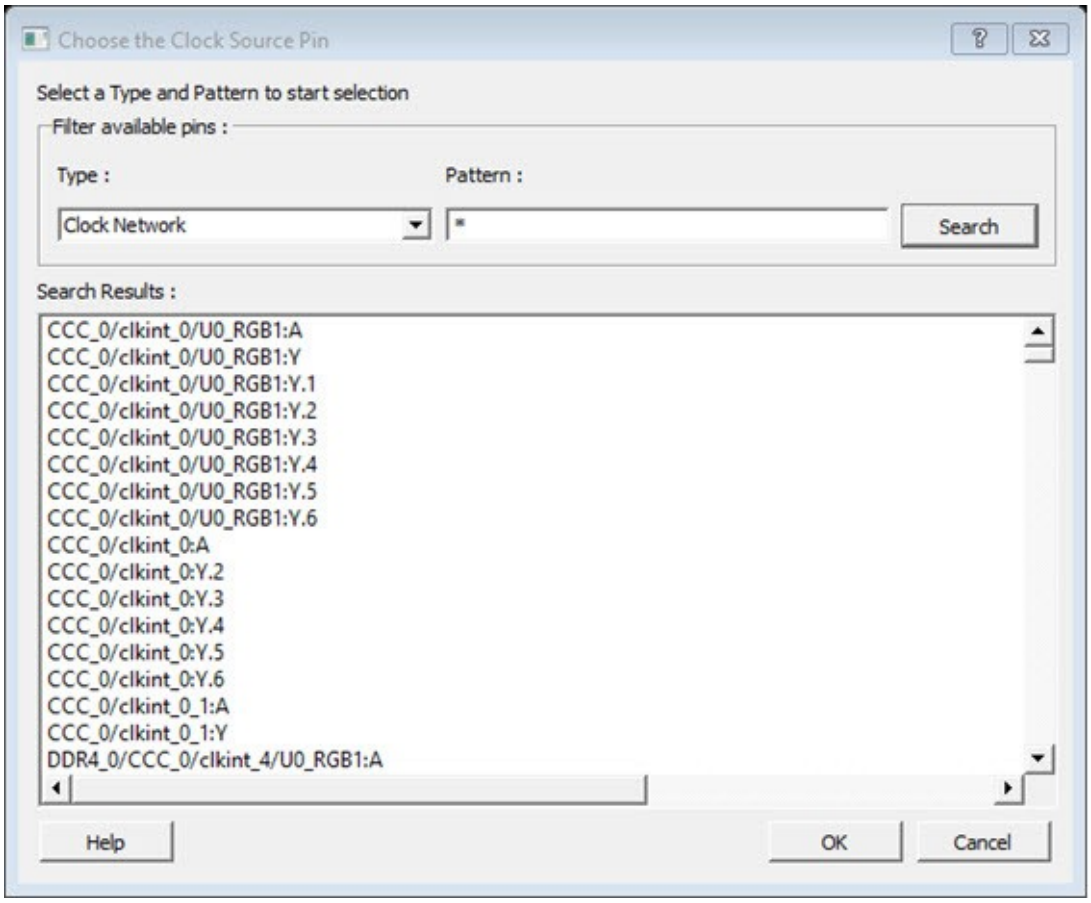
To manage the clock domains:

1. Right-click anywhere in the Domain Browser and choose **Manage Clock Domains**.
   The Manage Clock Domains dialog box appears.

Tip: You can click the icon in the SmartTime window bar to display the Manage Clock Domains dialog box.

2. To add a new domain, select a clock domain from the **Available clock domains** list and click **Add**. To add a non-explicit clock domain, click **New Clock**.
   The Choose the Clock Source Pin dialog box appears, and you can select the clock source pin. You can choose to filter the available pins and search.

Figure 6-2. Choose the Clock Source Pin Dialog Box



3. To remove a displayed domain, select a clock domain from the **Show the clock domains in this order** list and click **Remove**.
4. To change the display order in the Domain Browser, select a clock domain from the **Show the clock domains in this order** list, and then use **Move Up** or **Move Down** to change the order in the list.
5. Click **OK**.
   SmartTime updates the Domain Browser based on your specifications. If you added a new clock domain, it includes at least three path sets, as mentioned above.

6.5 Managing Path Sets

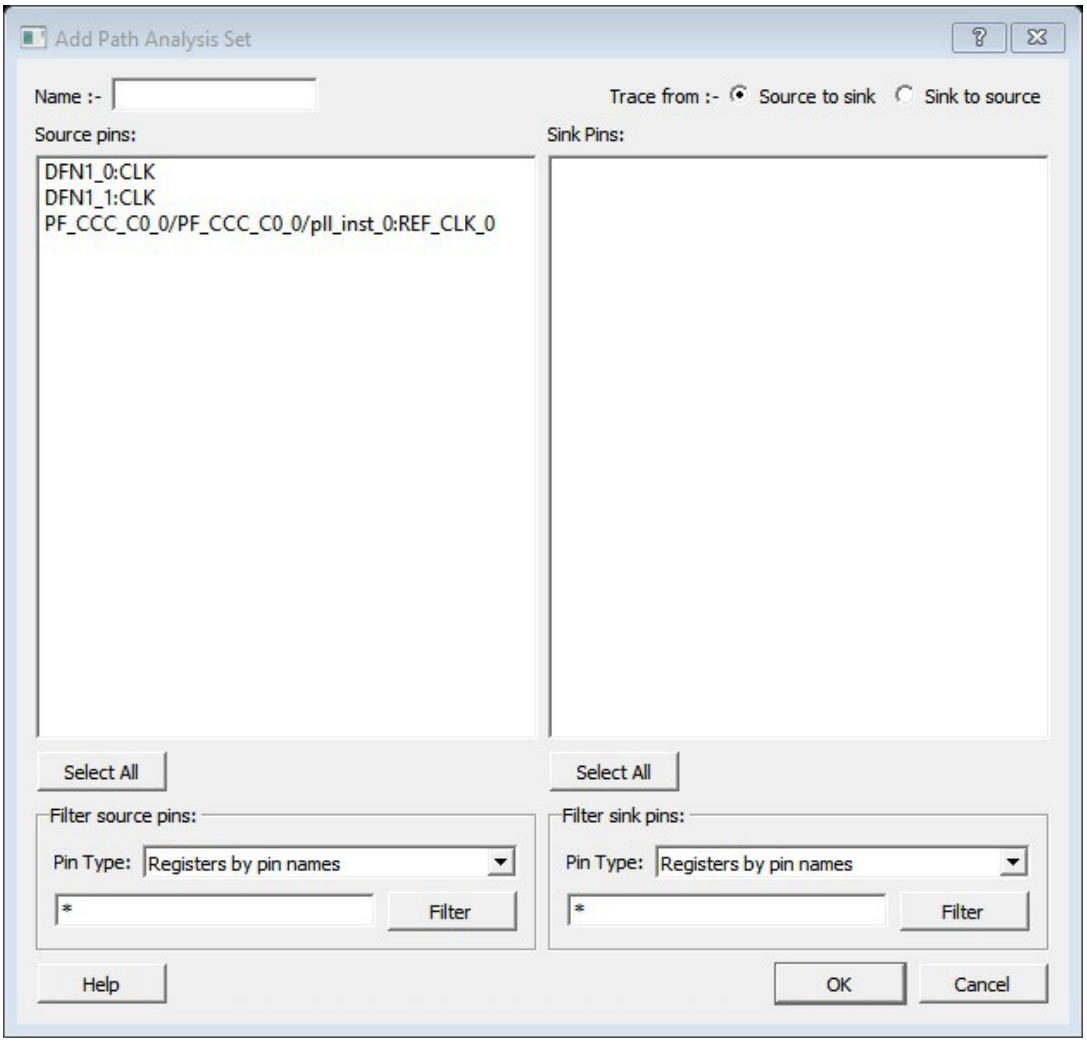
You can create and manage custom path sets for timing analysis and tracking purposes.

Path sets appear below **Custom Path Sets** at the bottom of the Domain Browser.
To manage path sets:

1. Right-click anywhere in the Domain Browser and choose **Add Set**.
   The Add Path Analysis Set Dialog Box appears.

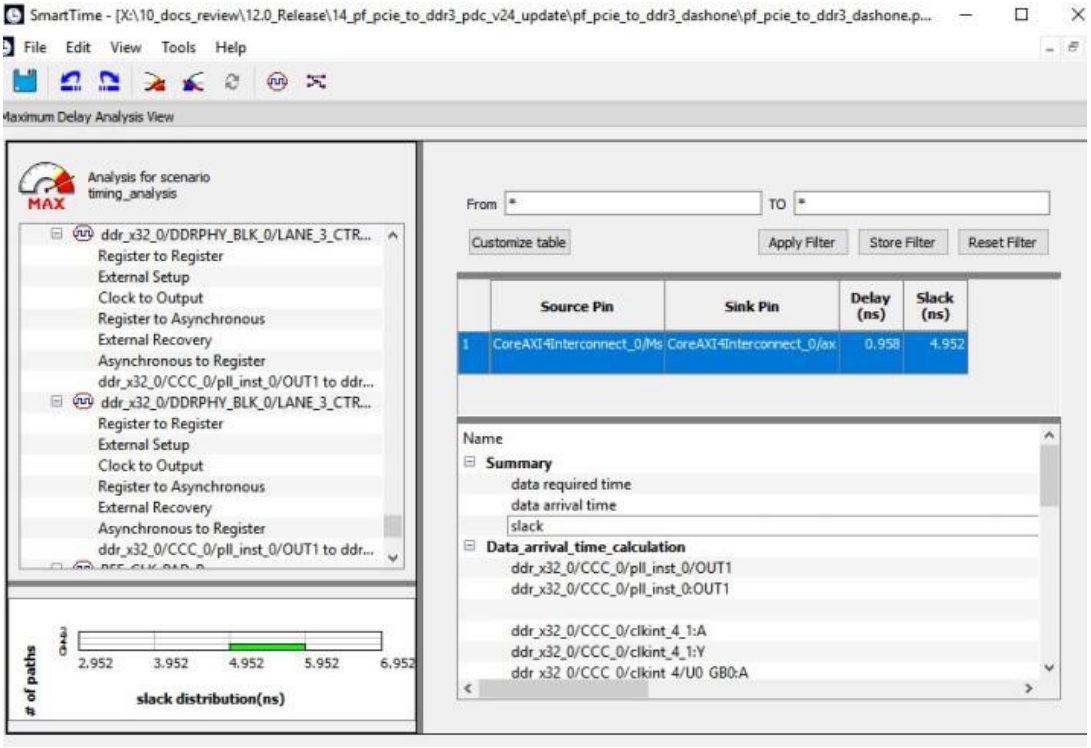
Tip: You can click the icon in the SmartTime window bar to display the Add Path Analysis Set dialog box.

Figure 6-3. Add Path Analysis Set Dialog Box



2. Enter a name for the path set.
3. Select the source and sink pins. You can use the filters to control the type of pins displayed.
4. Click **OK**.
   The new path set appears below **User Sets** in the Domain Browser.

Figure 6-4. Updated Domain Browser with User Sets



5. To rename a path:
   a) Select the path set from **User Sets** in the Domain Browser.
   b) Right-click the set you want to rename, and then choose **Rename Set** from the right-click menu.
   c) Edit the name directly in the Domain Browser.
6. To remove a path:
   a) Select the path set from **User Sets** in the Domain Browser.
   b) Right-click the set you want to delete, and then choose **Delete Set** from the right-click menu.

6.6 Displaying Path List Timing Information

Path List in the Timing Analysis View shows the timing information required to verify the timing requirements and identify violating paths. The Path List is organized in a grid where each row represents a timing path with the corresponding timing information displayed in columns. Timing information is customizable, allowing you to add or remove columns for each type of set.

By default, each type of set displays the following subset of columns:

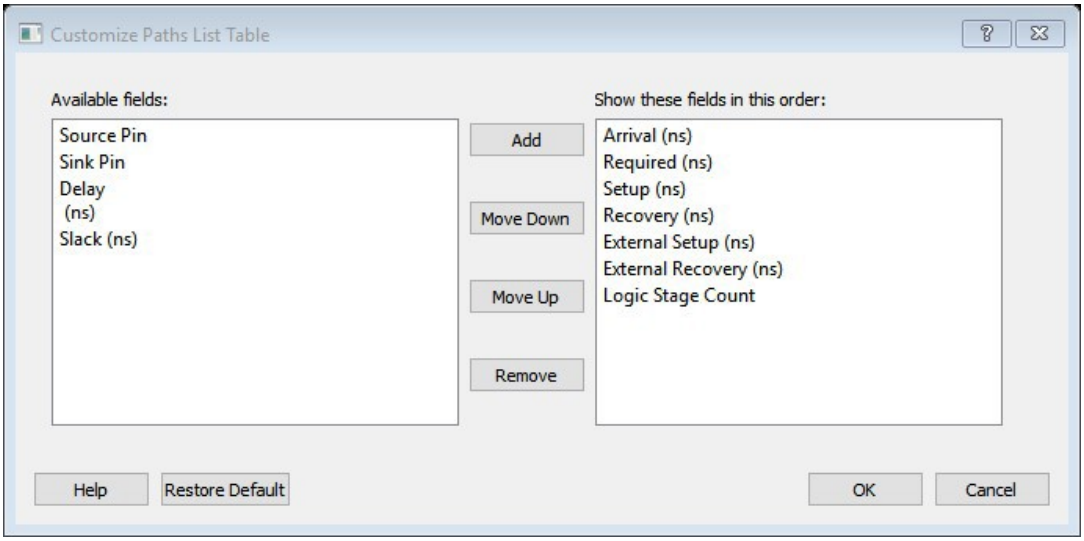
- Register to Register: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, Setup, Minimum Period, and Skew.
- External Setup: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, Setup, and External Setup.
- Clock to Out: Source Pin, Sink Pin, Delay, Slack, Arrival, Required, and Clock to Out.
- Input to Output: Source Pin, Sink Pin, Delay, and Slack.
- Custom Path Sets: Source Pin, Sink Pin, Delay, and Slack. You can add the following columns for each type of set:
  – Register to Register: Clock, Source Clock Edge, Destination Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Maximum Delay Constraint, and Multicycle Constraint.
  – External Setup: Clock, Destination Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Input Delay Constraint, Required External Setup, Maximum Delay Constraint, and Multicycle Constraint.
  – Clock to Out: Clock, Source Clock Edge, Logic Stage Count, Max Fanout, Clock Constraint, Output Delay Constraint, Required Maximum Clock to Out, Maximum Delay Constraint, and Multicycle Constraint.

– Input to Output: Arrival, Required, Setup, Hold, Logic Stage Count, and Max Fanout.
– Custom Path Sets

To customize the set of timing information in the Path List:

1. Choose **Customize table** on the top-left corner of path list to open the Customize Paths List Table dialog box.

Figure 6-5. Customize Paths List Table Dialog Box



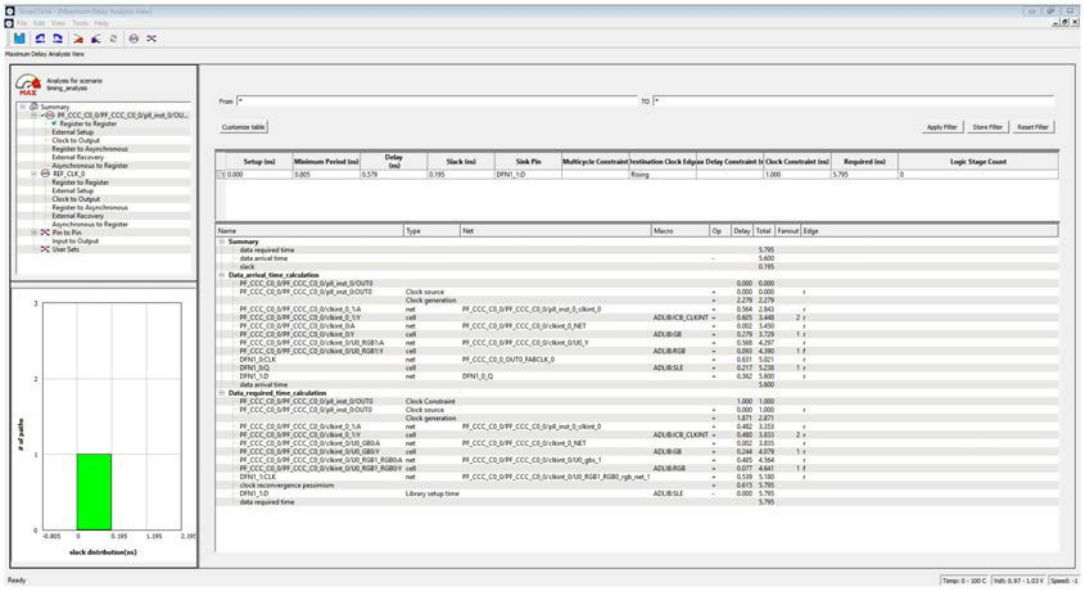
2. To add one or more columns, select the fields to add from the **Available fields** list and click **Add**.
3. To remove one or more columns, select the fields to remove from the **Show these fields in this order** list, and click **Remove**.
4. To change the order in which the fields appear, select fields in the **Show these fields in this order** list and click **Move Up** or **Move Down**.
5. Click **OK** to add or remove the selected columns.
   SmartTime updates the Timing Analysis View.

6.7 Displaying Expanded Path Timing Information

SmartTime displays the list of paths and path details for all parallel paths.

The Path Details grid displays the path details for all parallel paths. The Path List displays all parallel paths in your design.

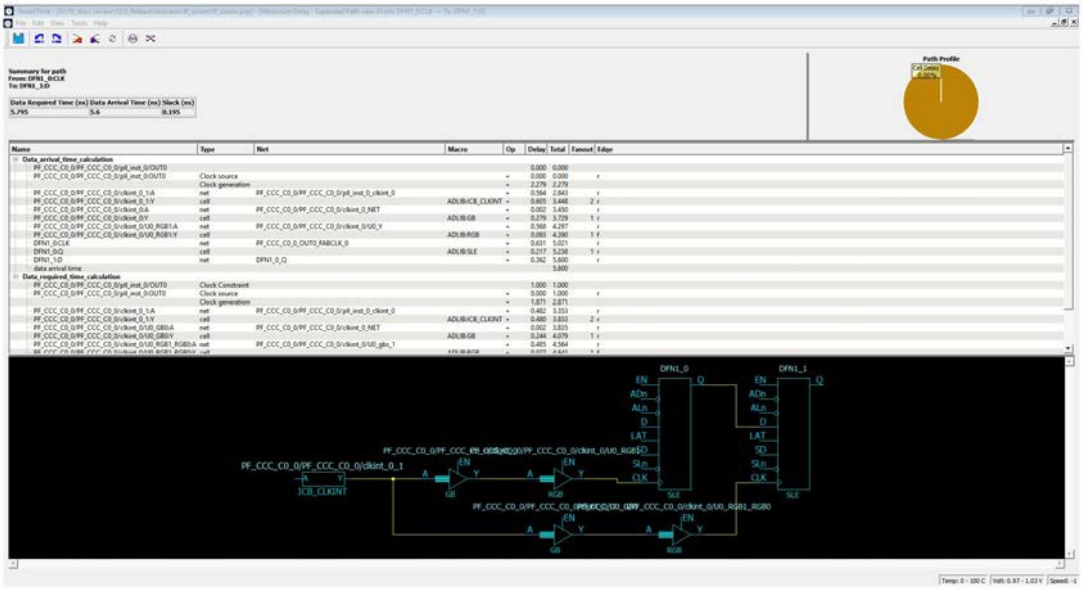
Figure 6-6. Path List View



To display the Expanded Path View:

1. From the Path List, double-click the path, or right-click a path and select **expand selected paths**.
2. From the Expanded Path View, double-click the path, or right-click the path and select **expand path**.

Figure 6-7. Expanded Path View



The Expanded Path Summary provides a summary of all parallel paths for the selected path. The Path Profile chart shows the percentage of time taken by cells and nets for the selected path. If no parallel path is selected in this view, the Path Profile shows the percentage for all paths. By default, SmartTime shows only one path for each Expanded Path. To change this default, use the SmartTime Options dialog box.

The Expanded Path View includes a schematic of the path and a path profile chart for the paths selected in the Expanded Path Summary.

6.8 Using Filters

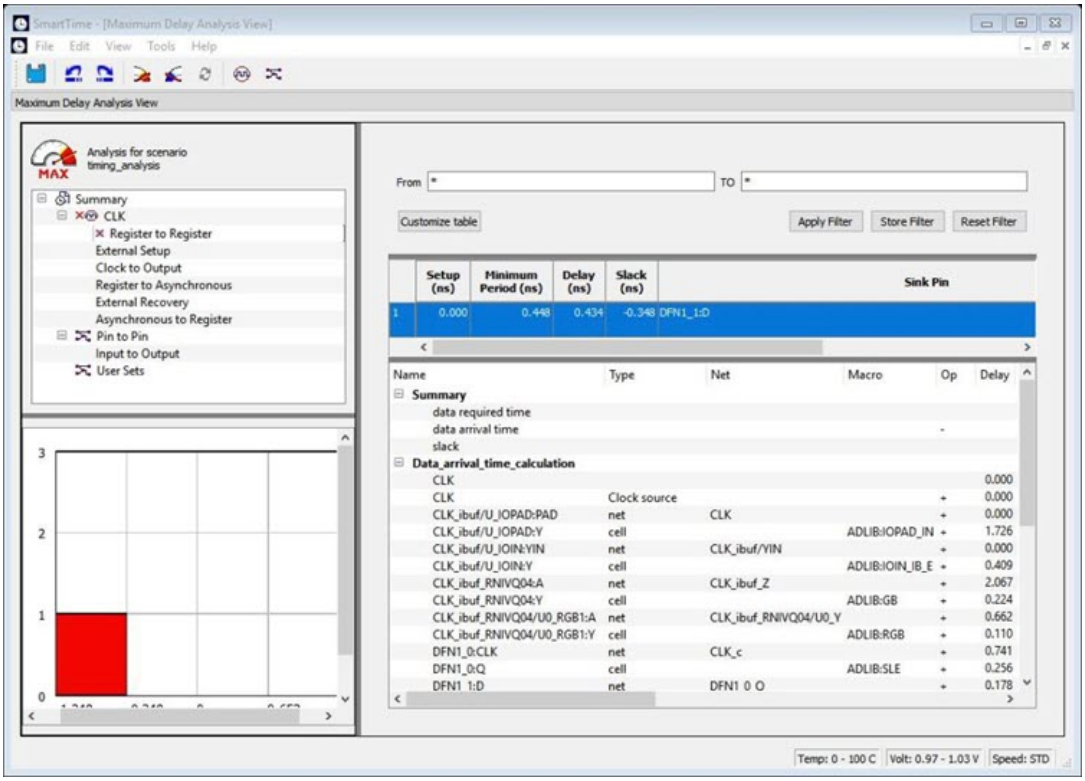
You can use filters in SmartTime to limit the Path List content (that is, create a filtered list on the source and sink pin names).

Filtering options appear at the top of the Timing Analysis View. You can save these filters one level below the set under which they have been created.

To use the filter:

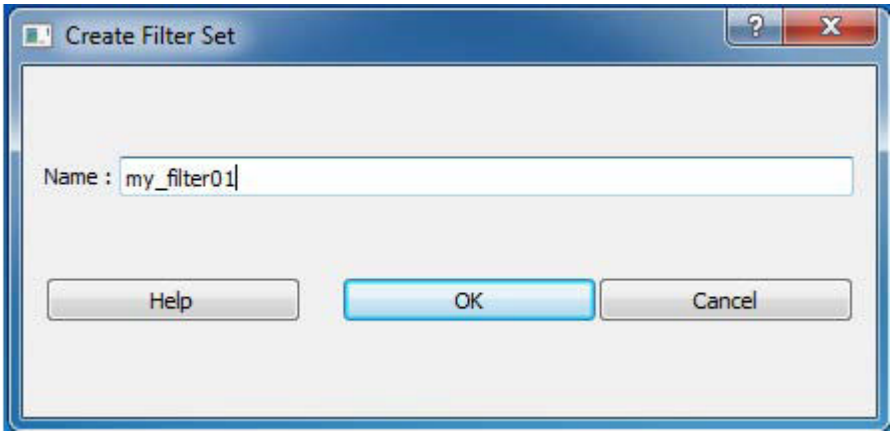
1. Select a set in the Domain Browser to display a given number of paths, depending on your SmartTime Options settings (100 paths by default).
2. Enter the filter criteria in both the From and To fields, and then click **Apply Filter**.
   The display limits the paths to those that match your filter criteria.

   Figure 6-8. Maximum Delay Analysis View



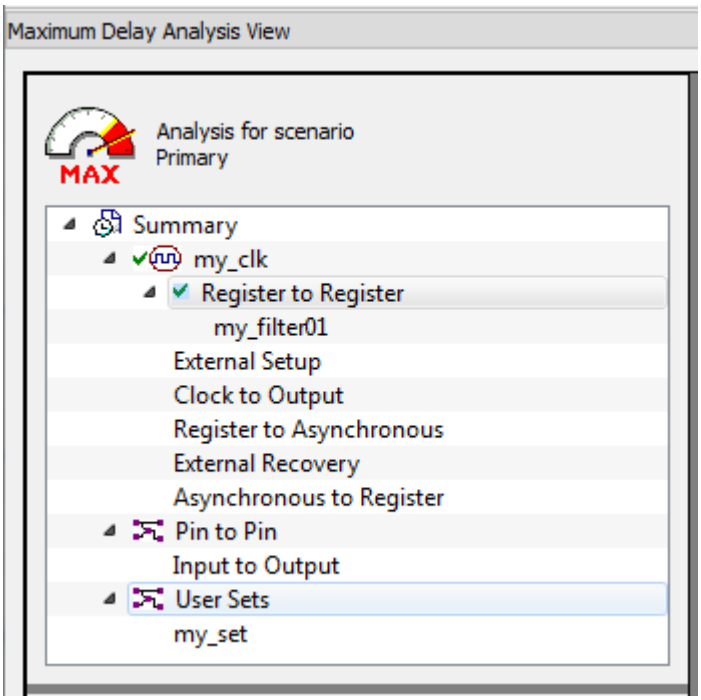
3. Click **Store Filter** to save your filter criteria with a special name.
   The Create Filter Set dialog box appears.

Figure 6-9. Create Filter Set Dialog Box



4. Enter a name for the filter, such as myfilter01, and click **OK**.
   Your new filter name appears below the set under which it was created.

Figure 6-10. Specifying the Filter my_filter01



5. Repeat this procedure to cascade as many sets as you need using the filtering mechanism.
6. To edit a filter in the set:
   a) Select the filter you want to edit.
   b) Right-click the filter and choose **Edit Set** from the shortcut menu.
7. To rename a set created with filters:
   a) Select the set that uses filters.
   b) Right-click the set, and choose **Rename Set** from the shortcut menu.
   c) Edit the name directly in the Domain Browser.

7. Advanced Timing Analysis

The following sections describe advanced timing analysis.

7.1 Understanding Inter-Clock Domain Analysis

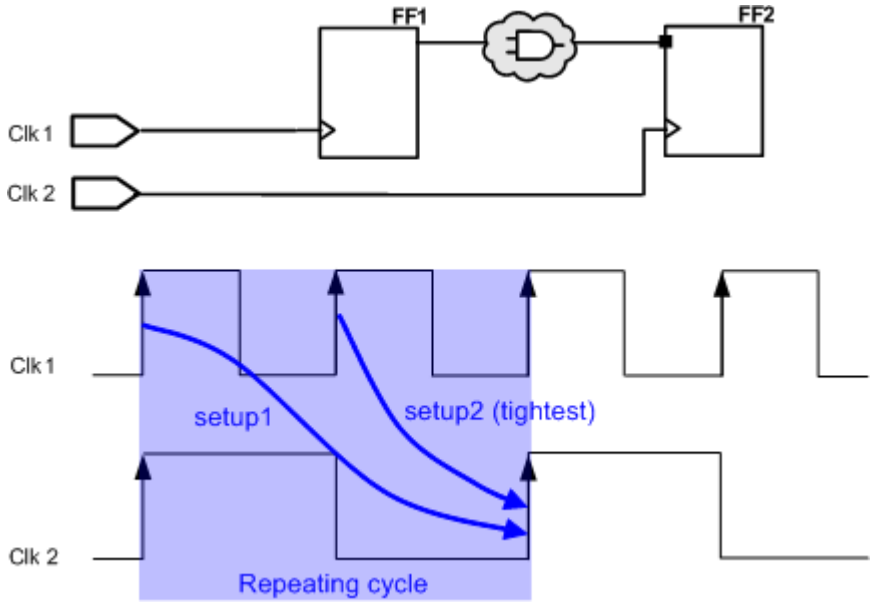
When functional paths exist across two clock domains (the register launching the data and the one capturing it are clocked by two different clock sources), you must provide accurate specification of both clocks to allow a valid inter-clock domain timing check. This is important especially when the clocks are specified with different waveforms and frequencies.

When you specify multiple clocks in your design, consider whether the inter-clock domain paths are false or functional. If the paths are functional, perform setup and hold checks between the clock domains in SmartTime. Unless specified otherwise, SmartTime considers the inter-clock domain as false, and therefore does not perform setup or hold checks between the clock domains.

If you have several clock domains that are subset of a single clock (such as if you want to measure clock tree delay from an input clock to a generated clock), you must configure Generated Clock Constraints for each of the clock domains in order for SmartTime to execute the calculation and show timing for each of the inter-clock domain paths.

Once you include the inter-clock domains for timing analysis, SmartTime analyzes for each inter-clock domain the relationship between all the active clock edges over a common period equal to the least common multiple of the two clock periods. The new common period represents a full repeating cycle (or pattern) of the two clock waveforms (as shown below).

Figure 7-1. New Common Period



For setup check, SmartTime considers the tightest relation launch-capture to ensure that the data arrives before the capture edge. The hold check verifies that a setup relationship is not overwritten by a following data launch.

7.2 Activating Inter-Clock Domain Analysis

To activate the inter-clock domain checking:

1. From the SmartTime **Tools** menu, choose **Options**.
   The SmartTime Options dialog box dialog box appears (as shown below).
2. In the **General** category, check **Include inter-clock domains in calculations for timing analysis**.

Figure 7-2. SmartTime Options Dialog Box for SmartFusion2, RTG4, and IGLOO2

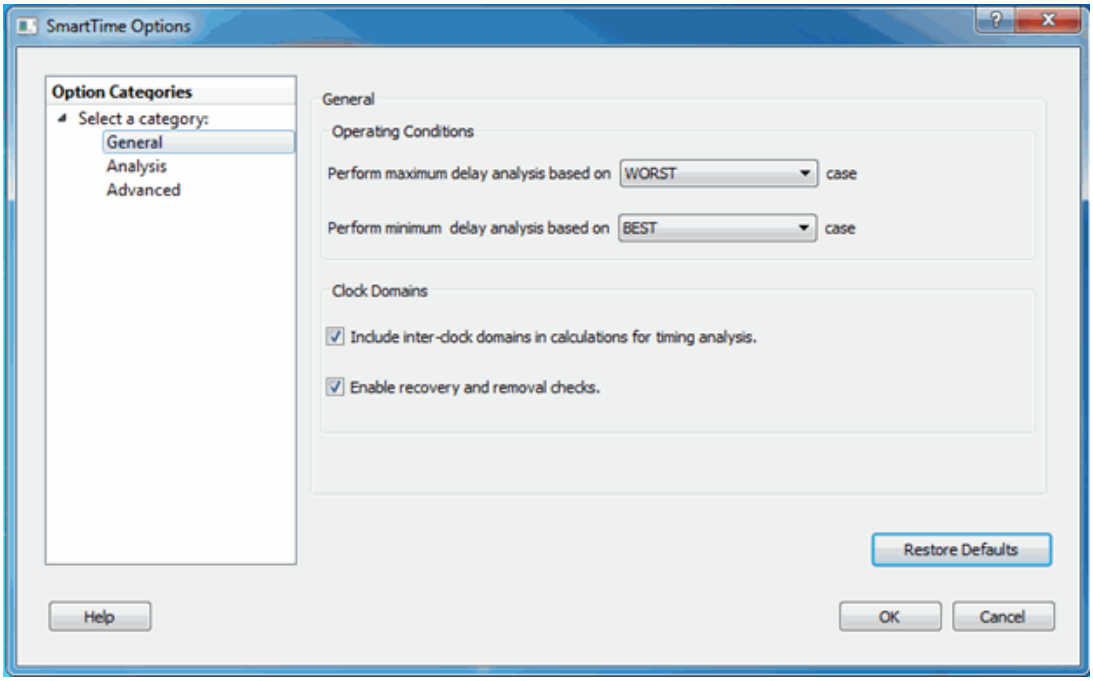
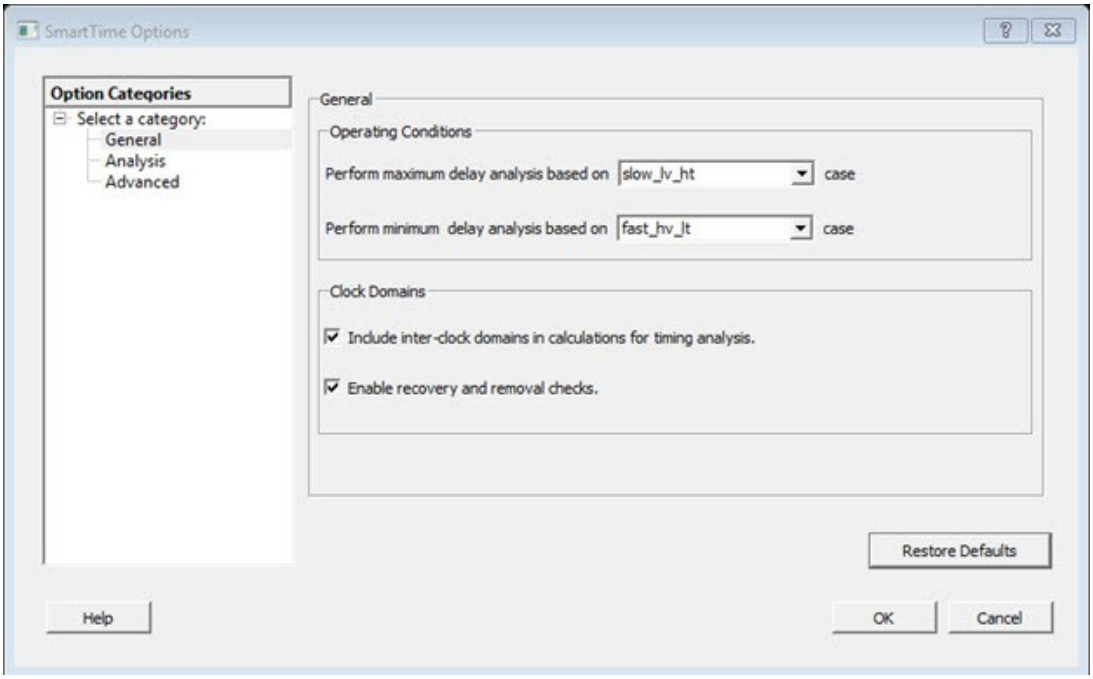


Figure 7-3. SmartTime Options Dialog Box for PolarFire



3. Click **OK** to save the dialog box settings.

7.3 Displaying Inter-Clock Domain Paths

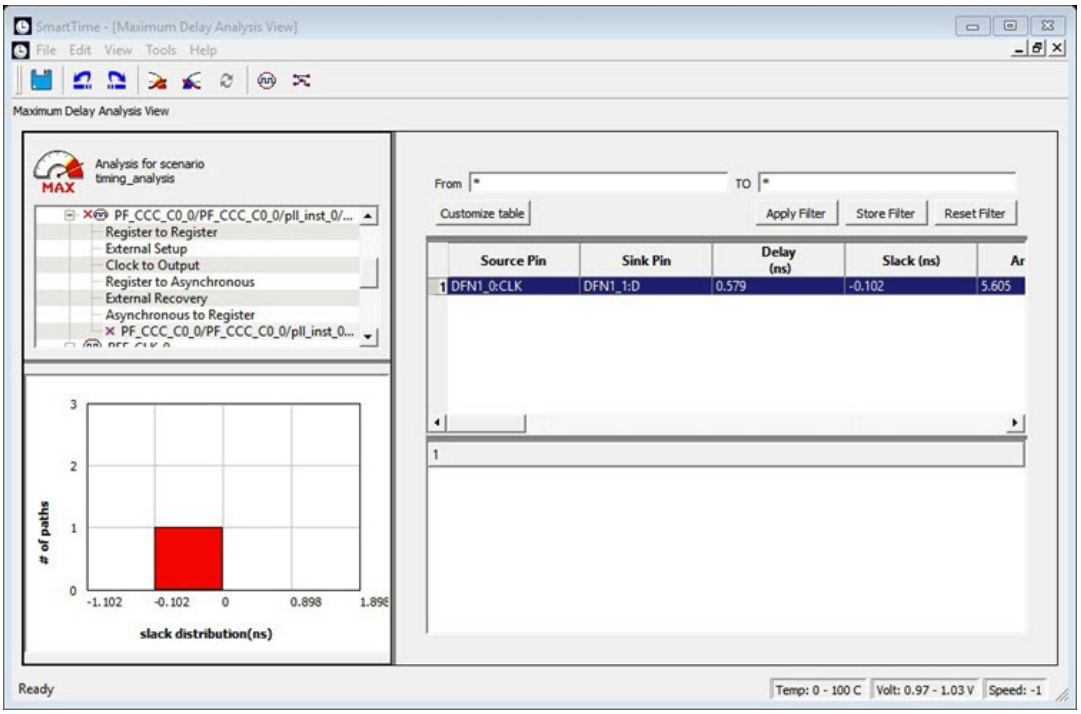
After you activate the inter-clock domain checking for a given clock domain CK1, SmartTime detects automatically all other domains CKn with paths ending at CK1.

SmartTime creates inter-clock domain sets CKn to CK1 under the domain CK1. Each set allows you to display the inter-clock domain paths between a given clock domain and CK1.

To display an inter-clock domain set:

1. Expand the receiving clock domain of the inter-clock domain in the Domain Browser to display its related sets. For the inter-clock domain CK1 to CK2, expand clock domain CK2.

Figure 7-4. Expanding the Inter-Clock Domain



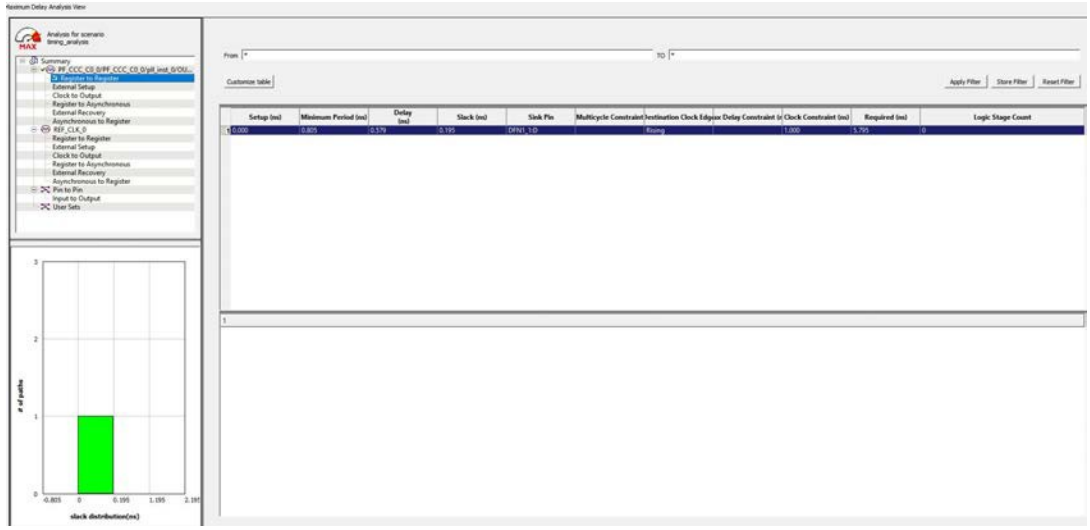
2. Select the inter-clock domain you want to expand from these sets.
   All paths between the related two domains are displayed in Paths List in the same way as any register to register set.

7.4 Deactivating a Specific Inter-Clock Domain

To deactivate the inter-clock domain checking for the specific clock domains clk2->clk1, without disabling this option for the other clock domains:

1. From the **Tools** menu, choose **Constraints Editor > Primary Scenario** to open the Constraints Editor View.
2. In the Constraints Browser, double-click **False Path** under **Exceptions**.
   The Set False Path Constraint dialog box appears.
3. Click the **Browse** button to the right of the **From** text box.
   The Select Source Pins for False Path Constraint dialog box appears.
4. For **Specify pins**, select **by keyword and wildcard**.
5. For **Pin Type**, select **Registers by clock names** from the **Pin Type** drop-down list.
6. In the filter box, type the inter-clock domain name (for example, Clk2), and then click **Filter**.
7. Click **OK** to begin filtering the pins by your criteria.
   In this example, [get_clocks {Clk2}] appears in the **From** text box in the Set False Path Constraint dialog box.
8. Repeat steps 3 to 7 for the **TO** option in the Set False Path Constraint dialog box and type `Clk2` in the filter box.
9. Click **OK** to validate the new false path and display it in the Paths List of the Constraints Editor.
10. Click the Recalculate All icon  in the toolbar.
11. Select the inter-clock domain set clk2 -> clk1 in the Domain Browser (as shown below).

Figure 7-5. Selecting the Inter-clock Domain Set clk2 -> clk1



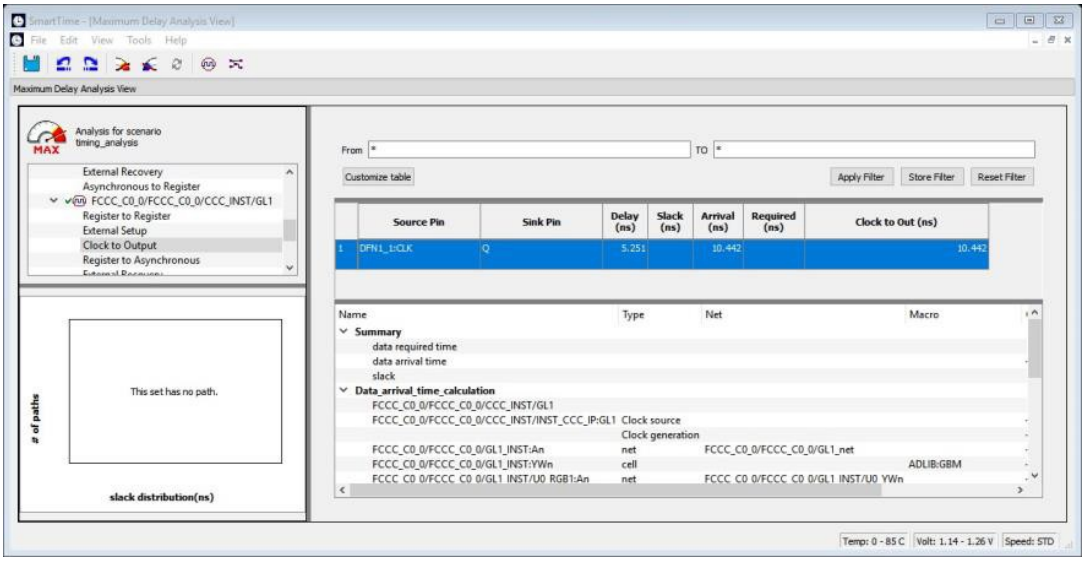
12. Verify that the set does not contain any paths.

7.5 Changing Output Port Capacitance

Output propagation delay is affected by both the capacitive loading on the board and the I/O standard.

The I/O Attribute Editor in Chip Planner provides a way to set the expected capacitance to improve the propagation delay model. SmartTime uses the modified delay model automatically for delay calculations.
To change the output port capacitance and view the effect of this change in SmartTime Timing Analyzer, see the following example. The following figure shows a delay of 6.603 ns from DFN1 to output port Q based on the default loading of 5 pF.

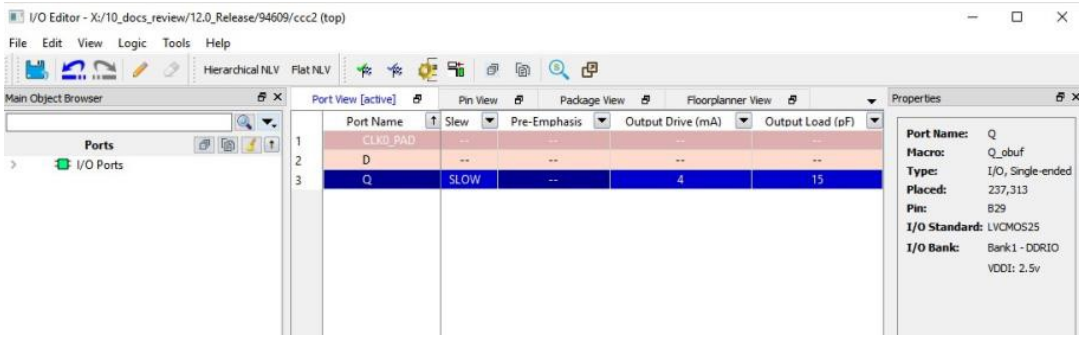
Figure 7-6. Maximum Delay Analysis View



If your board has an output capacitance of 15 pf on Q, perform the following steps to update the timing number.

1. Open the I/O Attribute Editor and change the output load to 15 pf.

Figure 7-7. I/O Attribute Editor



2. Select **File > Save**.
3. Select **File > Close**.
4. Open the SmartTime Timing Analyzer and confirm that the **Clock to Output** delay changed to 5.952 ns.

8. Generating Timing Reports

The following sections describe how to generate timing reports.

8.1 Types of Reports

The following table describes the types of timing reports you can generate using SmartTime.

Table 8-1. Types of Timing Reports

Report	Description
Timer Report	Displays the timing information organized by clock domain.
Timing Violations Report	Provides information about constraint violations.
Bottleneck Report	Displays points in the design that contribute to the most timing violations.
Datasheet Report	Describes the characteristics of the pins, I/O technologies, and timing properties in the design.
Constraints Coverage Report	Displays the overall coverage of the timing constraints set on the current design.
Combinational Loop Report	Displays loops found during initialization.
Clock Domain Crossing Report	Analyzes timing paths that cross from one clock domain (the source clock) to another clock domain (the destination clock).

8.2 Generating a Timing Report

The Timing Report allows you to determine whether timing problems exist in your design.

The Maximum Delay Analysis Timing Report lists the following information about your design:

- Maximum delay from input I/O to output I/O
- Maximum delay from input I/O to internal registers
- Maximum delay from internal registers to output I/O
- Maximum delays for each clock network
- Maximum delays for interactions between clock networks

To generate a Timing Report:

1. From the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Timer**.
   The Timing Report Options dialog box appears.
2. Select the options you want to include in the report, and then click **OK**.
   The Timing Report appears in a separate window.

8.3 Understanding Timing Reports

The Timing Report contains the following sections:

Table 8-2. Timing Report Sections

Section	Description
Header	Lists the: • Report type • Version of Designer used to generate the report • Date and time the report was generated • General design information (name, family, and so on)
Summary	Reports the timing information for each clock domain. By default, the clock domains reported are the explicit clock domains that are shown in SmartTime. To filter the domains and show only specific sections in the report, use the Timing Report Options dialog box.
Path	Lists the timing information for different types of paths in the design. This section is reported by default. You can deselect this option in the Timing Report Options dialog box. By default, the number of paths displayed per set is 5. You can filter the domains using the Timing Report Options dialog box. You can also view the stored filter sets in the generated report using the Timing Report options. The filter sets are listed by name in their appropriate section. The number of paths reported for the filter set is the same as for the main sets. By default, the filter sets are not reported.

8.3.1 Clock Domains

Paths are organized by clock domain.

8.3.2 Register to Register Set

This set reports the paths from the registers clock pins to the registers data pins in the current clock domain.

8.3.3 External Setup Set

This set reports the paths from the top-level design input ports to the registers in the current clock domain.

8.3.4 Clock to Output Set

This set reports the paths from the registers clock pins to the top-level design output ports in the current clock domain.

8.3.5 Register to Asynchronous Set

This set reports the paths from registers to asynchronous control signals, such as asynchronous set/reset.

8.3.6 External Recovery Set

This set reports the external recovery check timing for asynchronous control signals, such as asynchronous set/reset.

8.3.7 Asynchronous to Register Set

This set reports the paths from asynchronous control signals, such as asynchronous set/reset, to registers.

8.3.8 Inter-clock Domain

This set reports the paths from the registers clock pins of the specified clock domain to the registers data pins in the current clock domain. Inter-domain paths are not reported by default.

8.3.9 Pin to Pin

This set lists input to output paths and user sets. Input-to-output paths are reported by default. To see the user-defined sets, use the Timing Report Options dialog box.

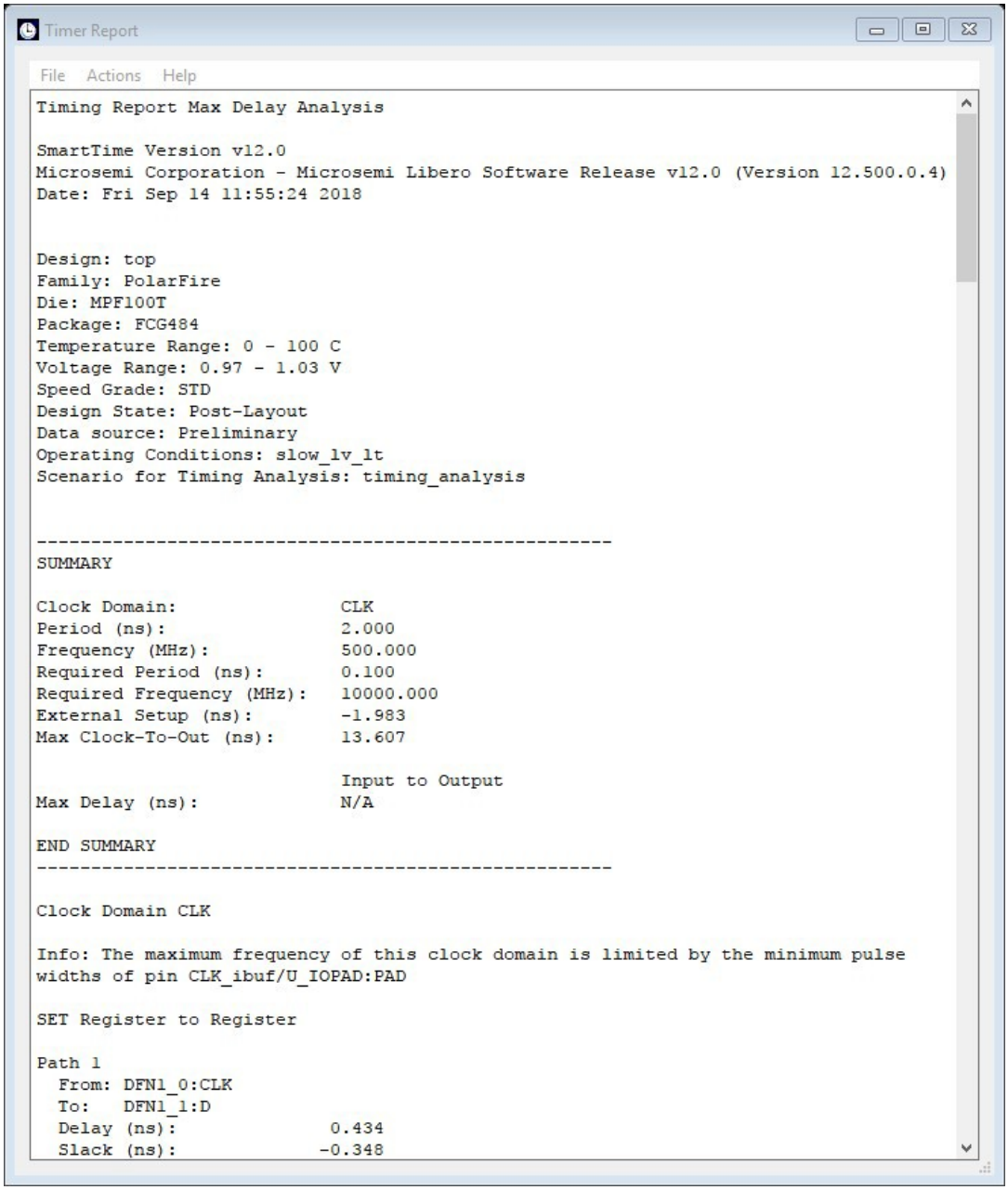
8.3.10 Input to Output Set

This set reports the paths from the top-level design input ports to the top-level design output ports.

8.3.11 Expanded Paths

Expanded paths can be reported for each set. By default, the number of expanded paths to report is set to 1. You can select and change the number when you specify Timing Report options.

Figure 8-1. Timing Report



8.4 Generating a Timing Violation Report

The Timing Violations Report provides a Flat Slack Report centered around constraint violations.

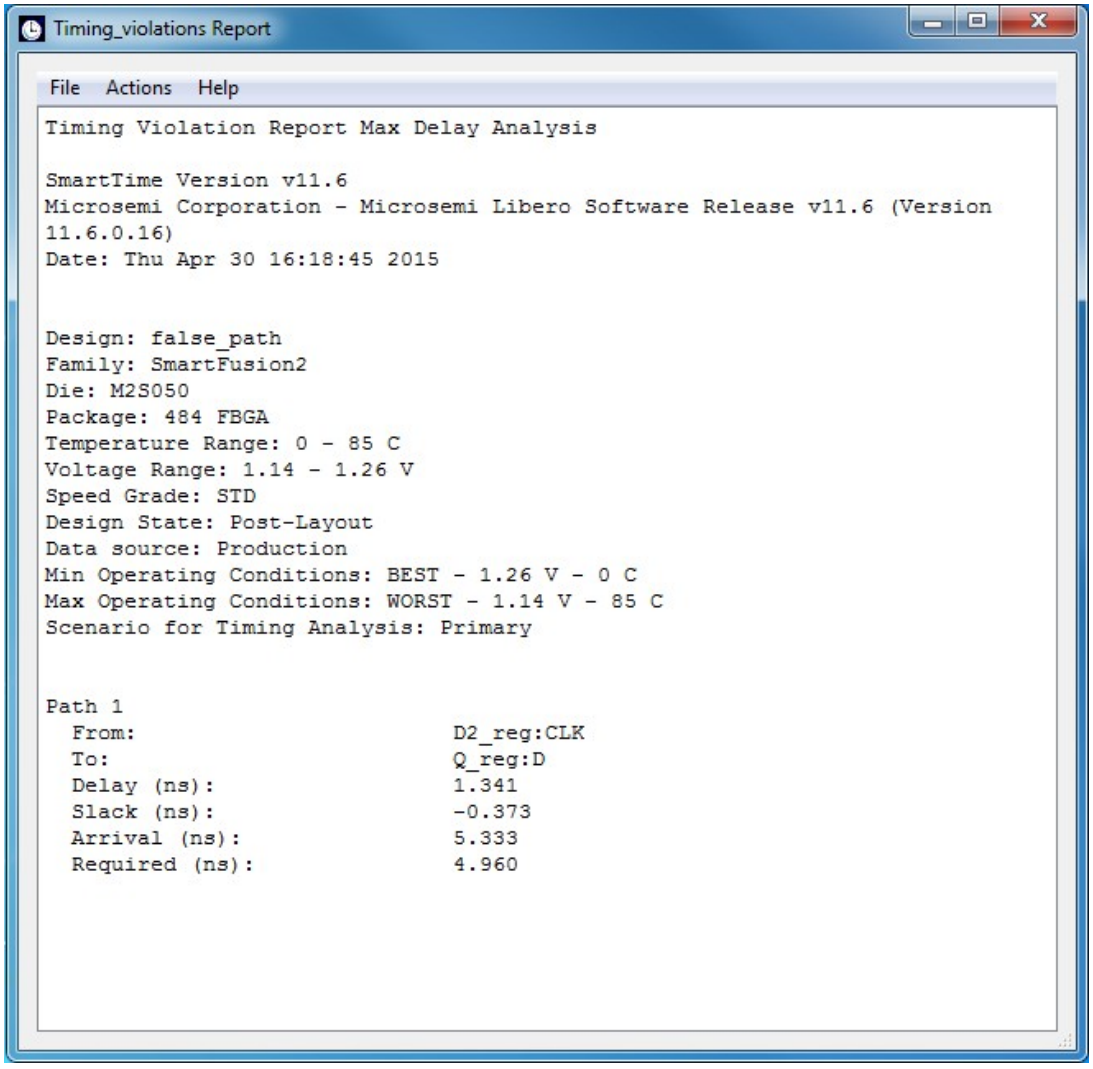
To Timing Violations Report:

1. From the SmartTime Max/Min Delay Analysis View window, choose **Tools > Reports > Timing Violations**. The Timing Violations Report Options dialog box appears.
2. Select the options you want to include in the report, and then click **OK**. The Timing Violations Report appears in a separate window.

8.5 Understanding Timing Violation Reports

The following figure shows an example of a Timing Violations Report.

Figure 8-2. Sample Timing Violation Report



The Timing Violation Report contains the following sections:

Table 8-3. Timing Violation Report Sections

Section	Description
Header	This section lists the: • Report type • Version of Designer used to generate the report • Date and time the report was generated • General design information (name, family, and so on)
Paths	This section lists the timing information for different types of paths in the design. The number of paths displayed is controlled by the following parameters: • A maximum slack threshold to report • A maximum number or path to report By default, the slack threshold is 0 and the number of paths is limited. The default maximum number of paths reported is 100.All clocks domains are mixed in this report. The paths are listed by decreasing slack. You can also choose to expand one or more paths. By default, no paths are expanded. For details, see the Timing Violation Report options.

8.6 Generating a Constraints Coverage Report

The Constraints Coverage Report contains information about the constraints in the design.

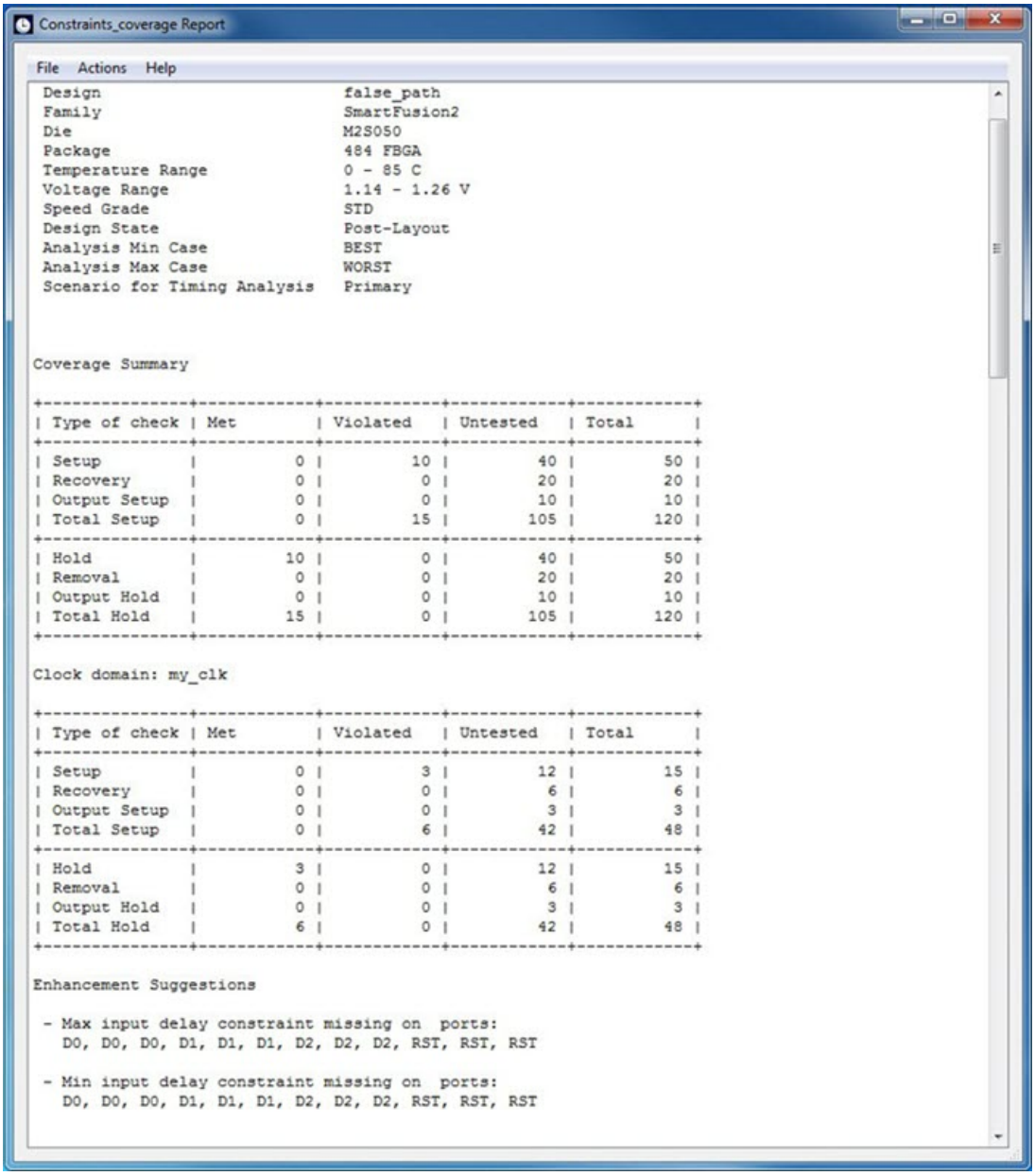
To generate a Constraints Coverage Report:

1. From the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Constraints Coverage**.
2. Select the text format and number of unconstrained instances and click **OK**.
   The report appears in a separate window.

8.7 Understanding Constraints Coverage Reports

The Constraints Coverage Report shows the overall coverage of the timing constraints set on the current design. You can generate this report either from within Designer or within SmartTime Analyzer.

Figure 8-3. Sample Constraints Coverage Report



Constraints_coverage Report

File Actions Help

```
Design                          false_path
Family                          SmartFusion2
Die                             M2S050
Package                         484 FBGA
Temperature Range               0 - 85 C
Voltage Range                   1.14 - 1.26 V
Speed Grade                     STD
Design State                    Post-Layout
Analysis Min Case               BEST
Analysis Max Case               WORST
Scenario for Timing Analysis    Primary


Coverage Summary

+---------------+------------+------------+------------+------------+
| Type of check | Met        | Violated   | Untested   | Total      |
+---------------+------------+------------+------------+------------+
| Setup         |          0 |         10 |         40 |         50 |
| Recovery      |          0 |          0 |         20 |         20 |
| Output Setup  |          0 |          0 |         10 |         10 |
| Total Setup   |          0 |         15 |        105 |        120 |
+---------------+------------+------------+------------+------------+
| Hold          |         10 |          0 |         40 |         50 |
| Removal       |          0 |          0 |         20 |         20 |
| Output Hold   |          0 |          0 |         10 |         10 |
| Total Hold    |         15 |          0 |        105 |        120 |
+---------------+------------+------------+------------+------------+

Clock domain: my_clk

+---------------+------------+------------+------------+------------+
| Type of check | Met        | Violated   | Untested   | Total      |
+---------------+------------+------------+------------+------------+
| Setup         |          0 |          3 |         12 |         15 |
| Recovery      |          0 |          0 |          6 |          6 |
| Output Setup  |          0 |          0 |          3 |          3 |
| Total Setup   |          0 |          6 |         42 |         48 |
+---------------+------------+------------+------------+------------+
| Hold          |          3 |          0 |         12 |         15 |
| Removal       |          0 |          0 |          6 |          6 |
| Output Hold   |          0 |          0 |          3 |          3 |
| Total Hold    |          6 |          0 |         42 |         48 |
+---------------+------------+------------+------------+------------+

Enhancement Suggestions

 - Max input delay constraint missing on  ports:
   D0, D0, D0, D1, D1, D1, D2, D2, D2, RST, RST, RST

 - Min input delay constraint missing on  ports:
   D0, D0, D0, D1, D1, D1, D2, D2, D2, RST, RST, RST
```

The Constraints Coverage Report contains the following sections:

Table 8-4. Constraints Coverage Report Sections

Section	Description
Coverage Summary	Shows statistical information about the timing constraint in the design. For each type of timing checks (Setup, Recovery, Output, Hold, and Removal), it specifies how many are Met (there is a constraint and it is satisfied), Violated (there is a constraint and it is not satisfied), or Untested (no constraint was found).
Results by Clock Domain	This section provides a coverage summary for each clock domain.

.....continued	
Section	**Description**
Enhancement Suggestions	Reports, per clock domain, a list of constraints that can be added to the design to improve the coverage. It also reports if some options impacting the coverage can be changed.
Detailed Stats	Provides detailed suggestions about specific clocks or I/O ports that may require to be constrained for every pin/port that requires checks.

8.8 Generating a Bottleneck Report

To generate a Bottleneck Report:

1. From the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Bottleneck**. The report appears in a separate window.

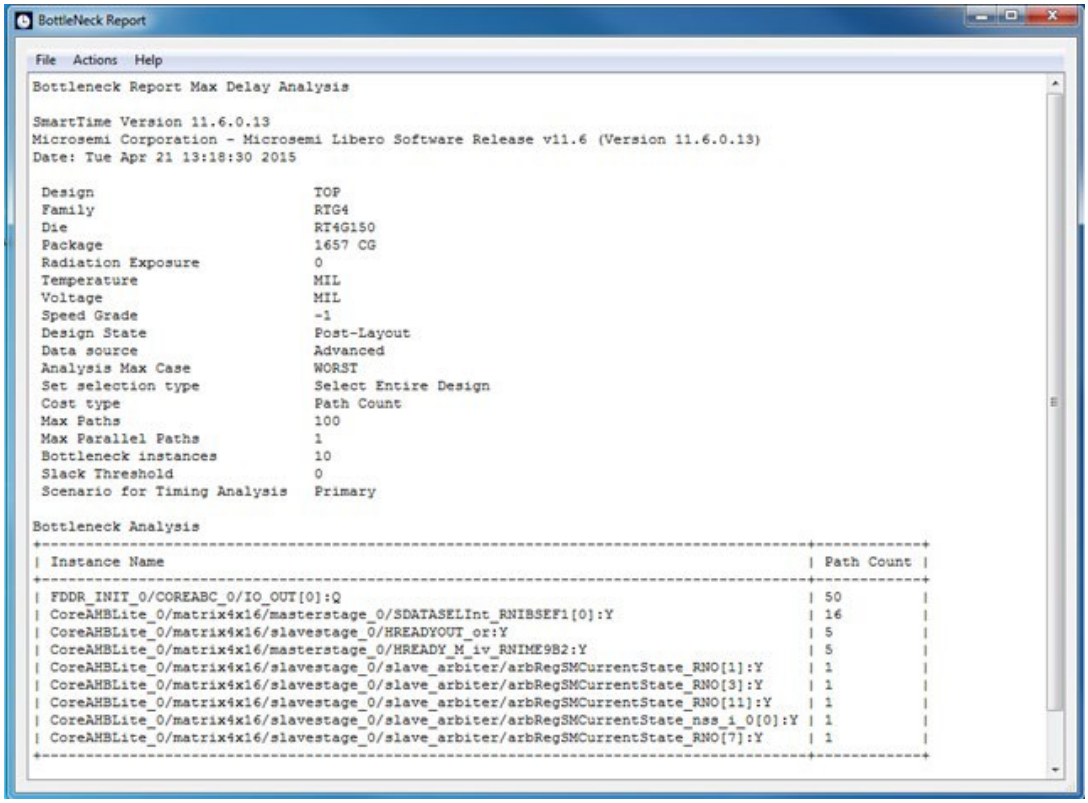
8.9 Understanding Bottleneck Reports - SmartFusion2, IGLOO2, RTG4, and PolarFire

A bottleneck is a point in the design that contributes to multiple timing violations. The Bottleneck Report lists the bottlenecks in the design. You can generate this report from SmartTime Analyzer.

Notes: The bottleneck can be computed only when a cost type is defined. There are two cost type options available:

- **Path count**: associates the severity of the bottleneck to the count of violating/critical paths that traverse the instance.
- **Path cost**: associates the severity of the bottleneck to the sum of the timing violations for the violating/critical paths that traverse the instance.

Figure 8-4. Sample Bottleneck Report



The Bottleneck Report contains the following parts:

Table 8-5. Bottleneck Report Sections

Part	Description
Device Description	Contains general information about the design, including: • Design name • Family • Die • Package • Software version
Bottleneck Analysis	Lists the core of the bottleneck information. It is organized into two columns: • Instance Name: refers to the output pin name of the instance. • Path Count: shows the number of violating paths that include the instance pin.

8.10 Generating a Datasheet Report

The Datasheet Report shows information about a design's external characteristics.

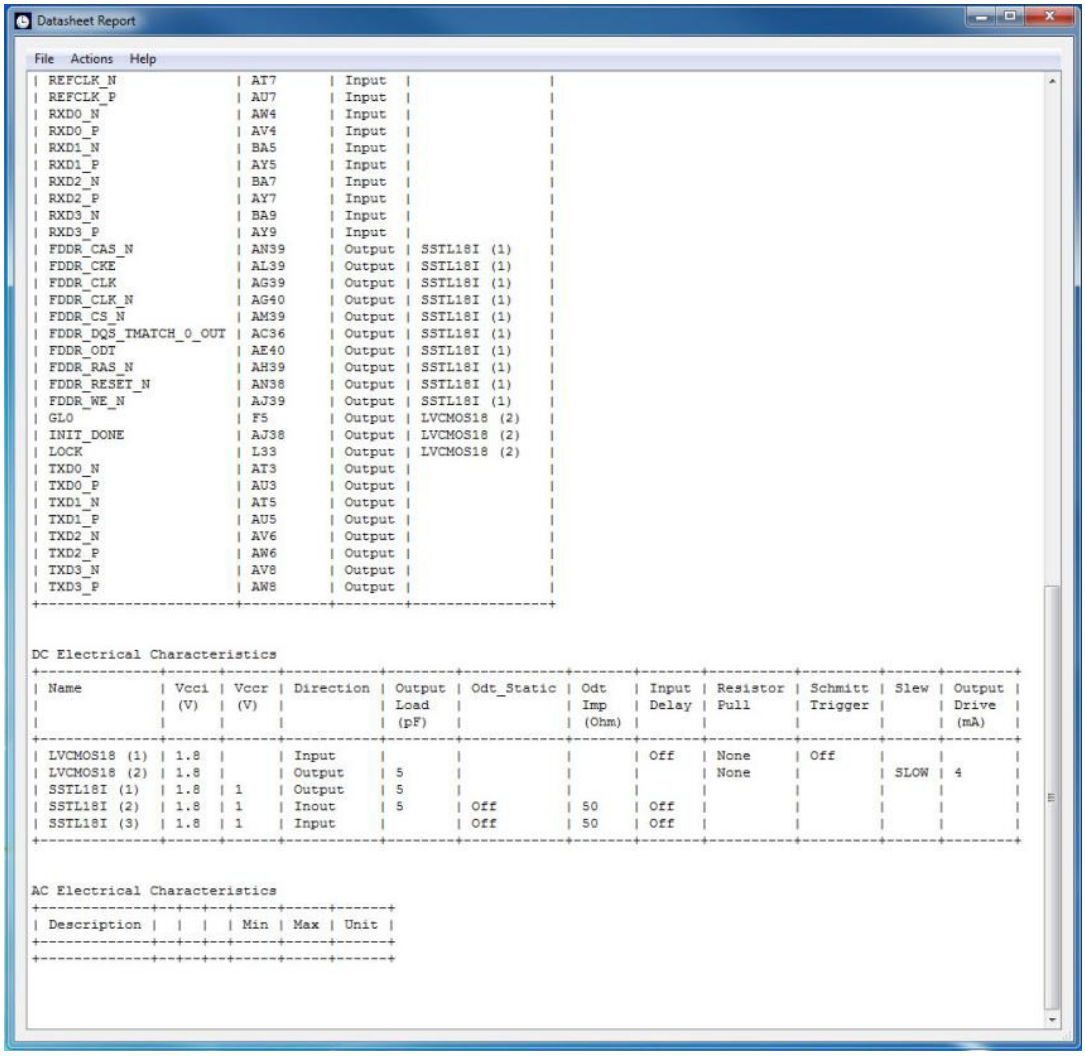
To generate a Datasheet Report:

1. From the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports > Datasheet**. The report appears in a separate window.

8.11 Understanding Datasheet Reports

The Datasheet Report displays the external characteristics of the design. You can generate this report from SmartTime Max/Min Delay Analysis View.

Figure 8-5. Sample Datasheet Report



The Datasheet Report contains three tables:

Table 8-6. Datasheet Report Tables

Table	Description
Pin Description	Provides the port name in the netlist, location on the package, type of port, and I/O technology assigned to it. Types can be input, output, or clock. Clock ports are ports shown as "clock" in the Clock domain browser.
DC Electrical Characteristics	Provides the parameters of the different I/O technologies used in the design. The number of parameters displayed depends on the family for which you have created the design.

.....continued

Table	Description
AC Electrical Characteristics	Provides the timing properties of the ports of the design. For each clock, this section includes the maximum frequency. For each input, it includes the external setup, external hold, external recovery, and external removal for every clock where it applies. For each output, it includes the clock-to-out propagation time. This section also displays the input-to-output propagation time for combinational paths.

8.12 Generating a Combinational Loop Report

The Combinational Loop Report shows all loops found during initialization and reports pins associated with the loop(s) and the location where a loop is broken.

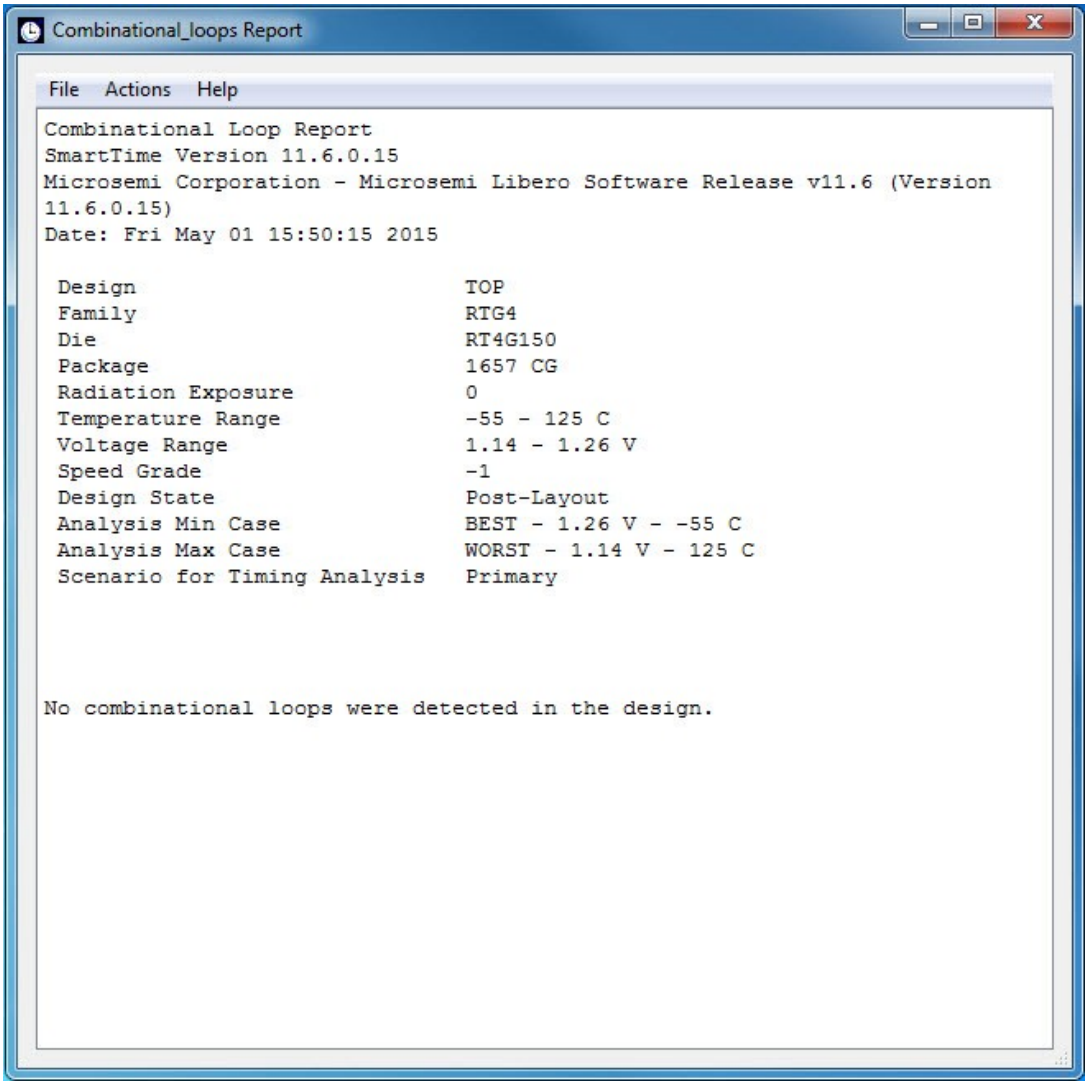
To generate a Combinational Loop Report:

1. From the **Tools** menu, choose **Reports > Combinational Loops**.
   The Combinational_Loops Report Options dialog box appears.
2. Select either **Plain Text** or **Comma Separated Values**.
3. Click **OK**.

8.13 Understanding Combinational Loop Reports

The Combinational Loop Report shows all loops found during initialization, reports the pins associated with the loops, and identifies the locations where loops are broken.

Figure 8-6. Sample Combinational Loop Report



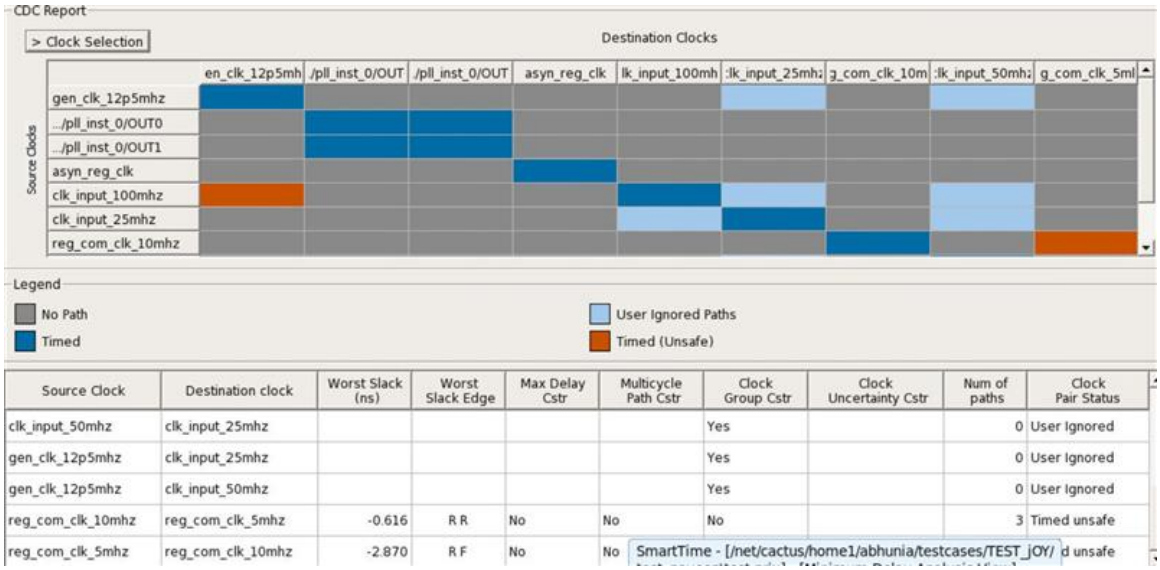
8.14 Generating a Clock Domain Crossing (CDC) Report

The Clock Domain Crossing (CDC) Report analyzes timing paths that cross from one clock domain (the source clock) to another clock domain (the destination clock). The CDC report helps identify instances where there may be data loss or metastability issues.

To generate the CDC Report:

1. From the **Tools** menu, choose **Reports > Clock Domain Crossing (CDC).**.
   The Clock Domain Crossing Report Options dialog box appears.
2. Select either **CDC Table** or **Comma Separated Values**.
3. Click **OK**.

   Selecting **CDC Table** displays a graphical table with color-coded cells. Each cell represents a CDC type between the source clock and the destination clock domains that have constraints. Clocks without constraints do not appear in the CDC table.



Source Clock	Destination clock	Worst Slack (ns)	Worst Slack Edge	Max Delay Cstr	Multicycle Path Cstr	Clock Group Cstr	Clock Uncertainty Cstr	Num of paths	Clock Pair Status
clk_input_50mhz	clk_input_25mhz					Yes		0	User Ignored
gen_clk_12p5mhz	clk_input_25mhz					Yes		0	User Ignored
gen_clk_12p5mhz	clk_input_50mhz					Yes		0	User Ignored
reg_com_clk_10mhz	reg_com_clk_5mhz	-0.616	R R	No	No	No		3	Timed unsafe
reg_com_clk_5mhz	reg_com_clk_10mhz	-2.870	R F	No	No	SmartTime - [/net/cactus/home1/abhunia/testcases/TEST_jOY/			d unsafe

The attributes present in the path table are as follows:

- Source Clock: Source of the clock
- Destination Clock: Destination of the clock
- Worst Slack (ns): Worst slack of the CDC path in nanoseconds
- Worst Slack Edge: This is the source/sink edge for the worst path of CDC
- Max Delay Cstr:

Value	Description
Yes	All paths in CDC have set_max_delay applied
No	No paths in CDC have the constraints applied
Partial	Any path in CDC has the constraint applied

- Multicycle Path Cstr:

Value	Description
Yes	All paths in CDC have set_multicycle_path applied
No	No paths in CDC have the constraints applied
Partial	Any path in CDC has the constraint applied

- Clock Group Cstr:

Value	Description
Yes	CDC has set_clock_group applied
No	CDC does not have set_clock_group applied

- Clock Uncertainty Cstr: It is the uncertainty value for the worst path in CDC; else, the clock uncertainty field is left empty.
- Num of Paths: Number of paths in CDC. For User Ignored paths, the value is 0.
- Clock Pair Status: The status can be Timed Safe, Timed Unsafe or User Ignored.

In the CDC Report dialog box, you can select the clocks to view or hide. Clicking the **Clock Selection** button at the top left of the dialog box lists all clocks that can be viewed or hidden. By default, all clocks are checked and visible. To hide a clock, clear its check box.

Figure 8-7. Showing or Hiding Clocks

The following table describes the colors in the CDC Report shown in the preceding figure.

Pattern	Status	Color
Paths from the source clock domain to the destination clock domain have all been disabled by false path or clock group constraints.	User-Ignored Paths	Light blue
No Paths found from the source clock domain to the destination clock domain.	No Paths	Gray
The source and destination clocks are synchronous: Both the clocks have a common primary clock and paths are found from the source clock domain to the destination clock domain.	Timed	Dark Blue
The source and destination clocks are asynchronous: Both the clocks have NO common primary clock, while paths are found from the source clock domain to the destination clock domain. Currently, synchronizers, if present, are not accounted for in this report.	Timed (unsafe)	Brown

There are certain scenarios related to the path table as explained in the following:

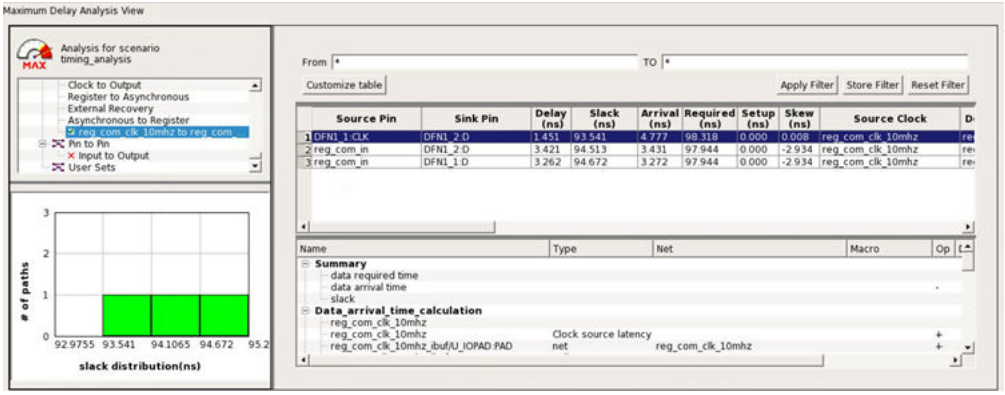
1. When CDC report is generated, path table is shown by default for all CDC having paths. Each row shows the worst slack for a clock crossing. Similarly, when clicking on a particular CDC crossing in CDC report, you can have a single row showing the worst slack for CDC crossing.

   Example: The path table shown in the following figure, the worst path for reg_com_clk_10mhz to reg_com_clk_5mhz has the worst slack of 93.541. The same path is displayed by default, when the CDC crossing is selected.

   Figure 8-8. Worst Path with Slack 93.541 ns

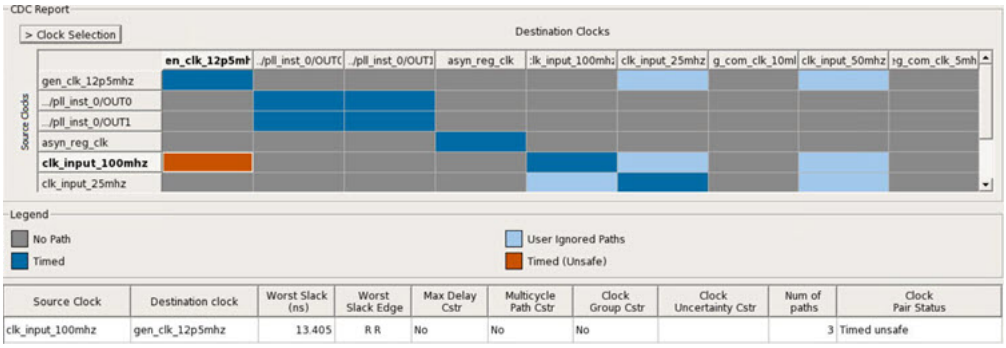
Source Clock	Destination clock	Worst Slack (ns)	Worst Slack Edge	Max Delay Cstr	Multicycle Path Cstr	Clock Group Cstr	Clock Uncertainty Cstr	Num of paths	Clock Pair Status
gen_clk_12p5mhz	clk_input_25mhz					Yes		0	User Ignored
gen_clk_12p5mhz	clk_input_50mhz					Yes		0	User Ignored
reg_com_clk_10mhz	reg_com_clk_5mhz	93.541	R R	No	No	No	5.000	3	Timed unsafe
reg_com_clk_5mhz	reg_com_clk_10mhz	89.703	R F	No	No	No	2.000	2	Timed unsafe

Figure 8-9. Smarttime Showing the Worst Path with Slack 93.541 ns



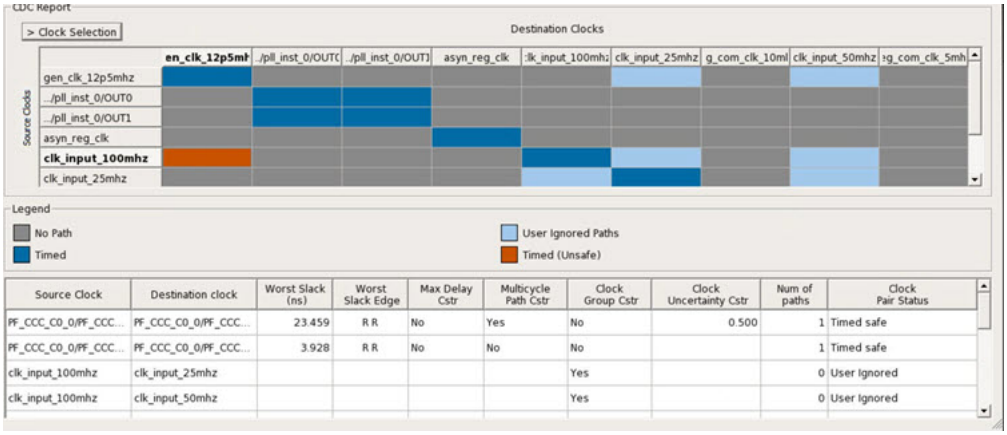
2. Clicking on the CDC box shows the worst slack for a clock crossing as in path table in the following figure.

Figure 8-10. Highlighted CDC Box Showing the Worst Slack in Path Table



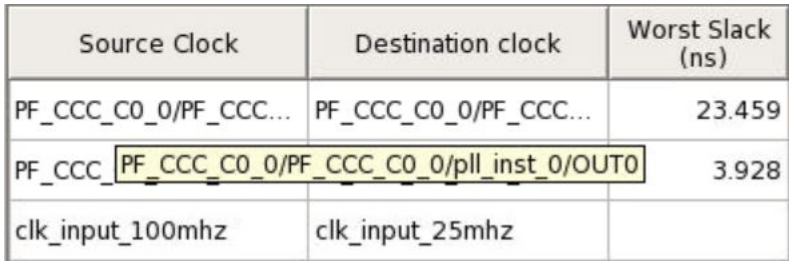
Clicking on the same CDC box again will show the details for all the clocks selected in CDC report.

Figure 8-11. CDC Path Table Showing All Clocks on Deselecting the Selected CDC Box



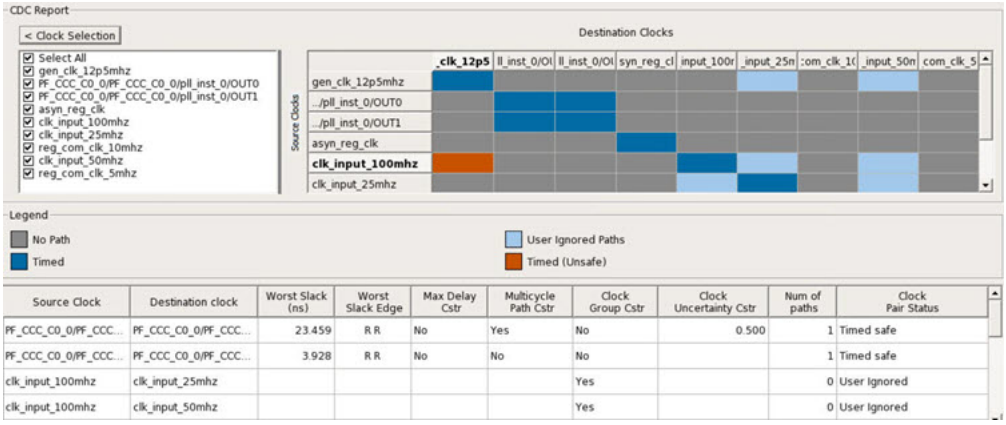
For all clocks having large names, tool-tips for columns have been added.

Figure 8-12. CDC Path Table Showing Tool-Tip for a Source Clock Name



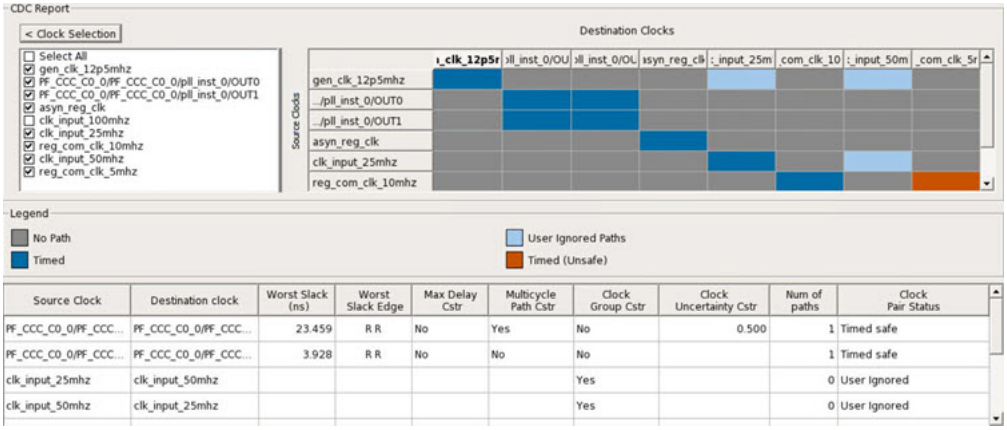
3. Selecting/deselecting clocks in clock selection will dynamically change the path table along with the CDC table. Both the tables are in sync. Example: Here, clk_input_100mhz is selected, therefore, the clock is displayed in CDC table and path table.

Figure 8-13. CDC Table in Sync with Clock Selection Section



When the clock clk_input_100mhz is unselected, then the same clock is removed from the CDC table. The crossings related to the clock are also removed from the path table as shown in the following figure.

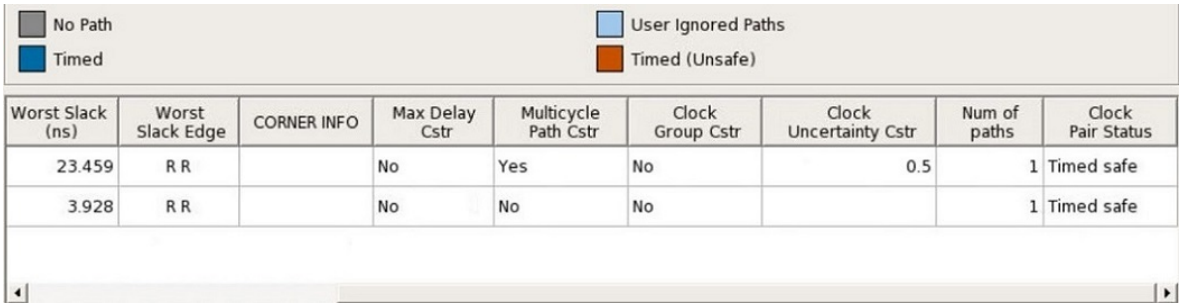
Figure 8-14. Deselecting a Clock in Clock Selection Section Syncs the Path Table Accordingly



On clicking any one of the four options in the CDC category, the clock table is filtered according to the CDC category selected.

The following is a scenario where Timed button has been selected, and Timed safe CDC is only displayed in the clock table.

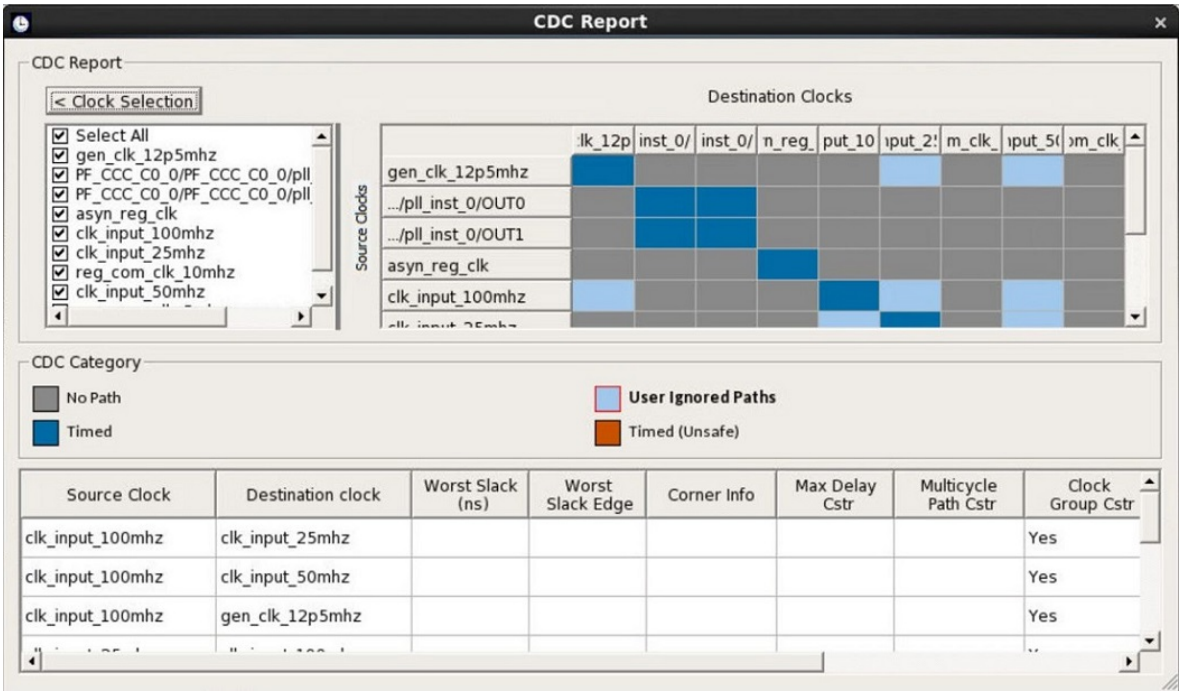
Figure 8-15. CDC Report When Timed Button is Selected in CDC Category



Worst Slack (ns)	Worst Slack Edge	CORNER INFO	Max Delay Cstr	Multicycle Path Cstr	Clock Group Cstr	Clock Uncertainty Cstr	Num of paths	Clock Pair Status
23.459	R R		No	Yes	No	0.5	1	Timed safe
3.928	R R		No	No	No		1	Timed safe

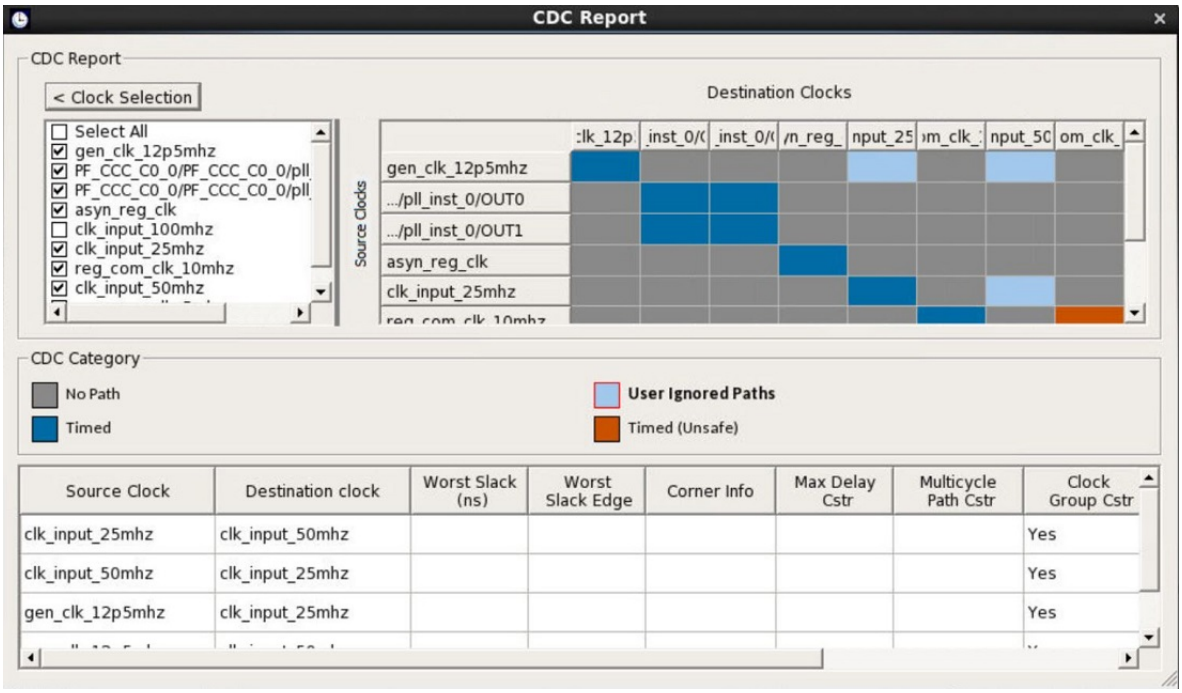
Clicking on the same CDC category shows the details for all the clocks selected in CDC report. Selecting/ unselecting clocks in clock selection does dynamically change the clock table along with the CDC table.

In the following figure, the User Ignored CDC category button is chosen and clk_input_100mhz is selected. Therefore, the clock is displayed in CDC table and clock table.



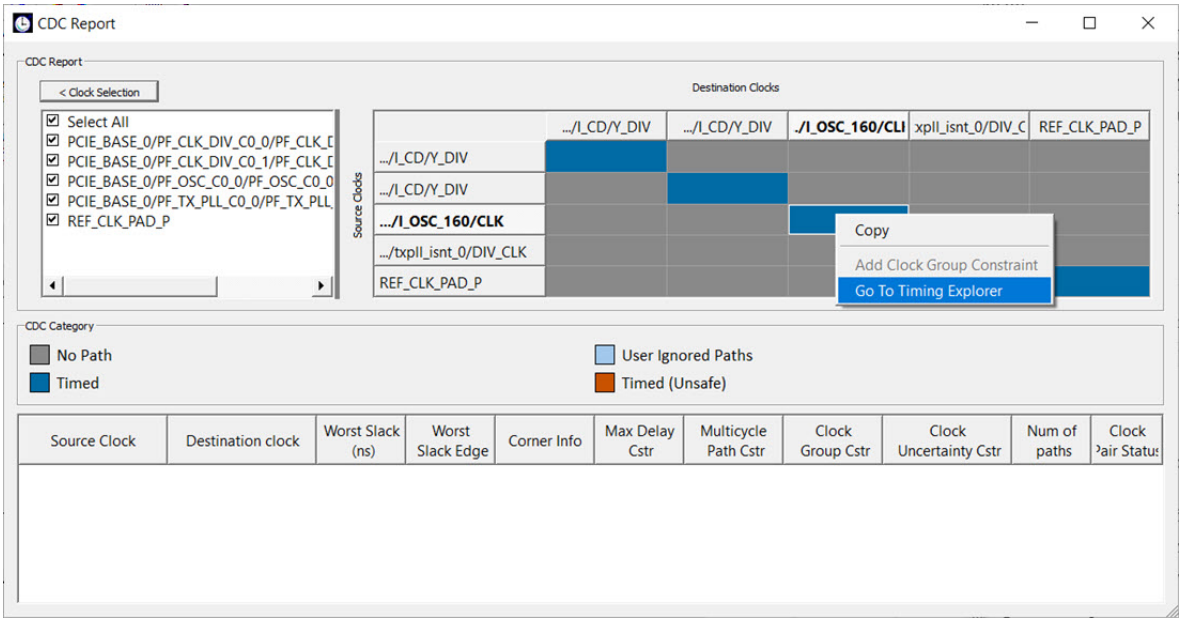
Source Clock	Destination clock	Worst Slack (ns)	Worst Slack Edge	Corner Info	Max Delay Cstr	Multicycle Path Cstr	Clock Group Cstr
clk_input_100mhz	clk_input_25mhz						Yes
clk_input_100mhz	clk_input_50mhz						Yes
clk_input_100mhz	gen_clk_12p5mhz						Yes

Now, when clock clk_input_100mhz is unselected, the same clock is moved from CDC table and the crossings related to that clock are also removed from clock table. Therefore, when the User Ignored CDC category is selected, entries related to clk_input_100mhz are not visible.



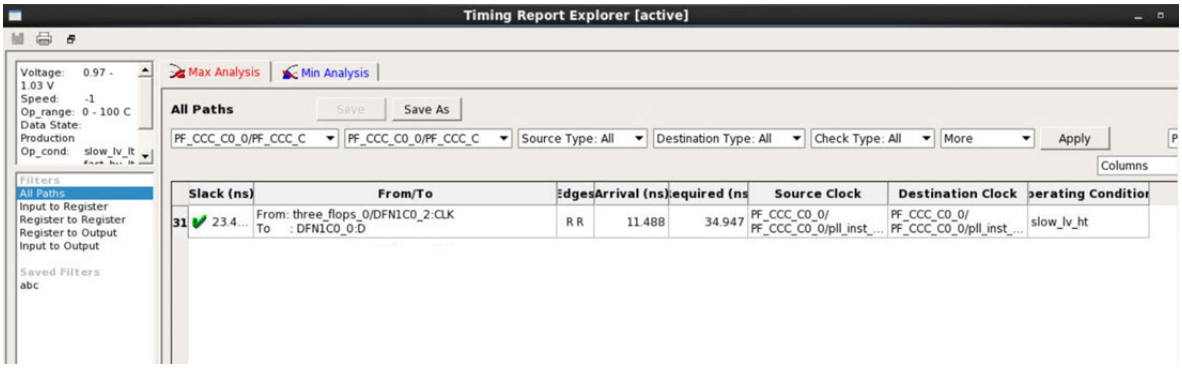
On right-clicking a CDC box, you can choose to **Copy**, **Add a Clock Group Constraint** or **Go to Timing Explorer**.

Figure 8-16. CDC Report with Go to Timing Explorer Option



Selecting the **Go to Timing Explorer** option opens the Timing Explorer dialog box.

Figure 8-17. Timing Report Explorer



There are corner scenarios when cross probing between CDC and Timing Explorer:

Scenario 1:

This is a scenario where difference is seen between SmartTime and Verify timing, when two clocks are defined on same port and when cross probing for CDC reg_com_clk_10mhz and reg_com_clk_5mhz is unable to find the same in Timing Report Explorer.

The constraints are as follows:

```
 create_clock -name {reg_com_clk_10mhz} -period 100 -waveform {0 50 } [ get_ports
{ reg_com_clk_10mhz } ]
create_clock -name {reg_com_clk_5mhz} -period 200 -waveform {0 100 } -add [ get_ports
{ reg_com_clk_10mhz } ]
```

The Timing Report Explorer does not pick reg_com_clk_5mhz as destination clock, and Smart time does pick the reg_com_clk_10mhz and reg_com_clk_5mhz pair as CDC, as shown in the following.

Figure 8-18. Timing Report Explorer Snapshot - 1

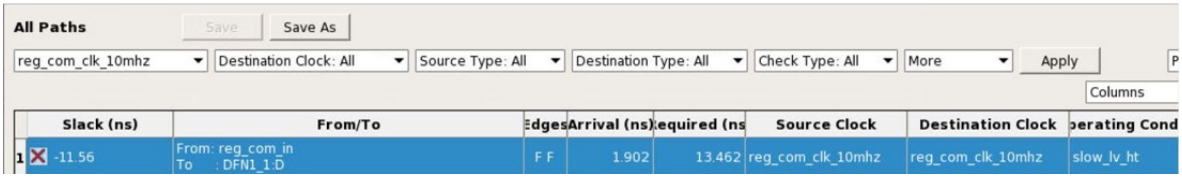


Figure 8-19. Timing Report Explorer Snapshot - 2

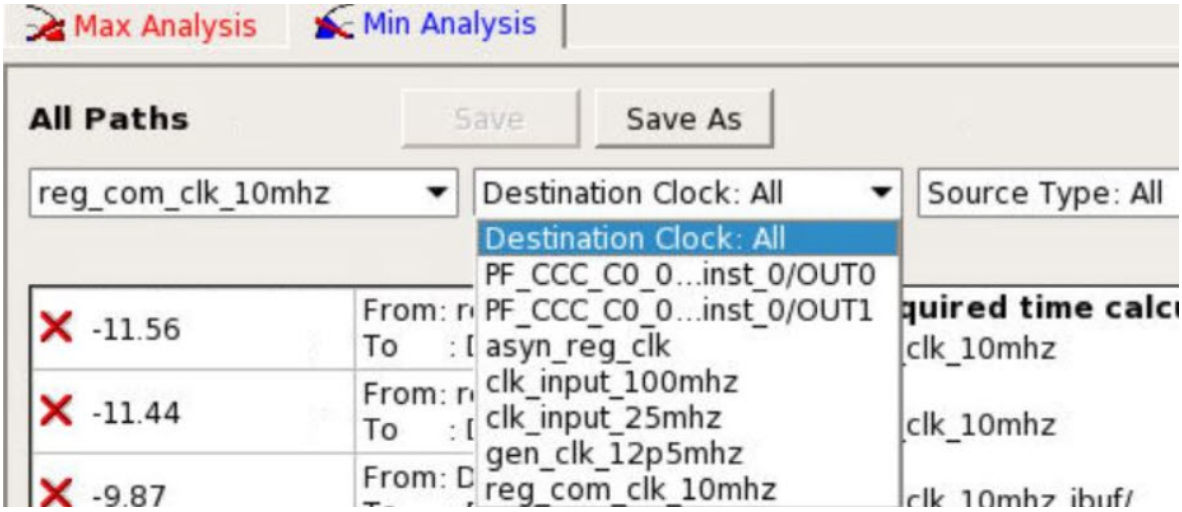


Figure 8-20. SmartTime Snapshot

Timing Explorer is picking the worst slack path for a pair of start and end point. Therefore, you can miss CDC and other reg to reg paths with lower slack values.

Scenario 2:

This is a scenario where due to different operating conditions set in Smart Time, you can have different results, when cross probing between CDC and Timing Report Explorer. SmartTime and CDC are in sync.

Figure 8-21. Worst Slack of 97.958 ns in Timing Report Explorer

Figure 8-22. Worst Slack of 98.154 ns in SmartTime

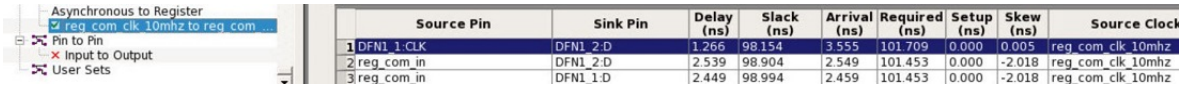


Figure 8-23. Operating Conditions

The Timing Report Explorer reports the path from slow_lv_lt, and SmartTime reports using the operating condition fast_hv_lt. When the operating condition in SmartTime is changed to slow_lv_lt, the worst slack becomes the same as in the Timing Report Explorer.

Figure 8-24. Slack After Changing the Operating Condition to slow_lv_lt

CDC reports worst path for a particular corner selected in SmartTime, and Timing Report Explorer reports the worst path across all the corners.

In such cases, you can see changes in values when navigating from CDC to Timing Report Explorer. To make you aware of such situations, Corner Info column is added to display the operating conditions.

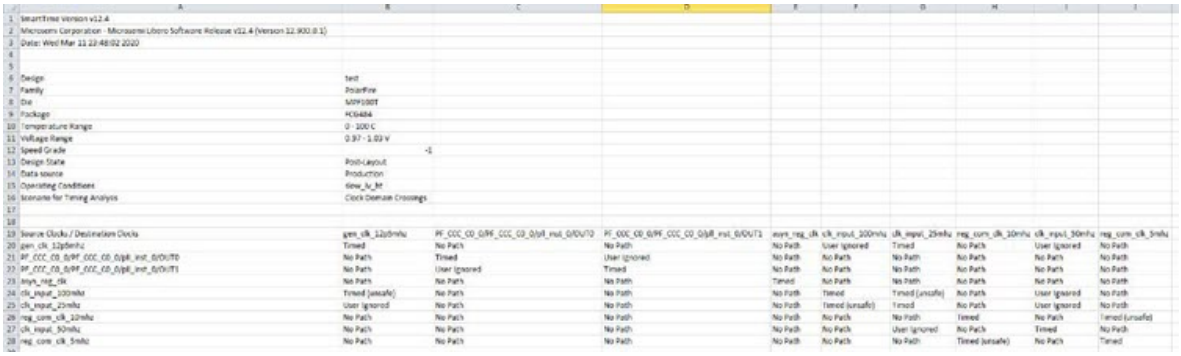
Note:

- The path details for the same clock crossing (C1 to C1) are not shown in the path tale as they are not valid clock crossings and are currently shown as timed safe by default in CDC report.
- The clock table has CDC details only related to clocks checked in clock selection from CDC report.
- Path table will not show any CDC having no paths.
- For User Ignored CDC columns, “Worst Slack (ns)”, “Worst Slack Edge”, “Max Delay Cstr”, “Multicycle Path Cstr”, and “Clock Uncertainty Cstr” are empty.
- Cross probing is allowed to Timing Report Explorer for the same clock crossing (C1 to C1).
- For User Ignored CDC category, Corner Info column is empty.

Selecting **Comma Separated Value** exports the CDC Report to a CSV file. If you select this option, a window appears in which you assign a name to the CSV file and specify the location where it will be exported. The

CSV file shows details about the CDC between each clock domain in numeric format. Each CDC type is represented as a number similar to colors in the table. The CSV file includes an explanation of each number type and CDC type.

Figure 8-25. Sample CSV Report



	A	B	C	D	E	F	G	H	I	J
1	SmartTime Version v12.4									
2	Microsemi Corporation - Microsemi Libero Software Release v12.4 (Version 12.900.0.1)									
3	Date: Wed Mar 11 23:48:02 2020									
4										
5										
6	Design	test								
7	Family	PolarFire								
8	Die	MPF100T								
9	Package	FCG484								
10	Temperature Range	0 - 100 C								
11	Voltage Range	0.97 - 1.03 V								
12	Speed Grade	-1								
13	Design State	Post-Layout								
14	Data source	Production								
15	Operating Conditions	slow_lv_ht								
16	Scenario for Timing Analysis	Clock Domain Crossings								
17										
18										
19	Source Clocks / Destination Clocks	gen_clk_12p5mhz	PF_CCC_C0_0/PF_CCC_C0_0/pll_inst_0/OUT0	PF_CCC_C0_0/PF_CCC_C0_0/pll_inst_0/OUT1	async_reg_clk	clk_input_100mhz	clk_input_25mhz	reg_core_clk_10mhz	clk_input_50mhz	reg_core_clk_5mhz
20	gen_clk_12p5mhz	Timed	No Path	No Path	No Path	User Ignored	Timed	No Path	User Ignored	No Path
21	PF_CCC_C0_0/PF_CCC_C0_0/pll_inst_0/OUT0	No Path	Timed	User Ignored	No Path	No Path	No Path	No Path	No Path	No Path
22	PF_CCC_C0_0/PF_CCC_C0_0/pll_inst_0/OUT1	No Path	User Ignored	Timed	No Path	No Path	No Path	No Path	No Path	No Path
23	async_reg_clk	No Path	No Path	No Path	Timed	No Path	No Path	No Path	No Path	No Path
24	clk_input_100mhz	Timed (unsafe)	No Path	No Path	No Path	Timed	Timed (unsafe)	No Path	User Ignored	No Path
25	clk_input_25mhz	User Ignored	No Path	No Path	No Path	Timed (unsafe)	Timed	No Path	User Ignored	No Path
26	reg_core_clk_10mhz	No Path	No Path	No Path	No Path	No Path	No Path	Timed	No Path	Timed (unsafe)
27	clk_input_50mhz	No Path	No Path	No Path	No Path	No Path	User Ignored	No Path	Timed	No Path
28	reg_core_clk_5mhz	No Path	No Path	No Path	No Path	No Path	No Path	Timed (unsafe)	No Path	Timed

9. Timing Concepts

The following sections describe timing concepts associated with the RTG4 FPGA Clock Conditioning Circuit with PLL configuration.

9.1 Static Timing Analysis Versus Dynamic Simulation

STA offers an efficient technique for identifying timing violations in your design and ensuring that it meets all your timing requirements. You can communicate timing requirements and timing exceptions to the system by setting timing constraints. A static timing analysis tool will then check and report setup and hold violations as well as violations on specific path requirements.

STA is well suited for traditional synchronous designs. The main advantage of STA is that, unlike dynamic simulation, it does not require input vectors. It covers all possible paths in the design and does all the above with relatively low run-time requirements. The major disadvantage of STA is that the STA tools do not automatically detect false paths in their algorithms.

9.2 Delay Models

The first step in timing analysis is the computation of single component delays. These components can be either a combinational gate or block or a single interconnect connecting two components.

Gates that are part of the library are pre-characterized with delays under different parameters, such as input-slew rates or capacitive loads. Traditional models provide delays between each pair of I/Os of the gate and between rising and falling edges.

The accuracy with which interconnect delays are computed depends on the design phase. These can be estimated using a simple Wire Load Model (WLM) at the pre-layout phase or a more complex Resistor and Capacitor (RC) tree solver at the post-layout phase.

9.3 Timing Path Types

Path delays are computed by adding delay values across a chain of gates and interconnects. SmartTime uses this information to check for timing violations. Traditionally, timing paths are presented by static timing analysis tools in four categories or "sets."

- **Paths between sequential components internal to the design**. SmartTime displays this category under the Register to Register set of each displayed clock domain.
- **Paths that start at input ports and end at sequential components internal to the design**. SmartTime displays this category under the External Setup and External Hold sets of each displayed clock domain.
- **Paths that start at sequential components internal to the design and end at output ports**. SmartTime displays this category under the Clock to Out set of each displayed clock domain.
- **Paths that start at input ports and end at output ports**. SmartTime displays this category under the Input to Output set.

9.4 Maximum Clock Frequency

Generally, you set clock constraints on clocks for which you have a specified requirement. The absence of violations indicates that this clock can run at least at the specified frequency. However, in the absence of such requirements, you may still be interested in computing the maximum frequency of a specific clock domain.

To obtain the maximum clock frequency, a static timing analysis tool computes the minimum period for each path between two sequential elements. To compute the maximum period, the tool evaluates the maximum data path delay and the minimum skew between the two elements, as well as the setup on the receiving sequential element. It also considers the polarity of each sequential element. The maximum frequency is the inverse of the largest value among the maximum period of all the paths in the clock domain. The path responsible for limiting the frequency of a given clock is called the “critical path.”

9.5 Setup Check

The setup and hold check ensures that the design works as specified at the required clock frequency.

Setup check specifies when data is required to be present at the input of a sequential component so that the clock can capture the data effectively into the component. Timing analyzers evaluate the setup check as a maximum timing budget allowed between adjacent sequential elements.

For more information about how setup check is processed, see Arrival Time, Required Time, and Slack.

9.6 Arrival Time, Required Time, and Slack

You can use arrival time and required time to verify timing requirements in the presence of constraints. The following simple example is applied to verify the clock requirement for setup between sequential elements in the design.

The arrival time represents the time at which the data arrives at the input of the receiving sequential element. In this example, the arrival time is considered from the setup launch edge at CK, taken as a time reference (instant zero). It follows the clock network along the blue line until the clock pin on FF1 (delay d1). Then it continues along the data path always following the blue line until the data pin D on FF2. Therefore,

Arrival_TimeFF2:D = d1 + d2

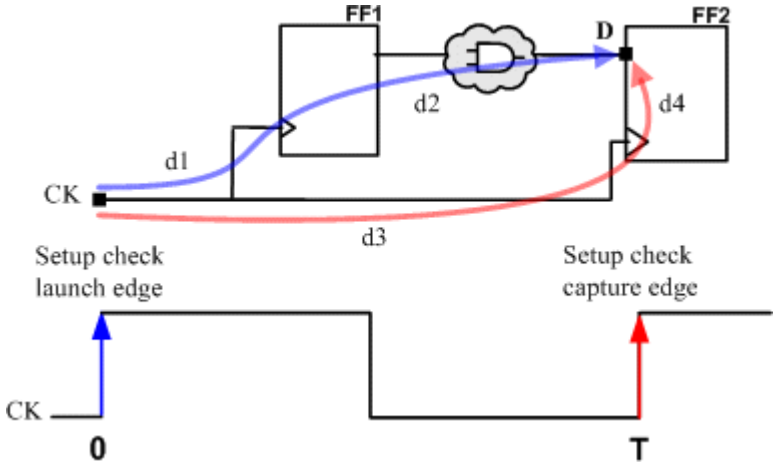
The required time represents when the data is required to be present at the same pin FF2:D. Assume in this example that in the presence of an FF with the same polarity, the capturing edge is simply one cycle following the launch edge. Using the period T provided to the tool through the clock constraint, the event gets propagated through the clock network along the red line until the clock pin of FF2 (delay d3). Taking FF2 setup (delay d4) into account. This means the clock constraint requires the data to be present d4 time before the capturing clock edge on FF2. Therefore, the required time is:

Required_TimeFF2:D = T + d3 - d4

If the slack is negative, the path is violating the setup relationship between the two sequential elements.

The slack is simply the difference between the required time and arrival time: SlackFF2:D = Required_TimeFF2:D - Arrival_TimeFF2:D

Figure 9-1. Arrival Time and Required Time for Setup Check



9.7 Timing Exceptions Overview

Use timing exceptions to overwrite the default behavior of the design path.

Timing exceptions include:

- Setting multicycle constraint to specify paths that (by design) will take more than one cycle.

- Setting a false path constraint to identify paths that must not be included in the timing analysis or the optimization flow.
- Setting a maximum/minimum delay constraint on specific paths to relax or to tighten the original clock constraint requirement.

9.8 Clock Skew

The clock skew between two sequential components is the difference between the insertion delays from the clock source to the clock pins of these components. SmartTime calculates the arrival time at the clock pin of each sequential component. Then it subtracts the arrival time at the receiving component from the arrival time at the launching component to obtain an accurate clock skew.

Both setup and hold checks must account for clock skew. However, for setup check, SmartTime looks for the smallest skew. This skew is computed by using the maximum insertion delay to the launching sequential component and the shortest insertion delay to the receiving component.

For hold check, SmartTime looks for the largest skew. This skew is computed by using the shortest insertion delay to the launching sequential component and the largest insertion delay to the receiving component.

SmartTime makes the distinction between setup and hold checks and hold checks automatically.

9.9 Cross Probing

Design objects displayed in SmartTime can be cross-probed into other Libero SoC tools. Libero SoC allows cross-probing from SmartTime to the Constraints Editor (but not vice versa) and from SmartTime to Chip Planner (but not vice versa). When cross-probing from SmartTime to one of the other tools, both SmartTime and the other tool must first be opened.

9.9.1 Cross-probing from SmartTime into the Constraints Editor

To add a timing exception constraint from SmartTime and have the Constraints Editor display the constraint:

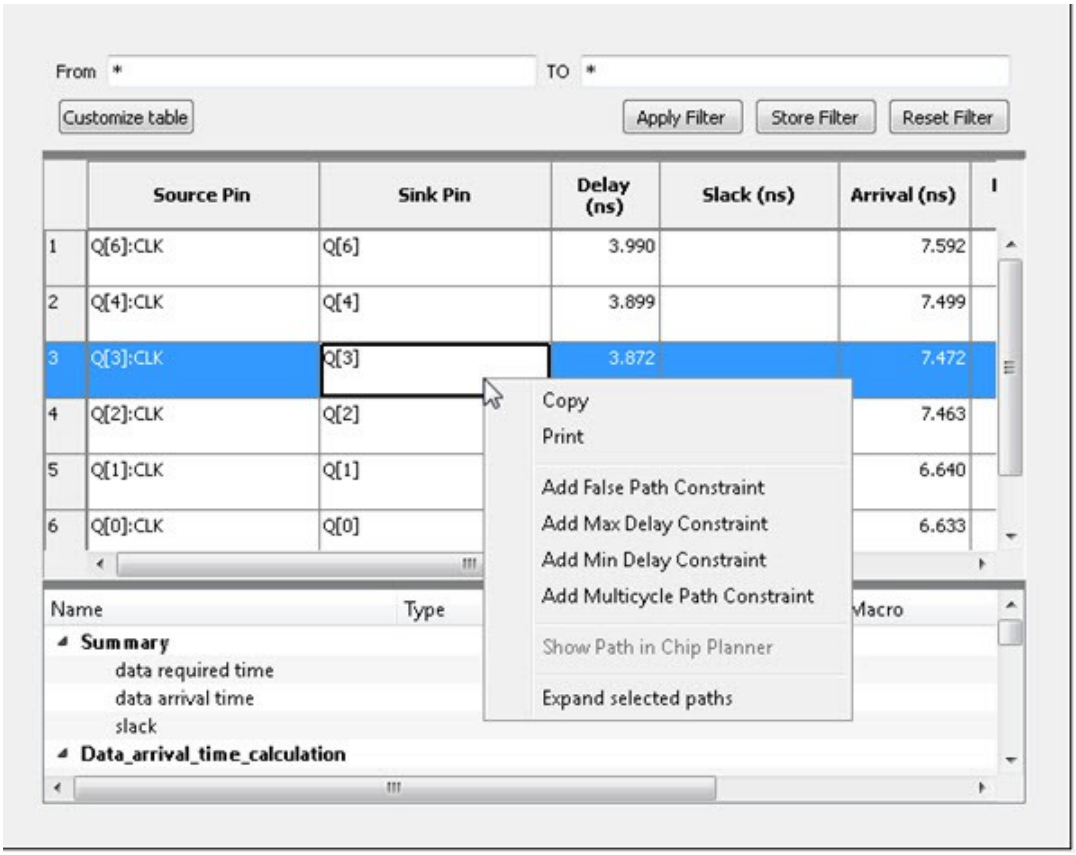
1. From the SmartTime Maximum or Minimum Delay Analysis view, click a timing path to add a timing exception constraint.
2. When the Constraints Editor's Add Constraint dialog box appears, the fields for source (from) pin and destination (to) pin are populated with the correct names from the timing path you selected.

9.9.2 Adding a Timing Exception Constraint from a Timing Path

To add a timing exception constraint from a timing path in SmartTime Max/Min Delay Analysis View:

1. Open SmartTime (**Design Flow Window > Verify Timing > Open interactively**).
2. Open the Constraints Editor (**Constraint Manager > Timing Tab > Edit with Constraints Editor**).
3. Select Max/Min Delay Analysis View, and then right-click a timing path in the table.
4. Select a timing exception constraint to add:
    - False Path Constraint
    - Maximum Delay Constraint
    - Minimum Delay Constraint
    - Multicycle Path Constraint

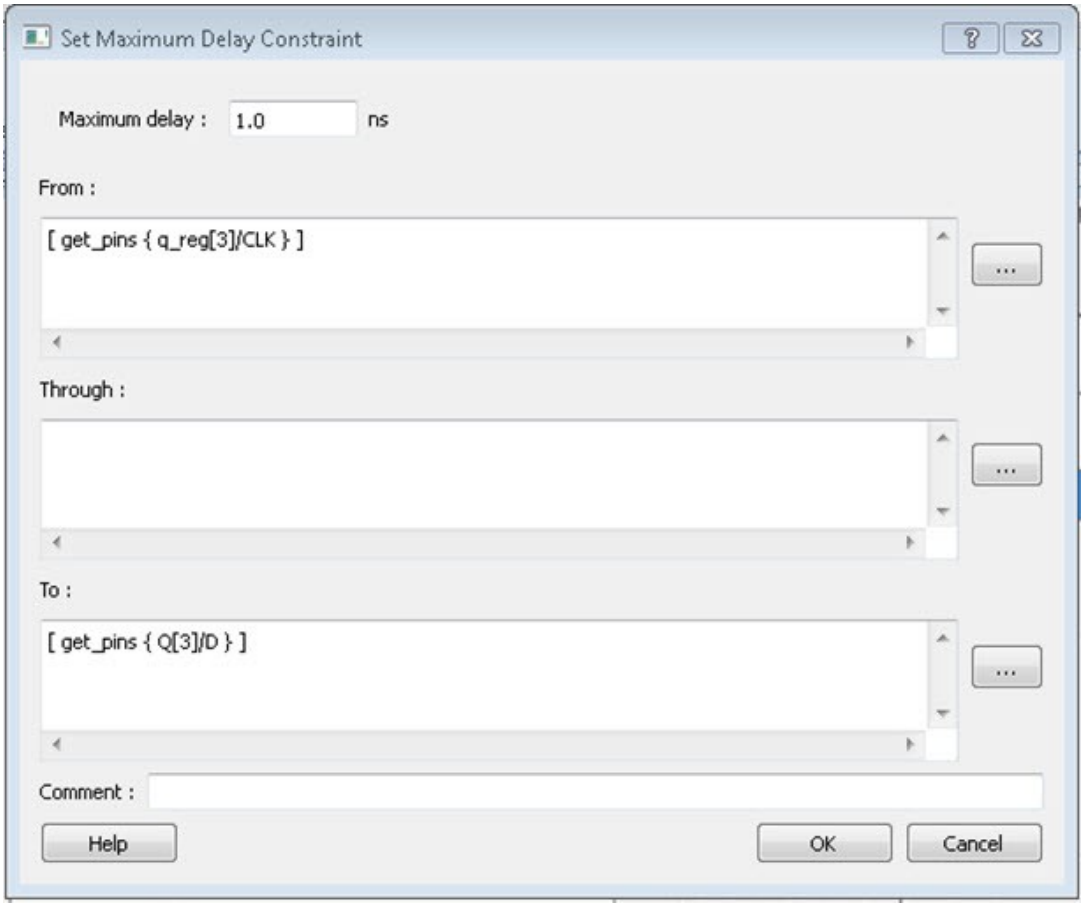
Figure 9-2. Add Timing Constraint from SmartTime's Reported Timing Path



Note: If the Constraint Editor is not open, the **Add Max/Min Delay**, **False Path**, and **Multicycle Path Constraint** menu items are grayed out.

5. Add the Constraint in the Add Constraint dialog box. The **source/from pin** and **destination/to pin** fields are populated with the appropriate pin names captured from the SmartTime reported path (Source Pin and Sink Pin) you clicked.
    a) Click **OK** to exit the Add Constraint dialog box.
    b) Click **Save** in the Constraints Editor.
    c) Exit the Constraints Editor.
    d) Exit SmartTime.
    e) If the newly added constraint that is added to a file (the Target file) is used for Place and Route and Verify Timing, rerun Place and Route.
    f) Open SmartTime Maximum/Minimum Delay Analysis View.

Figure 9-3. Add Maximum Delay Constraint



9.9.3 Cross-probing from SmartTime to Chip Planner

Cross-probing of design objects is available from SmartTime to Chip Planner, but not vice versa. Cross-probing allows you to select a design object in one application and display the selected object in another application.

Complete the Place and Route step on the design, and then open both SmartTime and Chip Planner.
Because Libero SoC allows you to cross-probe design objects from SmartTime to Chip Planner, you can better understand how the two applications interact with each other. With cross-probing, a timing path not meeting timing requirements can be fixed with relative ease when you see the less-than-optimal placement of the design object (in terms of timing requirements) in Chip Planner. Cross-probing from SmartTime to Chip Planner is available for the following design objects:

- Macros
- Ports
- Nets/Paths

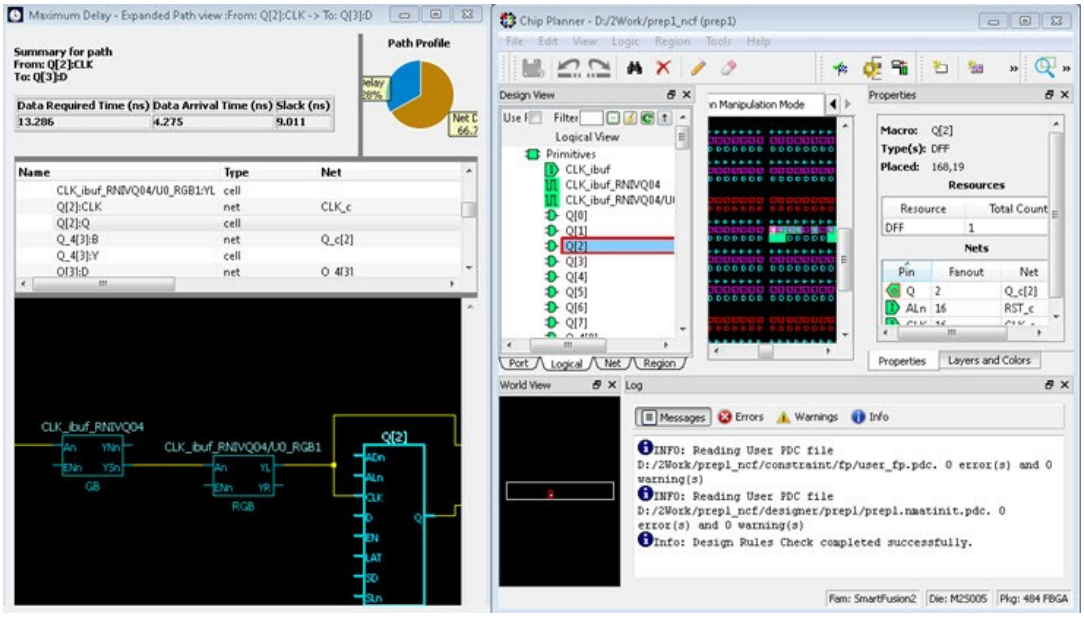
To cross-probe from SmartTime to Chip Planner, use a design macro in SmartTime.

9.9.4 Design Macro Example

1. Make sure the design completed the Place and Route step successfully.
2. Open SmartTime Maximum/Minimum Analysis View.
3. Open Chip Planner.
4. In the SmartTime Maximum Analysis View, right-click the instance Q[2] in the Timing Path Graph and choose **Show in Chip Planner**.
   The Properties window in Chip Planner displays the properties of Q[2].With cross-probing, the Q[2] macro is selected in Chip Planner's Logical View and highlighted (white) in the Chip Canvas.

Note: If Chip Planner is not open, **Show in Chip Planner** is gray and unavailable.

Figure 9-4. Cross-Probing – Macro



5. If necessary, zoom in to view the highlighted Q2 Macro in the Chip Canvas.

9.9.5 Timing Path Example

The following procedure provides an example of working with timing paths.

1. Make sure the design completed the Place and Route step successfully .
2. Open SmartTime Maximum/Minimum Analysis View.
3. Open Chip Planner.
4. In the SmartTime Maximum/Minimum Analysis View, right-click the net CLK_ibuf/U0/U_IOPAD:PAD in the table and choose **Show Path in Chip Planner**.
   The net is selected (highlighted in red) in the Chip Canvas view and the three macros connected to the net are highlighted in white in the Chip Canvas view.
   Note: If Chip Planner is not open, **Show Path** in Chip Planner is gray and unavailable.

Figure 9-5. Cross-Probing – Timing Path

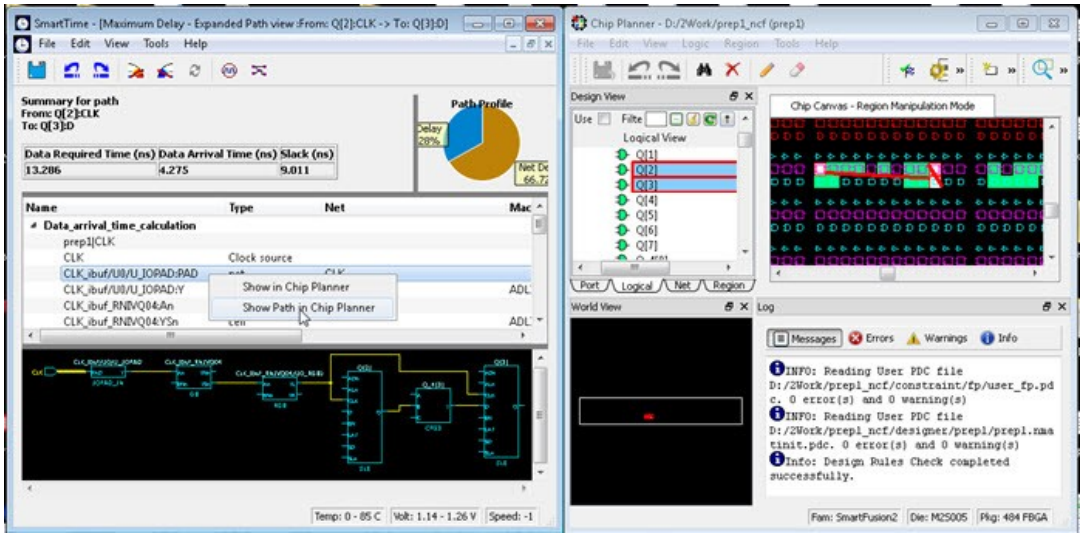
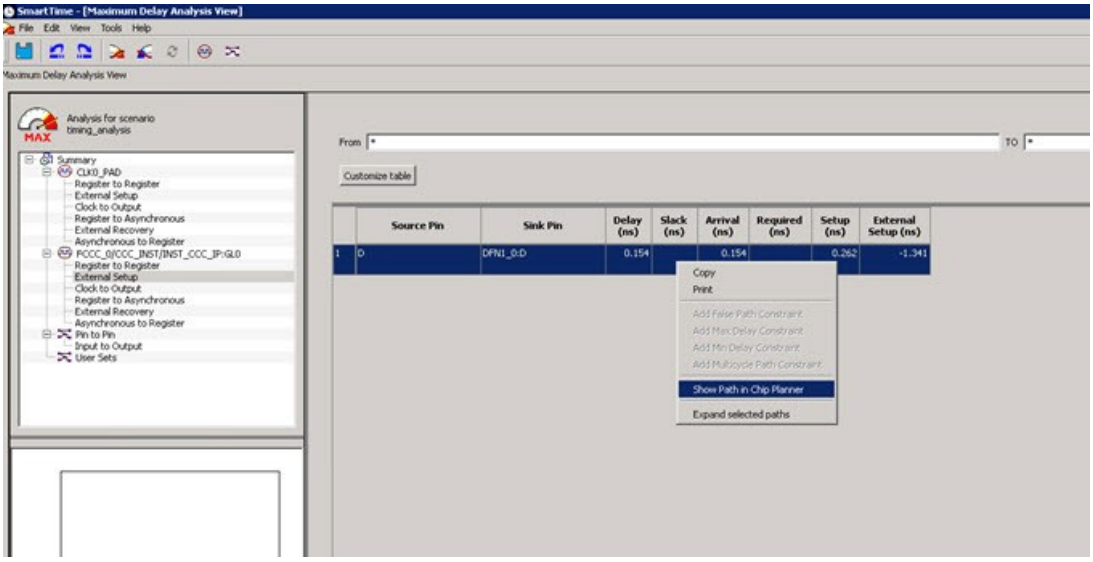


Figure 9-6. Cross-Probing Path from Max/Min Delay Analysis View Table

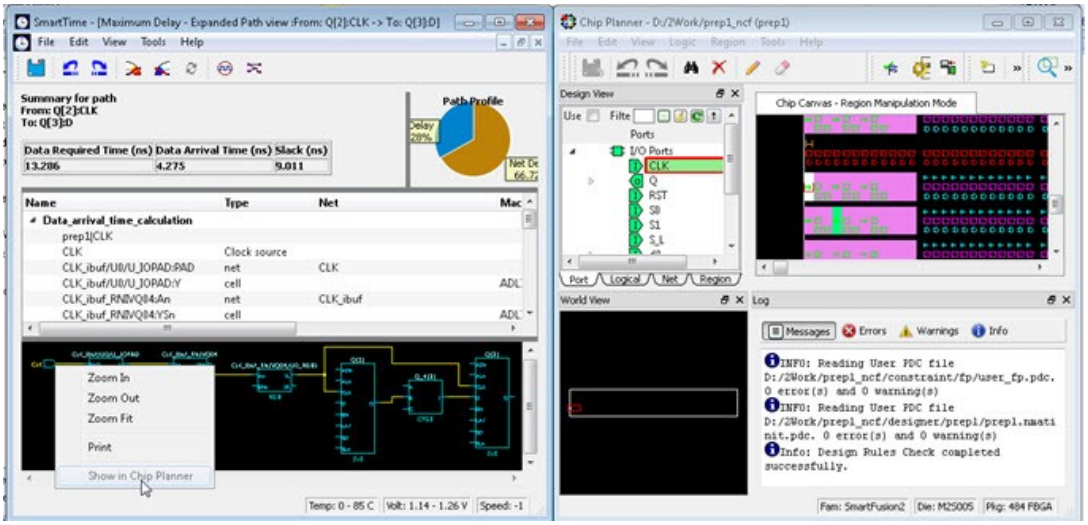


Instead of performing step 4, you can right-click a path in the Max/Min Delay Analysis View and choose **Show Path in Chip Planner** to cross-probe the path.

9.9.6 Port Example

1. Make sure the design completed the Place and Route step successfully.
2. Open SmartTime Maximum/Minimum Analysis View.
3. Open Chip Planner.
4. In the SmartTime Maximum/Minimum Analysis View, right-click the Port “CLK” in the Path and choose **Show in Chip Planner**.
   The Port “CLK” is selected and highlighted in the Chip Planner Port View.
   Note: If Chip Planner is not open, **Show in Chip Planner** is gray and unavailable.

Figure 9-7. Cross-Probing – Port

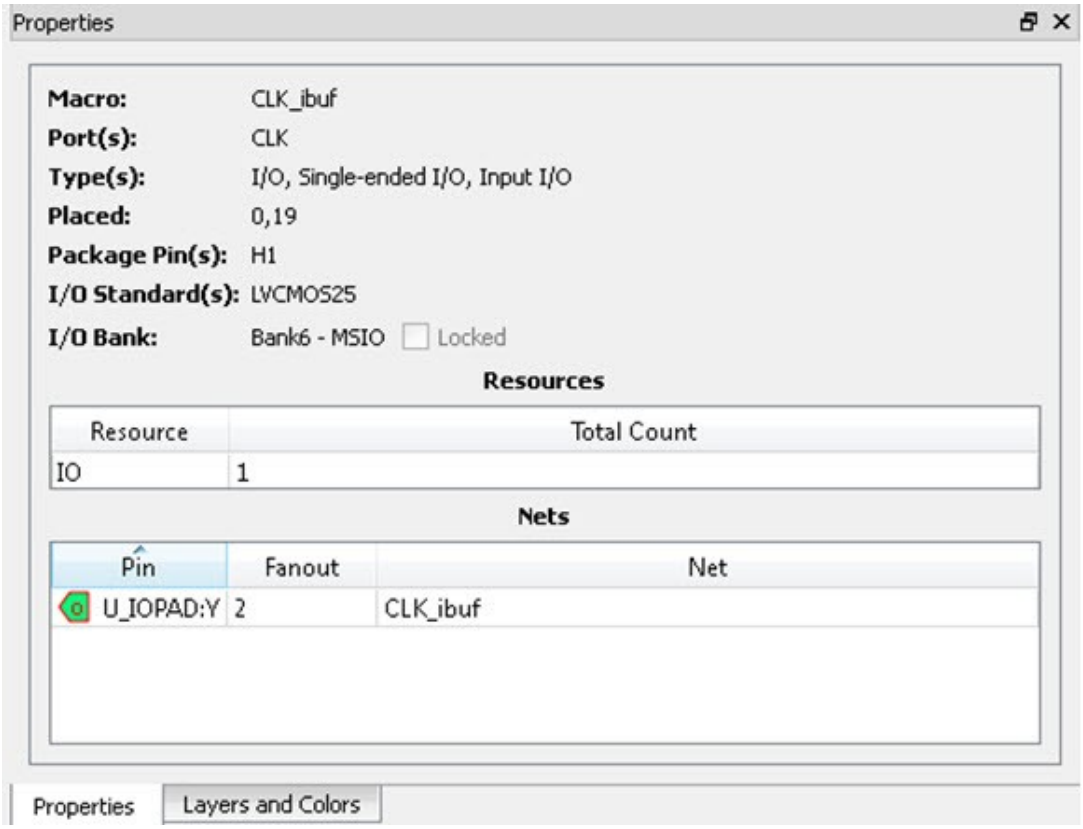


From the Properties View inside Chip Planner, you will find useful information about the Port “CLK” you are cross- probing:

- Port Type
- Port Placement Location (X-Y coordinates)
- I/O Bank Number

- I/O Standard
- Pin Assignment

Figure 9-8. Properties View of Port “CLK”



10. SmartTime Tutorials

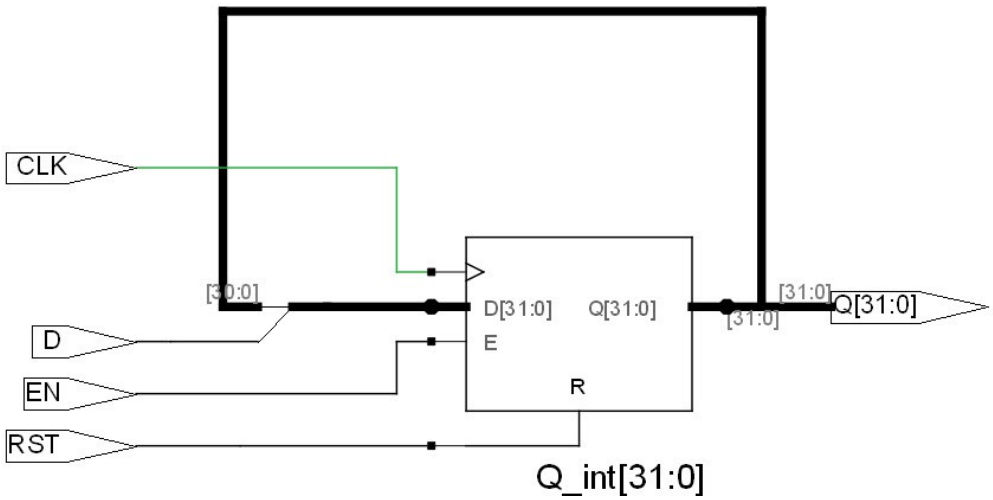
The following sections describe SmartTime tutorials.

10.1 Tutorial 1 - 32-Bit Shift Register with Clock Enable

This tutorial describes how to enter a clock constraint for the 32-bit shift register on SmartFusion2 device.

You will use the SmartTime Constraints Editor and perform post-layout timing analysis using the SmartTime Timing Analyzer.

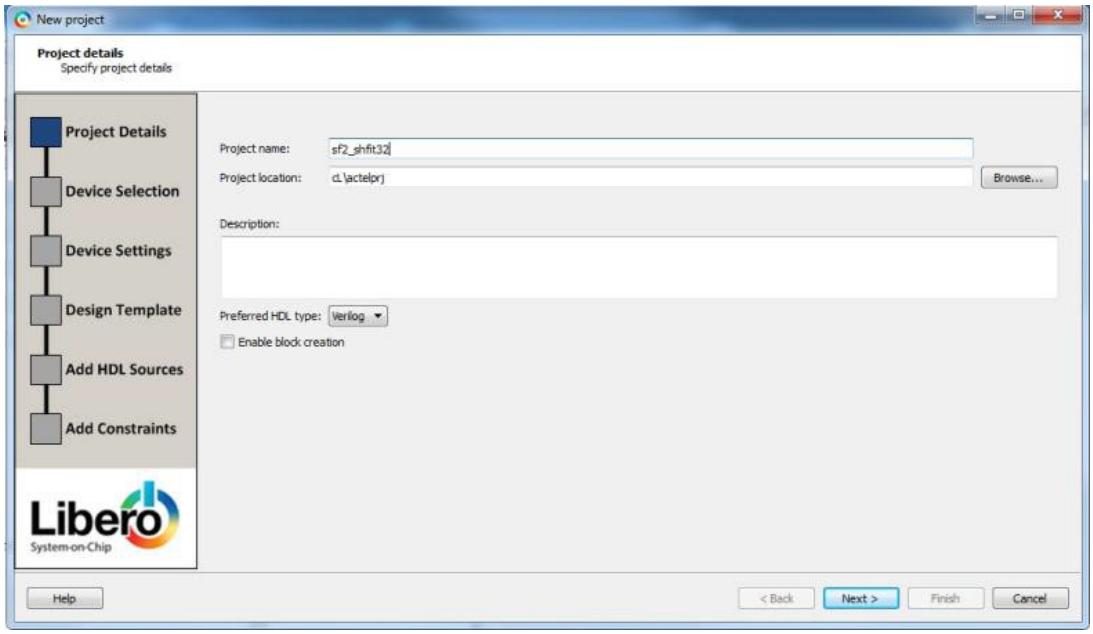
Figure 10-1. 32-bit Shift Register



To set up your project:

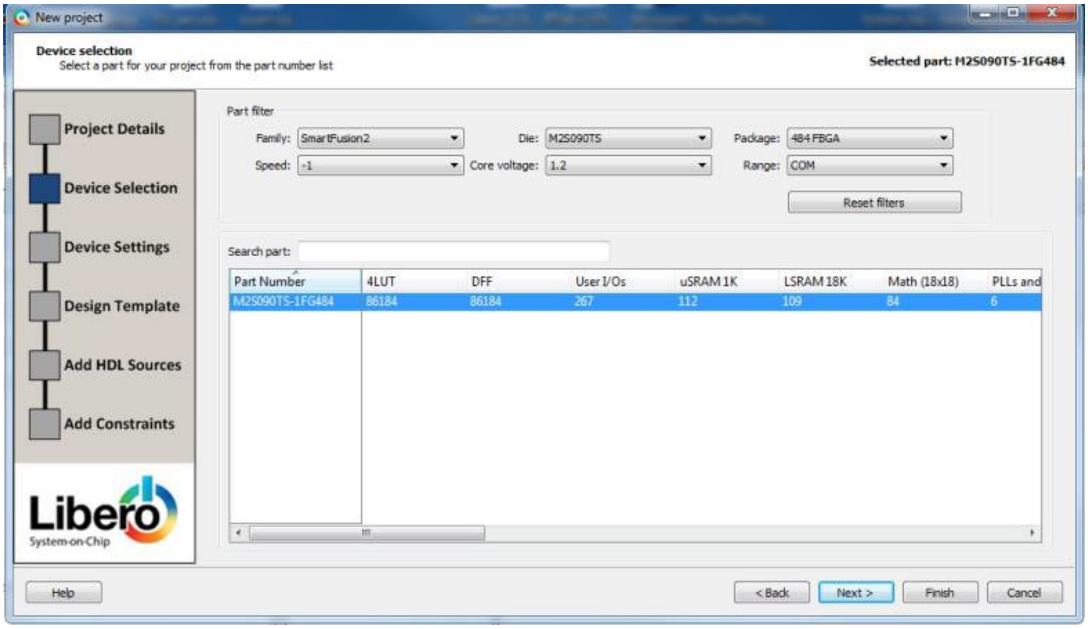
1. Invoke Libero SoC. From the **Project** menu, choose **New Project**.
2. Type `sf2_shift32` for your new project name and browse to a folder for your project location.
3. Select **Verilog** as the Preferred HDL Type.
4. Leave all other settings at their default values.

Figure 10-2. New Project Creation - 32 Bit Shift Register



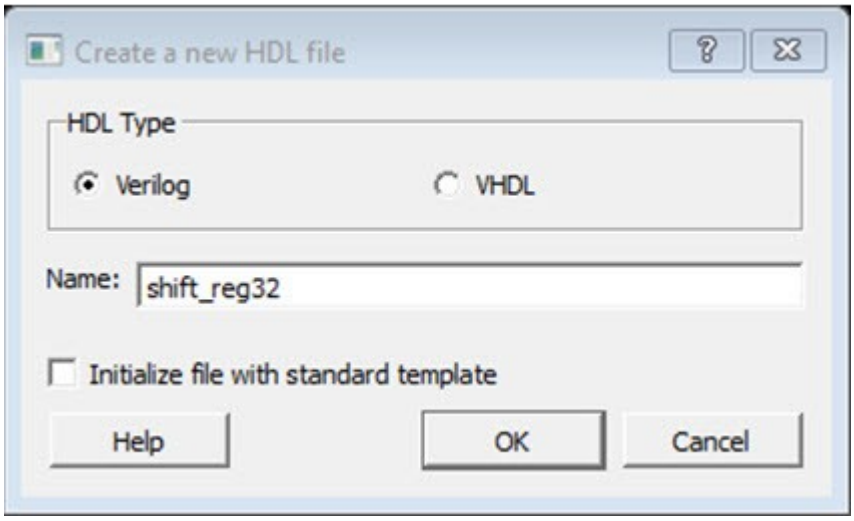
5. Click **Next** to go to Device Selection page. Make the following selection from the pull-down menus:
   - **Family**: SmartFusion2
   - **Die**: M2S090TS
   - **Package**: 484 FBGA
   - **Speed**: STD
   - **Core Voltage**: 1.2 V
   - **Range**: COM

Figure 10-3. Selections from Pull-down Menus



6. Click the M2S090TS-1FG484 part number and click .
7. Accept the default settings in the Device Settings page and click **Next**.
8. Accept the default settings in the Design Template page and click **Next**.
9. Click **Next** to go to the Add Constraints page.
10. Since you are not adding any constraints, click **Finish** to exit the New Project Creation wizard.
11. To add a new HDL file, select **File> New> HDL**.
    The Create a new HDL file dialog box appears.
12. Name the HDL file `shift_reg32` as shown below and click **OK**.

Figure 10-4. Create a New HDL File Dialog Box

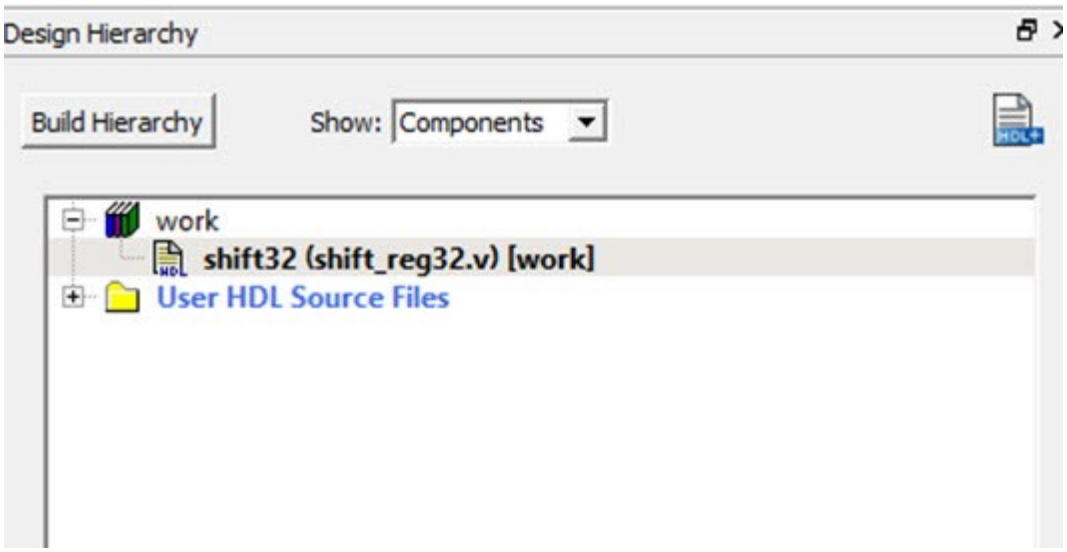


13. Copy the following code and paste it into the Verilog file:

```
module shift32 ( Q,CLK,D,EN,RESET); input D,EN,CLK,RESET;
output[31:0] Q; reg [31:0] Q_int;
assign Q=Q_int;
always@ (posedge CLK) begin
if(RESET)
Q_int<=0; else begin if(EN)
Q_int<={Q_int[30:0],D}; end
end endmodule
```

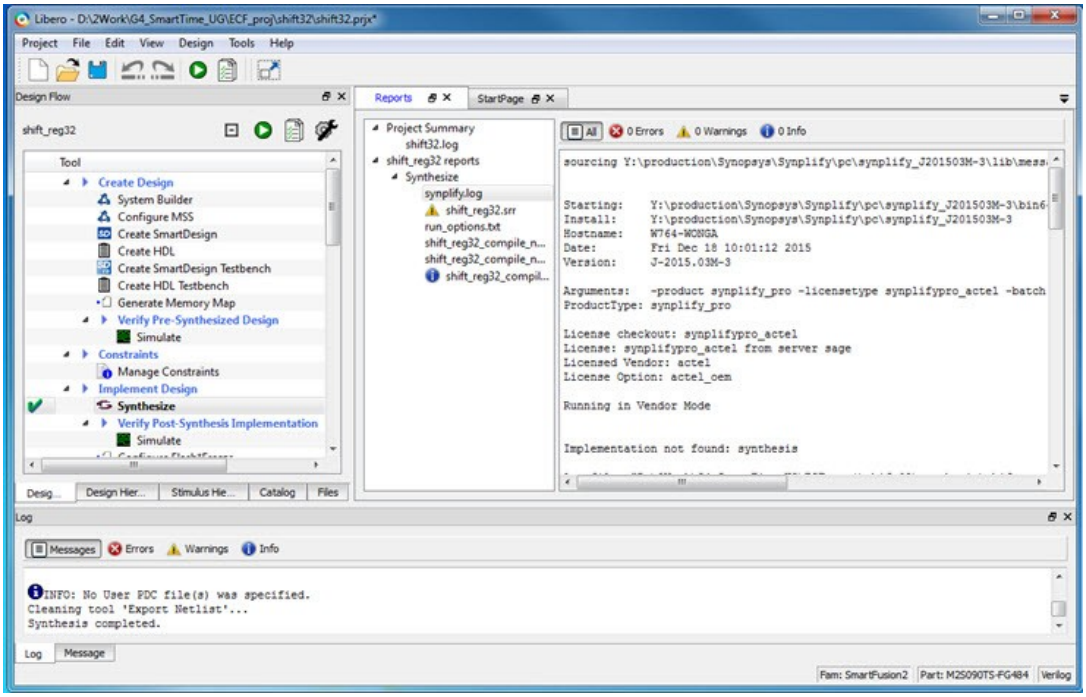
14. Check the HDL file to confirm there are no syntax errors.
15. Confirm that the shift_reg32 design appears in the Design Hierarchy window, as shown in the following figure.

Figure 10-5. shift_reg32 in the Design Hierarchy Window



16. In the Design Flow window, double-click **Synthesize** to run Synplify Pro with default settings. A green check mark appears next to **Synthesize** when Synthesis is successful, as shown in the following figure.

Figure 10-6. Synthesis and Compile Complete - 32-Bit Shift Register with Clock Enable

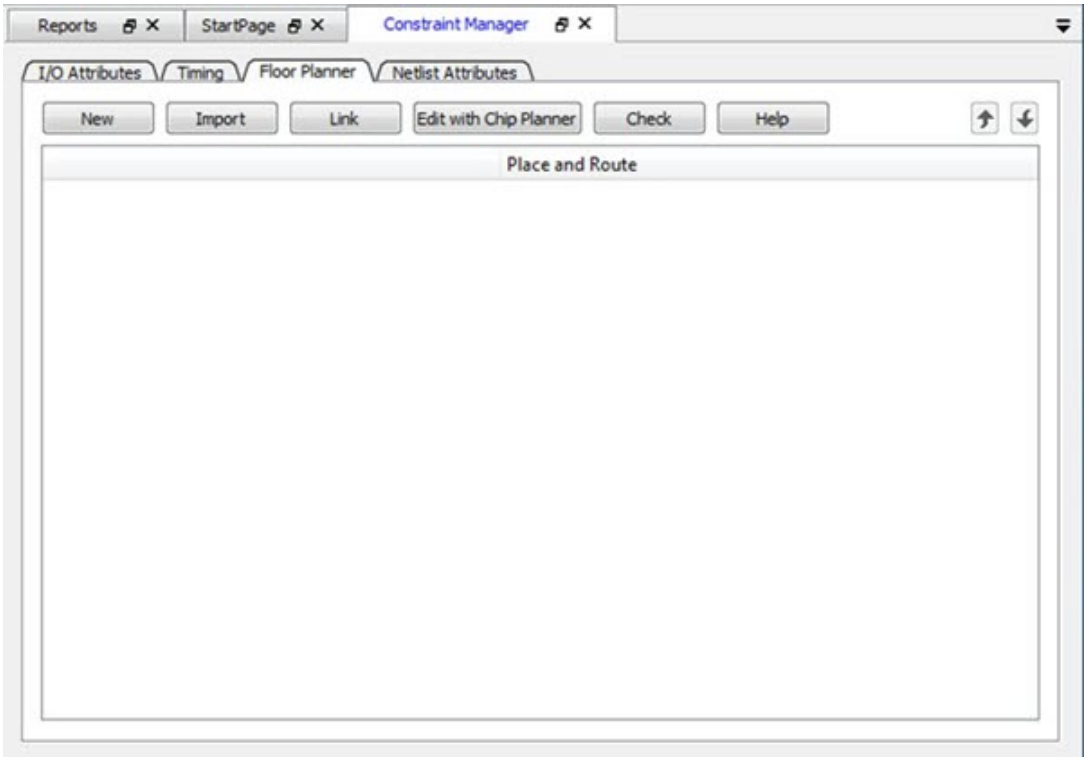


10.1.1 Add a Clock Constraint - 32 Bit Shift Register

To add a clock constraint to your design:

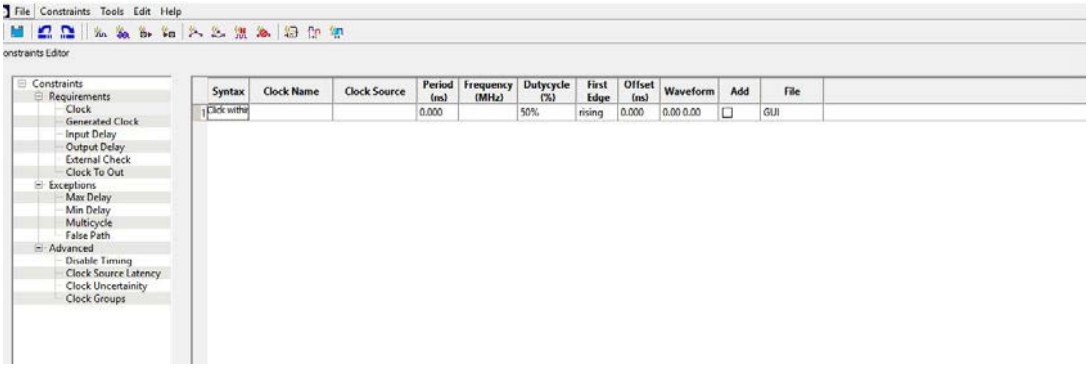
1. In the Design Flow window, double-click **Manage Constraints**.
   The Constraint Manager appears.

Figure 10-7. Constraint Manager



2. Click the **Timing** tab.
3. Click **Edit with Constraints Editor > Edit Place and Route Constraints**.

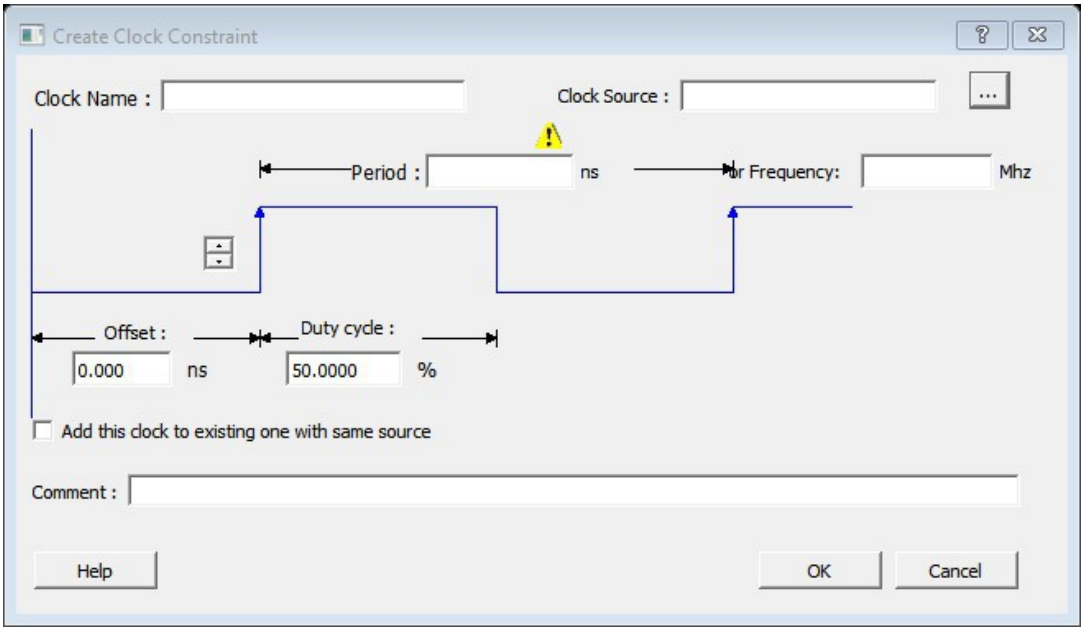
Figure 10-8. Constraints Editor – Add Clock Constraint



The Constraints Editor appears.

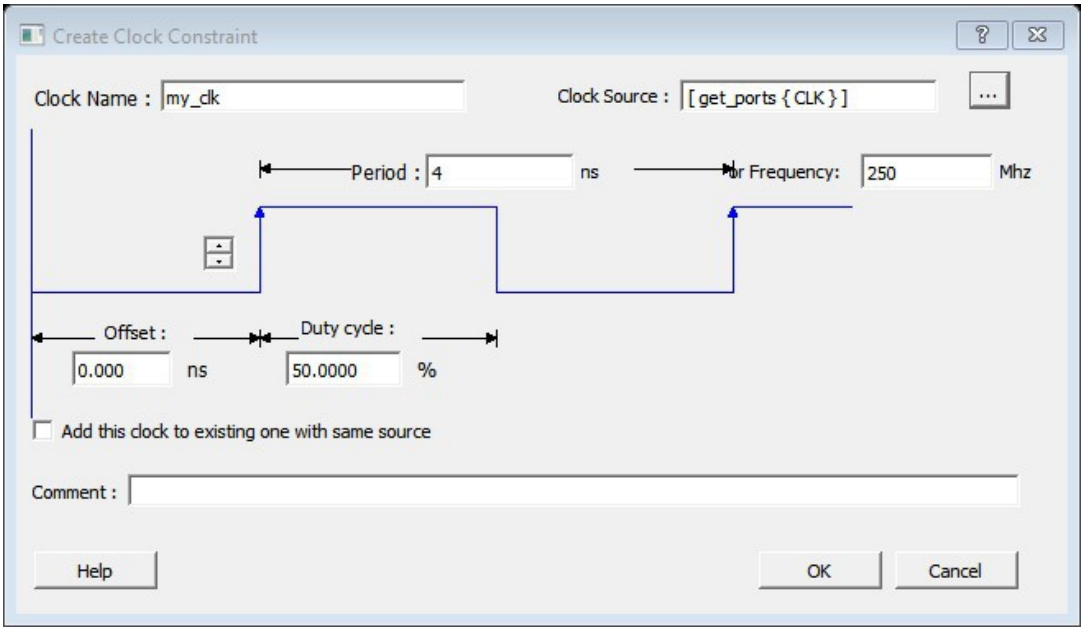
4. In the Constraints Editor, right-click **Clock** under **Requirement** and select **Add Clock Constraint**.
The Create Clock Constraint dialog box appears.

Figure 10-9. Create Clock Constraint Dialog Box



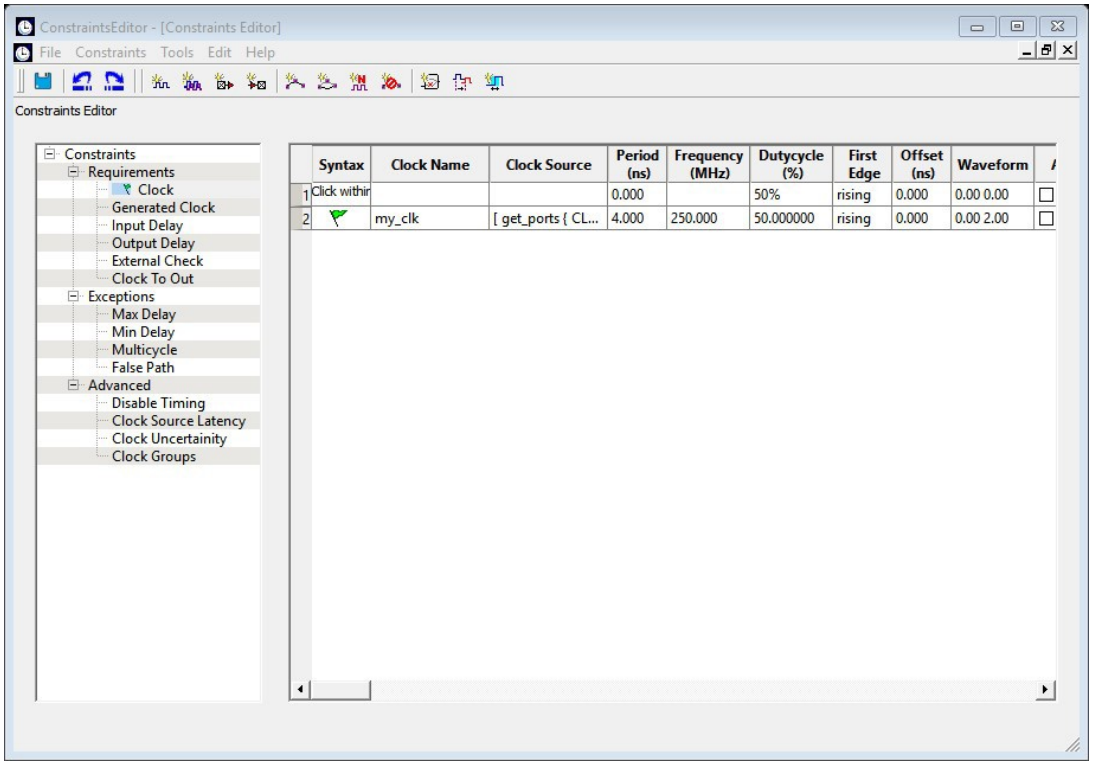
5. From the **Clock Source** drop-down menu, choose the **CLK** pin.
6. In the **Clock Name** field, type `my_clk`.
7. Set the **Frequency** to 250 MHz (as shown in the following figure) and accept all other default values.

Figure 10-10. Add a 250 MHz Clock Constraint



8. Click **OK** to continue.
   The clock constraint appears in the SmartTime Constraints Editor.

Figure 10-11. 250 MHz Clock Constraint in the Constraint Editor

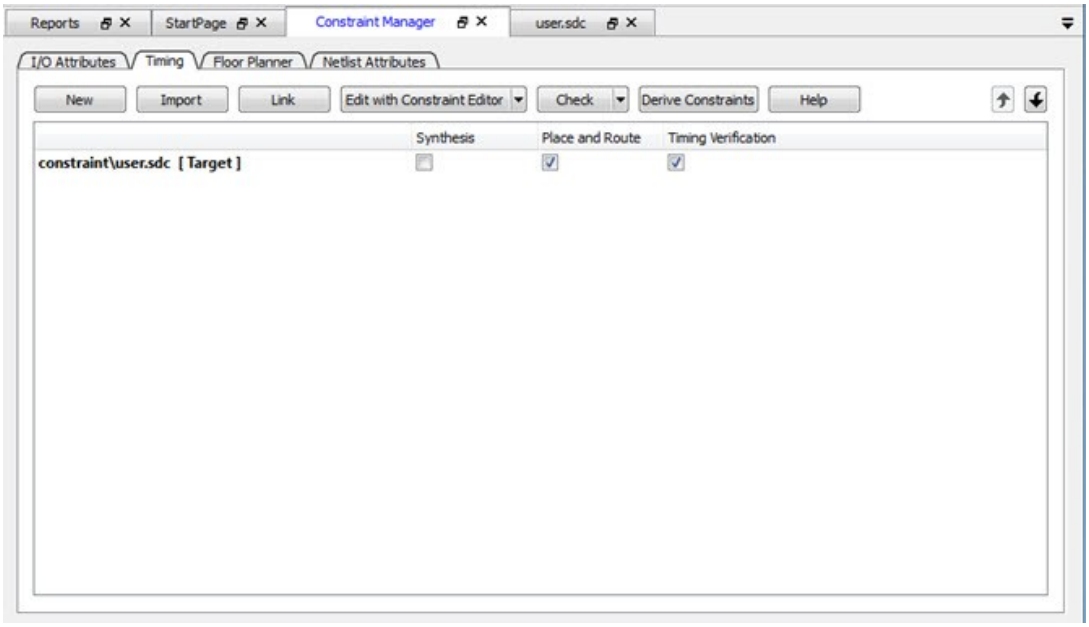


9. From the **File** menu, choose **Save** to save the constraints.
10. From the SmartTime **File** menu, choose **Exit** to exit SmartTime.
    Libero creates a constraint file to store the clock constraint. This file appears in the Constraint Manager. It is named **user.sdc** and designated as **Target**.

Note: A target file is used to store newly added constraints from the Constraint Editor. If you invoke the Constraint Editor with no SDC timing constraint file present, Libero SoC creates the user.sdc file and marks it as **Target** to store the timing constraints you create in the Constraint Editor.

11. In the Constraint Manager, check the check boxes under **Place and Route** and **Timing Verification** to associate the constraint file to the tools. The constraint file is used for both Place and Route and Timing verification.

Figure 10-12. SDC Constraint File and Tool Association

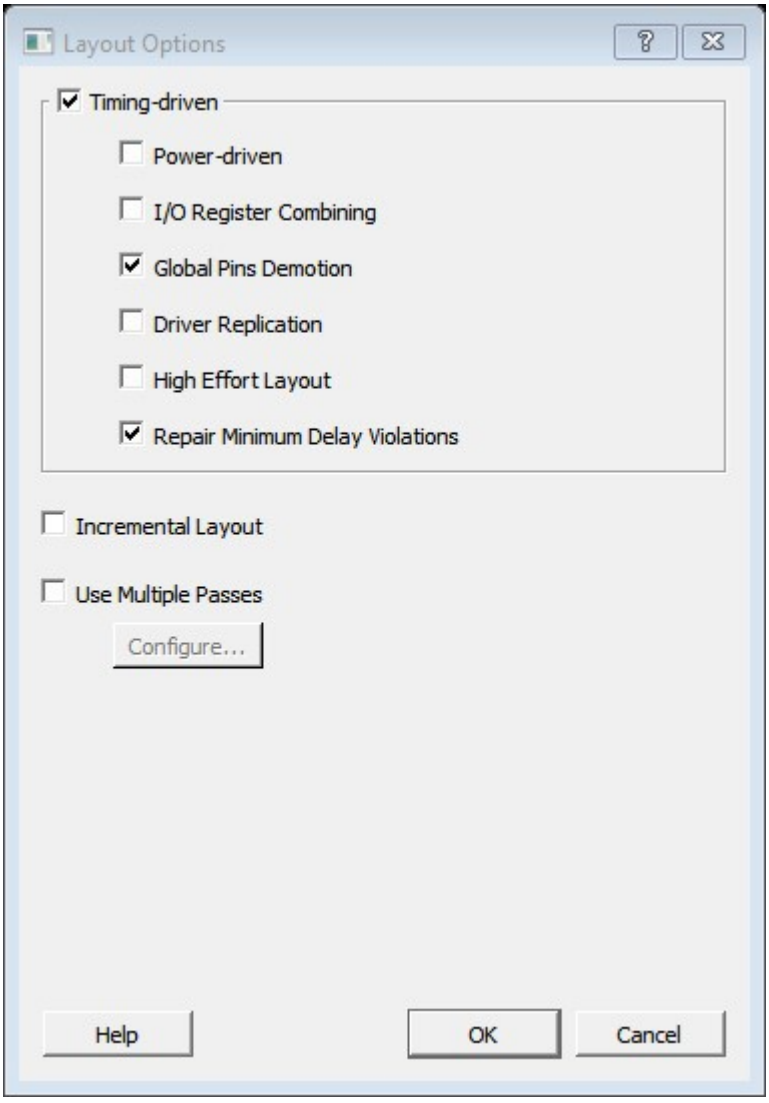


10.1.2 Run Place and Route

To run Place and Route:

1. Right-click **Place and Route** and choose **Configure Options**.
   The Layout Options dialog box appears.
2. Click the check box to enable **Timing-driven** layout ans accept the other default values shown in the following figure.

Figure 10-13. Layout Options Dialog Box



3. Click **OK** to continue.
4. In the Design Flow window, double-click **Place and Route** to start the Place and Route.

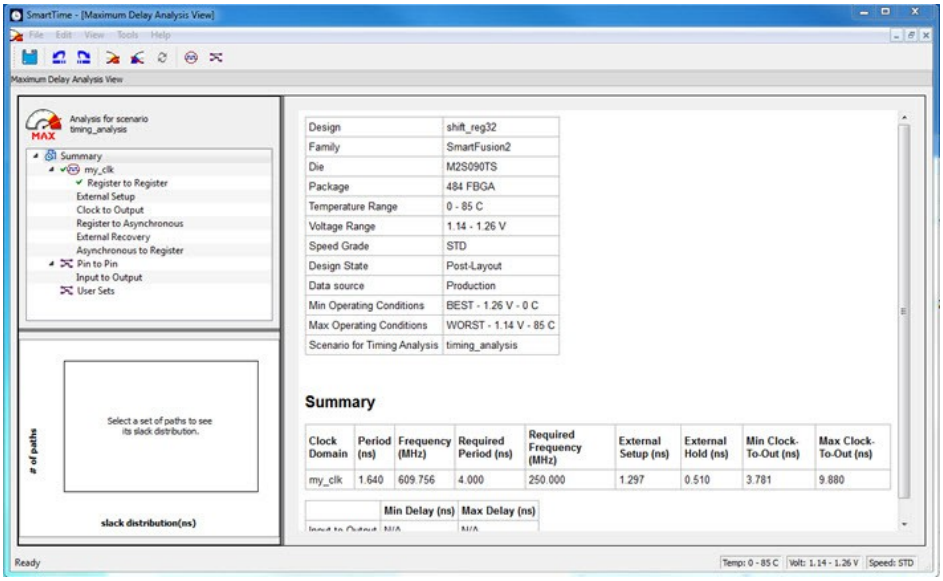
10.1.3 Maximum Delay Analysis with Timing Analyzer - 32-Bit Shift Register Example

The SmartTime Maximum Delay Analysis window shows the design maximum operating frequency along with any setup violations.

To perform maximum delay analysis:

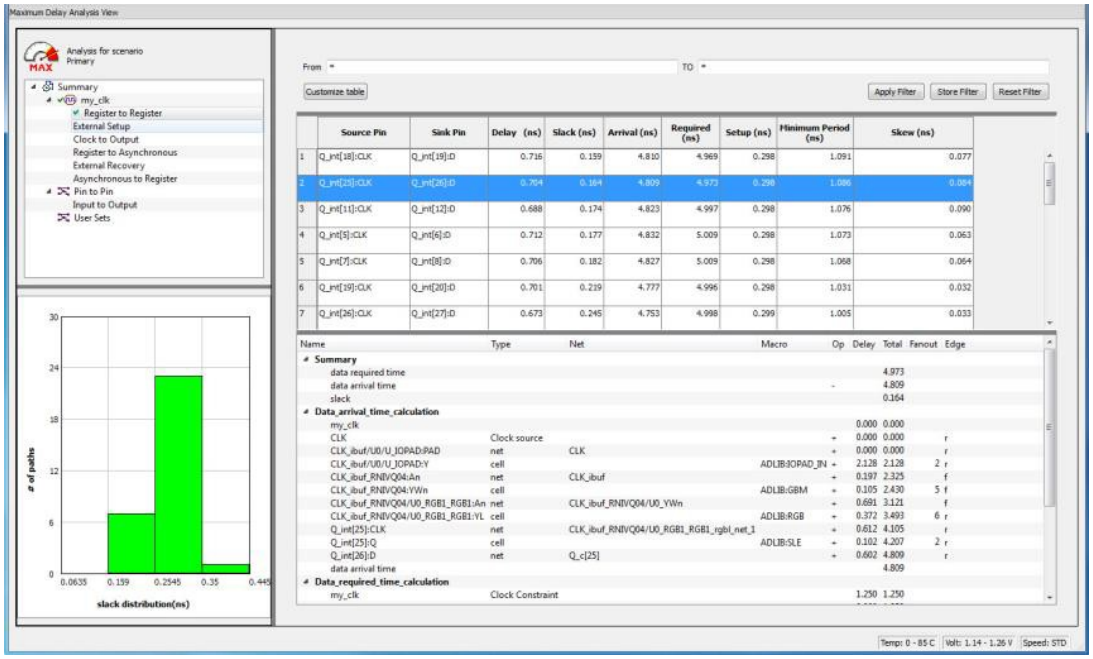
1. Right-click **Open SmartTime** in the Design Flow window and choose **Open Interactively** to open SmartTime. The Maximum Delay analysis window appears. A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.
   The Maximum Delay Analysis Summary appears with the following information shown:
   - Maximum operating frequency for the design
   - External setup and hold requirements
   - Maximum and minimum clock-to-out times. In this example, the maximum clock frequency for CLK is 609.75 MHz.

Figure 10-14. Maximum Delay Analysis - Summary



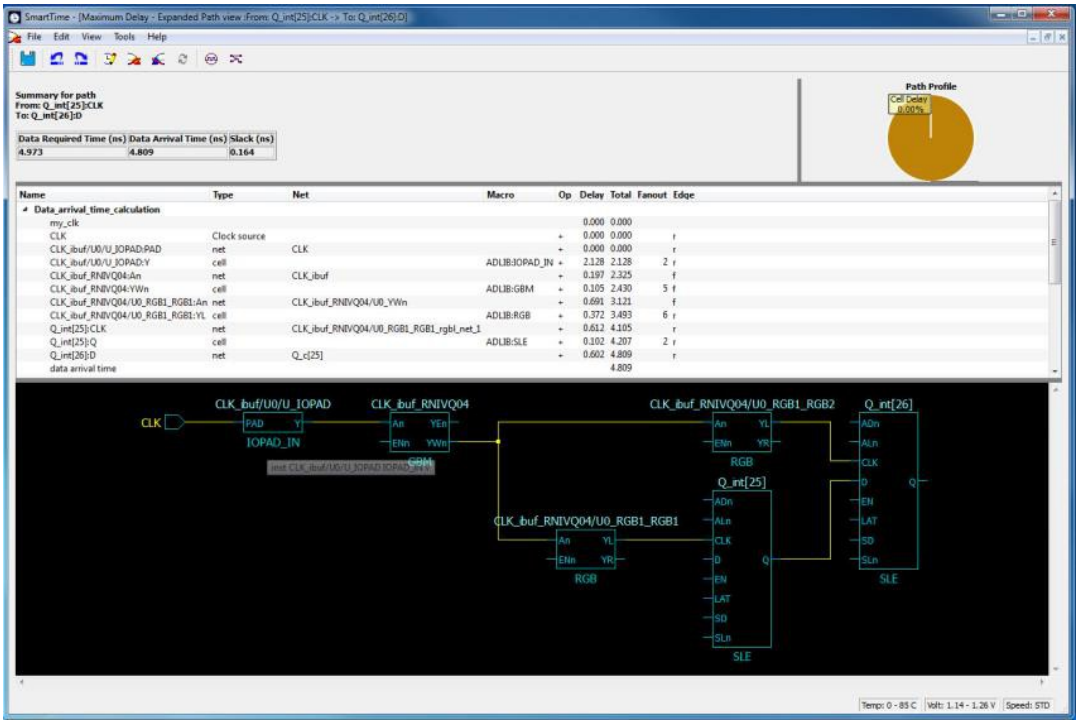
2. Expand **my_clk** to display the Register to Register, External Setup, and Clock to Output path sets.

Figure 10-15. SmartTime Register-to-Register Delay



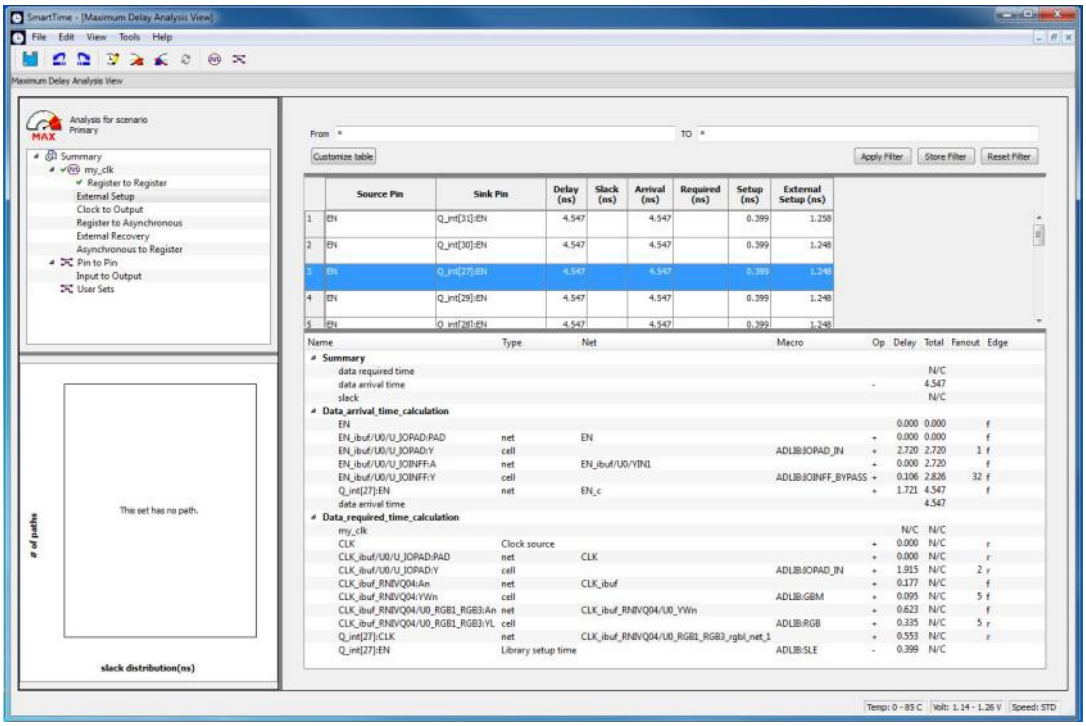
3. Select **Register to Register** to display the register-to-register paths.
   The window displays a list of register- to-register paths and detailed timing analysis for the selected path. All the slack values are positive, indicating that there are no setup time violations
4. Double-click a path row to open the Expanded Path window.
   The window shows a calculation of the data arrival and required times, along with a schematic of the path.
   Note: Timing numbers in the reports may vary slightly with different versions of the Libero software, and may not be what you see when you run the tutorial.

Figure 10-16. Register-to-Register Expanded Path View



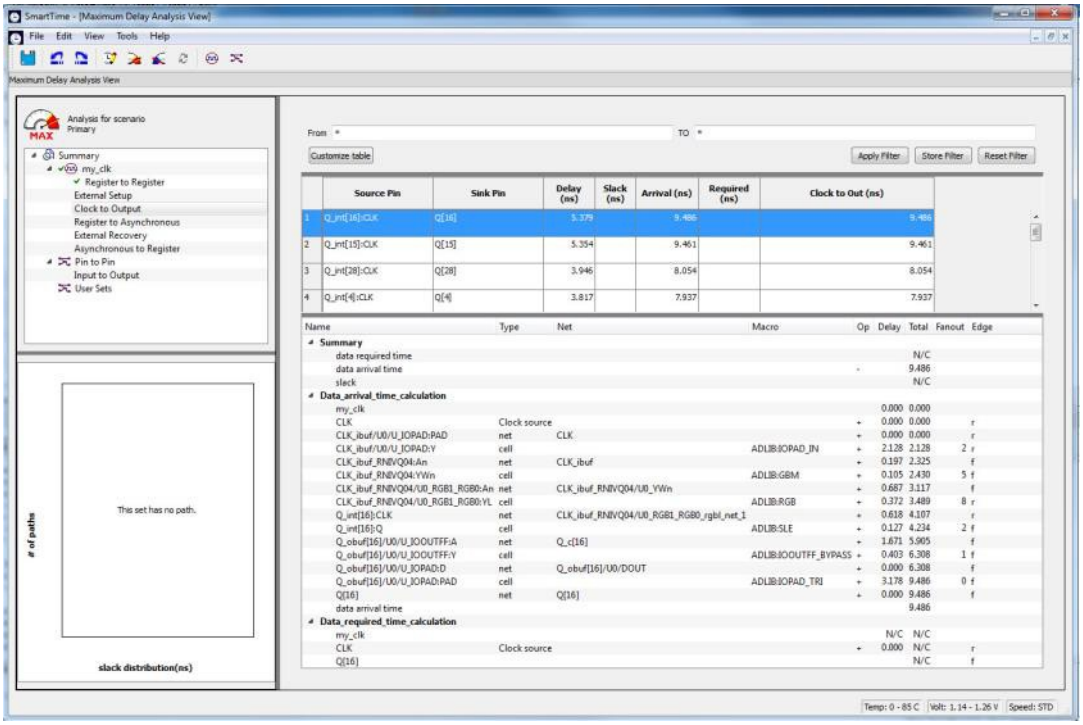
5. Select **External Setup** to display the Input to Register timing.
6. Select **Path 3**.
   The Input Arrival time from the EN pin to Q_int[27]:EN is 4.547 ns.

Figure 10-17. SmartTime - Input to Register Path Analysis



7. Select **Clock to Output** to display the register to output timing.
8. Select **Path 1**.
   The maximum clock to output time from Q_int[16]:CLK to Q[16] is 9.486 ns.

Figure 10-18. SmartTime Clock to Output Path Analysis



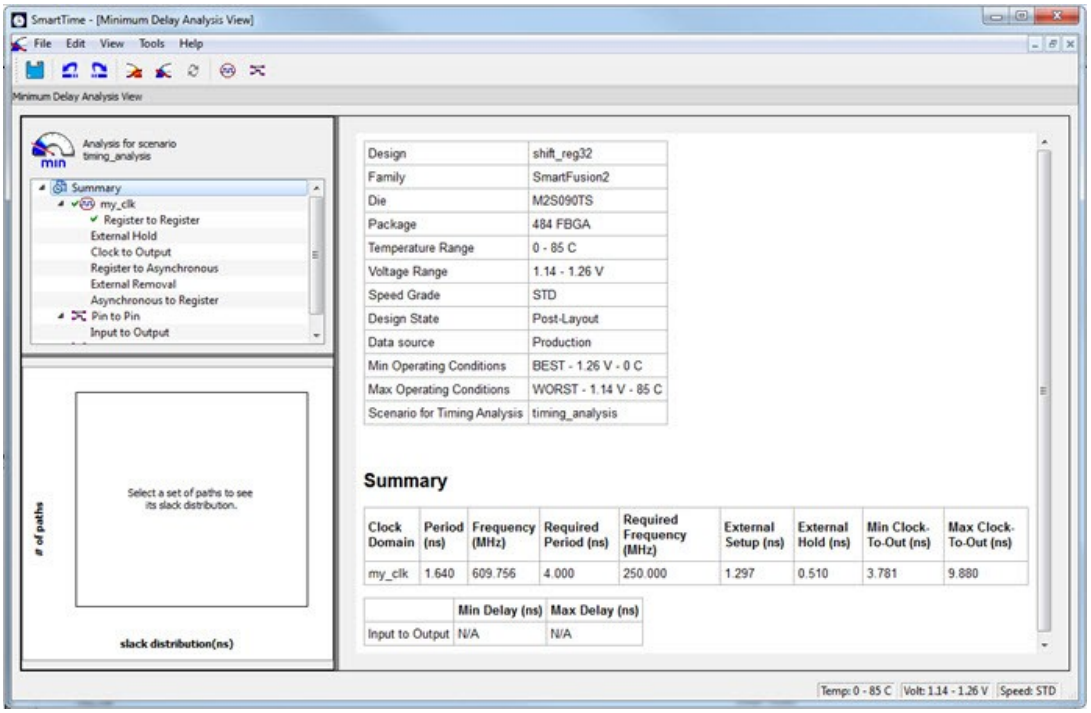
10.1.4 Minimum Delay Analysis with Timing Analyzer - 32-Bit Shift Register Example

The SmartTime Minimum Delay Analysis window identifies any hold violations that exist in the design.

To perform minimum delay analysis:

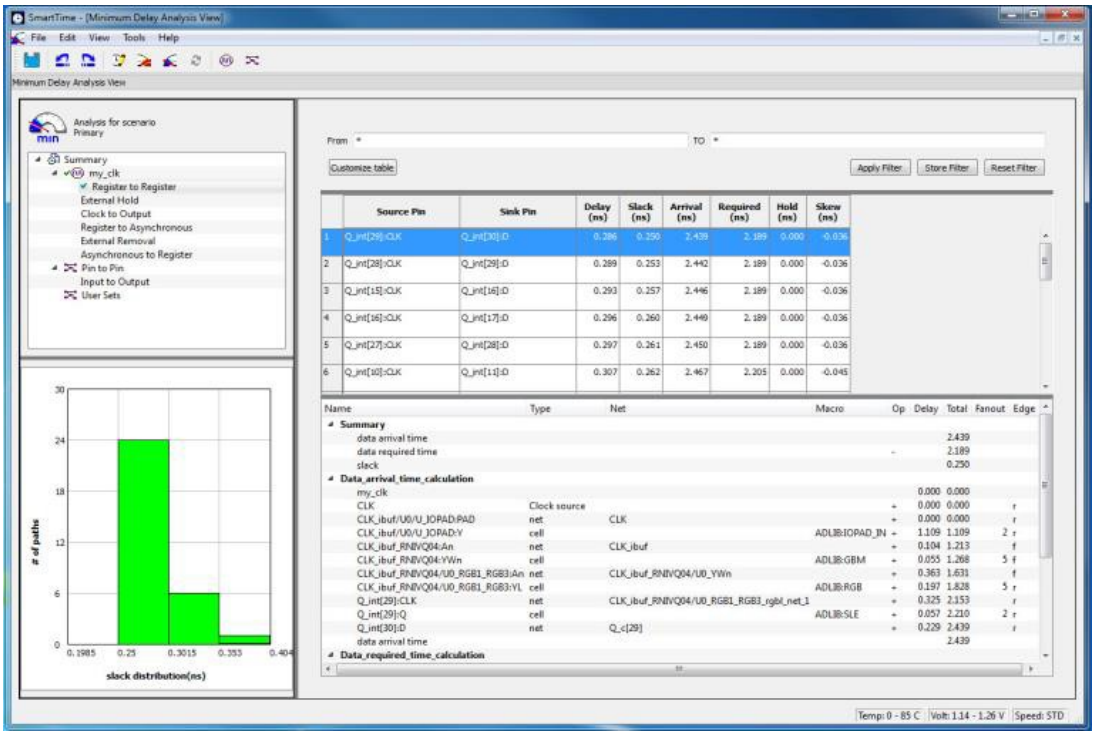
1. From the SmartTime Analysis window, choose **Tools > Minimum Delay Analysis**.
   The Minimum Delay Analysis View appears, as shown in the following figure.

Figure 10-19. SmartTime Minimum Delay Analysis View- Summary



2. Expand **my_clk** to display Register to Register, External Hold, Clock to Output, Register to Asynchronous, External Removal, and Asynchronous to Register path sets.
3. Click **Register to Register** to display the reg to reg paths.
   The window displays a list of register to register paths and detailed timing analysis for the selected path. All the slack value are positive, indicating that there are no hold time violations.
4. Click to select the first path and observe the hold analysis calculation details, as shown in the following figure.

Figure 10-20. SmartTime Minimum Delay Analysis

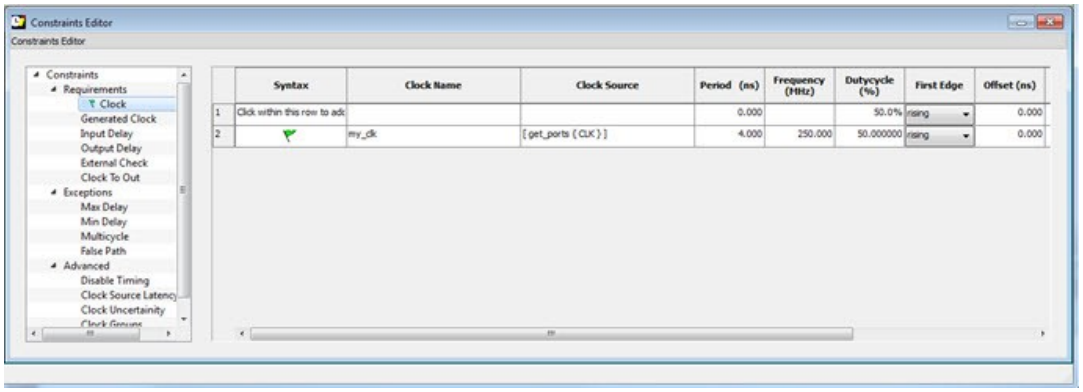


10.1.5 Changing Constraints and Observing Results - 32-Bit Shift Register Example

You can use the Constraints Editor to change your constraints and view the results in your design. The following procedure describes how.

1. Open the Constraints Editor (**Constraints Manager > Timing Tab > Edit Constraints with Constraint Editor > Edit Timing Verifications Constraints**).
   The Constraints Editor shows the clock constraint at 250 MHz you entered earlier.

Figure 10-21. Clock Constraint Set to 250 MHz

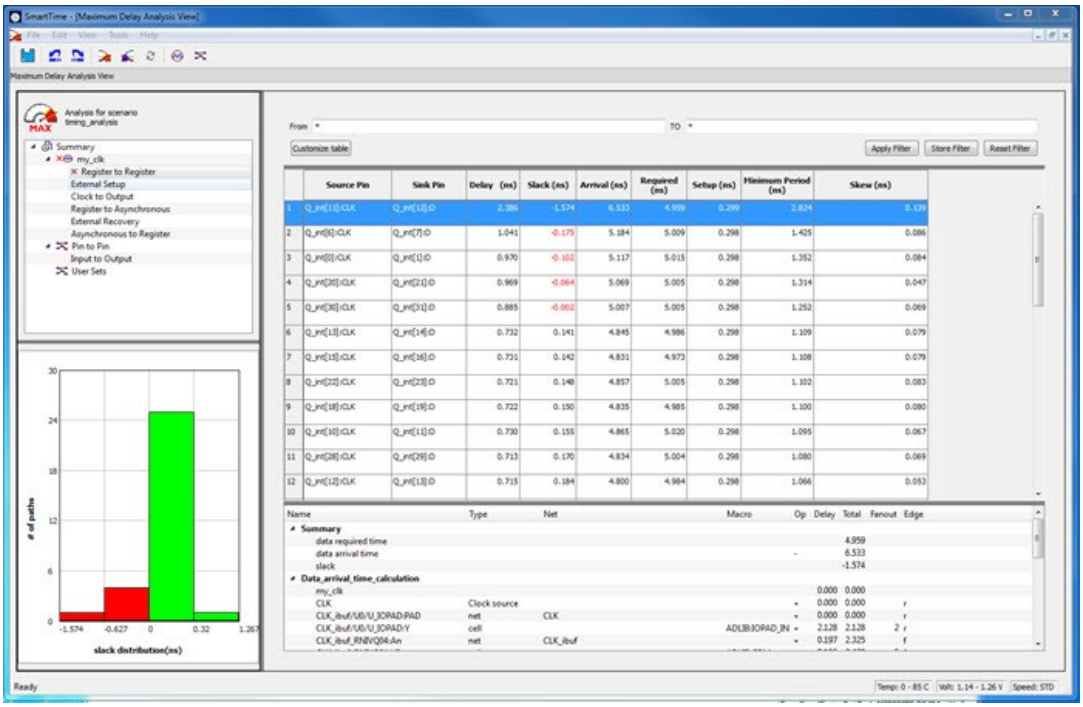


2. Select the second row. Right-click and choose **Edit Clock Constraint**.
   The Edit Clock Constraint dialog box appears.

3. Change the clock constraint from 250 MHz to 800 MHz, and then click the green check mark to continue.
4. Click **Open SmartTime > Open Interactively**.
5. Choose **Maximum Delay Analysis View** to view the max delay analysis.
6. In the Maximum Delay Analysis window, expand **my_clk**.
7. Click **Register to Register** to observe the timing information. The slacks decrease after you increase the frequency. You may see the slacks go negative, which indicates Timing Violations. Negative slacks are shown in red.

   Note: The actual timing numbers you see may be slightly different.

Figure 10-22. Maximum Delay Analysis After Setting Clock Constraint to 800 MHz

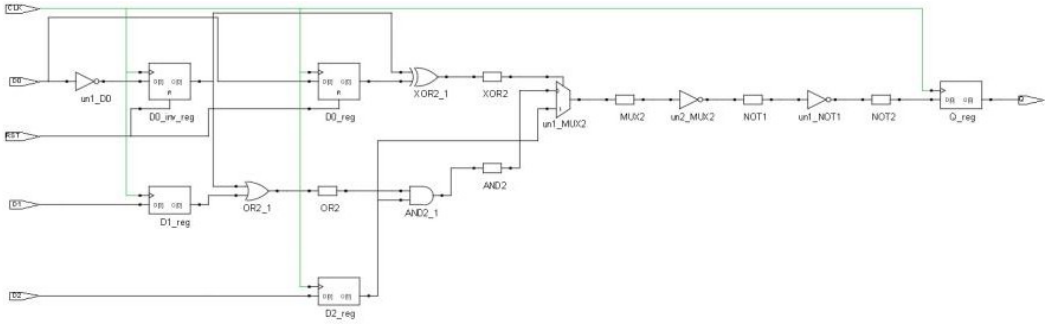


8. Close SmartTime. When prompted to save changes, click **No**.

10.2 Tutorial 2 - False Path Constraints

This section describes how to enter false path constraints in SmartTime. You will import an RTL source file from the following design. After routing the design, you will analyze the timing, set false path constraints, and observe the maximum operating frequency in the SmartTime Timing Analysis window.

Figure 10-23. Example Design with False Paths



10.2.1 Set Up Your False Path Example Design Project

To set up your false path example design project:

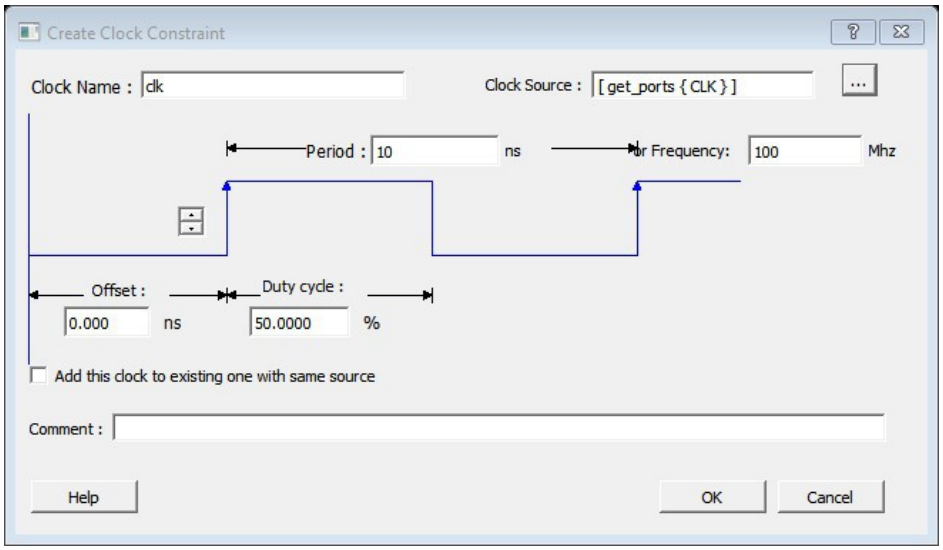
1. Open Libero.
2. From the **Project** menu, choose **New Project** to create a new project.
3. Name the project `false_path` and set the project location according to your preferences.
4. Click **Next**.
5. Enter the following values for your **Device Selection** settings:
   - **Family**: SmartFusion2
   - **Die**: M2S050
   - **Package**: 484 FBGA
   - **Speed**: STD
   - **Die Voltage**: 1.2 V
   - **Range**: COM
6. Click **Finish** to create the new project.

10.2.2 Import the false_path Verilog File and Add Constraints

For this tutorial, you will import the 10.2.5 false_path.v Verilog source file into your design, and then run Libero SoC. To import the Verilog source file:

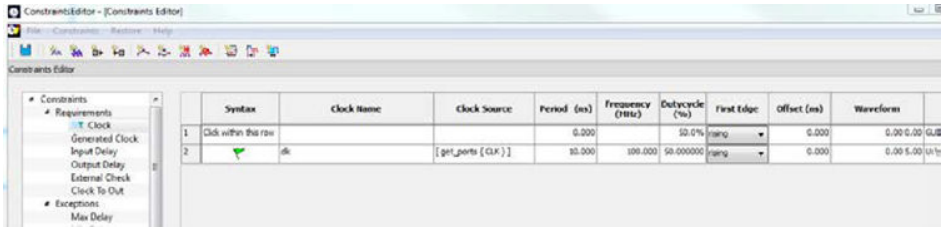
1. From the **File** menu, choose **Import > HDL Source Files**.
2. Browse to the location of the false_path.v you saved and select it. Click **Open** to import the file.
3. Verify that the file appears in Design Hierarchy.
4. In the Design Flow window, double-click **Synthesize** to run synthesis.
   A green check mark appears when the Synthesis step completes successfully.
5. Expand **Edit Constraints**.
6. Right-click **Timing Constraints** and choose **Open Interactively**.
7. Double-click **Manage Constraints**.
8. Select the **Timing** tab.
9. Expand the **Edit with Constraint Editor** sub-menu, and select **Edit Place and Route Constraints**.
   The Constraints Editor appears.
10. Double-click **Requirements: Clock**.
    The Create Clock Constraint dialog box appears.
11. Double click the **Browse** button for **Clock Source**, select **CLK**, and assign it a name (for example, `clk`).
12. Set the frequency to 100 MHz.

Figure 10-24. Clock Constraint of 100 MHz



13. Click **OK** to return to the Constraints Editor and observe that the clock information has been filled in, as shown in the following figure.

Figure 10-25. Clock Constraint of 100 MHz in false_path design



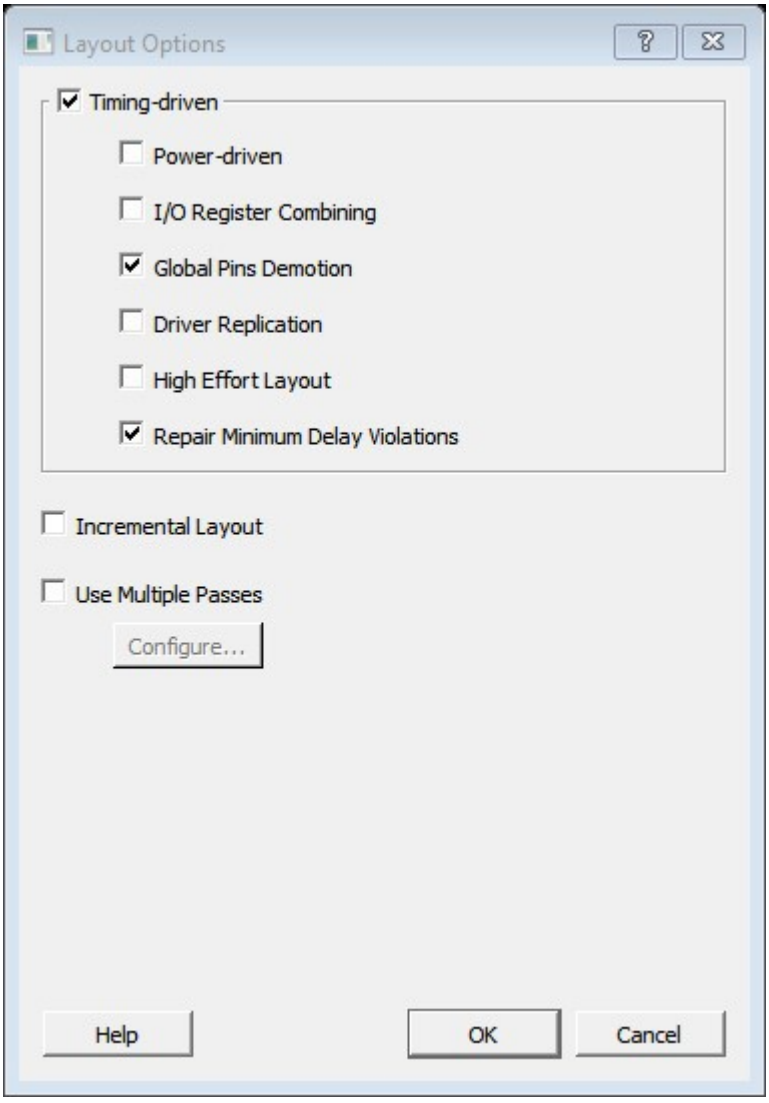
14. Save your changes (**File > Save**) and close the Constraints Editor (**File > Close**).
15. In the Constraint Manager, check the check boxes under **Place and Route** and **Timing Verification** to associate the constraint file to both tools. The constraint file is used for both Place and Route and Timing verification.

10.2.3 Place and Route Your FALSE_PATH Design

To run Place and Route on false_path design:

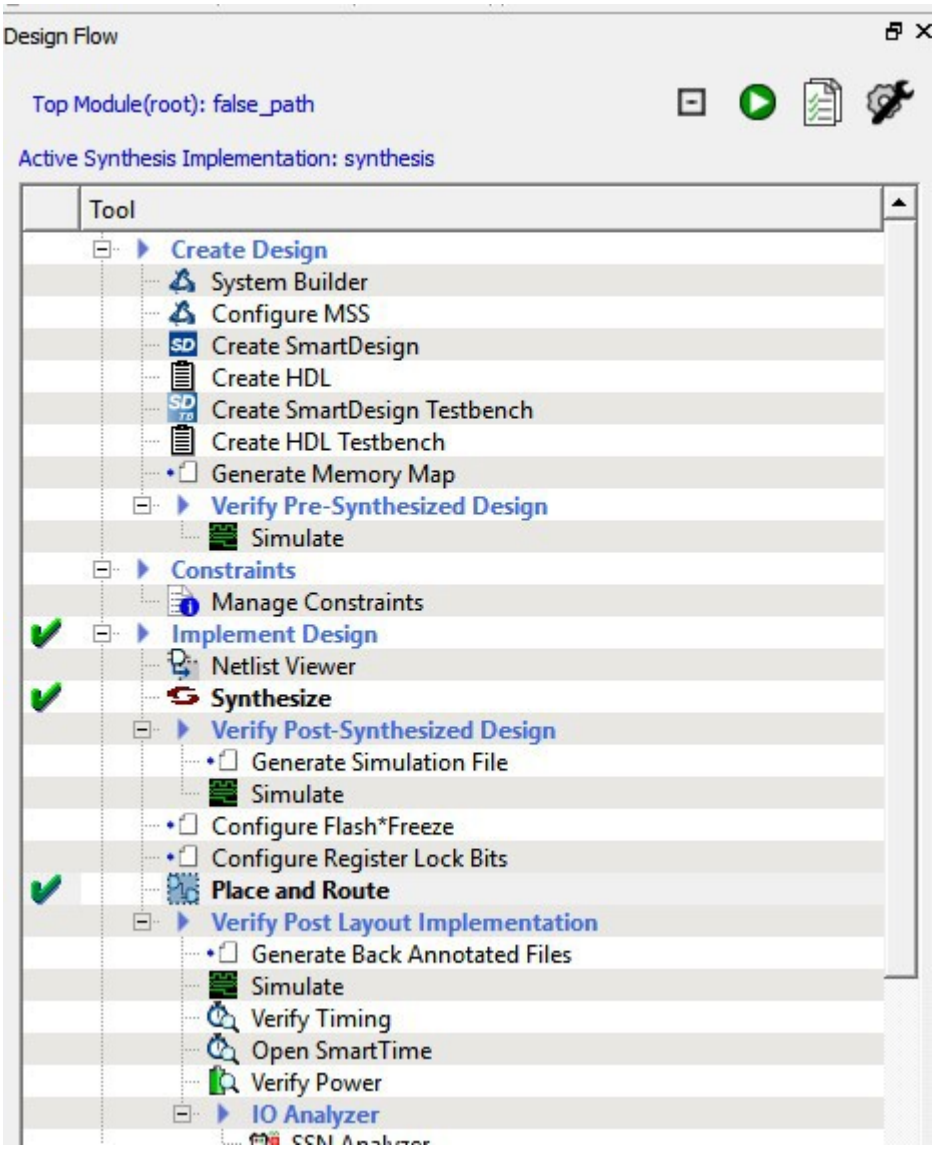
1. In Libero SoC, right-click **Place and Route** and choose **Configure Options**.
   The Layout Options dialog box appears.

Figure 10-26. Layout Options Dialog Box



2. Click the check box to enable **Timing-Driven** layout and leave all other values unchecked.
3. Click **OK** to close the Layout Options dialog box.
4. Right-click **Place and Route** and choose **Run**.
   A green check mark appears next to **Place and Route** in the Design Flow window when Place and Route completes successfully.

Figure 10-27. Synthesize and Place and Route Successful Completion



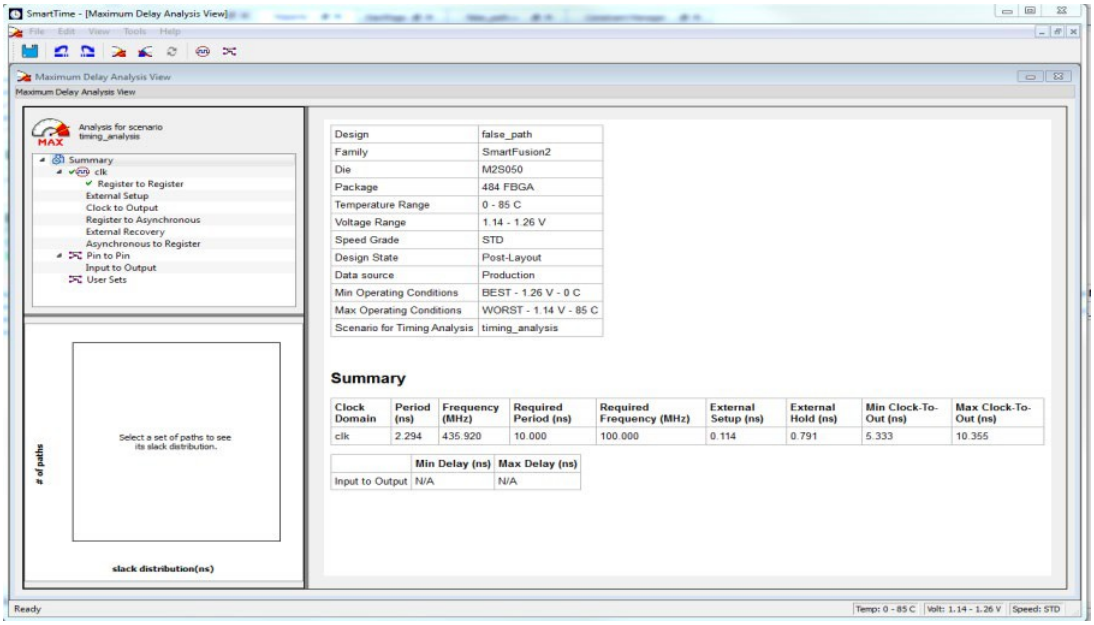
10.2.4 Timing Analysis - Maximum Clock Frequency

The SmartTime Maximum Delay Analysis View displays the design maximum operating frequency and lists any setup violations.

To perform maximum delay analysis:

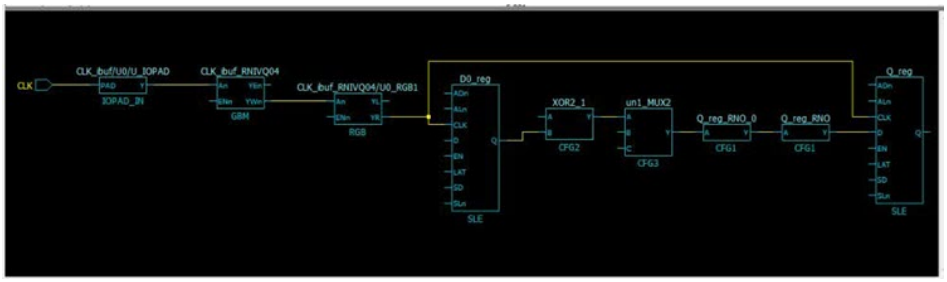
1. Expand **Verify Post Layout Implementation**.
2. Right-click **Open SmartTime** and choose **Open Interactively** to open SmartTime.
   The Maximum Delay Analysis View appears. The Maximum Delay Analysis View summarizes design performance and indicates that the design will operate at a maximum frequency of 442.48 MHz.
   Note: You may see a slightly different maximum frequency with a different version of Libero SoC.

Figure 10-28. Maximum Delay Analysis Summary



3. Expand **clk** to expand the display and show the Register to Register path sets.
4. Select **Register to Register** to display the register-to-register paths. Notice that the slack values are positive.

Figure 10-29. Expanded Path



5. Double-click to select and expand the row in the path list with the path is from the CLK pin of flip-flop D0_reg to the D input of flip flop Q_reg. Note that the path goes through the S input of multiplexer un1_MUX2.

   Looking at the code in false_path.v, you can see on lines 51 and 52, that D0_reg and D)_inv_reg are always the inverse of each other in "operational" mode (i.e., except for when RST is active). Line 56 says that XOR2 is the XOR of these two signals, and hence always 1 (except when RST is active). Line 59 says that XOR2 is the select of MUX2.

   We might reasonably decide that we are not interested in the reset mode delay for this design; therefore, this path is a false path for our timing analysis purposes.

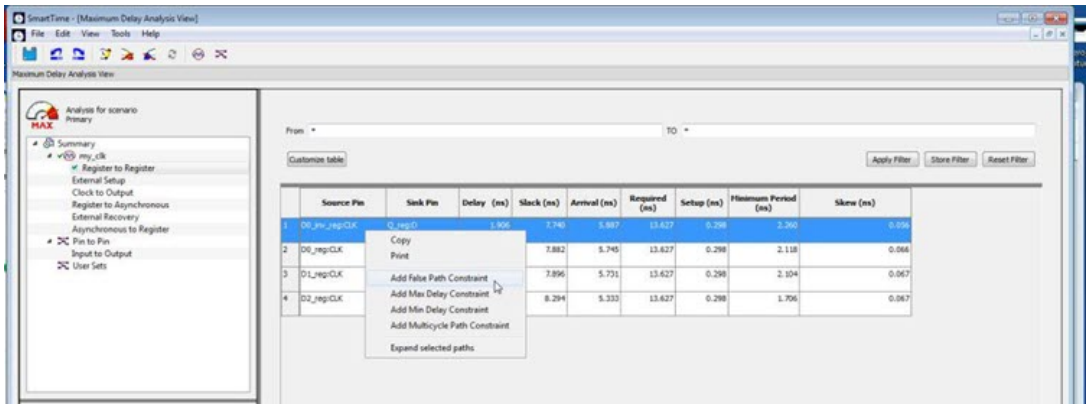
Figure 10-30. Analyzing the False Paths

```
43      if (RST)
44      begin
45          D0_reg      <= 1'b0;
46          D0_inv_reg  <= 1'b0;
47      end
48
49      else
50      begin
51          D0_reg      <= D0;
52          D0_inv_reg  <= ~D0;
53      end
54  end
55
56  assign XOR2 = D0_reg ^ D0_inv_reg;
57  assign OR2  = D0_inv_reg || D1_reg;
58  assign AND2 = OR2 && D2_reg;
59  assign MUX2 = (XOR2) ? (D2_reg) : (AND2);
60
61
```

Similar analysis shows that the path from D0_inv_reg:CLK to Q_reg:D shares exactly the same false-path characteristic. We should disable both paths.

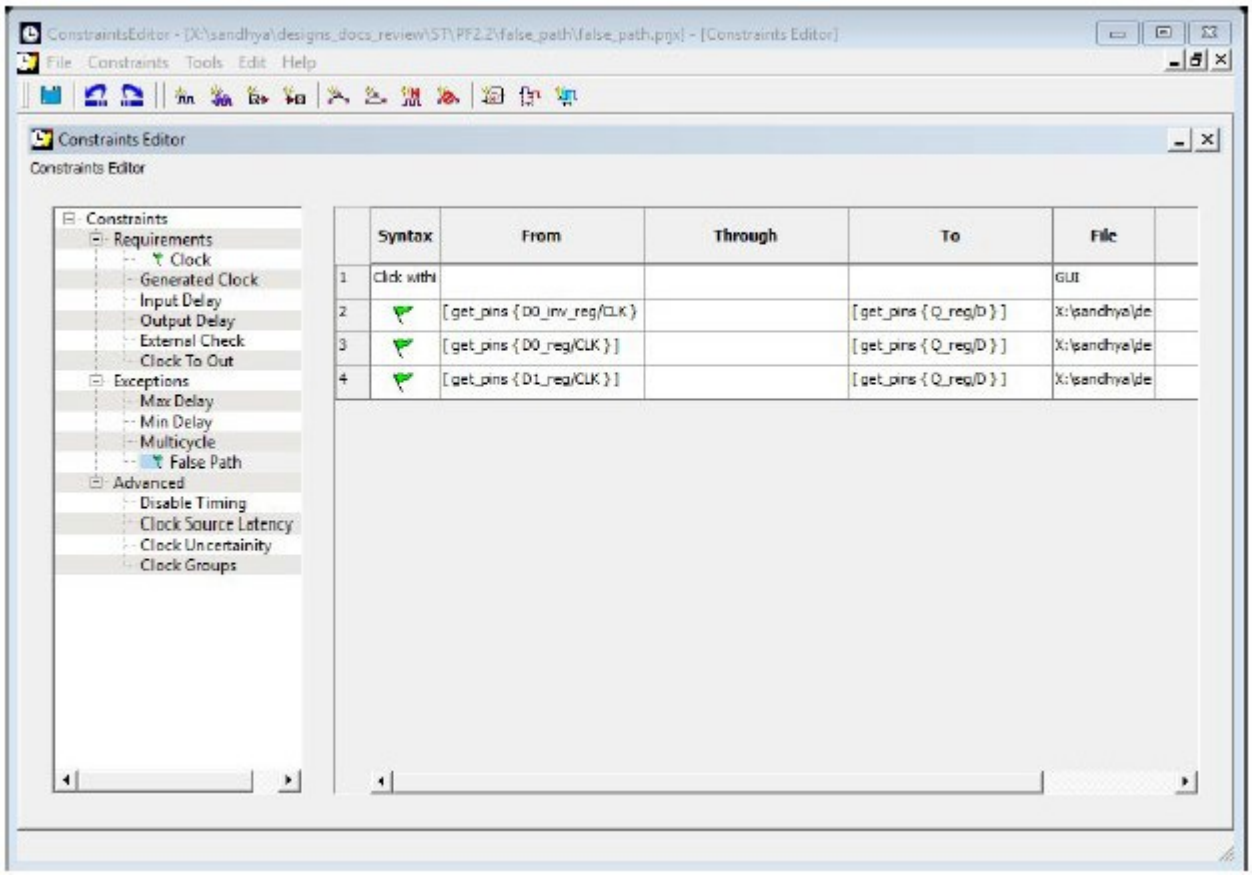
6. Restart the Libero Constraints Editor. The Constraints Editor must be running to use SmartTime's back-annotation feature. Go to the **Constraint Manager** tab, then go to the **Timing** sub-tab, pull down **Edit with Constraint Editor**, and choose **Edit Timing Verification Constraints**.
7. Leave this running and return to SmartTime.
8. From the **Tools** menu, select **Max Delay Analysis**.
9. To set the path from D0_inv_reg:CLK to Q_reg :D as false, select the row containing this path in the Register to Register path set, right-click and choose **Add False Path Constraint**.
   The Set False Path Constraint dialog box appears. It might pop behind the current dialog box, so check other Constraint Manager windows.

Figure 10-31. Right-clicking Add False Path Constraint



10. Click **OK** to close the Set False Path Constraint dialog box.
11. In the Constraints Editor window, check for an entry below **Exceptions > False Path**.
12. Return to the SmartTime window and repeat for the D0_reg:CLK -> Q_reg:D path.
13. Because we are interested only in timing analysis through the MUX when select = 1, we can ignore the MUX "0" path from D1_reg:D through the AND2. We make this a false path. At this point the Constraints Editor should now look as follows. Save the file and exit the Constraints Editor and SmartTime.

Figure 10-32. False Path Constraints in the SmartTime Constraint Editor

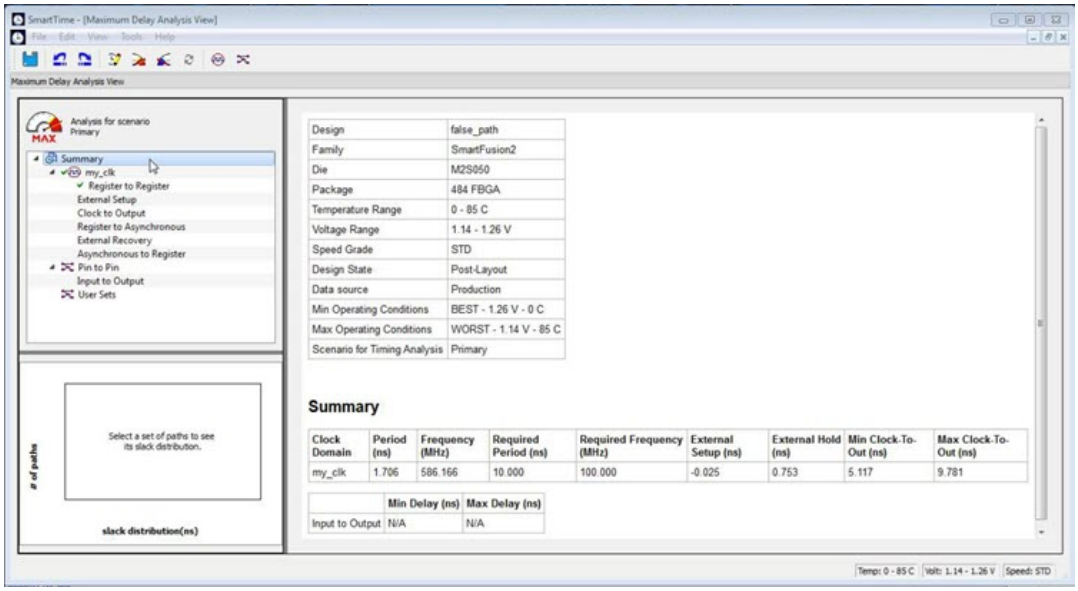


Place and Route is now invalidated and must be re-run before we can perform timing analysis again. This is because we changed the constraint file we are using for both P&R and for Timing Analysis. We can use different constraint files, in which case we would not need to re-run P&R.

14. Right-click **Open SmartTime** and choose **Update and Open Interactively**.
    You will see that Place and Route is run automatically before SmartTime is restarted.
15. View the summary in the Maximum Delay Analysis View (**Tools > Max Delay Analysis**). SmartTime now reports the maximum operating frequency as 586.17 MHz, as shown in the following figure.

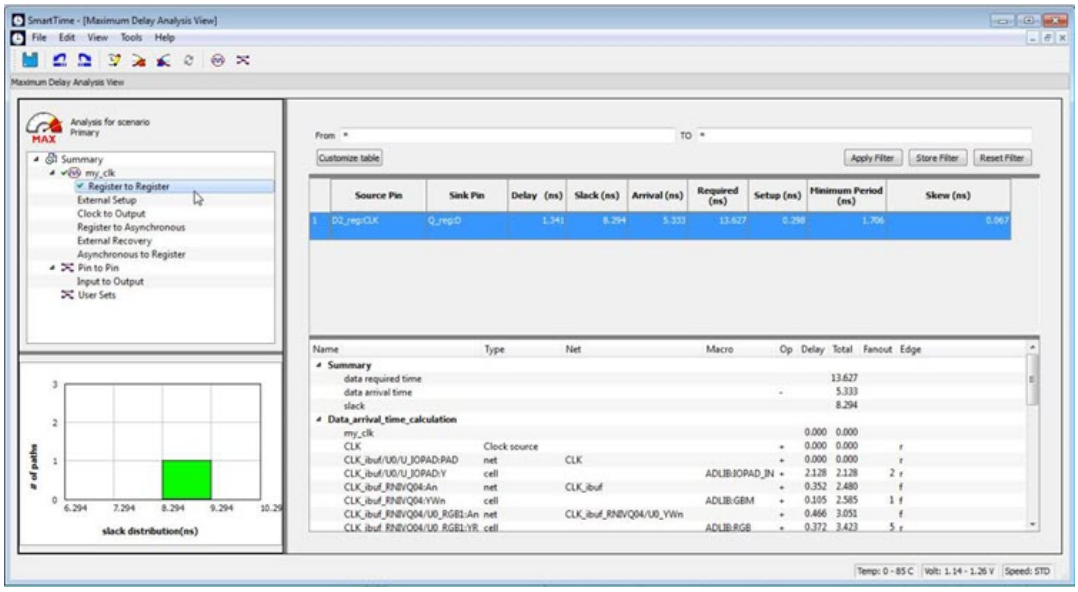
    Note: The maximum operating frequency may vary slightly with a different version of the Libero software.

Figure 10-33. Maximum Delay Analysis View - Summary



16. Select the Register to Register set for my_clk. Observe that only one path is visible, from D2_reg: CLK to Q_reg:D. This is the only path that propagates a signal, as shown in the following figure.

Figure 10-34. Maximum Delay Analysis View - Register to Register



17. Close SmartTime.
18. Close Libero SoC.

10.2.5 false_path.v

```
//////////////////////////////////////////////////////////////////
Company: Microsemi Corp
//
// File history:
// 0.1 Initial Version
//
// Description:
// Simple example design to demonstrate use of timing // constraints.
//
// Targeted device: Family::SmartFusion2; Die::M2S050;
// Package::484 FBGA;
```

```
//
// Author: Joe X // //
//
////////////////////////////////////////////////////////////
module     false_path (D0, D1, D2, RST, CLK, Q); input D0;
input      D1;
input      D2;
input      RST;
input      CLK;
output     Q;

reg        D0_reg;
reg        D0_inv_reg;
reg        D1_reg;
reg        D2_reg;

reg        Q_reg;

wire       XOR2          /*synthesis syn_keep=1*/;
wire       AND2          /*synthesis syn_keep=1*/;
wire       OR2           /*synthesis syn_keep=1*/;
wire       MUX2          /*synthesis syn_keep=1*/;
wire       NOT1          /*synthesis syn_keep=1*/;
wire       NOT2          /*synthesis syn_keep=1*/;

assign Q = Q_reg /*synthesis syn_keep=1*/;

always @(posedge CLK or posedge RST)

begin
          if (RST)
          begin
              D0_reg         <= 1'b0;
              D0_inv_reg     <= 1'b0;
          end
          else
          begin
              D0_reg         <= D0;
              D0_inv_reg     <= ~D0;
          end
end
          assign XOR2 = D0_reg ^ D0_inv_reg;
          assign OR2 = D0_inv_reg || D1_reg;
          assign AND2 = OR2 && D2_reg;
          assign MUX2 = (XOR2) ? (D2_reg) : (AND2);

          always @(posedge CLK)
          begin
              D1_reg     <= D1;
              D2_reg     <= D2;

              Q_reg <= NOT2;
          end

          not u1 (NOT1, MUX2);
          not u2 (NOT2, NOT1);


          endmodule
```

11. SmartTime Dialog Boxes

The following sections describe the SmartTime dialog boxes.

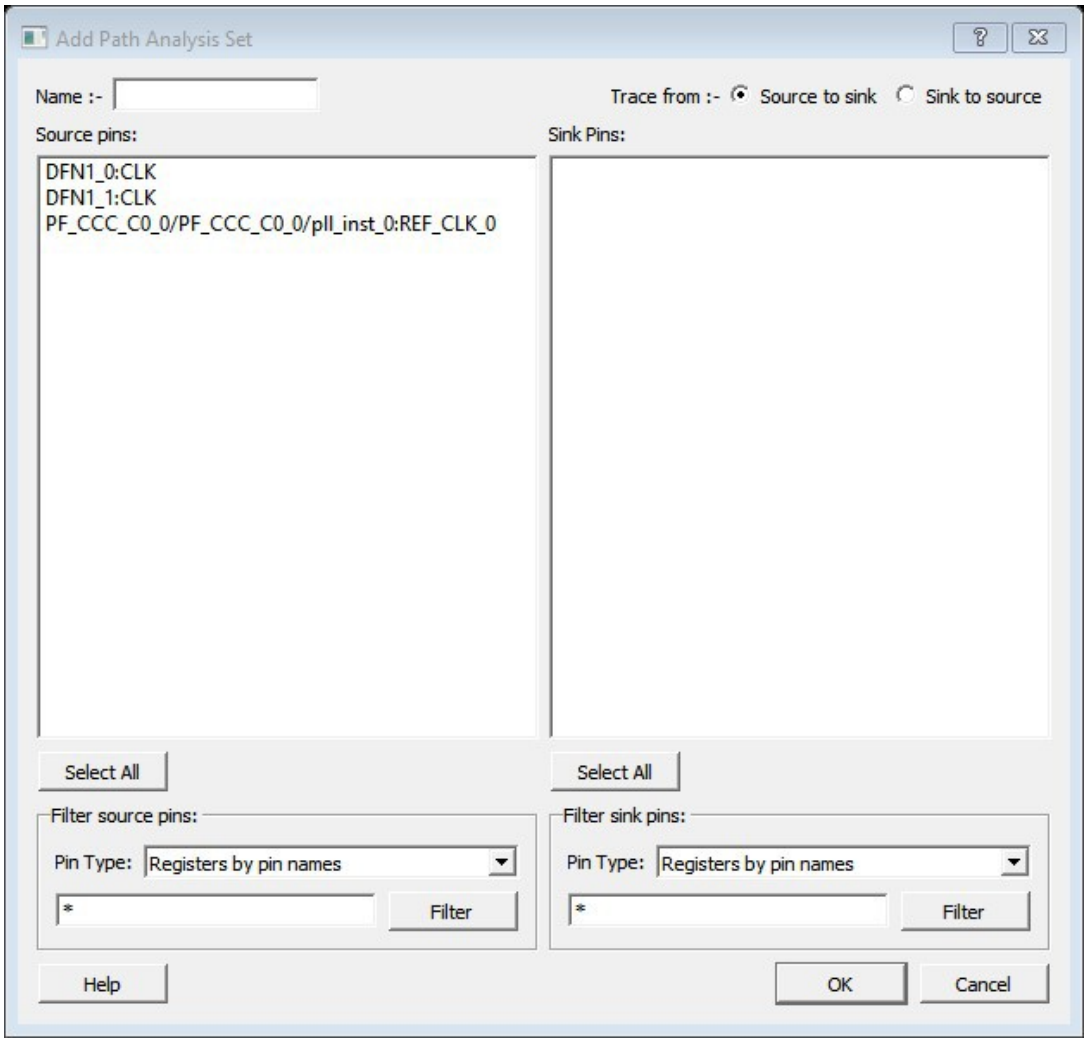
11.1 Add Path Analysis Set Dialog Box

Use the Add Path Analysis Set dialog box to specify a custom path analysis set.

To open the Add Path Analysis Set dialog box from the SmartTime Timing Analyzer, choose any path and right-click to select **Add Set**.

Note: The **Analysis** menu is available only in Maximum or Minimum Delay Analysis view.

Figure 11-1. Add Path Analysis Set Dialog Box



11.1.1 Name

Enter the name of your path set.

11.1.2 Trace from

Select whether you want to trace connected pins from **Source to sink** or from **Sink to source**. By default, the pins are traced Source to sink.

11.1.3 Source Pins

Displays a list of available and valid source pins. You can select multiple pins. To select all source pins, click the **Select All** button below the **Source Pins** list.

11.1.4 Select All

Selects all the pins in the **Source Pins** list to include in the path analysis set.

11.1.5 Filter Source Pins

Allows you to specify the source **Pin Type** and the **Filter**. The default pin type is Registers by pin name. You can specify any string value for the **Filter**. If you change the pin type, the **Source Pins** shows the updated list of available source pins.

11.1.6 Sink Pins

Displays list of available and valid pins. You can select multiple pins. To select all source pins, click the **Select All** button below the **Sink Pins** list.

11.1.7 Select All

Selects all the pins in the **Sink Pins** list to include in the path analysis set.

11.1.8 Filter Sink Pins

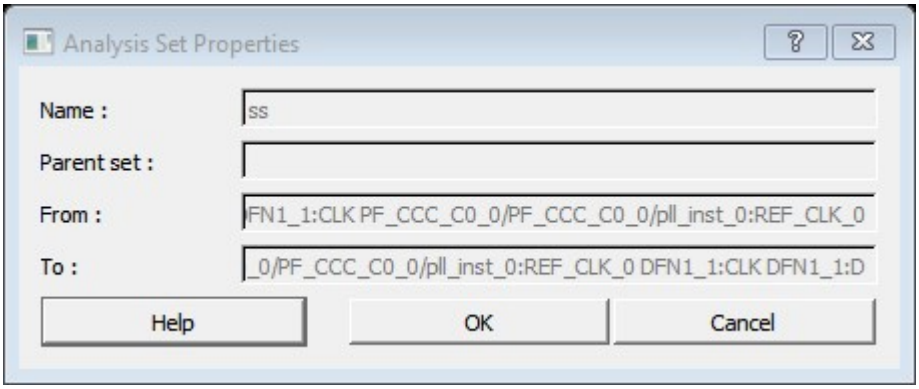
Allows you to specify the sink **Pin Type** and the **Filter**. The default pin type is **Registers (by pin)**. You can specify any string value for the **Filter**. If you change the pin type, the **Sink Pins** shows the updated list of available sink pins.

11.2 Analysis Set Properties Dialog Box

Use the Analysis Set Properties dialog box to view information about a user-created set.

To open the Analysis Set Properties dialog box from the Timing Analysis View, right-click a user-created set in the Domain Browser, and then choose **Properties** from the shortcut menu.

Figure 11-2. Analysis Set Properties Dialog Box



11.2.1 Name

Specifies the name of the user-created path set.

11.2.2 Parent Set

Specifies the name of the parent path set to which the user-created path set belongs.

11.2.3 Creation Filter

Specifies a list of source pins in the user-created path set.

11.2.4 To

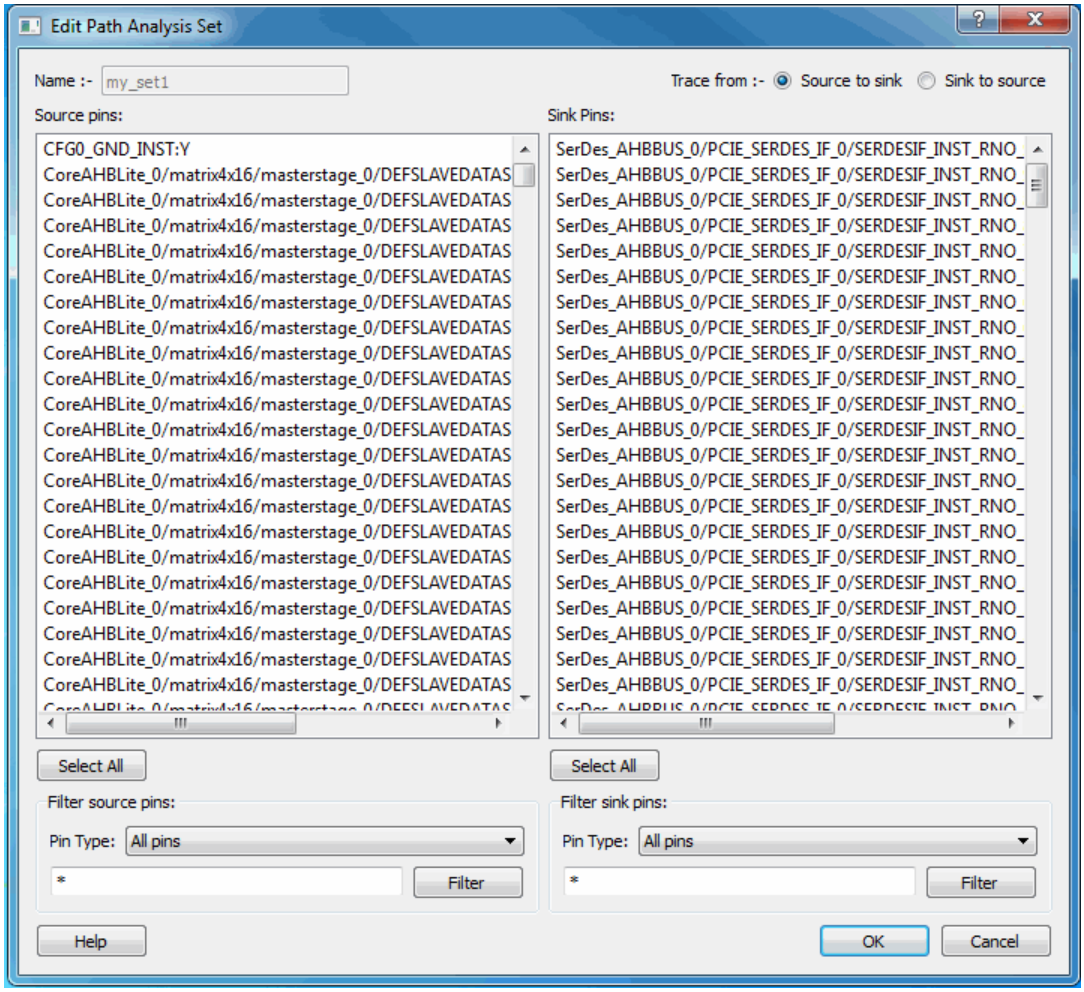
Specifies a list of sink pins in the user-created path set.

11.3 Edit Filter Set Dialog Box

Use the Edit Filter Set dialog box to specify a filter.

To open the Edit Filter Set dialog box from the SmartTime Max/Min Delay Analysis view, right-click a filter set in the clock domain browser, and then choose **Edit Set** from the shortcut menu.

Figure 11-3. Edit Path Analysis Set Dialog Box



11.3.1 Name

Specifies the name of the path you want to edit.

11.3.2 Creation filter

Source Pins: Displays a list of source pins in the user-created path set.

Sink Pins: Displays a list of sink pins in the user-created path set.

11.4 Customize Analysis View Dialog Box

Use the Customize Analysis View dialog box to customize the timing analysis grid.

To open the Customize Analysis View dialog box from the SmartTime Max/Min Delay Analysis View, click the **Customize table** button (circled in red in the following figure) in the Max/Min Delay Analysis View. The Customize Paths List Table dialog box appears.

Figure 11-4. Customize Table Button

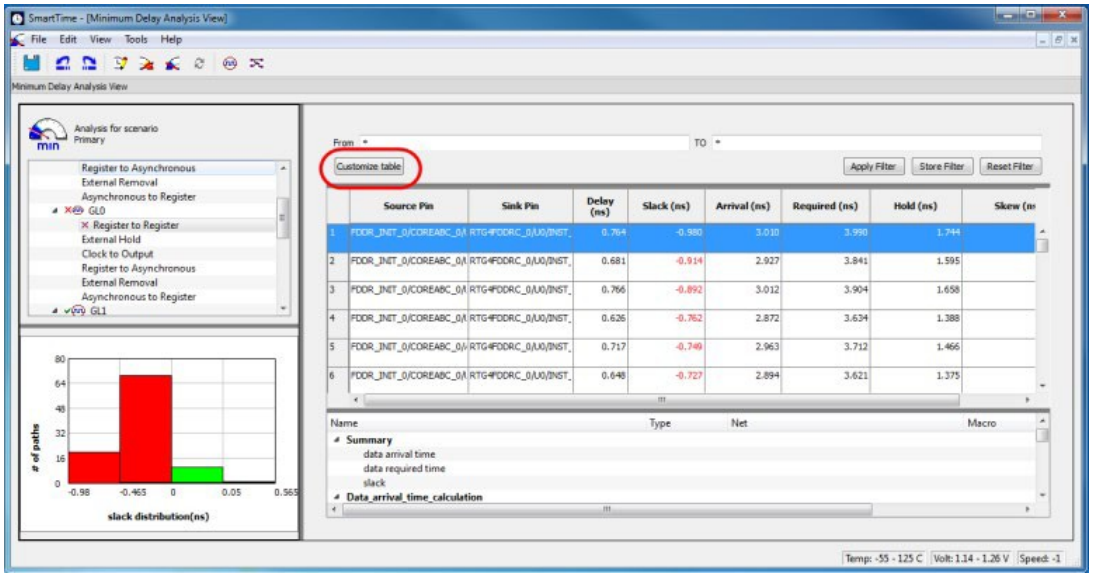
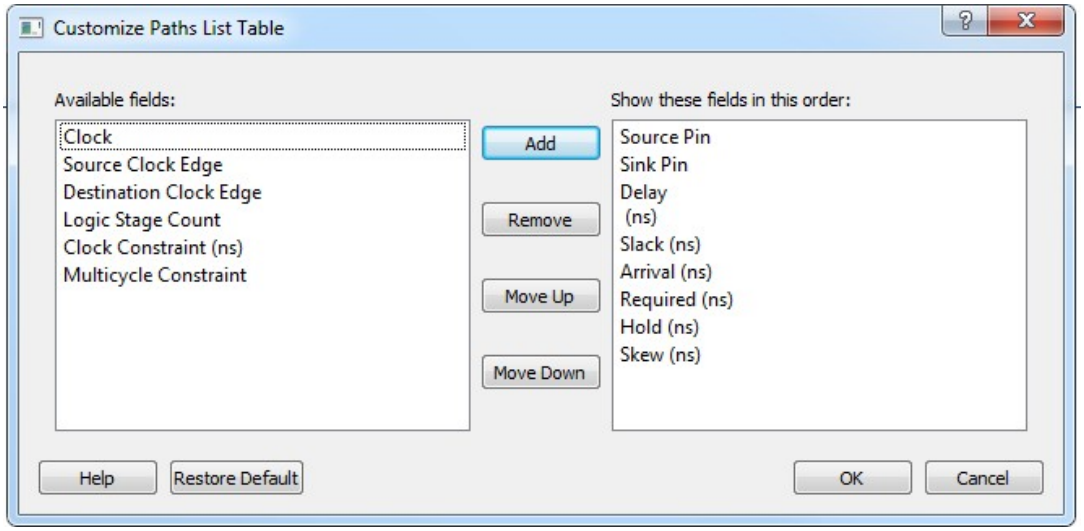


Figure 11-5. Customize Paths List Dialog Box



11.4.1 Available Fields

Displays a list of all the available fields in the timing analysis grid.

11.4.2 Show These Fields in This Order

Shows the list of fields you want to see in the timing analysis grid. Use **Add** or **Remove** to move selected items from **Available fields** to **Show these fields in this order** or vice versa. You can change the order in which these fields are displayed by using **Move Up** or **Move Down**.

11.4.3 Restore Defaults

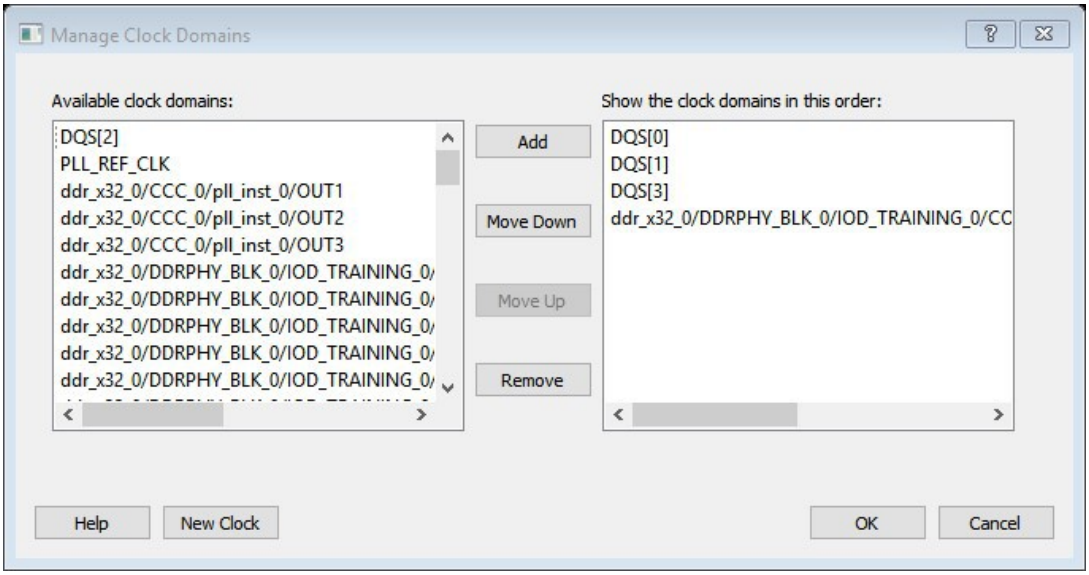
Resets all the options in the **General** panel to their default values.

11.5 Manage Clock Domains Dialog Box

Use the Manage Clock Domains dialog box to specify the clock pins you want to see in the Expanded Path view.

To open the Manage Clock Domain dialog box from the SmartTime Max/Min Delay Analysis view, click the icon.

Figure 11-6. Manage Clock Domains Dialog Box



11.5.1 Available Clock Domains

Displays alphanumerically sorted list of available clock pins. The first clock pin is selected by default.

11.5.2 Show the Clock Domains in This Order

Shows the clock pins you want to see in the Expanded Path view. Use **Add** or **Remove** to move selected items from **Available clock domains** to **Show the clock domains in this order** or vice versa. You can change the order in which these clock pins are displayed by using **Move Up** or **Move Down**.

11.5.3 New Clock

Allows you to add a non-explicit clock domain. Clicking this option opens the Choose the Clock Source Pin dialog box, where you can select the clock source pin.

11.6 Set False Path Constraint Dialog Box

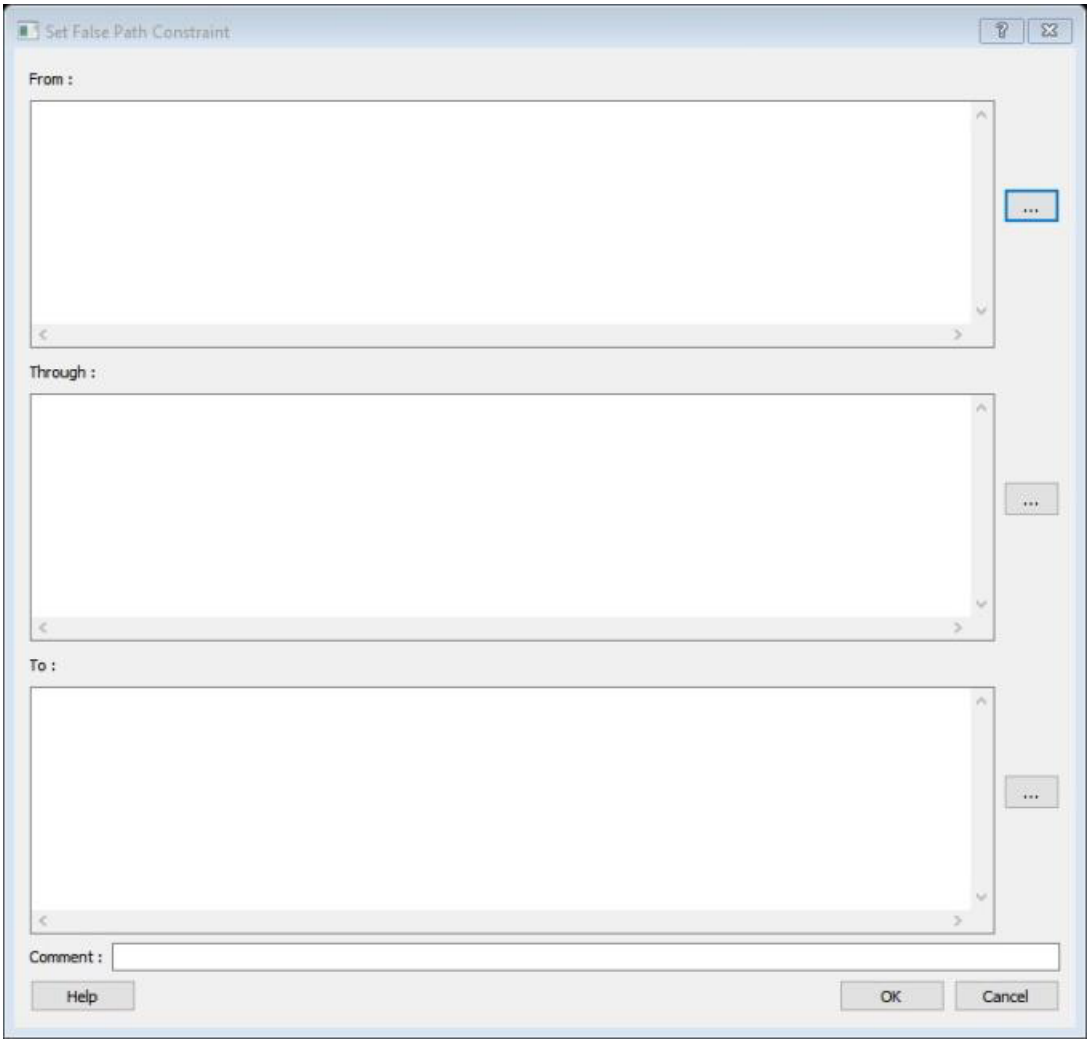
Use the Set False Path Constraint dialog box to define specific timing paths as being false.

This constraint removes timing requirements on these false paths so that they are not considered during the timing analysis. The path starting points are the input ports or register clock pins and path ending points are the register data pins or output ports. This constraint disables setup and hold checking for the specified paths.

Note: The false path information always takes precedence over multiple cycle path information and overrides maximum delay constraints.

To open the Set False Path Constraint dialog box from the SmartTime Constraints Editor, choose **Constraints > Exceptions False Path > Add False Path Constraint**.

Figure 11-7. Set False Path Constraint Dialog Box



11.6.1 From

Specifies the starting points for false path. A valid timing starting point is a clock, a primary input, an input port, or a clock pin of a sequential cell.

11.6.2 Through

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

11.6.3 To

Specifies the ending points for false path. A valid timing ending point is a clock, a primary output, an input port, or a data pin of a sequential cell.

11.6.4 Comment

Allows you to provide comments for this constraint.

11.7 SmartTime Options Dialog Box

Use the SmartTime Options dialog box to specify the SmartTime options to perform timing analysis. This interface includes the following categories:

- General
- Analysis
- Advanced

To open the SmartTime Options dialog box from the SmartTime tool, choose **Tools > Options**.

Figure 11-8. SmartTime Options- General Dialog Box for SmartFusion2, IGLOO2, and RTG4

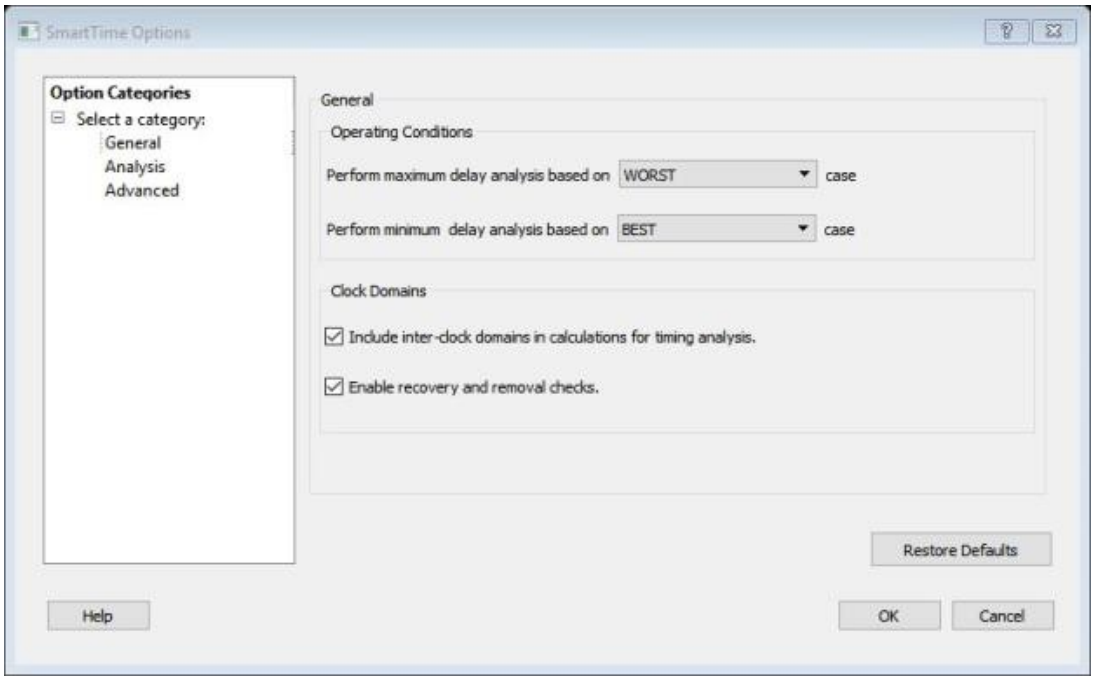
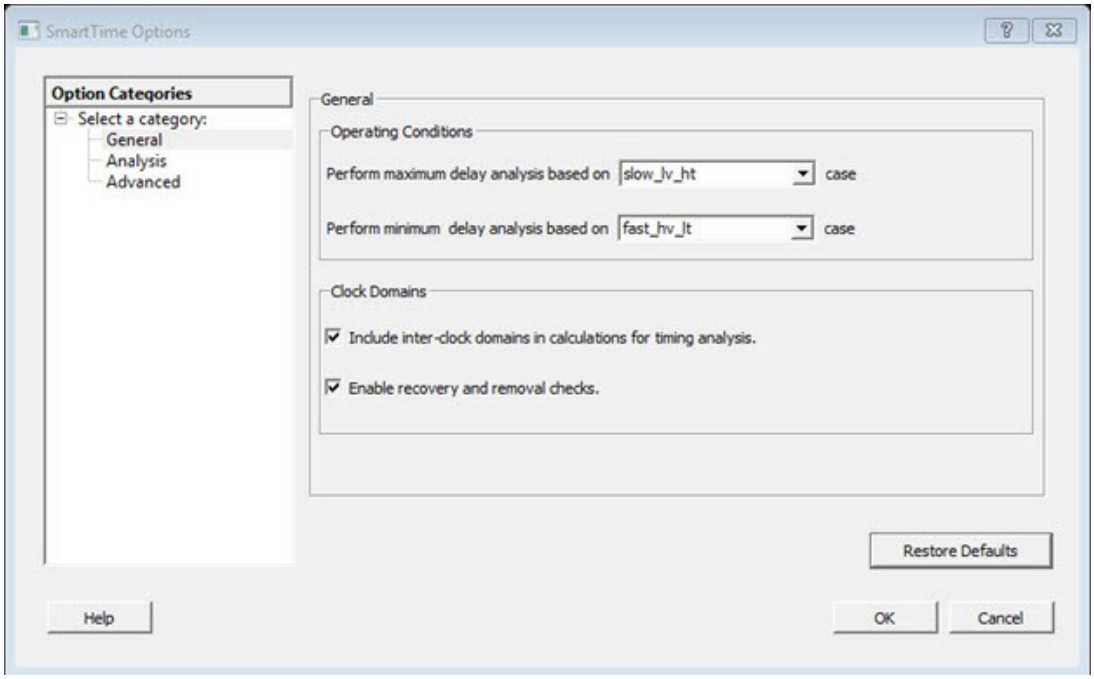


Figure 11-9. SmartTime Options - General Dialog Box for PolarFire



11.7.1 Operating Conditions

Allows you to perform maximum or minimum delay analysis based on the Best, Typical, or Worst case. By default, maximum delay analysis is based on WORST case and minimum delay analysis is based on BEST case.

11.7.2 Clock Domains

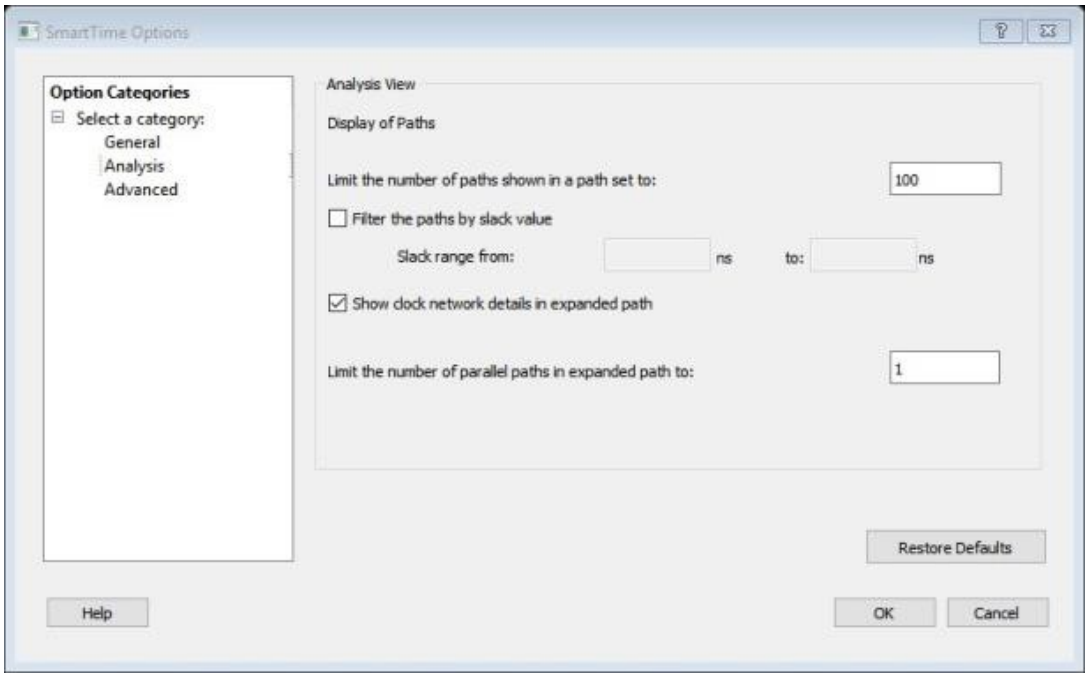
- **Include inter-clock domains in calculations for timing analysis**: Allows you to specify whether SmartTime must use inter-clock domains in calculations for timing analysis. By default, this option is unchecked.
- **Enable recovery and removal checks**: Allows SmartTime to check removal and recovery time on asynchronous signals. Additional sets are created in each clock domain in Analysis View to report the corresponding paths.

11.7.3 Restore Defaults

Resets all the options in the **General** panel to their default values.

11.7.4 Analysis

Figure 11-10. SmartTime Options - Analysis View Dialog Box



11.7.5 Display of Paths

Limits the number of paths shown in a path set for timing analysis. The default value is 100. You must specify a number greater than 1.

11.7.5.1 Filter the Paths by Slack Value

Specifies the slack range between minimum slack and maximum slack. This option is unchecked by default.

11.7.6 Show Clock Network Details in Expanded Path

Displays the clock network details as well as the data path details in the Expanded Path views.

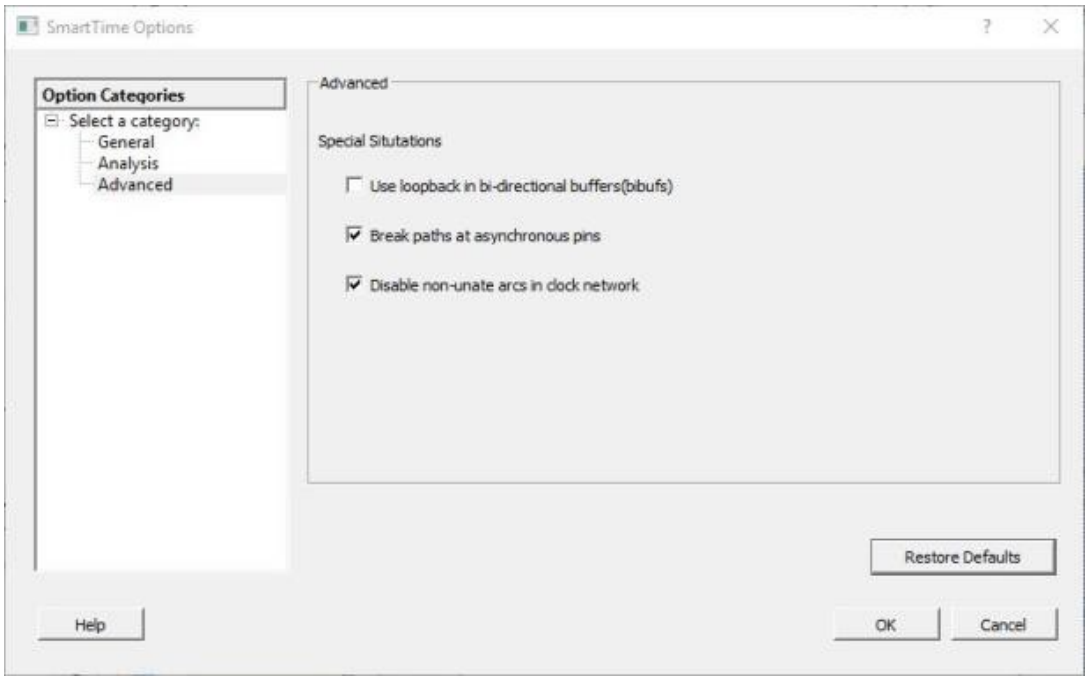
Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime displays. The default number of parallel paths is 1.

11.7.7 Restore Defaults

Resets all the options in the **Analysis View** panel to their default values.

11.7.8 Advanced Dialog Box

Figure 11-11. SmartTime Options - Advanced Dialog Box



11.7.9 Special Situations

Allows you to specify whether you need to use loopback in bi-directional buffers (bibufs) and/or break paths at asynchronous pins.

11.7.10 Scenarios

Allows you to select the scenario to use for timing analysis and for timing-driven place-and-route.

11.7.11 Restore Defaults

Resets all the options in the **Analysis View** panel to their default values.

11.8 Create Filter Set Dialog Box

Use the Create Filter Set dialog box to specify a filter.

To open the Create Filter Set dialog box from the SmartTime Timing Analyzer, select a path, and click the **Store Filter** button in the Analysis View Filter.

Figure 11-12. Create Filter Set Dialog Box

11.8.1 Name

Specifies the name of the filtered set.

11.9 Timing Bottleneck Analysis Options Dialog Box

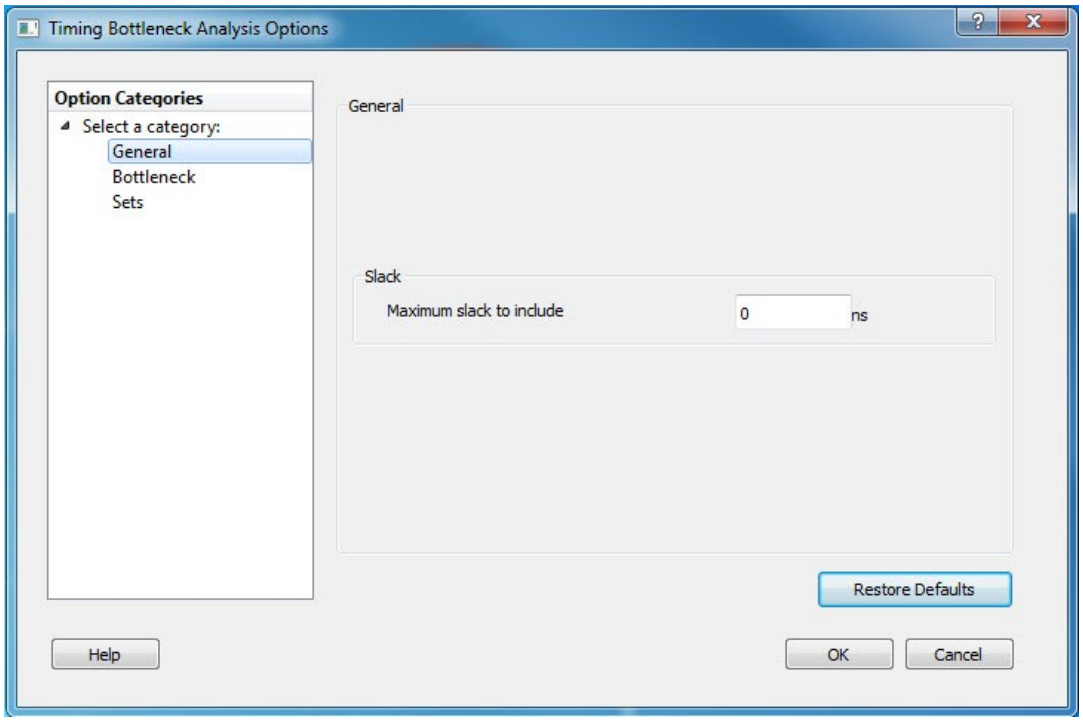
Use the Timing Bottleneck Analysis Options dialog box to customize the Timing Bottleneck Report. You can set report options for the following categories:

- General pane
- Bottleneck pane
- Sets pane

To open the Timing Bottleneck Analysis Options dialog box from the SmartTime tool, choose **Tools > Bottleneck Analysis**.

11.9.1 General Pane

Figure 11-13. Timing Bottleneck Report - General Pane Dialog Box



11.9.2 Slack

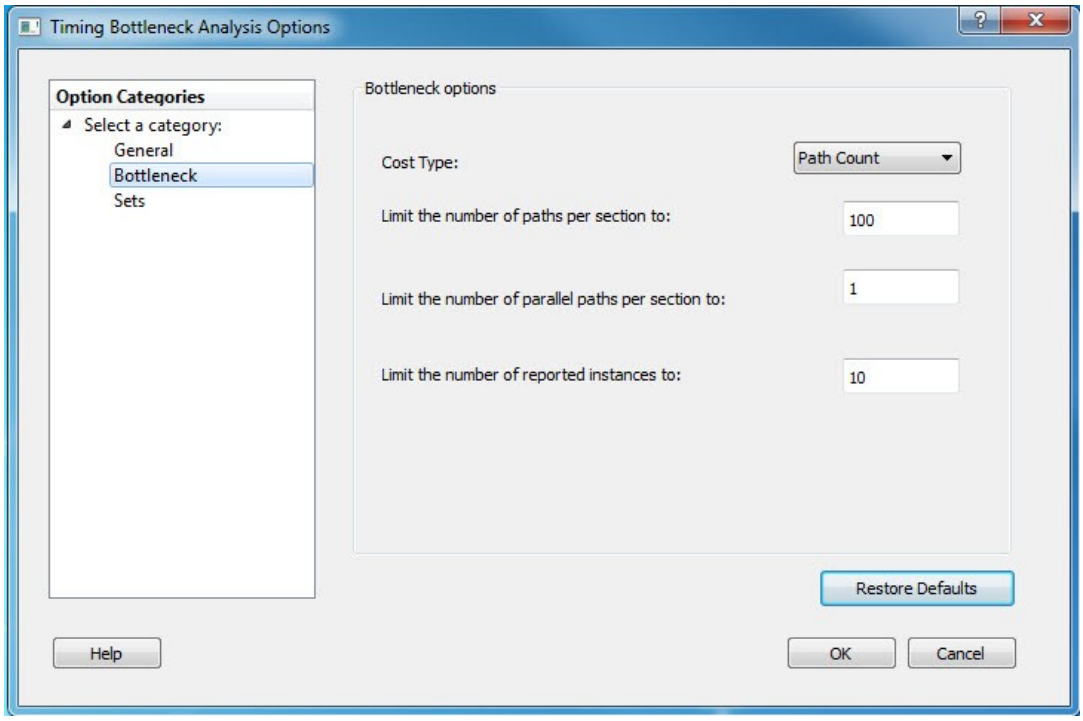
Allows you to specify whether the reported paths is filtered by threshold and, if so, what maximum slack to report. By default, the paths are filtered by slack and the slack threshold is 0.

11.9.3 Restore Defaults

Resets all the options in the **General** pane to their default values.

11.9.4 Bottleneck Pane

Figure 11-14. Timing Bottleneck Report - Bottleneck Pane Dialog Box



11.9.5 Bottleneck Options

Cost Type: Select the cost type that SmartTime will include in the Bottleneck Report. By default, path count is selected. You can select one of the following two items from the drop-down list:

- **Path Count**: This cost type associates the severity of the bottleneck to the count of violating/critical paths that traverse the instance. This is the default.
- **Path Cost**: This cost type associates the severity of the bottleneck to the sum of the timing violations for the violating/critical paths that traverse the instance.

Limit the number of paths per section to: Specify the maximum number of paths per set type that SmartTime will include per section in the report. The default maximum number of paths reported is 100.

Limit the number of parallel paths per section to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. Only cells that lie on these violating paths are reported. The default number of parallel paths is 1.

Limit the number of reported instances: Specify the maximum number of cells that SmartTime will include per section in the report. The default number of cells is 10.

11.9.6 Restore Defaults

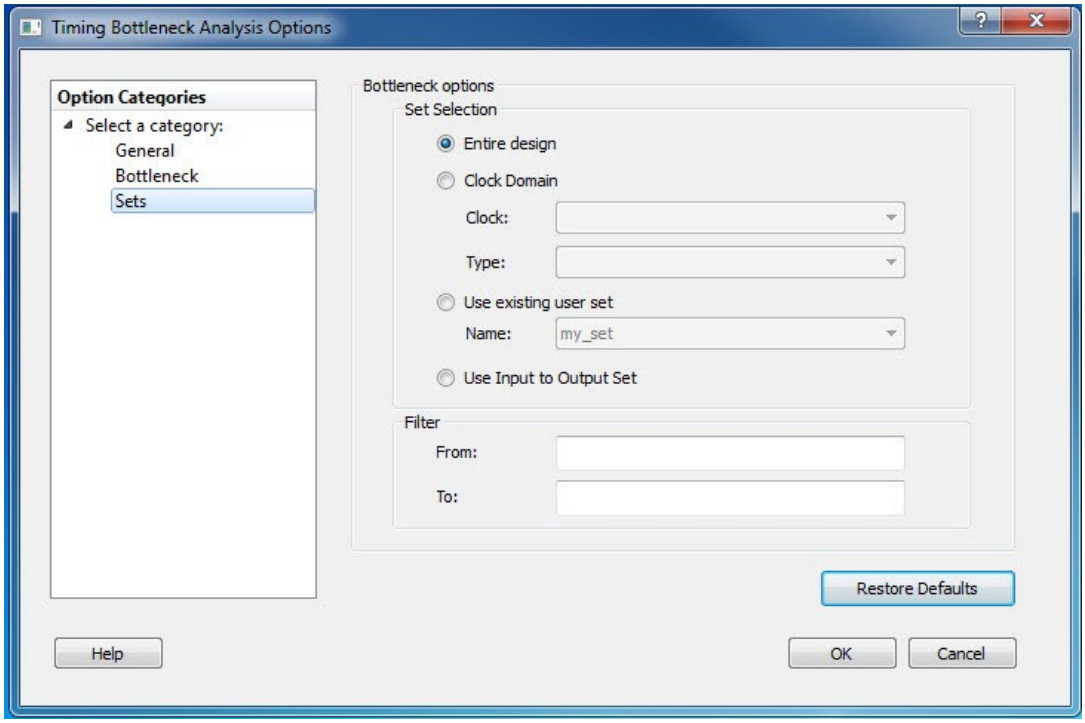
Resets all the options in the **Bottleneck** panel to their default values.

11.9.7 Sets Pane

The **Sets** pane has four mutually exclusive options:

- Entire design
- Clock Domain
- Use existing user set
- Use Input to Output Set

Figure 11-15. Timing Bottleneck Report - Sets Pane Dialog Box



Entire design: Displays bottleneck information for the entire design.

Clock Domain: Displays bottleneck information for the selected clock domain. You can specify the following options:

- **Clock**: Allows pruning based on a given clock domains. Only cells that lie on these violating paths are reported.
- **Type**: This option can only be used with -clock. The following table shows the acceptable values.

Table 11-1. Acceptable Type Values

Value	Description
Register to Register	Paths between registers in the design.
Asynchronous to Register	Paths from asynchronous pins to registers.
Register to Asynchronous	Paths from registers to asynchronous pins.
External Recovery	The set of paths from inputs to asynchronous pins.
External Setup	Paths from input ports to register.
Clock to Output	Paths from registers to output ports.

Use existing user set: Displays bottleneck information for the existing user set selected. Only paths that lie within the name set will be considered towards the Bottleneck Report.

Filter: Allows you to filter the Bottleneck Report by the following options:

- **From**: Reports only cells that lie on violating paths that start at locations specified by this option.
- **To**: Reports only cells that lie on violating paths that end at locations specified by this option. Filter defaults to all outputs.

11.9.8 Restore Defaults

Resets all the options in the **Paths** panel to their default values.

11.10 Timing Datasheet Report Options Dialog Box

Use the Timing Datasheet Report Options dialog box to select the output format for the Timing Datasheet Report.

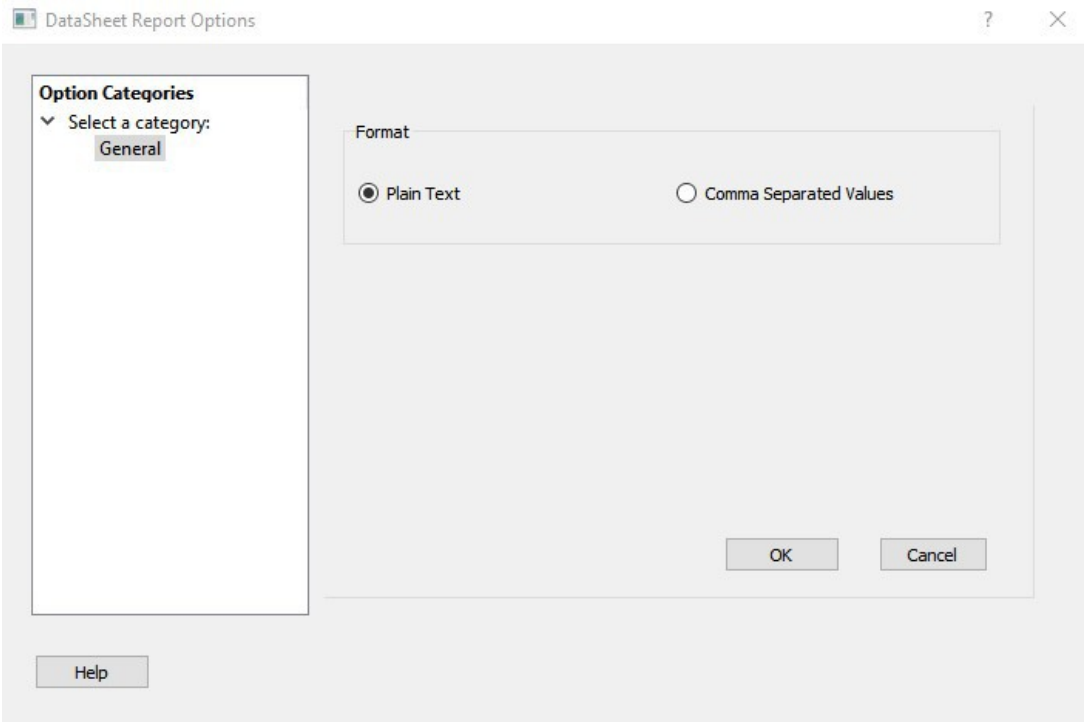
To open the Timing Datasheet Report Options dialog box from the SmartTime Max/Min Delay Analysis view, choose **Tools > Reports > Datasheet**.

You can generate your report in one of two formats:

- **Plain Text**: Saves your report to disk in plain ASCII text format.
- **Comma Separated Values**: Saves your report to disk in comma-separated value format (.CSV) format, which you can import into a spreadsheet

Note: This Datasheet Report feature is not supported for PolarFire.

Figure 11-16. Report Options Dialog Box



11.11 Timing Report Options Dialog Box

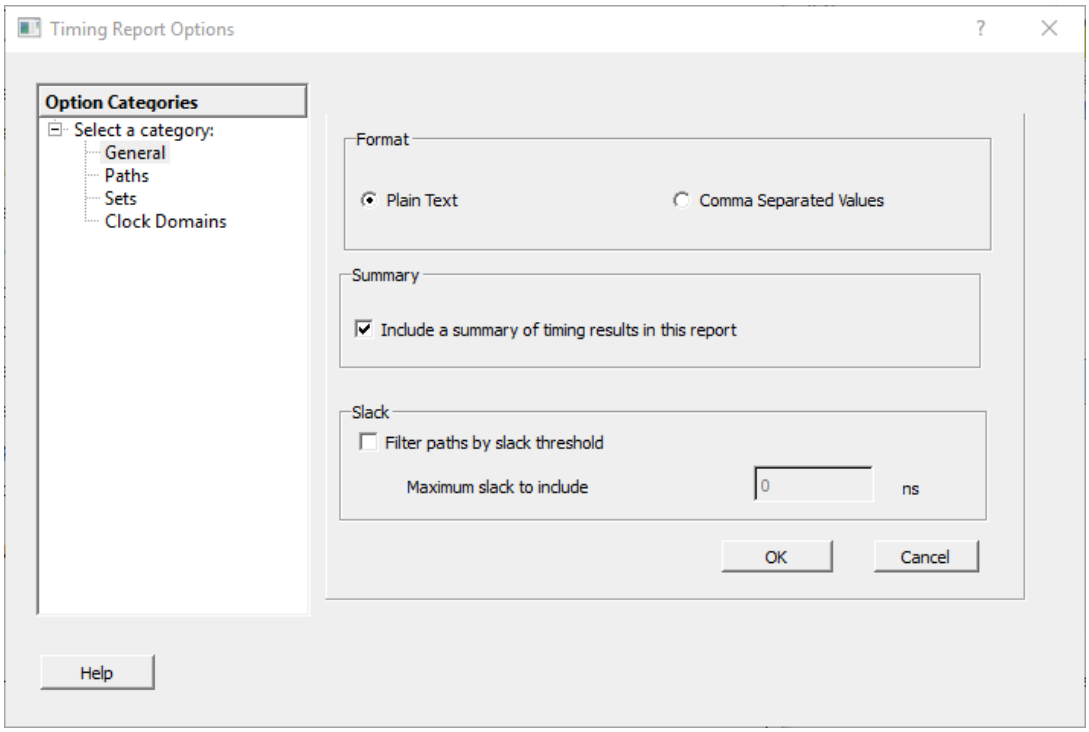
Use the Timing Report Options dialog box to customize the Timing Report. You can set report options for the following categories:

- General
- Paths
- Sets
- Clock Domains

To open the Timing Report Options dialog box from the SmartTime Max/Min Delay Analysis View, choose **Tools > Reports> Timer**.

11.11.1 General

Figure 11-17. Timing Report Options - General Dialog Box



11.11.1.1 Format

Specifies whether the report exports as a Comma Separated Value (CSV) file or a plain text file. By default, the **Plain Text** option is selected.

11.11.1.2 Summary

Specifies whether the summary section is included in the report. By default, this option is selected.

11.11.1.3 Analysis

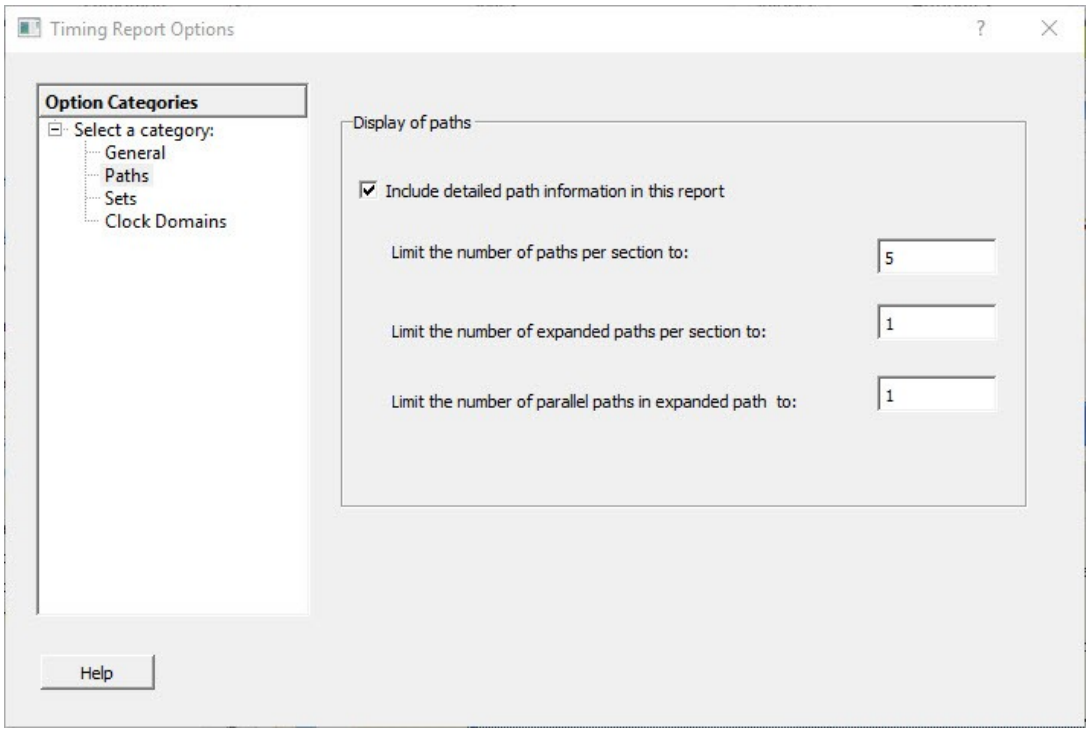
Specifies the type of analysis to be included in the Timing Report is a Maximum Delay Analysis Report or a Minimum Delay Analysis Report. By default, the Maximum Delay Analysis Report is included in the Timing Report.

11.11.1.4 Slack

Allows you to specify whether the reported paths is filtered by threshold and, if so, what maximum slack to report. By default, the paths are not filtered by slack.

11.11.2 Paths

Figure 11-18. Timing Report Options - Paths Dialog Box



11.11.3 Display of Paths

Include detailed path information in this report: Check this box to include the detailed path information in the Timing Report.

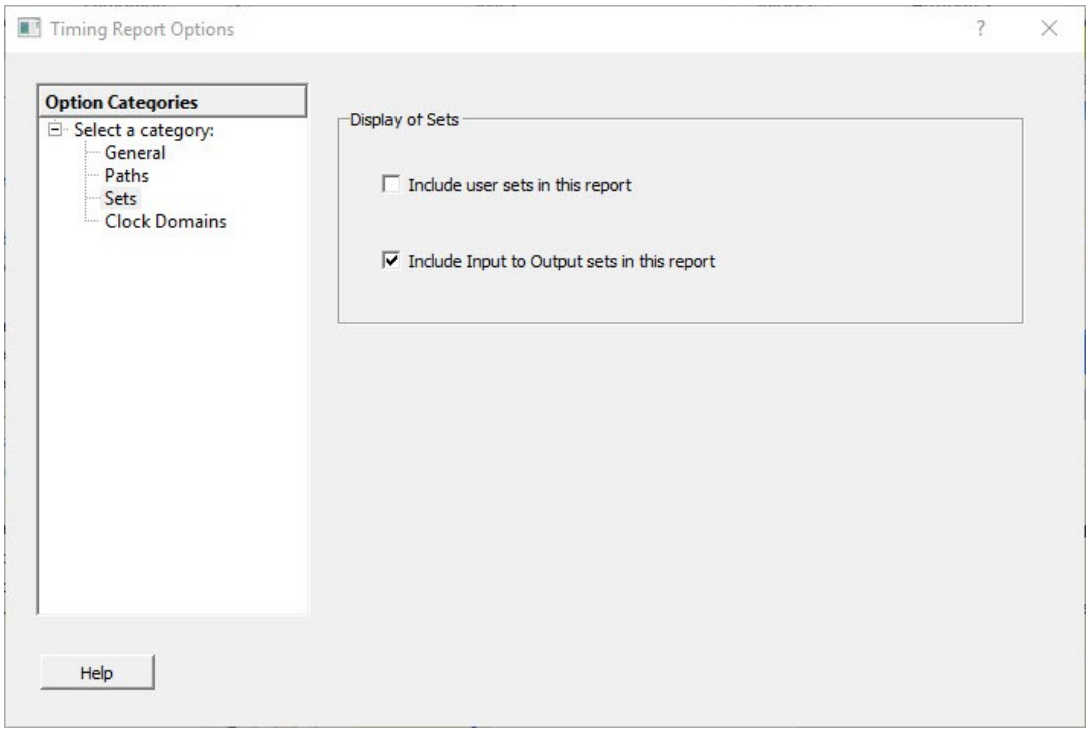
Limit the number of reported paths per section to: Specify the maximum number of paths that SmartTime will include per section in the report.

Limit the number of expanded paths per section to: Specify the maximum number of expanded paths that SmartTime will include per section in the report.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. The default number of parallel paths is 1.

11.11.4 Sets

Figure 11-19. Timing Report Options - Sets Dialog Box



11.11.4.1 Display of Sets

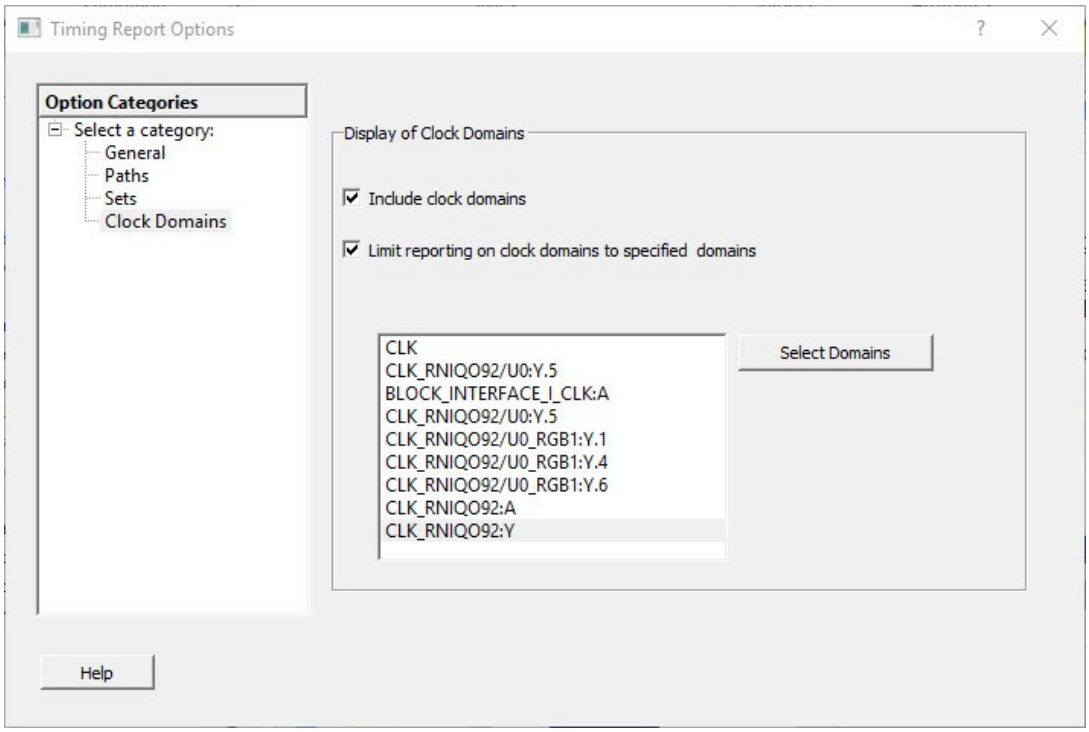
Specifies whether user sets are included in the Timing Report.

User sets are either filters you created and stored on the default paths sets (Register to Register, Inputs to Register, and so on) or Pin-to-Pin user sets. By default, the paths for these sets are not reported.

You can also specify whether the Inputs to Output sets are included in the report. By default, the Input to Output sets are reported.

11.11.5 Clock Domains

Figure 11-20. Timing Report Options - Clock Domains Dialog Box



11.11.5.1 Display of Clock Domains

Allows you to specify the clock domains included in the report. By default, the current clock domains used by the timing engine is reported.

11.11.5.2 Include Clock Domains

Allows you to include or exclude clock domains in the report. Click the check box to include clock domains.

11.11.5.3 Limit Reporting on Clock Domains to Specified Domains

Allows you to include clock domain names in the box, or include additional clock domain names using **Select Domains**.

11.12 Timing Violations Report Options Dialog Box

Use the Timing Violations Report Options dialog box to customize the Timing Violation Report. You can set report violation options for the following categories:

- General
- Paths

To open the Timing Report Options dialog box from the SmartTime tool, choose **Tools > Reports > Timing Violations**.

11.12.1 General

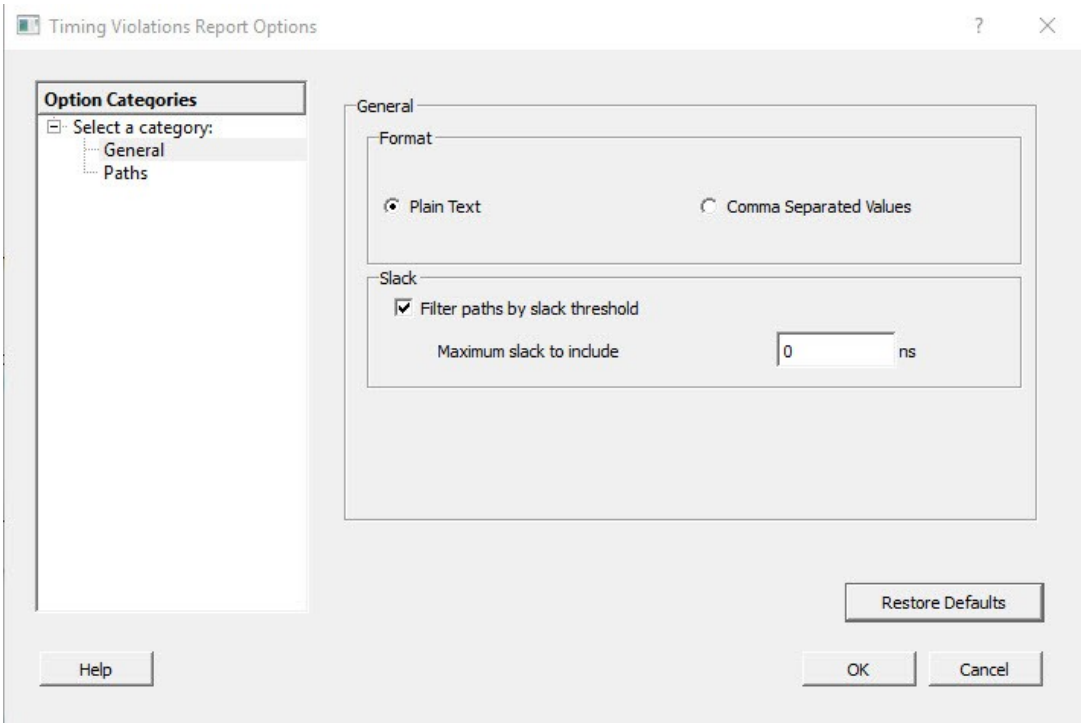


Figure 92 · Timing Violations Report - General Dialog Box

11.12.1.1 Format

Specifies whether the report exports as a Comma Separated Value (CSV) file or a plain text file. By default, the **Plain Text** option is selected.

11.12.1.2 Analysis

Allows you to specify what type of analysis is reported in the report. By default, the report includes Maximum Delay Analysis.

11.12.1.3 Slack

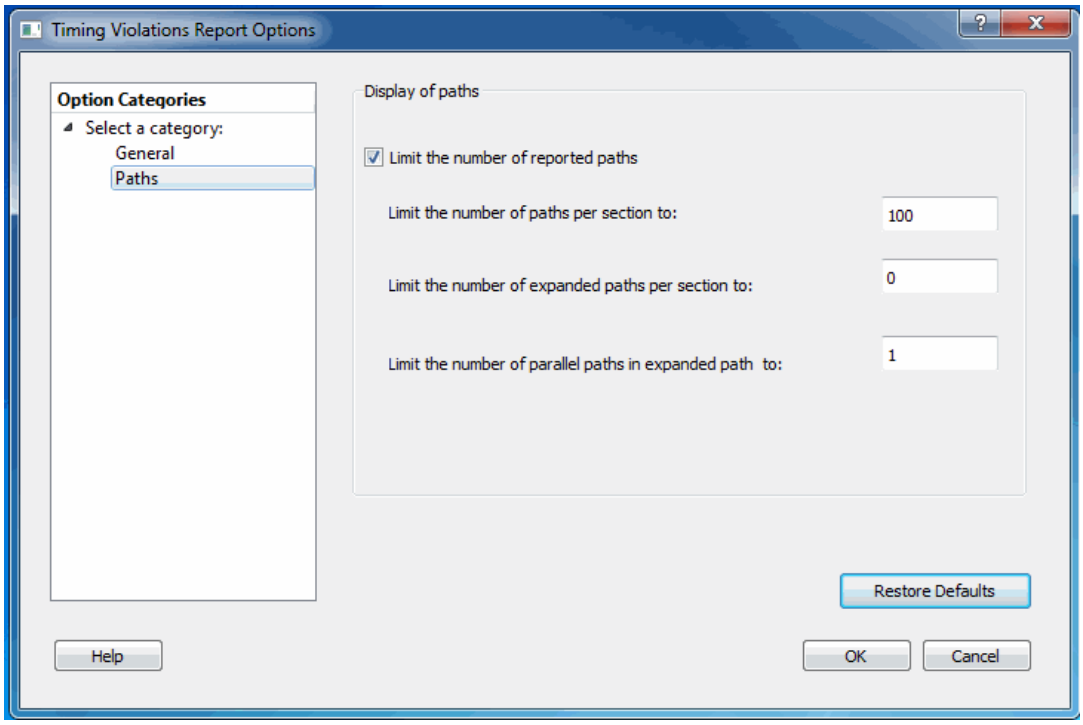
Allows you to specify whether the reported paths is filtered by threshold and, if so, what maximum slack to report. By default, the paths are filtered by slack and the slack threshold is 0.

11.12.1.4 Restore Defaults

Resets all the options in the **General** panel to their default values.

11.12.2 Paths

Figure 11-21. Timing Violations Report - Paths Dialog Box



11.12.2.1 Display of Paths

Limit the number of reported paths: Check this box to limit the number of paths in the report. By default, the number of paths is limited.

Limit the number of paths per section to: Specify the maximum number of paths that SmartTime will include per section in the report. The default maximum number of paths reported is 100.

Limit the number of expanded paths per section to: Specify the maximum number of expanded paths that SmartTime will include per section in the report. The default number of expanded paths is 0.

Limit the number of parallel paths in expanded path to: For each expanded path, specify the maximum number of parallel paths that SmartTime will include in the report. The default number of parallel paths is 1.

11.12.2.2 Restore Defaults

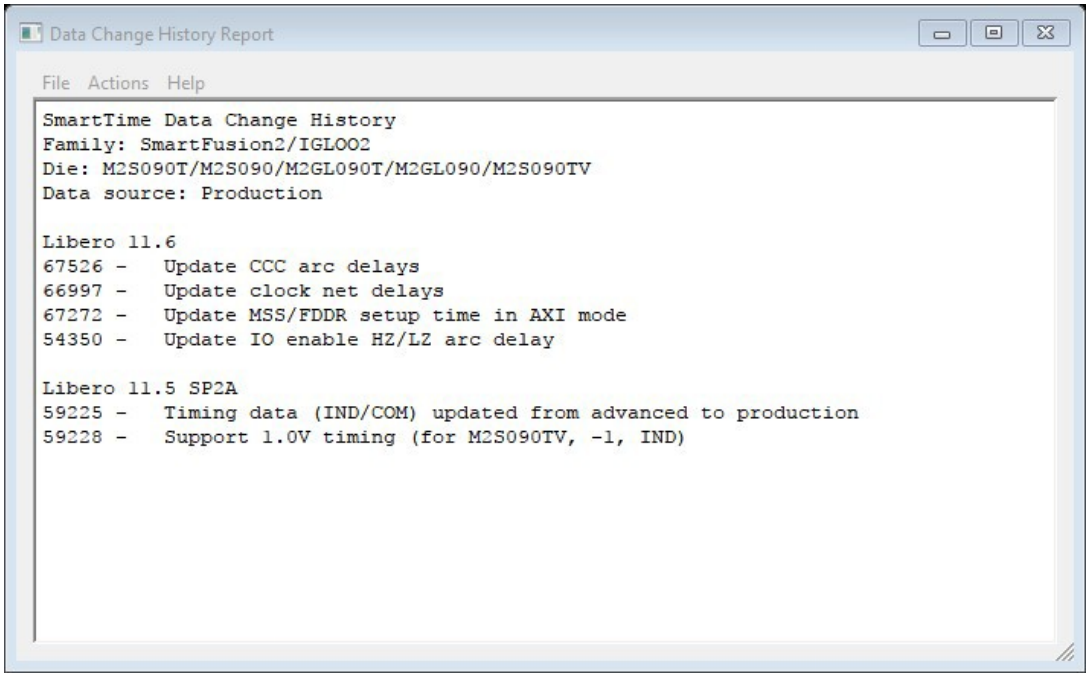
Resets all the options in the **Paths** panel to their default values.

11.13 Data Change History - SmartTime

The data change history lists features, enhancements, and bug fixes for the current software release that may impact timing data of the current design.

To generate a data change history, choose **Data Change History** from the **Help** menu to display a data change history in text format.

Figure 11-22. SmartTime Data Change History Report



12. Tcl Commands

For details about the Tcl commands supported by SmartTime, refer to the *SmartFusion2, IGLOO2, RTG4 Tcl Commands Reference Guide* or the *PolarFire FPGA Tcl Commands Reference Guide*.

13. Glossary

The following glossary defines terms in this user guide.

Table 13-1. Glossary

Term	Definition
Arrival time	Actual time in nanoseconds when data arrives at a sink pin when considering the propagation delays across the path.
Asynchronous	Two signals that are not related to each other. Signals not related to the clock are usually asynchronous.
Capture edge	The clock edge that triggers the capture of data at the end point of a path.
Clock	A periodic signal that captures data into sequential elements.
Critical path	A path with the maximum delay between a starting point and an end point. In the presence of a clock constraint, the worst critical path between registers in this clock domain is the path with the worst slack.
Data timing analysis	The standard method for verifying design functionality and performance. Both pre-layout and post-layout timing analysis can be performed via the SDF interface.
Exception	See timing exception.
Explicit clock	Clock sources that can be traced back unambiguously from the clock pin of the registers they deserve, including the output of a DLL or PLL.
Filter	A set of limitations applied to object names in timing analysis to generate target specific sets.
Launch edge	The clock edge that triggers the release of data from a starting point to be captured by another clock edge at an end point.
Minimum period	Timing characteristic of a path between two registers. It indicates how fast the clock will run when this path is the most critical one. The minimum period value takes into consideration both the skew and the setup on the receiving register.
Parallel paths	Paths that run in parallel between a given source and sink pair.
Path	A sequence of elements in the design that identifies a logical flow starting at a source pin and ending at a sink pin.
Path details	An expansion of the path that shows all the nets and cells between the source pin and the sink pin.
Path set	A collection of paths.
Paths list	Same as path set.

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Term	Definition
Post-layout	The state of the design after you run Layout. In post-layout, the placement and routing information are available for the whole design.
Potential clock	Pins or ports connected to the clock pins of sequential elements that the Static Timing Analysis (STA) tool cannot determine whether they are is enabled sources or clock sources. This type of clock is generally associated with the use of gated clocks.
Pre-layout	The state of the design before you run Layout. In pre-layout, the placement and routing information are not available.
Recovery time	The amount of time before the active clock edge when the de-activation of asynchronous signals is not allowed.
Removal time	The amount of time after the active clock edge when the de-activation of asynchronous signals is not allowed.
Required time	The time when data must be at a sink pin to avoid being in violation.
Requirement	See timing requirement.
Scenario (timing constraints scenario)	Set of timing constraints defined by the user.
Setup time	The time in nanoseconds relative to a clock edge during which the data at the input to a sequential element must remain stable.
Sink pin	The pin located at the end of the timing path. This pin is usually the one where arrival time and required time are evaluated for path violation.
Skew	The difference between the clock insertion delay to the clock pin of a sink register and the insertion delay to the clock pin of a source register.
Slack	The difference between the arrival time and the required time at a specific pin, generally at the data pin of a sequential component.
Slew rate	The time needed for a signal to transition from one logic level to another.
Source pin	The pin located at the beginning of a timing path.
STA	See static timing analysis.
Standard delay format (SDF)	A standard file format used to store design data suited for back-annotation.
Static timing analysis	An efficient technique to identify timing violations in a design and to ensure that all timing requirements are met. It is well suited for traditional synchronous designs. The main advantages are that it does not require input vectors, and it exclusively covers all possible paths in the design in a relatively short run-time.

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Term	Definition
Synopsys design constraint (SDC)	A standard file format for timing constraints. Synopsys Design Constraints (SDC) is a Tcl-based format used by Synopsys tools to specify the design intent, including the timing and area constraints for a design. Microsemi SoC tools use a subset of the SDC format to capture supported timing constraints. You can import or export an SDC file from the Designer software. Any timing constraint that you can enter using Designer tools, can also be specified in an SDC file.
Timing constraint	A requirement or limitation on the design to be satisfied during the design implementation.
Timing exception	An exception to a general requirement usually applied on a subset of the objects on which the requirement is applied.
Timing requirement	A constraint on the design usually determined by the specifications at the system level.
Virtual clock	A virtual clock is a clock with no source associated to it. It is used to describe clocks outside the FPGA that have an impact on the timing analysis inside the FPGA. For example, if the I/Os are synchronous to an external clock.
Wire Load Model (WLM)	A timing model used in pre-layout to estimate a net delay based on the fan-out.

14. Revision History

Revision	Date	Description
B	04/2021	Generating a CDC Report: Added information related to cross probing, corner scenarios, and updated notes.
A	11/2020	Document converted to Microchip template. Initial Revision.

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