

# SmartPower User Guide

### Introduction

SmartPower is a power-analysis tool that allows you to visualize power consumption and potential power consumption problems globally and in-depth within your design, so you can make adjustments – when possible – to reduce power.

SmartPower provides a detailed and accurate way to analyze designs for Microchip SoC FPGAs, from top-level summaries to deep-down specific functions within the design, such as gates, nets, I/Os, memories, clock domains, blocks, and power supply rails.

You can analyze the hierarchy of block instances and specific instances within a hierarchy, and each can be organized in various ways to show the respective power consumption of the component pieces.

SmartPower also analyzes power by functional modes, such as Active, Flash\*Freeze, Shutdown, Sleep, or Static, depending on the specific FPGA family used. You can also create custom modes that may have been created in the design. Custom modes can also be used for testing "what if" potential operating modes.

SmartPower has a unique feature that allows you to create test scenario profiles. A profile enables you to create sets of operational modes, so you can understand the average power consumed by this combination of functional modes. An example may be a combination of Active, Sleep, and Static modes — as would be used over time in an actual application.

SmartPower generates detailed hierarchical reports of the power consumption of a design for easy evaluation. This enables you to locate the power consumption source and take appropriate action to reduce the power if possible.

SmartPower supports use of files in the Value-Change Dump (VCD) format, as specified in the IEEE<sup>®</sup> 1364 standard, generated by the simulation runs. Support for this format lets you generate switching activity information from ModelSim or other simulators, and then use the switching activity-over-time results to evaluate average and peak power consumption for your design.

SmartPower supports SmartFusion<sup>®</sup>2, IGLOO<sup>®</sup>2, RTG4<sup>™</sup>, PolarFire<sup>®</sup>, and PolarFire<sup>®</sup> SoC devices.

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# 1. Starting SmartPower

Set the target clock and data frequencies before you evaluate your power consumption.

- 1. Open the Design Flow window.
- 2. In the Design Flow window, right-click Verify Power and choose Open Interactively.

The SmartPower analysis tool window appears.

### Figure 1-1. SmartPower User Interface (SmartFusion<sup>®</sup>2, IGLOO<sup>®</sup>2, and RTG4<sup>™</sup>)

1 sd * - SmartPower		– 0 ×
File Edit View Tools Simulation	Help	
	🗴 🐵 🖉 🕨 Typical 💌 MHz 💌 mW 💌	
Modes and Scenarios	😢 Summary 🕼 Domains 🔊 Analysis 🕼 Frequencies 🕏 Probabilities	
Pre-defined modes     Active	Power Consumption	
Static	Total Static	
		Dynamic
	111.468 mW 99.115 mV	V 12.353 mW
	Breakdown By Type Show  Grant  Grant	
	Breakdown By Type  Show  Grid	
	Power	Usage
	Other Rails Static 0.45 mVV	Gate
	0.4511/4	12.353 mW
	Core Static 98.665 m/V	
	[96.665 m/v]	
		Show Annotation Coverage
	Operating Conditions : Typical	
	Operating Conditions	Value
	1 0 Junction Temperature	25 C
	2 Process	Typical
	3 VDD	1V
	4 VDD18	1.8 V
	5 VDDI 1.8	1.8V
	6 VDDAUX 7 VDD25	2.5 V 2.5 V
	1 10023	
	Change Operating Conditions	
	Battery	
	Battery capacity 1000.00 mA*Hrs Set	Battery Life 9.967 Hour(s)
New Custom Mode		
New Custom Scenario		
		Active 25.00 C 1.00 V Speed: -1

-		
1 sd * - SmartPower		- 0 X
File Edit View Tools Simulation		
] 🖬 👌 👌 👂 🎝 🖓 🗗 😂 隆	1 🐵 🖉 🕨 Typical 💌 MHz 💌 mW 💌	
Modes and Scenarios 🗗 🗙	😢 Summary 🕼 Domains 🕼 Analysis 🕼 Frequencies 🕸 Probabilities	
Pre-defined modes     Fill Active     Static	Power Consumption Total Static 111.468 mW 99.115 mV Breakdown By Type Show C Chart C Grid Other Rais Static 045 mW Core Static 89.665 mW Core Static 89.665 mW	
	Operating Conditions : Typical	Show Annotation Coverage
	Operating Conditions	Value
	1 D Junction Temperature	25 C
	2 Process 3 VDD	Typical 1 V
	4 VDD18	1.8 V
	5 VDDI 1.8	1.8 V
	6 VDDAUX	2.5 V
	7 VDD25	2.5 V
	Change Operating Conditions  Battery	
New Custom Mode	Battery capacity 1000.00 mA*Hrs Set	Battery Life 9.967 Hour(s)
New Custom Scenario		
		Active 25.00 C 1.00 V Speed: -1

### Figure 1-2. SmartPower User Interface (PolarFire<sup>®</sup>)

# 2. SmartPower Interface

The following sections describe the SmartPower tabs, toolbars, and menu commands.

### 2.1 Summary Tab

The **Summary** tab is organized into the following sections:

- Power Consumption
- Breakdown
- Annotation Coverage
- Operating Conditions
- Battery

### Figure 2-1. SmartPower Summary Tab

	imary	ល Domains	🔎 Analysis	👘 Freq	uencies 🛛 🕏	Probabilites			
ower	r Consur	mption							
		Total		0.042 m	w				
		Static		0.042 m	w				
		Dyna		0 mW					
		Dyna		0 11117					
Break	down —	Ву Туре	•				Chart 🔿 Grid —		
					Power Us	age			
				ks Static .008 mVV		Core Stati			
						0.034 mV	<u></u>	Hide an	notation covera
\nnot	ation Co	overage Free	quency>=0	<b>•</b>				<u>inde dri</u>	
511100									
	F	Frequency>=		VCD	Manual	SmartTime	Vectorless	Fixed Values	Total
		Frequency>=	U An	notation	Annotation	Constraint	Estimation	Fixed Values	Total
1	Clocks		U An	notation 0 (0%)	Annotation 0 (0%)	Constraint 0 (0%)	Estimation 0 (0%)	5 (100%)	5
12	Clocks Registe	routputs	U An	notation 0 (0%) 0 (0%)	Annotation 0 (0%) 0 (0%)	Constraint 0 (0%) 0 (0%)	Estimation 0 (0%) 0 (0%)	5 (100%) 18 (100%)	5 18
1 2 3	Clocks Registe Combin	r outputs ational outputs	U An	notation 0 (0%) 0 (0%) 0 (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint 0 (0%) 0 (0%) 0 (0%)	Estimation 0 (0%) 0 (0%) 0 (0%)	5 (100%) 18 (100%) 59 (100%)	5 18 59
1 2 3 4	Clocks Registe Combin Set/Re:	r outputs ational outputs set nets	V An	notation 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	E stimation 0 (0%) 0 (0%) 0 (0%) 0 (0%)	5 (100%) 18 (100%) 59 (100%) 4 (100%)	5 18 59 4
1 2 3 4 5	Clocks Registe Combin Set/Res Primary	r outputs ational outputs set nets inputs	V An	notation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	E stimation           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	5 (100%) 18 (100%) 59 (100%) 4 (100%) 9 (100%)	5 18 59 4 9
1 2 3 4 5 6	Clocks Registe Combin Set/Re:	r outputs ational outputs set nets inputs pins	U An	notation 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	E stimation 0 (0%) 0 (0%) 0 (0%) 0 (0%)	5 (100%) 18 (100%) 59 (100%) 4 (100%)	5 18 59 4
1 2 3 4 5 6 7	Clocks Registe Combin Set/Re Set/Re Primary Enable Other pi	r outputs ational outputs set nets inputs pins	An	notation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	Estimation           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	5 (100%) 18 (100%) 59 (100%) 4 (100%) 9 (100%) 0 (0%)	5 18 59 4 9 0
1 2 3 4 5 6 7	Clocks Registe Combin Set/Re Set/Re Primary Enable Other pi	r outputs ational outputs set nets inputs pins ins nditions : Typica	An	notation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	Estimation           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	5 (100%) 18 (100%) 59 (100%) 4 (100%) 9 (100%) 0 (0%) 0 (0%)	5 18 59 4 9 0
1 2 3 4 5 6 7	Clocks Registe Combin Set/Re Set/Re Primary Enable Other pi	r outputs ational outputs set nets inputs pins ins nditions : Typica	An	notation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	Estimation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) Value 25 C	5 (100%) 18 (100%) 59 (100%) 4 (100%) 9 (100%) 0 (0%) 0 (0%)	5 18 59 4 9 0
1 2 3 4 5 6 7	Clocks Registe Combin Set/Re: Primary Enable Other pi	r outputs ational outputs set nets inputs pins ins nditions : Typica	An	notation           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           o (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	Estimation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) Value 25 C 1.2 V	5 (100%) 18 (100%) 59 (100%) 4 (100%) 9 (100%) 0 (0%) 0 (0%)	5 18 59 4 9 0
1 2 3 4 5 6 7	Clocks Registe Combin Set/Re: Primary Enable Other pi	r outputs ational outputs set nets inputs pins ins nditions : Typica	An	notation           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           o (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	Estimation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) Value 25 C	5 (100%) 18 (100%) 59 (100%) 4 (100%) 9 (100%) 0 (0%) 0 (0%)	5 18 59 4 9 0
1 2 3 4 5 6 7	Clocks Registe Combin Set/Re: Primary Enable Other pi	r outputs ational outputs set nets inputs pins ins nditions : Typica	An	notation           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           o (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	Estimation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) Value 25 C 1.2 V	5 (100%) 18 (100%) 59 (100%) 4 (100%) 9 (100%) 0 (0%) 0 (0%)	5 18 59 4 9 0
1 2 3 4 5 6 7	Clocks Registe Combin- Set/Re: Primary Enable Other pi ting Cor	r outputs ational outputs set nets inputs pins ins nditions : Typica	An An An An An An An An An An An An An A	notation           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           o (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	Estimation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) Value 25 C 1.2 V	5 (100%) 18 (100%) 59 (100%) 4 (100%) 9 (100%) 0 (0%) 0 (0%)	5 18 59 4 9 0
1 2 3 4 5 6 7 7	Clocks Registe Combin Set/Re: Primary Enable Other pi ting Cor	r outputs ational outputs set nets inputs pins ins nditions : Typica	An An An An An An An An An An An An An A	notation           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           o (0%)	Annotation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%)	Constraint           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	Estimation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) Value 25 C 1.2 V	5 (100%) 18 (100%) 59 (100%) 4 (100%) 9 (100%) 0 (0%) 0 (0%)	5 18 59 4 9 0
1 2 3 4 5 6 7 7	Clocks Registe Combin Set/Re: Primary Enable Other pi ting Cor	r outputs ational outputs set nets inputs pins ins nditions : Typics Of erating Condition	An An An An An An An An An An An An An A	notation           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           o (0%)	Annotation 0 (0%) 0 (0%	Constraint           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)           0 (0%)	Estimation 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) 0 (0%) Value 25 C 1.2 V	5 (100%) 18 (100%) 59 (100%) 4 (100%) 9 (100%) 0 (0%) 0 (0%)	5 18 59 4 9 0

### 2.1.1 Power Consumption

Displays the total power consumption and the static and dynamic power of the design. The information displayed is accurate after you enter your target clock and data frequencies.

### 2.1.2 Breakdown

Displays a breakdown of power consumption in the design. A drop-down list allows you to view the power breakdown by type of component, voltage rail, or clock domain.

### 2.1.2.1 Show

Displays power usage as a chart or as a grid.

When you select **By Type** from the drop-down list, the **Summary** tab displays a breakdown of the design's power usage by the following types:

- Net
- Gate
- I/O
- Memory
- Core Static
- Banks Static
- Analog (for Fusion Designs)

Any static power used by instances of a component in a design will be included in the appropriate category. As a result, the sum of the power in breakdown by type will be equal to the total static and dynamic power consumption of the design. Percentages displayed are fractions of the total power. Global nets are included in the net power types. To obtain the power of a clock, select breakdown by clock domain.

When you select **By Rail** from the drop-down list, the **Summary** tab displays a breakdown of the power usage by the rail that the power is drawn from and a breakdown for the current usage. The power, voltage, and current drawn for each rail are displayed.

When you select **By Clock Domain** from the drop-down list, the **Summary** tab displays a breakdown of the power usage by the clock domain that the power is drawn from. For each clock domain, the power and percentage of power drawn are displayed. Dynamic power is accounted for in breakdown by clock, but static power is not associated with any clock.

**By Mode** is available only when a scenario is selected. When you select **By Mode** in the Modes and Scenarios toolbar, the **Summary** tab shows power consumption, duration, and power duration weight by mode.

After you select **By Type**, **By Rail**, **By Mode**, or **By Clock Domain**, you can customize the columns in the grid by right-clicking the column headers. To exclude a column, remove its check mark from the right-click menu. Right-click a column header to set the column default size for the selected column or for all columns, and then sort the values in ascending order, descending order, or customize the columns.

To sort the contents of a column, double-click a column header.

To export the contents of the grid to a file, from the **File** menu, choose **Export Grid** or click its associated toolbar button.

To print the grid, from the **File** menu, choose **Print Grid** or click its associated toolbar button. To copy the grid, from the **Edit** menu, choose **Copy Grid** or click its toolbar button.

To copy the chart, click the contents of the chart, and from the right-click menu, choose **Copy Chart to Clipboard**.

To export the chart, click the contents of the chart, and from the right-click menu, choose Export Chart to File.

To rotate the chart by 90 degrees, click the contents of the chart, and from the right-click menu, choose **Rotate Chart Clockwise** or **Rotate Chart Counter-Clockwise**.

### 2.1.3 Annotation Coverage

Displays the number and percentage of pins annotated by each source (VCD, manual annotation, SmartTime constraint, vectorless estimation, and fixed values) for all clocks, register outputs, combinational outputs, set/reset nets, primary inputs, enable pins, and other pins.

- Hide annotation coverage link: hides the annotation coverage.
- Show annotation coverage link: shows the annotation coverage.
- **Annotation Coverage Summary** drop-down menu: shows probability or frequency annotation statistics (frequency=0 shows statistics for pins that have a frequency of 0).

- VCD: shows the number/percentage of pins with frequencies/probabilities imported from a VCD file.
- Manual annotation: shows the percentage of pins with manually annotated frequencies/probabilities.
- SmartTime constraint: shows the percentage of pins initialized with SmartTime.
- Fixed values: shows the percentage of pins with default frequency/probability.
- Vectorless estimation: shows the percentage of pins that have been annotated with vectorless estimation.

### 2.1.4 Operating Conditions

Displays the temperature and voltage operating conditions for the selected mode or scenario specified in the Operating Conditions dialog box. When you select a scenario, the temperature and voltage operating conditions for each mode in the scenario are displayed.

To change the operating conditions, click the **Change Operating Conditions** link or from the **Tools** menu, and then choose **Operating Conditions**.

#### 2.1.4.1 Battery

Allows you to set the battery capacity in mA/hr and reports the battery life.

### 2.2 Domains Tab

The **Domains** tab lists existing domains along with their corresponding clock and data frequencies and probability data for clock domains and sets of pins. In this tab, you can add, edit, or remove domains or sets of pins, and change the clock and/or data frequency for a selected domain.

When you start SmartPower for the first time, it automatically initializes frequencies from SmartTime with a default data toggle rate of 10%. However, if you update your timing constraints in SmartTime, you can use the Initialize Frequencies and Probabilities dialog box to update SmartPower with new frequencies from SmartTime. If you do not have timing constraints in SmartTime, you can initialize clock and data frequencies manually by directly editing the **Domains** tab grid or using the Initialize Frequencies and Probabilities Frequencies and Probabilities Frequencies and Probabilities dialog box.

If you import a VCD file, the **Domains** tab shows the average clock and data frequencies for each clock domain and input set. This average is calculated using VCD information.

**Note:** If you change a clock or data frequency in the **Domains** tab, it impacts only nets that use the default estimation source. Nets use the default estimation source when they have not been manually set to a specific frequency in the **Frequencies** tab, and when they have not been set by importing a VCD file. To see explicitly the list of nets using the default estimation source, refer to the Frequencies tab.

Figure 2-2	SmartPower	Domains	Tab
I Iguie Z-Z.		Domains	iab

🗞 Summary	💼 Domains	🔎 Analysis 🛛 👘 I	Frequencies 🛛 🔒	Probabilites				
Show : ( Clock domain:	• Frequencies	O Probabilities						
Status	;	Name		Clocks (MHz)	Register outputs	Set/Reset nets	Primary inputs (MHz)	Combinational outputs (MHz)
1 🗸	CLKIN			100	5 (10 %)	0(0%)	5 (10 %)	5 (10 %)
Set of pins —								Hide set of
Status				Name				▲ Data (MHz)
	Input to Out	put		Name				Data

**Note:** Data and clock frequencies are set to zero automatically when in non-active modes.

To hide or display the grid for set of pins, click the **Hide/Show set of pins link**. You can edit frequency or probability data directly from the grid.

To create a new clock domain or set of pins:

- 1. Right-click the clock domain or set of pins and choose create new clock domain or create new set of pins.
- 2. Enter a name and click **OK**. The new clock domain or set of pins appears in the **Domains** tab.
- 3. Modify the frequency and probability data as needed.

To initialize, clock domain frequencies, right-click the clock domain name and select **Initialize Frequencies and Probabilities**. If there is no frequency constraint set for the clock domain in SmartTime, the clock frequency of the domain is not changed.

The status of a clock frequency or probability is displayed in the first column by an icon. Mouse over the icon to identify the status (see the following table).

Table 2-1. Clock Frequency/Probability Status

lcon	Description
Δ	This clock has not been initialized.
	No constraints available for this clock from SmartTime.
✓	Average frequencies/probabilities imported from VCD.
✓	Clock constraints imported from SmartTime.
✓	This clock has been initialized manually.

**Note:** The frequency and probability distribution feature is available only in active operating mode or when in a mode based on the Active mode.

An icon in the first column shows the status of a set of pins. Mouse over the icon to identify the status (see the following table).

#### Table 2-2. Set of Pins Status

lcon	Description
▲	This set has not been initialized.
✓	Average frequencies/probabilities imported from VCD.
✓	This set has been manually initialized

**Note:** The frequency and probability distribution feature is available only in active operating mode or when in a mode based on the Active mode.

To remove one or multiple clock domains, select the clock domain(s) and click Remove Selected Domains(s).

To edit a clock domain or a set of pins:

1. Select the clock domain and from the right-click menu, and choose **Edit Domain**. The Clock Domain or Set-of-Pins window appears.

### Figure 2-3. Clock Domain Window

CLK/Clk1_reg:Q Pins (Clock Domain)	
Any pins that do not belong to a domain are listed in the ''Unclassi pin from the 'Unclassified Pins' list box and add it to CLK/Clk1_reg You may also want select a pin from CLK/Clk1_reg:Q and remove appear in the Unclassified Pins list box).	:Q.
Unclassified Pins: CLK/U108:Y CREG/U36:Y CS_N CTRL/U10:Y CTRL/U10:Y CTRL/U12/U0:Y CTRL/U12:Y CTRL/U14:Y CTRL/U15/U0:Y	Clock Pins
* Set Select All	× Set Select All
Help	OK Cancel

Any pins that do not belong to a domain appear under **Unclassified Pins**. You can select a pin from this list and add it to the current domain. You can also select a pin from the current domain and remove it from the domain (this pin will appear under **Unclassified Pins**).

**Clock Pins and Data Pins:** Select **Clock Pins** from the pull-down list to display all clock pins for the selected domain, or select **Data Pins** to display registers, asynchronous signals, primary input, and combinational signals for the selected domain.

Use the filter boxes to narrow your search for a specific pin. The boxes are text filters; \* is a wildcard.

2. Click OK.

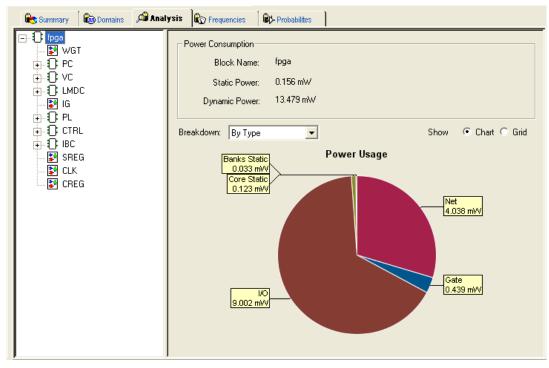
To delete a clock domain or a set-of-pins, select the clock domain or set-of-pins and choose **Remove Domain** from the right-click menu.

### 2.3 Analysis Tab

The **Analysis** tab allows you to inspect detailed hierarchical reports of the power consumption. The **Analysis** tab consists of two windows:

- Hierarchy of Instances window
- · Analysis window

### Figure 2-4. SmartPower Analysis Tab



### 2.3.1 Hierarchy of Instances Window

SmartPower lists the hierarchy of instances in the Hierarchy of Instances window. Clicking the plus sign (+) next to a block expands the block to show its sub-blocks. Only hierarchical blocks are displayed in this list (no gates or nets).

When you select a block of the hierarchical tree, SmartPower displays its name and power consumption in the Analysis window.

### 2.3.2 Analysis Window

The Analysis window is organized into two sections:

- Power Consumption
  - Breakdown

### 2.3.2.1 Power Consumption

Displays the name of the currently selected block from the hierarchy of instances window, as well as the static and dynamic power consumption of the selected block.

### 2.3.2.2 Breakdown

Displays a breakdown of power usage of the currently selected block. Use the drop-down list to view the power breakdown by type of component (instance, or clock domain).

When you select **By Type** from the drop-down list, the **Analysis** tab shows a breakdown of the selected block's power usage by the following types:

- Net
- Gate

- I/O
- Memory
- Core Static
- Banks Static
- Analog

Any static power used by instances of a component in a design are included in the appropriate category.

The sum of the power in breakdown by type equals the total static and dynamic power consumption of the design. Percentages displayed are fractions of the total power. Global nets are included in the net power types. To obtain the power of a clock, select breakdown by clock domain.

When you select **By Clock Domain** from the drop-down list, the **Analysis** tab shows a breakdown of the power usage by the clock domain that the power is drawn from. For each clock domain, the power and percentage of power drawn are displayed. Dynamic power is accounted for in breakdown by clock, but static power is not associated by any clock.

When you select **By Type**, **By Instance** or **By Clock Domain**, you can customize which columns are displayed in the grid by right-clicking the column headers. To exclude a column, remove its check mark from the right-click menu. Right-click a column header to set the column default size for the selected column or for all columns, and then sort the values in ascending order, descending order, or customize the columns.

To sort the contents of a column, double-click a column header.

To export the contents of the grid to a file, choose **Export Grid** from the **File** menu, or click its associated toolbar button.

To print the grid, choose **Print Grid** from the **File** menu, or click its associated toolbar button. To copy the grid, choose **Copy Grid** from the **Edit** menu or click its toolbar button.

To copy the chart, right-click the contents of the chart and choose Copy Chart to Clipboard.

To export the chart, right-click the contents of the chart and choose **Export Chart to File**.

To rotate the chart by 90 degrees, click the contents of the chart and choose **Rotate Chart Clockwise** or right-click **Rotate Chart Counter-Clockwise**.

To view an instance's properties, right-click any instance and choose **Instance Properties**. The Instance Properties window appears, with the instance name, type and power and other properties specific to each type of instance (see the following figure).

### Figure 2-5. Instance Properties: Gate

Inst	ance Properti	es			×
	Property Name Power Type Macro		Value U141 OmW Gate ADLIB:INV		
	Pin List:	Ninh	Damain	Exec (Mile)	
	Pin U141:A U141:Y	Net BusOutput DRAMData	Domain CPUClk (data) CPUClk (data)	Freq. (MHz) 0.000 0.000	
	Help			Close	

The Instance Properties window allows you to access a list of pins of a gate, and check their domain and frequency.

For more information, see:

- 4.16 Analyzing Results
- 4.3 Advanced Analysis of I/Os

### 2.3.2.2.1 Show

Displays power usage as a chart or grid.

Note: The power usage chart is not available when breakdown by instance is selected.

### 2.4 Frequencies Tab

Use the **Frequencies** tab to attach switching frequency attributes to the interconnects of the design.

The Frequencies tab is organized into the following areas:

- Switching Frequencies
- Average Frequencies
- Annotation Statistics

### Figure 2-6. Frequencies Tab

Image: constraint of the second se		Driver	Domain: All	Source: All     Domain	Frequency	Source	
2       PWM_out_pad/U0/U0:PAD       PWM_out       un1_dataa_int       0       Fixed Values         3       nPWM_out_pad/U0/U1:DOU       nPWM_out_pad/U0/NET1       un1_dataa_int       0       Fixed Values         4       nPWM_out_pad/U0/U0:PAD       nPWM_out       un1_dataa_int       0       Fixed Values         5       un1_dataa_int_NE:Y       un1_dataa_int_NE       un1_dataa_int       0       Fixed Values         6       PWM_out:Q       PWM_out_c       un1_dataa_int       0       Fixed Values         7       nPWM_out:Q       nPWM_out_c       un1_dataa_int       0       Fixed Values         8       Aclr_pad/U0/U0:Y       Aclr_pad/U0/NET1       PWM_clk (set/       0       Fixed Values         9       PWM_clk       PWM_clk       PWM_clk (set/       0       Fixed Values         10       PWM_clk_pad/U0/U0:Y       PWM_clk_pad/U0/NET1       PWM_clk (cloc       0       Fixed Values         12       PWM_data_in<5>       PWM_data_in[5]       PWM_clk (prim       Fixed Values         12       PWM_data_in<3>       PWM_data_in[3]       PWM_clk (prim       Fixed Values	_						-1.
3       nPWM_out_pad/U0/U1:DOU       nPWM_out_pad/U0/NET1       un1_dataa_int       0       Fixed Values         4       nPWM_out_pad/U0/U0:PAD       nPWM_out       un1_dataa_int       0       Fixed Values         5       un1_dataa_int_NE:Y       un1_dataa_int_NE       un1_dataa_int       0       Fixed Values         6       PWM_out:Q       PWM_out_c       un1_dataa_int       0       Fixed Values         7       nPWM_out:Q       nPWM_out_c       un1_dataa_int       0       Fixed Values         8       Aclr_pad/U0/U0:Y       Aclr_pad/U0/NET1       PWM_clk (set/       0       Fixed Values         9       PWM_clk       PWM_clk       PWM_clk (cloc       0       Fixed Values         10       PWM_clk_pad/U0/U0:Y       PWM_clk_pad/U0/NET1       PWM_clk (cloc       0       Fixed Values         11       PWM_clk_pad/U0/U0:Y       PWM_clk_pad/U0/NET1       PWM_clk (cloc       0       Fixed Values         11       PWM_clk_pad/U0/U0:Y       PWM_clk_pad/U0/NET1       PWM_clk (cloc       0       Fixed Values         12       PWM_data_in<5>       PWM_data_in[5]       PWM_clk (prim       0       Fixed Values         12       PWM_data_in<3>       PWM_data_in[3]       PWM_clk (prim       Fixed Valu							_
4       nPWM_out_pad/U0/U0:PAD       nPWM_out       un1_dataa_int       0       Fixed Values         5       un1_dataa_int_NE:Y       un1_dataa_int_NE       un1_dataa_int       0       Fixed Values         5       PWM_out:Q       PWM_out_c       un1_dataa_int       0       Fixed Values         7       nPWM_out:Q       nPWM_out_c       un1_dataa_int       0       Fixed Values         8       Aclr_pad/U0/U0:Y       Aclr_pad/U0/NET1       PWM_clk (set/       0       Fixed Values         9       PWM_clk       PWM_clk       PWM_clk (set/       0       Fixed Values         10       PWM_clk_pad/U0/U0:Y       PWM_clk_pad/U0/NET1       PWM_clk (cloc       0       Fixed Values         10       PWM_clk_pad/U0/U0:Y       PWM_clk_pad/U0/NET1       PWM_clk (cloc       0       Fixed Values         11       PWM_data_in<5>       PWM_data_in[5]       PWM_clk (prim       0       Fixed Values         12       PWM_data_in<3>       PWM_data_in[3]       PWM_clk (prim       Fixed Values							-
i       un1_dataa_int_NE:Y       un1_dataa_int_NE       un1_dataa_int       0       Fixed Values         i       PWM_out:Q       PWM_out_c       un1_dataa_int       0       Fixed Values         i       PWM_out:Q       PWM_out_c       un1_dataa_int       0       Fixed Values         i       PWM_out:Q       nPWM_out_c       un1_dataa_int       0       Fixed Values         i       PWM_out:Q       nPWM_out_c       un1_dataa_int       0       Fixed Values         i       PWM_out:Q       nPWM_out_c       un1_data_int       0       Fixed Values         i       PWM_clk       PWM_clk       PWM_clk (cloc       0       Fixed Values         i       PWM_clk_pad/U0/U0:Y       PWM_clk_pad/U0/NET1       PWM_clk (cloc       0       Fixed Values         i       PWM_data_in<5>       PWM_data_in[5]       PWM_clk (prim 0       Fixed Values         i       PWM_data_in<3>       PWM_data_in[3]       PWM_clk (prim 0       Fixed Values							-11
B       PWM_out:Q       PWM_out_C       un1_dataa_int       0       Fixed Values         C       NPWM_out:Q       NPWM_out_C       un1_dataa_int       0       Fixed Values         B       Aclr_pad/U0/U0:Y       Aclr_pad/U0/NET1       PWM_clk (set/       0       Fixed Values         B       PWM_clk       PWM_clk       PWM_clk (cloc       0       Fixed Values         B       PWM_clk_pad/U0/U0:Y       PWM_clk_pad/U0/NET1       PWM_clk (cloc       0       Fixed Values         D       PWM_clk_pad/U0/U0:Y       PWM_clk_pad/U0/NET1       PWM_clk (cloc       0       Fixed Values         1       PWM_data_in<			-				_
nPWM_out:Q       nPWM_out_c       un1_data_int       0       Fixed Values         Aclr_pad/U0/U0:Y       Aclr_pad/U0/NET1       PWM_clk (set/       0       Fixed Values         PWM_clk       PWM_clk       PWM_clk (cloc 0       Fixed Values         0       PWM_clk       PWM_clk (cloc 0       Fixed Values         0       PWM_clk_pad/U0/NET1       PWM_clk (cloc 0       Fixed Values         1       PWM_data_in<5>       PWM_data_in[5]       PWM_clk (prim 0       Fixed Values         2       PWM_data_in<3>       PWM_data_in[3]       PWM_clk (prim 0       Fixed Values							_
Aclr_pad/U0/U0:Y       Aclr_pad/U0/NET1       PWM_clk (set/ 0       Fixed Values         PWM_clk       PWM_clk       PWM_clk (cloc 0       Fixed Values         0       PWM_clk_pad/U0/NET1       PWM_clk (cloc 0       Fixed Values         0       PWM_clk_pad/U0/NET1       PWM_clk (cloc 0       Fixed Values         1       PWM_data_in<5>       PWM_data_in[5]       PWM_clk (prim 0       Fixed Values         2       PWM_data_in<3>       PWM_data_in[3]       PWM_clk (prim 0       Fixed Values							_
PWM_clk         PWM_clk         PWM_clk (cloc 0         Fixed Values           0         PWM_clk_pad/U0/U0:Y         PWM_clk_pad/U0/NET1         PWM_clk (cloc 0         Fixed Values           1         PWM_data_in<5>         PWM_data_in[5]         PWM_clk (prim 0         Fixed Values           2         PWM_data_in<3>         PWM_data_in[3]         PWM_clk (prim 0         Fixed Values							-11
.0 PWM_clk_pad/U0/U0:Y PWM_clk_pad/U0/NET1 PWM_clk (cloc 0 Fixed Values .1 PWM_data_in<5> PWM_data_in[5] PWM_clk (prim 0 Fixed Values .2 PWM_data_in<3> PWM_data_in[3] PWM_clk (prim 0 Fixed Values							-
.1 PWM_data_in<5> PWM_data_in[5] PWM_clk (prim 0 Fixed Values .2 PWM_data_in<3> PWM_data_in[3] PWM_clk (prim 0 Fixed Values		-		- '			_
.2 PWM_data_in<3> PWM_data_in[3] PWM_clk (prim 0 Fixed Values				- `			_
							_
Set Frequencies for selected pins Reset Frequencies for selected pins	.2	PWM_data_in<3>	PWM_data_in[3]	PWM_clk (prim	0	Fixed Values	1
		Set Frequencies for selected pins	Reset Frequencies for select	ed pins		Selec	tall
verage Frequencies:	vera	age Frequencies:	A	nnotation Statistics:			

#### 2.4.1 Switching Frequencies

Displays the pins and lists the net, domain, frequency, and frequency source for each pin.

The **Driver** box allows you to filter the list of pins based on the criteria entered. Enter text in the filter box and click **Set** to apply this text as a filter. Use the \* character to display all pins or as a wildcard.

Use the Domain drop-down list to select a different domain (All, CLKIN, Default, or Input to Output).

Use the Source drop-down list to select a different source (All, Default, Manual Annotation, or VCD Import).

To change the frequency, enter a new value in the **Frequency** column, or select multiple pins, click the **Set frequencies for selected pins** button, and enter a new frequency. Use **Reset frequencies for selected pins** to revert to the default frequency.

To select all the pins, click Select All.

### 2.4.2 Average Frequencies

Displays the average frequency of all pins displayed in the grid.

Average frequencies are useful when you import a VCD file. Because these files allow you to specify the frequency of each pin individually, it is useful to know the average clock pin or data pin frequency for a particular clock domain.

If you did not specify a frequency annotation for any clock pin in this clock domain, the average value is equal to the default clock frequency of the clock domain. If you set one or several clock pins, SmartPower takes those annotations to compute an average value.

If you did not specify a frequency annotation for any data pin in this clock domain, the average value is equal to the default data frequency of the clock domain. If you set one or several data pins, SmartPower considers these annotations into account to compute an average value.

#### 2.4.3 Annotation Statistics

VCD import: displays the percentage of pins with frequencies imported from the \*.vcd file.

Manual annotation: displays the percentage of pins with manually-annotated frequencies.

Fixed values: displays the percentage of pins with default frequency.

### 2.5 Probabilities Tab

The **Probabilities** tab displays the drivers, nets, types, polarity, rates, and source for each pin. Use the **Probabilities** tab to control the probabilities for all pins.

- **Bidirectional and Tristate I/Os**: controls the output probability of each tristate and bidirectional I/O. The probability is the percentage of time that the I/O is used as an output. You can change the default value and set a specific value for each bidirectional or tristate I/O.
- **Memories**: controls the read cycle probability or the write cycle probability of a memory block. The probability is the percentage of time that a memory block will be used in a read cycle or a write cycle. You can change the default value and set a specific value for each enable pin of each memory block available in the design. If an enable pin is active low, assign it a probability of 0% to completely enable the I/O or the memory block, or 100% to disable it completely.

Driver:	Set	Type: All	Polarity: All	<b>_</b>	Source: All	<b>_</b>
	Driver	Net	Туре	Polarity	Probability (%)	Source
	rst_n	rst_n	Input to		99.9949	Manual A
2	rst_n_pad/U0/U0:Y	rst_n_pad/U0/NET1	Input to		99.9949	Manual A
3	rst_n_pad/U0/U1:Y	rst_n_c	Input to		99.9949	Manual A
t I	fpu_op<0>	fpu_op[0]	Input to		0	Manual A
5	fpu_op_pad[0]/U0/U0:Y	fpu_op_pad[0]/U0/NET1	Input to		0	Manual A
i i	fpu_op_pad[0]/U0/U1:Y	fpu_op_c[0]	Input to		0.000003	Manual A
7	UUT/un1_fpu_op_3_0_a2	UUT/N_1112	Input to		0.000003	Manual A
3	UUT/fracta_mul_w_0_a2	UUT/N_1111	Input to		0.000003	Manual A
)	fpu_op<1>	fpu_op[1]	Input to		0	Manual A
LO	fpu_op_pad[1]/U0/U0:Y	fpu_op_pad[1]/U0/NET1	Input to		0	Manual A
L1		fpu_op_c[1]	Input to		0.000003	Manual A
L2	UUT/un1_fpu_op_1_0_a2	UUT/N_1026	Input to		0.000003	Manual A
13	fpu_op<2>	fpu_op[2]	Input to		0	Manual A
L4	fpu_op_pad[2]/U0/U0:Y	fpu_op_pad[2]/U0/NET1	Input to		0	Manual A
.5	fpu_op_pad[2]/U0/U1:Y	fpu_op_c[2]	Input to		0.000003	Manual A
.6	UUT/fract_denorm[30]:Q		UUT/un3_out_		0.0125	Manual A
.7	UUT/fract_denorm[32]:Q	UUT/fract_denorm[32]	UUT/un3_out_		0.0125	Manual A
8	UUT/fract_denorm[31]+0	HUT/fract_denorm[31]	HUT/up3 out		0.0125	Manual A 🔛

#### Figure 2-7. SmartPower Probabilities Tab

In designs with a cascaded memory, all memory enable pins are shown in the **Probabilities** tab. To simulate realworld power consumption, selectively enable only some memory enable pins, as specified in the memory cascading structure.

- For purely vertical cascading, enable the pins that belong to one RAM block.
- · For purely horizontal cascading, enable all pins belonging to all RAM blocks of the cascaded memory.

To find which RAM block corresponds to which pin, cross-probe with the MVN NetlistViewer.

The **Driver** box allows you to filter the list of drivers based on the criteria entered. Enter text in the filter box, and click **Set** to apply this text as a filter. Use the \* character as a wildcard.

Use the Type drop-down list to filter the pin list by different type (All, All enable, CLKIN, Default, or Input to Output).

Use the **Polarity** drop-down list to filter the pin list by polarity (Low, High, or All).

Use the **Source** drop-down list to filter the pin list by source (All, Default Estimation, Manual Annotation, SDC, VCD Import).

To change the rate, enter a new value in the **Rate** column, or select multiple pins, click the **Set Probabilities for selected pins** button, and enter a new frequency in the Set Default Probabilities dialog box.

#### Figure 2-8. Set Probability for Pins Dialog Box

Set probability for	pin(s)	×
Probability:		
50.00		
ОК	Cancel	1
	Cancer	J

Use **Reset Probabilities for selected pins** to revert to the default polarity. You can change the default probability from the **Domains** tab.

To select all the drivers, click Select All.

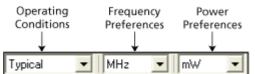
You can set or reset the probabilities, set a default probability, copy, export, or print the grid by selecting one or multiple pins and choosing an option from the right-click menu.

For more information, see 4.13 Specifying Individual Pin Probabilities.

### 2.6 Preferences Toolbar

The SmartPower Preferences toolbar appears on the right side of the row below the menus. It provides quick access to commonly used settings. Mouse over the toolbar button to view a description of the command. Use the drop-down list to select your settings.

#### Figure 2-9. SmartPower Preferences Toolbar



Operating Conditions: allows you to set the operating conditions: Best, Typical, or Worst. The actual voltage
and temperature of a given operating condition is defined by the operating condition range selected for the
current design (COM, IND, MIL, Auto, TGrade1, TGrade2, and Custom). For SmartPower, unlike SmartTime, the
worst voltage is the upper bound of the range. That is, higher (worst-case) power comes from higher voltage,
while higher voltage results in best-case speed.

Note: Worst-case and best-case calculations are available only for certain families and devices.

- Frequency Preferences: sets unit preferences for frequency: Hz, KHz, MHz.
- · Power Preferences: sets unit preferences for power: W, mW, or uW.

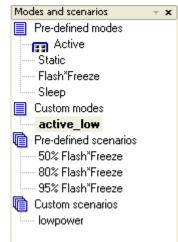
### 2.7 Modes and Scenarios Toolbar

The Modes and Scenarios toolbar appears as the left pane in the SmartPower interface. It displays all predefined modes, custom modes, predefined scenarios, and custom scenarios.



The Modes and Scenarios toolbar is shown by default, but can be closed or undocked. To view the toolbar, choose **Modes and Scenarios toolbar** from the **View** menu.

### Figure 2-10. Modes and Scenarios Toolbar



From this toolbar, you can:

- Select a predefined mode by clicking the mode name.
- Select a custom mode by clicking the mode name.
- Select a custom mode for power-driven layout by right-clicking the active-based mode and selecting **Use for PDPR**.
- Re-import a VCD file from an Active mode or a custom mode by right-clicking the VCD file and selecting **Re-import VCD File**.
- Remove a VCD file from an Active mode or a custom mode by right-clicking the VCD file and selecting Remove VCD File from <mode name> Mode or by choosing Remove VCD File <file name> from the Simulation menu.
- Generate an Activity and Hazards Power report by right-clicking the VCD file and selecting Activity and Hazards Power Report
- Create a new custom mode by clicking **Custom modes** and selecting **New Custom Mode**, or by clicking the **New Custom Mode** hyperlink.
- Edit and delete a custom mode by right-clicking the mode name and selecting Edit custom mode or Delete custom mode.
- Copy a custom or predefined mode by right-clicking the mode name and selecting **Create a copy of this mode**.
- Select a scenario by clicking the scenario name.
- Create a new custom scenario by clicking **Scenarios** and selecting **New custom scenario**.
- Edit and delete a custom scenario by right-clicking the scenario name and selecting Edit custom scenario.
- Copy a scenario by right-clicking the scenario name and selecting Create a copy of this scenario.
   Note: When a scenario is selected, only the Summary tab is available.

### 2.8 SmartPower Standard Toolbar and Menu Commands

The SmartPower standard toolbar contains commands for performing common SmartPower operations on your designs. Roll the mouse pointer over the toolbar button to view a description of the button. Click the button to access the command.



### **Toolbar Button** Description Commit 6 **Settings Summary** 0 **Operating Conditions** a Options **Export Path Grid Copy Path Grid** ₿**≥ Print Grid** 8 **Generate Power Report** 2 Initialize Frequencies and Probabilities 0 Refresh vectorless estimation С Freeze/Unfreeze Calculations

### Table 2-3. SmartPower Toolbar

The PC and UNIX workstation versions of SmartPower have the same menus. However, some dialog boxes, field locations and names, and buttons may look slightly different on the two platforms due to the different window environments.

### 2.9 File Menu

Menu	Description
Commit	Commits power information. You must commit your changes if you wish to save your settings in SmartPower. If you commit your changes, the information is stored in the .adb file, and your settings are restored the next time you open your design in SmartPower.
Export Grid	Exports the selected area of the Report window to a text (.txt) file.
Print Grid	Prints the selected area of the Report window.
Settings Summary	Displays a summary of the power settings for the current design.

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## **SmartPower Interface**

	continued		
I	Menu	Description	
	Close	Closes SmartPower.	

# 2.10 Edit Menu

Menu	Sub-Menu	Description
Domains	New Clock Domain	Adds a clock domain.
	New Set of Pins	Adds a set of pins.
	Delete Domain	Deletes a clock domain.
	Edit Domain	Edits a clock domain.
Modes and Scenarios	Use for Analysis > mode or scenario name	Sets the selected mode or scenario to be used for analysis.
	Use for PDPR > mode or scenario name	Sets the selected mode or scenario to be used for a power-driven layout.
	Custom Modes > New Custom Mode	Creates a new custom mode.
	Custom Modes > Edit Custom Mode	Edits a custom mode.
	Custom Modes > Delete Custom Mode	Deletes a custom mode.
	Custom Scenarios > New Scenario	Creates a new custom scenario.
	Custom Scenarios > Edit Scenario	Edits a custom scenario.
	Custom Scenarios > Delete Scenario	Deletes a custom scenario.
Copy Grid	—	Copies the selected cells of the dynamic grid onto the Clipboard.

# 2.11 View Menu

Menu	Description
Standard Toolbar	Displays or hides the Standard toolbar.
Preferences Toolbar	Displays or hides the Preferences toolbar.
Modes and Scenarios Toolbar	Displays or hides the Modes and Scenarios toolbar.
Unprocessed Simulation Files Toolbar	Displays or hides the Unprocessed Simulation Files toolbar.
Customize Columns	Selects and orders the columns displayed in the user interface.
Reset Window Layout	Resets the window layout to the default layout.

### 2.12 Tools Menu

Menu	Sub-Menu	Description
Initialize Frequencies and Probabilities		Imports clock constraints from SmartTime, and allows you to enter frequencies and probabilities for the design, as shown in the Initializing Frequencies and Probabilities section.
Operating Conditions	—	Allows you to customize the operating conditions used in SmartPower.
Options	_	Displays the Options dialog box, where you can set analysis and display preferences.
Reports	Power Report	Generates a power report.
	Scenario Power Report	Generates a scenario power report.
	Activity and Hazards Power Report	Generates an activity and hazards power report.
Export Report for MPE	—	Exports a report for Microchip Power Estimator (MPE).
Freeze/Unfreeze Calculations	—	Freezes or unfreezes the computations that happen to avoid the SmartPower tool from slowing down

### 2.13 Simulation Menu

Menu	Description
Import VCD File	Displays the Import VCD Options dialog box.
Remove VCD file	Removes the selected VCD file from the design.
Audit files	Audits simulation files within the project.

### 2.14 Help Menu

Menu	Description
Help on <i>current tab</i>	Displays the help content for the current tab.
Help Topics	Opens the help files for SmartPower.
SmartPower User's Guide	Displays the SmartPower User's Guide.
Data Change History	Displays the data change history report.

For more information, see the SmartPower Preferences Toolbar.

### 2.15 Power-Settings Summary

The Power-Settings Summary dialog box summarizes the power settings for the current design. To open the dialog

box, choose Settings Summary from the File menu or click the oicon in the SmartPower toolbar.

Figure 2-11. Power-Settings Summary Dialog Box

Power - Settings Summary >			
Attribute	Value		
Data Source	Production		
Design	sd		
Die	RT4G150_ES		
Family	RTG4		
Operating Conditions	Typical		
Operating Mode	Active		
Package	1657 CG		
Temperature Range	MIL		
Voltage Range	MIL		
ОК			

The Power-Settings Summary dialog box shows the following information.

### Table 2-4. Power-Settings Summary Dialog Box Attributes

Attribute	Description
Data Source	Displays the data source.
Design	Displays the name of the design.
Family	Displays the device family used in the design.
Die	Displays the die.
Package	Displays the package.
Temperature Range	Displays the temperature range.
Voltage Range	Displays the core supply voltage.
Operating Condition	Displays the operating conditions that SmartPower uses to calculate static and dynamic power contributions.
Operating Mode	Displays the operating mode that SmartPower uses to calculate static and dynamic power contributions.

**Note:** The status bar also shows the ambient temperature, VCCA, and speed grade.

### 2.16 Initializing Frequencies and Probabilities

The Initialize Frequencies and Probabilities dialog box allows you to initialize the frequencies and probabilities for your design.

### **SmartPower Interface**

To open the Initialize Frequencies and Probabilities dialog box, choose Initialize Frequencies and Probabilities

from the **Tools** menu, or click the <sup>1</sup>/<sub>100</sub> icon in the SmartPower toolbar.

Note: This feature is available only in the Active operating mode or in modes derived from the Active mode.

The dialog box is organized into the following panels:

- General
- Clocks
- Register Outputs
- Set/Reset Nets
- Primary
- Inputs
- Combinational Outputs
- · Enables Sets of Pins
- · Other Sets of Pins

### 2.16.1 General

### Figure 2-12. Initialize Frequencies and Probabilities Dialog Box – General

SmartPower - Initialize Frequencies and Probabilities		
Select a Category:	General	
<ul> <li>General</li> <li>Clocks</li> <li>Set/Reset nets</li> <li>Primary inputs</li> <li>Combinational outputs</li> <li>Set of pins</li> <li>Enables</li> <li>Others</li> </ul>	Use this dialog box to initialize frequencies and probabilities for your design. Initialize mode: Active	
Help	OK Cancel	

**Initialize mode**: select an active-based mode for which you want to initialize the frequencies and probabilities. For pins that have not been annotated, SmartPower can estimate their frequency and probability using vectorless analysis or fixed values:

- · Use vectorless analysis: SmartPower initializes frequencies and probabilities with vectorless analysis.
- **Use fixed values**: SmartPower initializes frequencies and probabilities (%) of all registers with a default toggle rate (when using toggle rates), frequency, and probability.

Based on the selected mode, a warning appears with information about the annotated pins. If the selected mode contains annotations, you can remove them by selecting one or both of the following options:

- · Remove Simulation file (VCD) if any: removes the simulation file for the selected mode.
- **Remove any manual annotations**: removes all manual pin annotations for the selected mode.

### 2.16.2 Clocks

SmartPower - Initialize Frequen	ies and Probabilities	×
Select a Category:	Clocks	
<ul> <li>General</li> <li>Clocks</li> <li>Register outputs</li> <li>Set/Reset nets</li> <li>Primary inputs</li> <li>Combinational outputs</li> <li>Set of pins</li> <li>Enables</li> <li>Others</li> </ul>	<ul> <li>Initialize clock frequencies and duty cycles</li> <li>with clock constraint if available in SmartTime</li> <li>else, with default frequency</li> <li>10.00</li> <li>MHz</li> <li>and duty cycle</li> <li>50,00</li> <li>%</li> </ul>	
Help	OK Cancel	

- Initialize clock frequencies and duty cycles: initializes clock frequencies and duty cycles with one of the following:
  - with clock constraint if available in SmartTime: when only this box is checked, SmartPower initializes all clock domains in SmartPower with clock constraints from SmartTime. If there is no frequency constraint set for this clock domain in SmartTime, the clock frequency of the domain will not be updated.
  - else, with default frequency (MHz) and duty cycle (%): when only this box is checked, SmartPower initializes all clock domains in SmartPower with the specified default frequency and duty cycle.

**Note:** When both boxes are checked, and **with clock constraint if available in SmartTime**, **else default frequency**, and **and duty cycle** selected, SmartPower initializes all clock domains with clock constraints from SmartTime. If there is no frequency constraint set for a clock domain in SmartTime, it is initialized with the specified default frequency and duty cycle.

### 2.16.3 Register Outputs

Figure 2-14. Frequencies and Probabilities Dialog Box –Registers

SmartPower - Initialize Frequenci	ies and Probabilities 🛛 🔀
Select a Category: Codes Clocks Set/Reset nets Set/Reset nets Combinational outputs Set of pins Enables Others	Register outputs         Initialize frequencies and probabilities         • with Vectorless analysis         • with fixed values         toggle rate       10.00         probability       50.00
Help	OK Cancel

Initialize frequencies and probabilities: initializes frequencies and probabilities for register outputs in your design.

with Vectorless analysis: SmartPower initializes frequencies and probabilities using vectorless analysis.

with fixed values: SmartPower initializes frequencies and probabilities (%) of all register outputs with a default toggle rate (available only when using toggle rates) or frequency (when not using toggle rates), and a default probability.

### 2.16.4 Set/Reset Nets

Figure 2-15. Frequencies and Probabilities Dialog Box – Set/Reset nets

SmartPower - Initialize Frequenci	es and Probabilities	
Select a Category: General Clocks Set/Register outputs Set/Reset nets Primary inputs Combinational outputs Set of pins Enables Others	✓ Initialize frequencies and probabilities         with fixed toggle rate       0.00       %         with fixed probability       \$0.00       %	
Help	OK Cancel	

Initialize frequencies and probabilities: initializes frequencies and probabilities for set/reset nets in your design.

with fixed frequency (MHz): SmartPower initializes all primary inputs in SmartPower with the specified fixed frequency. This option is available only when not using toggle rates.

with fixed toggle rate (%): SmartPower initializes frequencies and probabilities of all set/reset nets with the specified fixed toggle rate. This option is available only when using toggle rates.

with fixed probability (%): SmartPower initializes probabilities of all set/reset nets with the specified fixed probability.

### 2.16.5 Primary Inputs

Figure 2-16. Frequencies and Probabilities Dialog Box – Primary Inputs

SmartPower - Initialize Frequenci	es and Probabilities	
Select a Category:	Primary inputs	
<ul> <li>General</li> <li>Clocks</li> <li>Set/Register outputs</li> <li>Set/Reset nets</li> <li>Primary inputs</li> <li>Combinational outputs</li> <li>Set of pins</li> <li>Enables</li> <li>Others</li> </ul>	✓ Initialize frequencies and probabilities with fixed toggle rate 10.00 % with fixed probability \$50.00 %	
Help	OK Cancel	

**Initialize frequencies and probabilities**: initializes frequencies and probabilities for the primary inputs in your design.

with fixed toggle rate (%): SmartPower initializes frequencies and probabilities of all primary inputs with the specified fixed toggle rate. This option is available only when using toggle rates.

**with fixed frequency (MHz)**: SmartPower initializes all primary inputs in SmartPower with the specified default frequency. This option is available only when not using toggle rates.

with fixed probability (%): SmartPower initializes probabilities of all primary inputs with the specified fixed probability.

### 2.16.6 Combinational Outputs

Figure 2-17. Frequencies and Probabilities Dialog Box – Combinational Outputs

SmartPower - Initialize Frequenci	ies and Probabilities	
Select a Category: General Clocks Set/Reset nets Primary inputs Combinational outputs Set of pins Enables Others	✓ Initialize frequencies and probabilities         ● with Vectorless analysis         ● with fixed values         toggle rate       10.00       %         probability       50.00       %	
Help	OK Cancel	

**Initialize frequencies and probabilities**: initializes frequencies and probabilities for the combinational outputs in your design.

with Vectorless analysis: SmartPower initializes frequencies and probabilities with vectorless analysis.

with fixed values: SmartPower initializes frequencies and probabilities (%) of all combinational outputs with a default toggle rate (available only when using toggle rates) or frequency (when not using toggle rates), and a default probability.

#### 2.16.6.1 Enables

#### Figure 2-18. Frequencies and Probabilities Dialog Box – Enables

SmartPower - Initialize Frequenci	es and Probabilities	X
Select a Category:	Enables	
💮 General		
N Clocks		
	Initialize frequencies and probabilities	
	County the standard and have	
Primary inputs	<ul> <li>with Vectorless analysis</li> </ul>	
	C with fixed values	
Set of pins	Frequency Pro	obability
Enables	Domain MHz	%
Others		12.50
	2 MemoriesEnableSet 0.00	12.50
Help	OK Cancel	

**Initialize frequencies and probabilities**: initializes frequencies and probabilities for the enable sets of pins in your design.

with Vectorless analysis: SmartPower initializes frequencies and probabilities with vectorless analysis.

with fixed values: SmartPower initializes frequencies and probabilities of all enables sets of pins with the specified default probability and frequency.

### 2.16.6.2 Others

#### Figure 2-19. Frequencies and Probabilities Dialog Box – Others

SmartPower - Initialize Frequenci	es and Probabilities	$\mathbf{X}$
Select a Category:	Others	
General     Clocks     Set/Reset nets     Set/Reset nets     Primary inputs     Combinational outputs     Set of pins     Enables     Others	<ul> <li>✓ Initialize frequencies and probabilities</li> <li> <ul> <li>with Vectorless analysis</li> <li>primary inputs frequency</li> <li>1.00</li> <li>MHz</li> <li>primary inputs probability</li> <li>50.00</li> <li>%</li> </ul> </li> <li> <ul> <li>with fixed values</li> <li>frequency</li> <li>1.00</li> <li>MHz</li> <li>probability</li> <li>50.00</li> <li>%</li> </ul> </li> </ul>	
Help	OK Cancel	

**Initialize frequencies and probabilities**: initializes frequencies and probabilities for the other sets of pins in your design with default values.

with Vectorless analysis: SmartPower initializes frequencies and probabilities with vectorless analysis as specified in the primary inputs frequency and probability.

with fixed values: SmartPower initializes frequencies and probabilities (%) of all other sets of pins with a default frequency and probability.

### 2.17 Operating Conditions

The SmartPower Operating Conditions dialog box allows you to customize the operating conditions used in SmartPower for voltage and temperature.

Note: Changes will apply only to SmartPower and will not change the operating conditions set in Designer.

The **General** panel allows you to select the operating condition you want to apply to SmartPower: Best, Typical, or Worst.

SmartPower - Operating Conditions	<u> </u>
Select a Category:	General
General Process settings Temperature settings Voltage settings VODAUX VDD VDDAUX VDD 1.8 VDD25 VDD18	Use this dialog box to customize the operating conditions used in SmartPower. Changes will apply only to SmartPower and will not change the operating conditions set in the Designer. Select an active operating condition for SmartPower from the options below:
Help	OK Cancel

Figure 2-20. SmartPower Operating Conditions Dialog Box - General

The process settings panel allows you to select the process characteristic.

Figure 2-21. SmartPower Operating Conditions Dialog Box - Process Settings

SmartPower - Operating Conditions			8 23
Select a Category:	Process settings		
General Process settings Temperature settings Thermal resistance settings Voltage settings VDD VDDAUX VDD11.8 VDD25 VDD18	Select the process characteristic: "Typical" is based on average standby power consumption "Maximum" can be used for worst-case analysis Typical	•	
Help		ОК	Cancel

You can customize temperature settings in the Temperature Settings panel, and the voltage settings in the Voltage Settings panels — each VCC voltage used in the design appears under Voltage settings.

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SmartPower - Operating Conditions		8 23
Select a Category:	Temperature settings	
General Process settings Temperature settings Voltage settings Voltage settings VDD VDDAUX VDDAUX VDD1.8 VDD25 VDD18	Use: Design operating range (default)	
10010	- Junction Temperaure( in degrees Celsius )	
	Best: 0.00	_
	Settings tance settings SmartPower uses the operating range specified in the Device Selection Wizard: This design uses "EXT" settings. Junction Temperaure( in degrees Celsius )	
	Worst: 100.00	
Help	ОК	Cancel

Figure 2-22. SmartPower Operating Conditions Dialog Box - Temperature Settings

Select one of three options to specify the temperature or voltage settings:

- **Design operating range (default)**: sets the temperature or voltage operating range as specified in your Project Settings.
- **Custom operating range**: sets the temperature (junction or ambient) or voltage operating range for the current design in SmartPower only. Enter temperature values in degrees Celsius and voltage values in volts for Best, Typical, and Worst.
- Mode by mode operating range: sets the temperature (junction or ambient) or voltage for each mode in SmartPower only. Use the grid to enter temperature values in degrees Celsius and voltage values in volts for each mode, or select multiple modes in the grid, and click the Set values for selected modes button to enter the same values for all selected modes.

elect a Category:	Temperature sett	ings			
General Process settings Temperature settings Voltage settings VDD VDDAUX VDDI 1.8 VDD25 VDD18	Use: Mode by mode oper SmartPower uses a diffe Operating ranges for ear only. Specify (in Celcius degree Junction Temperature Junction Temperature	erent operating ran ch mode can be sp <u>res):</u> re		apply to SmartPower	
	Mode	Best	Typical	Worst	
	1 Static	0.00	25.00	100.00	
	2 Active	0.00	25.00	100.00	
	Set values for select	ed and (c)		Select All	1

Figure 2-23. SmartPower Operating Conditions Dialog Box - Mode-Specific Temperature Settings

The junction temperature and static power are computed iteratively until they converge. The formulas are:

# $\mathbf{T}_{J} = \mathbf{T}_{A} + \boldsymbol{\theta}_{JA} \cdot (\mathbf{P}_{dynamic} + \mathbf{P}_{static}) \mathbf{P}_{static} = f(\mathbf{T}_{J}) = \mathbf{P}_{0} + \mathbf{P}_{1} \cdot \mathbf{T}_{J}$

If the computed junction temperature is outside the operating condition range (smaller than the best case value or greater than the worst case value), a violation warning will be reported.

Both TJ and Pstatic will be re-computed when any of the following parameters are changed:

- Ambient temperature
- · Cooling style
- Custom thermal resistance or any parameters/options that affect the static or dynamic power values:
- Junction Temperature Display Mode
- Operating Condition (Affect dynamic power)
- Operating Mode (Affect dynamic power)
- Any of the clock domain frequencies (Affect dynamic power)

If you specified the Ambient temperature in the Temperature Settings panel, you can select the thermal characteristic for ThetaJA.

General	Thermal resistance sett			
Process settings	Select the thermal charac	cteristic for ThetaJA		
Temperature settings	C Custom	Estimated		
Voltage settings				
VDD VDDAUX	Theta 1A	0	C/W	
VDDA0A	metaja	Jo		
VDD25	Heat Sink	20mm - High Profile	•	
UND18	Air Flow	2.5 m/s	•	
		12.5 11/3	_	
	Custom ThetaSA	0	C/W	
	Board Thermal Model	JEDEC (2s2p)	<u> </u>	
	🔥 This setting only applies if yo		ture	
	in the 'Temperature settings	page.		

Figure 2-24. SmartPower Operating Conditions Dialog Box - Thermal Resistance Settings

The thermal resistance is predefined for Still Air, 300 ft/min and Case Cooling. To enter a custom thermal resistance, select **Custom** from the thermal characteristic for ThetaJA

SmartPower also reports the thermal resistance ThetaJA.

### 2.17.1 Custom Operating Modes

SmartPower allows you to use predefined and custom operating modes. A predefined operating mode is an inherent mode of a family of devices that comes with a number of hard availability constraints on the FPGA resources. Custom operating modes are user-defined modes based on one of the predefined modes available for the family, where parameters such as clock, data, and toggle rate frequencies have been customized. A custom mode can also be linked to a VCD.

Custom modes can be used:

- To define additional modes where the chip is in the active predefined mode, but where the clock frequencies or the toggle rates are scaled up or down.
- To import multiple VCD files that capture individual steps that take place in different modes.
- To define a sequence of modes with a duration for each mode and get an estimate of the overall power consumption, from which extrapolate the battery life for the application. The Scenario Power report allows you to define a sequence of modes and estimate the weighted average of the power consumption of the chip over the entire sequence.
- To define additional modes where the chip is in a predefined mode, but the junction/ambient temperature or the rails' voltage modes are different.

#### 2.17.1.1 Setting the Current Mode

To set the current mode:

 From the Edit menu in SmartPower, choose Modes and Scenarios > Use for Analysis > mode name or select the mode in the Modes and Scenarios toolbar. Enter the result of your step here (optional).

#### 2.17.1.2 Creating a New Custom Mode

To create a new custom mode:

1. From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Modes > New Custom Mode or click Custom Modes in the Modes and Scenarios toolbar, and select New custom mode. The New Custom Mode dialog box appears. Figure 2-25. New Custom Mode Dialog Box

Power - New Custom	Mode 🛛 🔀
Name:	Mode3
Based on mode:	Active
Comment:	
Frequency 15 MHz	
Help	OK Cancel

- 2. Enter the mode name, select the base mode, and enter comments that describe the mode. The base mode can be either a user-defined custom mode or the active mode. The new mode will inherit all clock and data frequencies and annotations of its base mode.
- 3. Click **OK**. The newly created operating mode is set as default in the Modes and Scenarios toolbar.

### 2.17.1.3 Editing a Custom Mode

To edit a custom mode:

 From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Modes > Edit Custom Mode, or right-click the mode in the Modes and Scenarios toolbar and select Edit custom mode. The Edit Custom Mode dialog box appears.

### Figure 2-26. Edit Custom Mode Dialog Box

Power - Edit Custom M	o de [custom_mo de]	×
Name:	custom_mode	
Comment:		
Copied from "Sleep"		
This mode is derived from th	ne "Sleep" low power mode.	
Help	OK Cance	

2. Edit the mode name and comments.

#### 3. Click OK.

**Note:** You can only use the Edit Mode dialog box to edit the name and comment of the current mode. To edit the mode properties, such as clock and data frequencies, use the SmartPower tabs.

### 2.17.1.4 Copying a Custom Mode

To copy a custom mode:

1. Right-click the mode in the Modes and Scenarios toolbar and choose **Create a copy of this mode**. The New Custom Mode dialog box appears.

### Figure 2-27. New Custom Mode Dialog Box

Power - New Custom	Mode 🛛 🔀
Name:	Copy of Active
Based on mode:	Active
Comment:	
Copied from "Active"	
Help	OK Cancel

- 2. Edit the mode name and comments.
- 3. Click OK.

### 2.17.1.5 Deleting a Custom Mode

To delete a custom mode:

 From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Modes > Delete Custom Mode; or right-click the mode in the Modes and Scenarios toolbar, and select Delete Mode. This brings up the Delete Custom Mode dialog box.

The Delete Custom Mode appears.

### Figure 2-28. Delete Custom Mode Dialog Box

Power - Delete Custom Mode	
Choose the custom mode to del Mode3	ete:
Help ОК	Cancel

Select the mode from the pull down and click OK.
 Note: You can delete only custom operating modes. You cannot delete predefined modes.

### 2.18 Scenarios

A scenario is a sequence of previously defined operating modes with a specific duration for each mode. When you create a new design, SmartPower will create predefined scenarios automatically that can be used as is, or copied to create a new scenario based on the predefined one.

Note: You cannot edit or delete predefined scenarios.

### 2.18.1 Creating a New Custom Scenario

To create a new custom scenario:

- 1. From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Scenarios > New Custom Scenario; or click Scenarios in the Modes and Scenarios toolbar, and select New custom scenario.
- 2. Enter the scenario name, enter a duration (total duration for the sequence must equal to 100%) and select previously defined operating modes for this sequence.

### 3. Click OK.

The newly created scenario is set as default in the Modes and Scenarios toolbar.

#### 2.18.2 Editing a Custom Scenario

To edit a custom scenario:

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 From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Scenarios > Edit Custom Scenario; or right-click the scenario in the Modes and Scenarios toolbar, and select Edit custom scenario. The Edit Custom Scenario dialog box appears.

P	ower -	Edit Custom Sce	nario [Copy of 50% Flash*F	. 🗙
I	Vame:	1	Copy of 50% Flash*Freeze	
		Duration (%)	Mode	^
	1	50	Active	
	2	50	Flash*Freeze	
	3			
	4			
	5			
	6			
	7			
	8			
	9			~
	Total: 10	0%	Delete en	try
(	Comment	:		
	Copied f	rom "50% Flash*Fre	eze"	
	Help	>	OK Cancel	

Figure 2-29. Edit Custom Scenario Dialog Box

- 2. Edit the information.
- 3. Click OK.

### 2.18.3 Copying a Scenario

To copy a scenario:

1. Right-click the scenario in the Modes and Scenarios toolbar, and select **Create a copy of this scenario**. The New Custom Scenario dialog box appears.

	wer - ame:	New Custom Scen	opy of scenario1	2
Г		Duration (%)	Mode	
ľ	1	20	Active	
	2	80	Sleep	1 =
	3			
	4			
	5			
	6			
	7			
ŀ	8			-
L	9			<b>×</b>
T	otal: 10(	0%	Delete er	ntry
С	omment	:		
F	Copied f	rom "scenario1"		
	Help	<b>.</b>	OK Cance	

### Figure 2-30. New Custom Scenario Dialog Box

- 2. Edit the information.
- 3. Click OK.

### 2.18.4 Deleting a Custom Scenario

To delete a custom scenario:

 From the Edit menu in SmartPower, choose Modes and Scenarios > Custom Scenarios > Delete Custom Scenario or right-click the scenario in the Modes and Scenarios toolbar, and select Delete Scenario. The Delete Custom Scenario dialog box appears.

Figure 2-31. Delete Custom Scenario Dialog Box

Power - Delete Custom Scenario	X
Choose the custom scenario to o	delete:
Help OK	Cancel

2. Select the scenario from the pull down and click **OK**.

### 2.18.5 Breakdown by Instance

Using the **Breakdown by Instance** panel, you can include the breakdown by instance in the report and set specific options.

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Select a Category	Breakdown by Instance
<ul> <li>General</li> <li>Operating Conditions</li> <li>Options</li> <li>Breakdown by Instance</li> <li>Frequency Summary</li> <li>Probability Summary</li> </ul>	□ Include Breakdown by Instance         □ Limit the number of reported instances to       0         □ Report only instances with power greater than       0.00         □ Sort by :       Power Values         ▼       Sort order :         □ Descending       ▼

Figure 2-32. SmartPower Power Report Dialog Box - Breakdown By Instance Panel

**Include Breakdown by Instance**: shows the power consumption of each element that has been instantiated in the design: gates, nets, memories, and I/Os. The breakdown by instance can be filtered by:

- Limit the number of reported instances to: limits the number of instances reported to the specified number.
- **Report only instances with power greater than**: does not report instances with power consumption below the selected value.

This section can be sorted by selecting the preferred method:

- Sort by: sorts by name (alphabetical) or power values.
- Sort order: sorts by ascending or descending order. Note: The filter reduces the number of lines in the report by one per instance.

### 2.19 Power Reports

The Power report allows you to identify power consumption problems in your design. You can generate this report from the **Tools** menu and from SmartPower.

The Power Report dialog box is organized into the following panels:

- General
- · Operating Conditions
- · Options
- Breakdown by Instance
- Frequency Summary
- · Probability Summary

### 2.19.1 Generating Power Reports from the Tools Menu

To generate Power reports from the **Tools** menu:

- 1. From the **Tools** menu, choose **Reports > Power**. The Power Report dialog box appears.
- 2. Select the options you want to include in the report.
- 3. Click OK.

The Power Report appears in a separate window.

### 2.19.2 Generating Power Reports from within SmartPower

To generate Power reports from within SmartPower:

- 1. From the **Tools** menu, choose **Reports > Power Report** or click the **Report** button to open the Report dialog box. By default, the report includes global design information and a power summary.
- 2. Specify which results you want to display by selecting the categories and their options.

#### 2.19.3 General

The General panel allows you to select what to include in the report, the report format, and the report mode.

#### Figure 2-33. SmartPower Power Report Dialog Box - General Panel

Select a Category General Operating Conditions Options Breakdown by Instance Frequency Summary Probability Summary	Include in the report          1       Image: Power summary         2       Breakdown by rail         3       Breakdown by type         4       Breakdown by clock domain         5       Thermal summary         6       Battery life         7       Clock domain summary	×
	Report Format: XML Modes: Static	- -

#### 2.19.4 Include in the Report

Select the options you want to include in the Power report:

**Power summary**: reports the static, dynamic, and total power consumption of the design.

Breakdown by rail: shows the power consumption of each rail.

Breakdown by type: reports power consumption according to gates, nets, clocks, core static, I/Os, and memories.

Breakdown by clock domain: reports power consumption of each clock domain.

**Thermal summary**: includes a thermal report. The ambient temperature can be defined by operating conditions or ambient temperature.

When operating conditions is selected, the following characteristics are reported:

- Operating conditions
- · Temperature range
- Junction temperature

When ambient temperature is selected, the following characteristics are reported:

- · Ambient temperature
- Cooling style
- Package
- Thermal resistance Theta-JA
- Junction temperature
- Temperature range

• Junction temperature range limits specification

Battery life: reports the battery life.

Clock Domain summary: reports clock and data frequencies for each clock domain.

Operating Condition Summary: reports operating conditions.

**Annotation Coverage**: reports the number and percentage of pins annotated by each source (VCD, manual annotation, SDC constraint, vectorless estimation, and fixed values) for all clocks, register outputs, combinational outputs, set/reset nets, primary inputs, enable pins, and other pins.

#### 2.19.5 Report Format

Select Text, XML, or CSV (comma-separated value) as the desired export format.

#### 2.19.6 Mode

Select a mode for generating the report.

#### 2.19.7 Operating Conditions

The **Operating Conditions** panel allows you to select the operating conditions for the current report. **Figure 2-34. SmartPower Power Report Dialog Box - Operating Conditions Panel** 

1 Power Report		<b>?</b> X
Select a Category General Operating Conditions	Operating Conditions	
<ul> <li>Operating Conditions</li> <li>Options</li> <li>Breakdown by Instance</li> <li>Frequency Summary</li> <li>Probability Summary</li> </ul>		
	Case: Typical	
Help	ОК	Cancel

#### 2.19.8 Options

The **Options** panel allows you to select power and frequency units and to use toggle rates.

Figure 2-35. SmartPower Power Report Dialog Box - Options Panel

Power Report  Select a Category  General  Operating Conditions  Options  Preakdown by Instance  Frequency Summary  Probability Summary	Units         Power:       mW         Frequency:       MHz         ✓         Use Toggle Rates	
Help	ОК	Cancel

#### 2.19.8.1 Units

Frequency: sets unit preferences for frequency: Hz, KHz, MHz.

**Power**: sets unit preferences for power: W, mW, or uW.

#### 2.19.8.2 Use Toggle Rates

When toggle rates are active (**Use Toggle Rates** box is checked), the data frequency of all the clock domains is defined as a function of the clock frequency. This updates the data frequency automatically when you update the clock frequency. Toggle rates allow you to specify the data frequency as a percentage of clock frequency; however, you can specify the data frequency only as a percentage of the clock frequency, not as a number. To set the data frequency again, clear the **Use Toggle Rates** option.

#### 2.19.9 Breakdown by Instance

Using the **Breakdown by Instance** panel, you can include the breakdown by instance in the report and set specific options.

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Select a Category	Breakdown by Instance
<ul> <li>General</li> <li>Operating Conditions</li> <li>Options</li> <li>Breakdown by Instance</li> <li>Frequency Summary</li> <li>Probability Summary</li> </ul>	Include Breakdown by Instance  Limit the number of reported instances to  Report only instances with power greater than  Sort by : Power Values Sort order : Descending

Figure 2-36. SmartPower Power Report Dialog Box - Breakdown By Instance Panel

**Include Breakdown by Instance**: shows the power consumption of each element that has been instantiated in the design: gates, nets, memories, and I/Os. The breakdown by instance can be filtered by:

- Limit the number of reported instances to: limits the number of instances reported to the specified number.
- **Report only instances with power greater than**: does not report instances with power consumption below the selected value.

This section can be sorted by selecting the preferred method:

- Sort by: sorts by name (alphabetical) or power values.
- **Sort order**: sorts by ascending or descending order. **Note:** The filter reduces the number of lines in the report by one per instance.

#### 2.19.10 Frequency Summary

Using the Frequency Summary panel you can include the frequency summary in the report and set specific options.

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Select a Category	Frequency Summary	
<ul> <li>General</li> <li>Operating Conditions</li> <li>Options</li> <li>Breakdown by Instance</li> <li>Frequency Summary</li> <li>Probability Summary</li> </ul>	☐ Include Frequency Summary         ☐ Limit the number of reported pins to         0         ☐ Report only pins with frequencies greater than         0.00         Sort by :         Frequency         Sort order :         Descending	MHz

Figure 2-37. SmartPower Power Report Dialog Box - Frequency Summary Panel

**Include Frequency Summary**: section shows the frequency summary and reports the pin, net, domain, frequency, and frequency source for each pin.

The frequency summary can be filtered by:

- Limit the number of reported pins to: limits the number of pins reported to the specified number.
- **Report only pins with frequencies greater than**: any pin with a frequency below the selected value is not reported.

This section can be sorted by selecting the preferred method:

- Sort by: sorts by pin name, net name, domain, frequency, or source.
- Sort order: sorts by ascending or descending order.

#### 2.19.11 Probability Summary

Using the **Probability Summary** panel you can include the probability summary in the report and set specific options.

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Select a Category	Probability Summary
General Operating Conditions Options Breakdown by Instance Frequency Summary Probability Summary	Tinclude Probability Summary Sort by : Pin Name Sort order : Descending
Help	OK Cancel

Figure 2-38. SmartPower Power Report Dialog Box - Probability Summary Panel

**Include Probability Summary**: shows the probability summary and reports the driver, net, rate, source, and type for each pin. This section can be sorted by selecting the preferred method:

- Sort by: sorts by pin name, net name, rate, source, or type.
- Sort order: sorts by ascending or descending order.

#### Figure 2-39. SmartPower Report

File Actions				
Power Report for d	lesion top w	ith the follow	ing settings:	
•				
Vendor: Micros	semi Corporat	cion		
	semi Libero : Laht (C) 1989		ase v12.1 (Version 12.600.0.14)	
Date: Thu Ma	ay 2 16:29:3	27 2019		
Version: 3.0				
Design:	top			
Family:	Pola	Fire		
Die:	MPF1			
Package:	FCG4	34		
Temperature Range				
	EXT			
Operating Conditi		cal		
Operating Mode:	Stat:	ic		
Process:	Typi	cal		
Data Source:	Produ	action		
ower Summary				
++-		++		
		Percentage		
Total Power				
Static Power				
Dynamic Power				
++-		++	2	

In addition to the information selected on the Power Reports dialog box, the report contains global design information.

**Global design information**: shows the target family, the package and the die. It also shows information about the operating conditions, speed grade, and power mode. This option is set by default.

### 2.20 Scenario Power Report

The Scenario Power report allows you to select a previously defined scenario and calculate the average power consumption and the battery life for this scenario. You can generate this report from the **Tools** menu and from within SmartPower.

The Scenario Power Report dialog box is organized into the following panels:

- General
- · Operating Conditions
- Options
- Battery life

#### 2.20.1 Generating Scenario Power Reports from the Tools Menu

Make sure your design contains one or more scenarios. To generate a Scenario Power report from the **Tools** menu:

- 1. From the **Tools** menu, choose **Reports > Power > Scenario Power Report**. The Scenario Power Report dialog box appears.
- 2. Select the options you want to include in the report, and then click **OK**. The Scenario Power report appears in a separate window.

#### 2.20.2 Generating Scenario Power Reports from within SmartPower

Make sure your design contains one or more scenarios. To generate Scenario Power reports from within SmartPower:

- 1. From the **Tools** menu, choose **Reports > Scenario Power Report** or click the **Scenario Power Report** button to open the Power Scenarios dialog box. By default, the report includes global design information and power sequencer summary.
- 2. Specify which results you want to display by checking the boxes to be included in the report.

#### 2.20.3 General

The **General** panel allows you to select what to include in the report, the report format, and the scenario for which you want to generate the report.

Scenario Power Report	
Select a Category: General Operating Conditions Options Battery life	Include in the report         Breakdown by rail         Breakdown by type         Breakdown by mode         Operating condition summary         Report format:         Text         Scenario:         scenario2
Help	OK Cancel

#### Figure 2-40. SmartPower Scenario Power Report Dialog Box – General Panel

#### 2.20.4 Include in the report

Breakdown by rail: shows the power consumption of each rail.

Breakdown by type: reports on the power consumption according to: gates, nets, clocks, core static, I/Os, and memories.

Breakdown by mode: reports on power consumption by mode.

Operating condition summary: reports the operating conditions.

#### 2.20.4.1 Report format

Select Text or CSV (comma-separated value) as the desired export format.

#### 2.20.4.2 Scenario

Select a previously defined scenario to generate the report from.

#### 2.20.5 Operating Conditions

The **Operating Conditions** panel allows you to select the operating conditions case for the current design.

Scenario Power Report	
Select a Category:	Operating Conditions
Help	OK Cancel

Figure 2-41. SmartPower Scenario Power Report Dialog Box – Operating Conditions Panel

#### 2.20.6 Options

The **Options** panel allows you to select power and frequency units and use toggle rates.

Figure 2-42. SmartPower Scenario Power Report Dialog Box – Options Panel

Scenario Power Report	× 1
Select a Category:	Options Units Power: m₩ ▼ Frequency: MHz ▼
Help	OK Cancel

#### 2.20.7 Units

Frequency: sets unit preferences for frequency (Hz, KHz, MHz).

**Power**: sets unit preferences for power (W, mW, or υW).

#### 2.20.8 Use Toggle Rates

When toggle rates are active (**Use Toggle Rates** box is checked), the data frequency of all the clock domains is defined as a function of the clock frequency. This updates the data frequency automatically when you update the clock frequency. Toggle rates allow you to specify the data frequency as a percentage of clock frequency; however,

you can specify the data frequency only as a percentage of the clock frequency, not as a number. To set the data frequency again, clear the **Use Toggle Rates** option.

#### 2.20.9 Battery life

The Battery life panel reports the battery capacity and the battery life. Enter a battery capacity in MA/Hrs.

#### Figure 2-43. SmartPower Scenario Power Report Dialog Box – Battery Life Panel

Scenario Power Report	
Select a Category: General Operating Conditions Diptions Battery life	■       Include battery life         Battery capacity:       1000.00       mA * Hrs
Help	OK Cancel

The SmartPower Scenario Power report returns the average power consumption and battery life for this sequence.

Vendor:	Corporation Designer So:	_	igloo with 1	the following settings:
Vendor: Program: Date: Thu Ma	Corporation Designer So:	_	igloo with 1	the following settings:
Program: Date: Thu Ma	Designer So:	ftware, Rei		
			lease 8.4, (	Copyright (C) 1989-2008
Design: Family: Die: Package: Temperature Range Voltage Range: Operating Condit: Data Source: Scenario Name:	COM ions: Typic Advan	DOV5 FBGA cal		
Scenario Average H				
	Power (mW)	Percentag	ge	
++   Total Power     Static Power     Dynamic Power	10.926 0.138 10.788	100.0   1.3   98.7	D%   3%   7%	
++ Battery Life +   Battery Capacity +   Battery Life	7   1000.000 207.803	) mA*Hours Hours	-+   -+	
+ Breakdown by mode +				
				Power*Duration Weight
Mode Active     Mode Static     Mode Sleep		21.733   0.156   0.033	50.0% 35.0% 15.0%	99.5% 0.5%

In addition to the information selected in the Scenario Power Reports dialog box, the report contains global design information, a mode summary, and the sequence average power.

**Global design information**: shows the target family, the package and the die. It also shows information about the operating conditions, speed grade, and power mode. This option is set by default.

**Power Summary**: reports the power consumption of the sequence by mode. This option is set by default.

Sequence Average Power: reports the average power consumption of the sequence. This option is set by default.

### 2.21 Activity and Hazards Reports

Traditional Power Analysis based on a VCD simulation file reports an average power value that will account for all nets switching in the design. This switching includes functional transitions and spurious transitions. Due to the delay of each gate, paths arriving at one internal gate may have different propagation delays. Therefore, a gate may exhibit multiple spurious transitions before settling to the correct logic level.

The Activity and Hazards Power report allows to identify gates and nets of the design that consume power because of spurious transitions. This is helpful to understand and further minimize power consumption. The activity and hazards report reads a VCD file and reports transitions and hazards for each clock cycle of the VCD file.

The Activity and Hazards report dialog box is organized into the following panels:

- General
- Partial Parsing
- Top-Level Name
- Glitch Filtering
- Clock Domains

#### 2.21.1 Generating Activity and Hazard Reports from the Tools Menu

To generate Activity and Hazard reports from the Tools menu:

- 1. From the **Tools** menu, choose **Reports > Power > Activity and Hazards Report**. The Activity and Hazards Power Report dialog box appears.
- 2. Select the options you want to include in the report, and then click **OK**. The Activity and Hazards report appears in a separate window.

#### 2.21.2 Generating Activity and Hazard Reports from within SmartPower

To generate Activity and Hazard reports from within SmartPower:

1. From the **Tools** menu, choose **Reports > Activity and Hazards Report**, or select a VCD file from the Modes and Scenarios toolbar and from the right-click menu, select **Tools > Power Activity and Hazards**.

#### 2.21.3 General

#### Figure 2-45. SmartPower Activity and Hazards Report Dialog Box – General

Activity And Hazards Power Repo	rt	×
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Clock domains	General         VCD file:       D:\work\code\design_vcd\BMotor.vcd         Report format:       Text         Use operating conditions from:       Active         Report type:       Report by Net - summary         For each net, report activity and power; sort by total power; sort order descending; Limit the number of reported nets to 40.	
Help	OK Cancel	

VCD file: select the VCD file you want to import.

Report format: select Text or CSV (comma-separated value) as the desired export format.

Use operating conditions from: select the mode from which the operating conditions will be used.

**Report type**: select the report type:

- Report by Net summary: summary report by net.
- Report by Net detailed: detailed report by cycle.
- Report by Cycle summary: summary report by net.
- Report by Cycle detailed: detailed report by cycle. The selected report type reports activity and power for each
  net sorted by power in descending order and limits the number of reported nets to 40 by default. To change
  these options, click each option and from the pop-up menu, select the desired option:
  - Report: select the query report type: activity, power, or activity and power.
  - Sort by: select the query sort by functional power, functional transitions, spurious power, spurious transitions, or total power.
  - Sort order: select the query sort order: ascending or descending.
  - Limit the number of reported nets: enter the query filter limit.

#### 2.21.4 Partial parsing

#### Figure 2-46. SmartPower Activity and Hazards Report Dialog Box – Partial Parsing

Activity And Hazards Power Repo	rt	
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Clock domains	Partial parsing Partially parse VCD Start time: End time:	0.00 ns 10000.00 ns
Help		OK Cancel

**Partially parse VCD**: specify the **Start time** and **End time** to partially parse the VCD file. This option can be used for large VCD files.

#### 2.21.5 Top level name

Figure 2-47. SmartPower Activity and Hazards Report Dialog Box – Top-Level Name

Activity And Hazards Power Repo	rt 🔀
Select a Category:	Top level name
General VCD parsing options Partial parsing Top level name Glitch filtering Clock domains	Automatic detection     Specify:
Help	OK Cancel

This option allows you to select how the top-level name is specified. Select **Automatic detection** to let the VCD reader detect the top-level name of the design automatically or select **Specify** to specify the top-level name manually.

#### 2.21.6 Glitch Filtering

#### Figure 2-48. SmartPower Activity and Hazards Report Advanced Options Dialog Box – Glitch Filtering

Activity And Hazards Power Repo	ort 🛛 🔀
Select a Category: General VCD parsing options Pattial parsing Top level name Glitch filtering Clock domains	C Off Automatic glitch filtering Specify filtering threshold: 100 ps
Help	OK Cancel

This option allows you to filter out pulses of short durations by selecting **Automatic glitch filtering** or by entering a value in the **Specify filtering threshold** field. The default glitch filtering option is **Automatic glitch filtering**.

### 2.21.7 Clock Domains

Figure 2-49. SmartPower Activity and Hazards Report Advanced Options Dialog Box – Clock Domains

Activity And Hazards Power Re	port	×
Select a Category:	Clock domains	
General VCD parsing options Partial parsing Top level name	Clock domain  Clock domain  Automatic construction	
Glitch filtering	C Specify: Period: 10000.00 ps First edge: 0.00 ps	
	Clock domain Active clock Active edge	
	1 PWM_clk true ▼ rising ▼ 2 un1_dataa_int_NE true ▼ rising ▼	
Help	OK Cancel	

The clock domain can be automatically constructed or specified by you.

**Automatic construction**: constructs the clock domain automatically. SmartPower analyzes your design automatically to assess if a clock is active and what is the active edge.

Specify: select this option to specify the period and first edge.

Use the clock domain table to set the active edge (rising, falling or both) and to set a clock as transparent. The results are displayed in the following Activity and Hazards Power report.

Figure 2-50	SmartPower Activity and Hazards Repo	rt
-------------	--------------------------------------	----

	Power_activity_ar	nd_hazards Report						
e Actions Help								
ctivity map r	eport							
		signer Software Release	8.4 (Ve	rsion 8.4.0.0)				
opyright (c)	1989-2008 06 10:43:59 200							
ace: Iue hay	06 10:43:59 200	18						
esign : simple	e PWM 8							
amily : IGLOO								
ie : AGL600V2								
ackage : 256	FBGA							
'emperature Ra								
oltage Range								
	itions : Typics	1						
perating Mode ata Source :								
ata source :	Advanced							
cd file: D:/w	ork/code/design	vcd/BMotor.vcd						
ctivity Map :	Summary							
-	-	+						
		Dynamic Power (mW)						
Total		0.155						
Functional		0.128						
Spurious		0.027						
+	+-	+						
+	+-							
ctivity Map: 1	Net Summary	+						
ctivity Map: )	Net Summary							
ctivity Map: )	Net Summary	+   Clock Domain	Type	Functional	Spurious	Functional	Spurious	
ctivity Map: )	Net Summary	Clock Domain	Type		Spurious   Transitions	Functional   Power	Spurious	
ctivity Map: ) Net	Net Summary	Clock Domain	Type     	Functional   Transitions   +	Spurious   Transitions   +	Functional   Power   (mW) +	Spurious   Power   (mW) +	   
Ctivity Map: 1	Net Summary	Clock Domain	Type     	Functional   Transitions   +	Spurious   Transitions   +	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Ctivity Map: ) Net	Net Summary	Clock Domain	Type     	Functional   Transitions   +	Spurious   Transitions   +	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Ctivity Map: ) Net	Net Summary	Clock Domain	Type     	Functional   Transitions   +	Spurious   Transitions   +	Functional   Power   (mW) +	Spurious   Power   (mW) +	   
ctivity Map: ) Net	Net Summary	Clock Domain	Type     	Functional   Transitions   +	Spurious   Transitions   +	Functional   Power   (mW) +	Spurious   Power   (mW) +	   
Ctivity Map: ) Net	Net Summary	Clock Domain	Type     	Functional   Transitions   +	Spurious   Transitions   +	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Ctivity Map: 1	Net Summary	Clock Domain	Type     	Functional   Transitions   +	Spurious   Transitions   +	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Ctivity Map: 1	Net Summary	Clock Domain	Type     	Functional   Transitions   +	Spurious   Transitions   +	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Ctivity Map: 1	Net Summary	Clock Domain	Type     	Functional   Transitions   +	Spurious   Transitions   +	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Ctivity Map: ) Net	Net Summary UO/NET1 DWACT_FINC_E[0] t_0_i	<pre></pre>	Type     Clock   Data   Clock   Data   Data   Data   Data   Data	Functional   Transitions     5999   1   5999   1   5999   1   746   0   23   1   2087	Spurious   Transitions   0   0   2986   0   1492   0   746   350   2986	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Ctivity Map: 1	Net Summary UO/NET1 DWACT_FINC_E[0] t_0_i	<pre></pre>	Type     Clock   Data   Clock   Data   Data   Data   Data   Data	Functional   Transitions     5999   1   5999   1   5999   1   746   0   23   1   2087	Spurious   Transitions   0   0   2986   0   1492   0   746   350   2986	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Net PUM_clk_c PUM_clk_c PUM_clk_pad/ Qaux[1] un3_qaux_U1_ Qaux[2] Qaux[3] un1_dataa_in: I_4	Net Summary UO/NET1 DWACT_FINC_E[0] t_0_i	<pre></pre>	Type     Clock   Data   Clock   Data   Data   Data   Data   Data	Functional   Transitions     5999   1   5999   1   5999   1   746   0   23   1   2087	Spurious   Transitions   0   0   2986   0   1492   0   746   350   2986	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Net PUM_clk_c PUM_clk_cO Qaux[0] PUM_clk_pad/ Qaux[1] un3_qaux_U1_1 Qaux[2] Qaux[3] un1_dataa_ini I_4 I_5	Net Summary UO/NET1 DWACT_FINC_E[0] t_0_i	<pre></pre>	Type     Clock   Data   Clock   Data   Data   Data   Data   Data	Functional   Transitions     5999   1   5999   1   5999   1   746   0   23   1   2087	Spurious   Transitions   0   0   2986   0   1492   0   746   350   2986	Functional   Power   (mW) +	Spurious   Power   (mW)   0.000   0.000   0.000   0.005   0.000   0.003   0.002   0.001   0.000   0.000   0.000	
Net PWM_clk_c PWM_clk_c Qaux[0] Qaux[1] Qaux[2] Qaux[3] Qaux[3] un1_dataa_in I_4 I_5 PWM_out_pad/	Net Summary UO/NET1 DWACT_FINC_E[0] t_0_i	<pre></pre>	Type     Clock   Data   Clock   Data   Data   Data   Data   Data	Functional   Transitions     5999   1   5999   1   5999   1   746   0   23   1   2087	Spurious   Transitions   0   0   2986   0   1492   0   746   350   2986	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Net PUM_clk_c PUM_clk_c PUM_clk_c0 Qaux[0] Qaux[1] Qaux[2] Qaux[3] un1_dataa_in I_4 I_5 PUM_out_pad/ un1_dataa_in I_9 Qaux[4]	Net Summary UO/NET1 DWACT_FINC_E[0] t_0_i	<pre></pre>	Type     Clock   Data   Clock   Data   Data   Data   Data   Data	Functional   Transitions     5999   1   5999   1   5999   1   746   0   23   1   2087	Spurious   Transitions   0   0   2986   0   1492   0   746   350   2986	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Net PUM_clk_c PUM_clk_c PUM_clk_c0 Qaux[0] PUM_clk_pad/ Qaux[1] un3_qaux_U1_1 Qaux[2] Qaux[3] un1_dataa_ini I_4 I_5 PUM_out_pad/ un1_dataa_ini I_9 Qaux[4] I_13	Net Summary UO/NET1 DWACT_FINC_E[0] t_0_i	<pre></pre>	Type     Clock   Data   Clock   Data   Data   Data   Data   Data	Functional   Transitions     5999   1   5999   1   5999   1   746   0   23   1   2087	Spurious   Transitions   0   0   2986   0   1492   0   746   350   2986	Functional   Power   (mW) +	Spurious   Power   (mW) +	
Net Net PWM_clk_c PWM_clk_c_O Qaux[0] PWM_clk_c_O Qaux[1] un3_qaux_U1_j Qaux[2] Qaux[2] un1_dataa_in I_4 I_5 PWM_out_pad/ un1_dataa_in I_9 Qaux[4] I_13 Landaria_in I_9 Qaux[4] Landaria_in I_9 Qaux[4] Landaria_in I_9 Qaux[4] Landaria_in I_9 Qaux[4] Landaria_in	Net Summary UO/NET1 DWACT_FINC_E[0] t_0_i	<pre>     Clock Domain     Clock Domain     PWM_clk     PWM_clk     Wnf_clk     uni_dataa_int_NE:Y     PWM_clk     uni_dataa_int_NE:Y     uni_dataa_int_NE:Y     uni_dataa_int_NE:Y     uni_dataa_int_NE:Y     WM_clk     uni_dataa_int_NE:Y     wMi_clk     uni_dataa_int_NE:Y     wMi_clk     uni_dataa_int_NE:Y     wMi_clk     uni_dataa_int_NE:Y     WMi_clk     uni_dataa_int_NE:Y     PWM_clk     uni_dataa_int_NE:Y     PWI_clk     VM_clk     PWI_clk     PWI_cl</pre>	Type       Clock   Data   Clock   Data   Data	<pre>Functional Transitions 5999 5999 1 5999 1 1 746 0 23 1 2987 1 2987 24 21 1 747 21 1 747 2 373 746</pre>	Spurious Transitions 0 0 2986 0 2986 0 1492 0 350 2986 0 350 2986 0 0 1492 0 1492 0 1492 0 1492 0 1492 0 1492 0 1492 0 1492 0 0 1492 0 0 1492 0 0 0 1492 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Functional Power ( mW) 0.090 0.019 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.001 0.001 0.001 0.001 0.001 0.001 0.001 0.001 0.001 0.000 0.000 0.000 0.000	Spurious   Power   (mW)   0.000   0.000   0.003   0.003   0.003   0.003   0.002   0.001   0.000   0.000   0.000   0.000   0.000   0.000	
Net PUM_clk_c PUM_clk_c PUM_clk_c0 Qaux[0] PUM_clk_pad/ Qaux[1] un3_qaux_U1_1 Qaux[2] Qaux[3] un1_dataa_ini I_4 I_5 PUM_out_pad/ un1_dataa_ini I_9 Qaux[4] I_13	Net Summary UO/NET1 DWACT_FINC_E[0] t_0_i	Clock Domain	I Type I Type I Clock I Clock I Data I Data	Functional Transitions 5999 5999 1 1 5999 1 1 746 0 23 1 1 2987 1494 21 1 2987 1494 21 1 1 747 2 3 3 3 3 3 4 9 4 3 3 3 3 3 3 3 3 4 6 4 5 9 9 9 9 1 9 9 9 9 1 9 9 9 9 1 9 9 9 1 9 9 9 1 9 9 9 1 9 9 9 1 9 9 9 1 9 9 9 1 9 9 9 1 9 9 9 1 9 9 9 1 9 9 9 1 1 1 1 9 9 9 9 1 1 1 1 1 1 1 7 46 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Spurious Transitions 	Functional Power (mW) 0.090 0.019 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.000 0.001 0.001 0.001 0.001 0.001 0.000 0.000 0.000 0.000 0.000 0.000	Spurious   Power   (mW) +	   

## 2.22 Export Report for Microchip Power Estimator (MPE)

This option exports an .xml report from SmartPower, which can be imported into the MPE tool. To export the MPE report, go to **Tools > Export Report for MPE**.

The generated .xml report contains the following information:

- · Device Settings
- · Thermal Settings
- Voltage Source
- Clocks
- Logic Breakdown
- · LSRAM Breakdown with Advanced Settings
- uSRAM Breakdown with Advanced Settings
- · Math Breakdown with Advanced Settings
- PLL and DLL
- I/Os
- Crypto
- Transceivers

In addition, the following information is available for PolarFire SoC devices:

- MSS RISC-V (Quad U54)
- AXI MSS/Fabric Interfaces
- MDDR
- MSS I/O Interfaces
- User Crypto

MPE has an import feature, which allows the user to import either the existing MPE spreadsheet (.xls format) or Power estimation results from Libero SoC SmartPower (.xml format), as shown in the following figure.

#### Figure 2-51. MPE with Import Data

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pard (s)		C Import existing Microchip Power Estimator (MP	E) ovraadebaat (= vie=)
c	✓ <i>f</i> * D	E F	1
	Initialize Power Estimator	Design Data     C Append imported data to existing design data     Overwrite existing design data	ign data
mport	Initialize Power Estimator	Advance Options	
Project		Import Device Settings	
Project Settings		F Import Device Settings	
	General	F Import Thermal Inputs	
	General PolarFire	F Import Thermal Inputs	
Settings	Contracting States	F Import Thermal Inputs	
Settings Family	PolarFire	F Import Thermal Inputs  I Import Voltage Settings I Import Snapshots	
Settings Family Device	PolarFire MPF300TLS	F Import Thermal Inputs	Brows
Settings Family Device Package	PolarFire MPF300TLS FCG484 Extended	File name :	
Settings Family Device Package Range	PolarFire MPF300TLS FCG484 Extended	File name :	port Cance
Settings Family Device Package Range Core Voltage	PolarFire MPF300TLS FCG484 Extended 1.0 V Typical	File name :	

## 2.23 Freeze/Unfreeze Calculations

Freeze/Unfreeze calculation option allows a more responsive User Interface and avoids runtime slowness due to a re-computation that occurs on every value changes. A toggle play pause button is provided to freeze the computation until the user is ready to re-compute. Only when the user clicks the play button, all the changes done will be computed and the User Interface gets updated.

To Freeze/Unfreeze Calculations, go to **Tools > Freeze/Unfreeze Calculations**.

#### Figure 2-52. Freeze/Unfreeze Calculations

拍 shift32 * - Sm	artPower	
File Edit View	Tools Simulation Help	
Modes and Scenarios	Options	
Static	ReportsExport Report for MPERefresh Vectorless	
	Freeze/Unfreeze Calculations	

## 2.24 Importing a VCD File

The Value Change Dump (VCD) file is a simulation file. The format of this file is specified in the IEEE 1364 standard.

You can configure the Project Manager to generate VCD files automatically using ModelSim. You can also generate a VCD file with a ModelSim simulator using the following commands:

vcd file example.vcd vcd add -r /testbench/<top>\_0/\* run 1 us vcd flush

This example creates a VCD file called example.vcd, adds all signals recursively, runs the simulation for one microsecond, and quits. You must quit ModelSim to obtain an accurate result from SmartPower.

If you have not completed the layout of the design, the design software guides you through place-and-route so you can import the VCD file. To annotate your VCD values to the design successfully, complete place-and-route even if you generated VCD files using timing simulation (pre-layout).

**Note:** SmartPower has been validated with VCD files generated by ModelSim. However, you may use any Verilog/ VHDL simulator that offers a VCD dump feature.

For more information about how to generate a VCD file, refer to the user manual for your simulation tool.

1. From the **Simulation** menu, choose **Import VCD File**. The Import VCD Options dialog box appears.

#### Figure 2-53. Import VCD File Dialog Box

Import VCD Options		×
Select a Category: General VCD parsing options Patial parsing Top level name Glitch filtering Remaining signals	General         VCD file:       D:\work\code\sub.vcd         Import in:            Existing mode:         Active         New mode:	
Help	OK Cancel	

- 2. Select the VCD file you want to import and select a mode to import it in, or click **New mode** and enter a mode name.
- 3. Select the options you want to specify.
  - Figure 2-54. Import VCD File Dialog Box Partial Parsing

Import VCD Options		×
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Remaining signals	Partial parsing Partially parse VCD Start time: 0.00 ns End time: 10000.00 ns	
Help	OK Cancel	

- **Partial parsing**: specify the **Start time** and **End time** to partially parse the VCD file. This option can be used for large VCD files.
- **Top level name**: allows you to select how the top-level name is specified. The **Top level name** is the instance name of your design instantiated in the simulation testbench.
- 4. Select **Automatic detection** to let the VCD reader detect the top-level name of the design automatically or select **Specify** to specify the top-level name manually.

Figure 2-55	Import VCD File	Dialog Box -	<b>Top-Level Name</b>
1 iguie 2-33.			

Import VCD Options	X
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Remaining signals	Top level name     Automatic detection     Specify:
Help	OK Cancel

- **Glitch filtering**: allows you to filter pulses of short durations by selecting **Automatic glitch filtering** or by entering a value in the **Specify filtering threshold** field. The default option is **Automatic glitch filtering**.
- Remaining signals: some signals may not be annotated by the VCD reader. This generally happens with VCD files created from a behavioral or a post-synthesis simulation. For those signals, you can either complete the annotation with the vectorless analysis or with the average values computed from the VCD file.

Figure 2-56. Import VCD File Dialog Box — Glitch Filtering

Import VCD Options		×
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Remaining signals	C Off Automatic glitch filtering Specify filtering threshold: 100 ps	
Help	OK Cancel	

Filtering: allows you to filter pulses of short durations by selecting Automatic Glitch Filtering or by entering a value in the Specify Filtering Threshold field. The default option is Automatic Glitch Filtering.
 Remaining Signals: some signals may not be annotated by the VCD reader. This generally happens with VCD files created from a behavioral or a post-synthesis simulation. For those signals, you can either complete the annotation with the vectorless analysis or with the average values computed from the VCD file.

Import VCD Options	
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering Remaining signals	Remaining signals
Help	OK Cancel

#### Figure 2-57. Import VCD File Dialog Box — Remaining Signals

#### 5. Click OK.

When the VCD file is imported successfully, the file appears under the imported mode in the Modes and Scenarios toolbar and the following messages appear in the Designer Log window: Info:

VCD:34 glitch(es) filtered with 1000 ps threshold

The message above reports the number of glitches that have been filtered by the VCD reader.

Info:

VCD: Annotation Statistics Percentage of Annotated Pins:100.00 % Percentage of Unannotated Pins:0.00 %

Percentage of Annotated Pins with Zero Frequency: 25.99 %

If the percentage of annotated pins is less than 50.00%, a warning message is generated.

If the percentage of annotated pins is low, you may want to verify that signals at all levels of hierarchy were added recursively (for example using vcd add -r in ModelSim).

If you simulate a pre-synthesis netlist or a post-synthesis RTL netlist, it is possible to get a low percentage of annotated pins. This happens because not all logic elements are in the pre-synthesis netlist and the post-synthesis RTL netlist. For accurate power estimation, it is best to run post-layout simulation with a back-annotated netlist.

To see which pins are not annotated, open the SmartPower **Frequencies** tab. If your file was imported successfully, a list of pins with annotated individual frequencies displayed with **VCD Import** appear as a source. The unannotated pins are displayed with **Default Estimation** as source. If your design has enable pins, open the SmartPower **Probabilities** tab.

After completing the import VCD process, you can create a custom mode based on the active mode. This custom mode will inherit all the clock and toggle frequencies of the active mode you set through the VCD import. This final step is optional. It gives you the flexibility to modify the active mode frequencies while saving the VCD scenario in SmartPower. For more information, refer to 2.17.1 Custom Operating Modes.

#### 2.25 Removing a VCD File

The Value Change Dump (VCD) file is a simulation file whose format conforms to the IEEE 1364 standard.

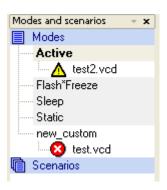
To remove a VCD file, perform one of the following steps:

- Select the VCD file from Active mode or a custom mode, right-click the VCD file and select Remove VCD File from <mode name> Mode.
- From the Simulation menu, choose Remove VCD File > <file name> Note: The annotation is removed when you remove the VCD file.

## 2.26 Auditing Files

When you start SmartPower, it performs an audit automatically. During the audit, SmartPower checks the time stamps of VCD files and reports any missing or out-of-date files. You can also initiate a file audit manually from the **Simulation** menu by choosing **Audit Files**. After an audit is run, an icon displaying the file status appears in the Modes and Scenarios toolbar next to the VCD file. Mousing over the icon displays more information.

Figure 2-58. Audit Files Results



#### Table 2-5. Audit Files Icons and Descriptions

lcon	Description
Δ	Indicates that the VCD file has been modified
0	Indicates that the VCD file is missing

To re-import the VCD file, right-click the VCD file and select **Re-import VCD File**. Then use the Import VCD Options dialog box to re-import the file.

## 3. **Power Options**

Allows you to set options that affect graphical and textual reports.

To open the SmartPower Power Options dialog box:

- 1. From the File menu, choose Options.
- 2. Select the **Options** panel in the Power Report dialog box.
- 3. Click the licon in the SmartPower toolbar.

Figure 3-1. SmartPower Preferences Dialog Box

Power - Options	
Units Power: mW • Frequency MHz • Vse toggle rates	
Help OK	Cancel

The dialog box has two sections: Units and Use Toggle Rates.

- Units: sets unit preferences for power (W, mW, and uW) and frequency (Hz, KHz, and MHz).
- **Use toggle rates**: when checked, the data frequency of all the clock domains is defined as a function of the clock frequency. This updates the data frequency automatically when you update the clock frequency. Toggle rates allow you to specify the data frequency as a percentage of clock frequency, but you can no longer specify the data frequency as a number, only as a percentage of the clock frequency. To specify data frequencies, clear the **Use toggle rates** option in the Preferences window.

You can set the data frequency percentage when you create a new clock domain with toggle rates active. In addition, when toggle rates are active you can set the data frequency percentage in the **Domain and Frequencies** tabs.

#### Figure 3-2. Create Clock Domain – Toggle Rates Enabled

Create Clock Domain	×
Potential Clock Pin CLK_pad/IOTILE:Y0	Create
Clock Frequency 10 MHz	Cancel
Data Frequency 20 %	

## 4. Calculating Power

### 4.1 Calculating Power

Use the following steps to calculate the power consumption of your design. The list of screens and steps appear in the order in which you should view them to analyze your power accurately.

- 1. Summary tab: view global power at the design level and view its impact on junction temperature.
- 2. **Domains** tab: define clock domains and specify a clock frequency and a data frequency for each clock domain.
- 3. **Analysis** tab (optional): view detailed hierarchical analysis of your power consumption. If your power consumption exceeds your budget, this step helps you understand where there is room for improvement.
- 4. **Frequencies** tab (optional): specify individual pin frequencies. This step provides pin-by-pin control of the frequency.
- 5. Probabilities tab (optional): specify probabilities. You can use the default probabilities or set your own.

## 4.2 Extracting Power Consumption of a Specific Clock Domain

To calculate the power consumption of a single clock domain (clock tree and data path) in a design:

- 1. Set SmartPower in toggle-rate mode. This is the default setting. To confirm that SmartPower is in toggle-rate mode, choose **Preferences** from the **File** menu. Select the **Use Toggle Rates** check box.
- 2. In the **Domains** tab, set all the **Clock Frequencies** to zero except for the clock domain for which you are calculating the power consumption.

## 4.3 Advanced Analysis of I/Os

SmartPower allows you to estimate the power consumption related to I/Os. You can then analyze power consumption in detail.

To display I/O power consumption:

- 1. In the Summary tab, select By Type from the Breakdown drop-down list. The grid displays the total power consumption of all I/Os in the design, as well as all other components. If you use different I/O standards, and different Vcci power rails, you can also display the power consumption for each rail by selecting By Rail from the Breakdown drop-down list. Breakdown By Rail shows the power consumption and current for each Vcci rail in the design.
- 2. In the **Analysis** tab, select the highest hierarchy level in the Hierarchy tree in the left pane. Select **By Instance** from the Breakdown drop-down list.
- 3. In the Analysis tab, unselect all categories under Instances Contributions except I/Os, and then click Apply. The table then displays a list of all I/Os in the design, along with the power contribution of each individual I/O. The columns display important I/O attributes: external port name, load, standard, drive- strength, slew, and macro.
- 4. In the **Probabilities** tab, you can control the output probability of each tri-state and bidirectional I/O. The probability is the percentage of time that the I/O is used as an output. The default value can be changed and a specific value can also be set for each bidirectional or tri-state I/O.

## 4.4 Adding a New Clock Domain

When you run SmartPower, it researches your existing clock domains and partitions your design automatically.

You may want to review the list of clock domains in the **Domains** tab to ensure that all the clocks of your design are included in the list. Add or remove clocks as necessary. To add a new clock domain:

- 1. Click the **Domains** tab, and then click the **Add Domain** button.
- 2. Select **Clock Domain** from the drop-down list. The Create Clock Domain dialog box appears.

Figure 4-1. Create Clock Domain Dialog Box – Toggle Rates Disabled

Create Clock Domain	×
Potential Clock Pin CLK_pad/IOTILE:Y0	Create
Clock Frequency 10 MHz Data Frequency 1 MHz	Cancel

3. To create a new clock, select a **Potential Clock Pin**, specify a clock and data frequency and click **Create**. The new clock domain appears in the Domains window. If you select an existing clock pin from the drop- down list, the lists of clock pins and data pins of this new clock domain are computed automatically based on the netlist topology.

**Note:** Select **Use Toggle Rates** in the SmartPower Preferences to define your data frequency as a percentage of your clock frequency. If your data frequency is 20% of your clock frequency, type **20** in the **Data Frequency** text box.

Create Clock Domain	×
Potential Clock Pin CLK_pad/IOTILE:Y0	Create
Clock Frequency 10 MHz	Cancel
Data Frequency 20 %	

If you want to create an empty clock domain and fill the lists of clock-pins and data pins manually, do not select a clock pin. Instead, type a new name for your clock domain.

## 4.5 Verifying Lists of Clock and Data Pins of a Clock Domain

Beyond the verification of the list of clock domains, you may also wish to verify that the lists of clock pins and data pins computed for each clock domain are correct.

To verify the lists of clock pins and data pins of a clock domain:

- 1. Click the **Domains** tab and select a specific **Domain** in the list.
- 2. **Display the list of clock pins or data pins of this Domain.** A drop-down list in the **Domains** tab allows you to select clock pins or data pins. SmartPower displays the list of pins corresponding to your selection below the drop-down list. You can add or remove clock pins and data pins as necessary.
- 3. **Remove a pin from a clock domain.** Highlight the selected pin and click the **Remove** button. The pin is removed from the clock domain and is made available in the list of pins that you can add in another clock domain.
- 4. Highlight the selected pin in the list of pins that are not yet in a domain and click the **Add** button to add a pin in a clock domain.

This pin is added to the clock domain. The pin is a clock or data pin, depending on the specification of the drop-down list when you clicked the **Add** button.

**Note:** You cannot add a pin that exists in another domain until you free it from its existing domain. The pin is unavailable until you remove it from that domain.

After you verify that all the clocks of your designs are correctly identified and constructed, specify the correct clock and data frequency for each clock domain.

### 4.6 Adding a New Set of Pins

To add a new set of pins:

- 1. Open the Create Clock Domain dialog box.
- 2. Click the Domains tab and click the Add Domain button.
- 3. Select Set of Pins from the drop-down list.
- 4. **Create a Set of Pins.** Name your new set of pins, specify a data frequency, and click **Create Figure 4-2. Create Set of Pins Dialog Box**

Create Set of Pi	ins		×
Set Name	Output		Create
		1	Cancel
Frequency	1	MHz	

The new set of pins appears in the Domains window.

### 4.7 Specifying Clock and Data Frequencies in SmartPower

To specify a clock and data frequency:

- 1. Click the **Domains** tab.
- 2. Select the Clock/Data frequency cell and enter a new value.

SmartPower defaults to 0 MHz for the clock frequency. Import your clock frequency from SmartTime by using the Initialize Frequencies dialog box in SmartPower or input your target for each clock frequency in the **Domains** tab. You must also specify a data frequency (5% of your clock frequency is a typical guideline for your data frequency – this corresponds to a toggle rate of 10%).

Not all the pins/gates/nets of your design are associated with a specific clock. For example, the frequency of a design input port is not always correlated to a clock frequency. By extension, all pins that are upstream of the first level of sequential elements are not associated with any clock. SmartPower creates an InputSet by default that it uses to group all the pins that are controlled by design inputs (instead of sequential elements). You may want to view and verify the InputSet to further evaluate your design.

### 4.8 Verifying the InputSet

To verify the InputSet:

- 1. Click the Domains tab and select the domain named InputSet in the list.
- Verify the list of pins of this domain. All the input ports of your design (except the clocks) belong in the InputSet. All pins between these input ports and the first level of sequential elements belong in the InputSet. You can add or remove pins as necessary.
- 3. Specify an average input frequency. SmartPower uses the same frequency for all pins of the InputSet. The default InputSet frequency is 1 MHz. Enter a new value to change it.

### 4.9 Splitting the InputSet

You might want to split the InputSet into several sets in order to specify different frequencies. For example, you might want to create a ResetSet — a reset tree with a very low frequency.

To split the InputSet:

- 1. Create a new set of pins: In the **Domains** tab, click the **New** button, and select **Set of Pins** from the dropdown menu.
- 2. In the Create Set of Pins dialog box, type a name and a frequency for the new set and click **Create**. The new set of pins appears in the Domains window. You can only create an empty set of pins, but it is possible to add pins to this domain later.
- 3. Remove a group of pins from the **InputSet**. Click the **Domains** tab and select the domain named **InputSet** in the list.

4. Select the pins that you want to remove and click the **Remove** button.

## 4.10 Specifying Individual Pin Frequencies

The **Frequencies** tab allows you to specify an average clock and data frequency for each clock domain, and also an average frequency for each set of pins. This gives you an initial estimate of the power consumption of your design. However, if this estimate is not sufficiently accurate, you can refine it with a pin-by-pin annotation of the frequency.

The following procedure describes how to set the frequency of an individual pin. Performing this procedure does not remove the pin from its clock domain. A frequency annotation merely overrides the domain level frequency.

- 1. Locate the pin in the **Frequencies** tab. You may need to select different clock domains from the drop-down list on the **Frequencies** tab. You can use filters to facilitate this search.
- 2. Select the pin(s) in the grid and click the **Set frequencies for selected pins** button.
- 3. Enter a new frequency value and click **OK**. This specifies a new frequency for the selected pin(s).

## 4.11 Changing the Frequency Annotation of a Pin

The following procedure describes how to change the frequency annotation of an individual pin. This may be useful when you import a VCD (value change-dump) file (see ).

- 1. Locate the pin in the **Frequencies** tab. You may need to select different clock domains from the drop-down list on the **Frequencies** tab. You can use filters to facilitate the search.
- 2. Select the pin(s) in the grid and click the **Set frequency for selected pins** button.
- 3. Enter a new frequency value and click **OK**. This specifies a new frequency for the selected pin(s).

## 4.12 Removing the Frequency Annotation of a Pin

This procedure describes how to remove the frequency annotation of an individual pin. This may be useful when you import a VCD (value change-dump) file.

- 1. Locate the pin in the **Frequencies** tab. You may need to select different clock domains from the drop-down menu on the **Frequencies** tab. You can use filters to facilitate the search.
- 2. Select the pin(s) in the grid and click the **Reset frequencies for selected pins** button. This removes the specified frequency from the selected pins.

## 4.13 Specifying Individual Pin Probabilities

The **Probabilities** tab allows you to specify the default output probability value for memory blocks, and tristate and bidirectional I/Os. In addition, you can increase the accuracy of the power estimation by annotating the probability of specific pins.

To specify or change the probability for one or multiple pins:

- 1. Locate the pin(s) in the **Probabilities** tab. You can use filters to facilitate this search.
- 2. Select the pin(s) and click the Set probabilities for selected pins button.
- 3. Enter a new probability value and click **OK**.

#### 4.13.1 Specifying or Changing Probability for One or More Pins

To specify or change the probability for one or multiple pins:

- 1. Locate the pin(s) in the **Probabilities** tab. You can use filters to facilitate this search.
- 2. Select the pin(s) and click the Set probabilities for selected pins button.
- 3. Enter a new probability value and click **OK**.

#### 4.13.2 Resetting the Probability for One or More Pins

To reset the probability for one or multiple pins:

- 1. Locate the pin(s) in the **Probabilities** tab. You can use filters to facilitate this search.
- 2. Select the pin(s) and click the Reset Probabilities for selected pinsbutton.

### 4.14 Vectorless Estimation

The Vectorless estimation method is an accurate method of annotating individual pins with frequencies and probabilities. It uses primary inputs, clock frequencies, and nets annotated with other methods as a starting point, and uses a Monte Carlo simulation to annotate all nets in the design with frequencies and probabilities.

Vectorless estimation is available for SmartFusion2, IGLOO2, RTG4, PolarFire and PolarFire SoC families of devices.

Vectorless estimation can be enabled from the Initialize Frequencies and Probabilities dialog box or from the VCD Import dialog box.

Changes to probabilities or frequencies in the Probabilities, Frequencies, or Domains tabs result in an out-of-date

vectorless estimation. To update vectorless estimation, press the refresh vectorless 🔽 button.

### 4.15 Viewing Results (Design Level)

Click the **Summary** tab to view global power consumption at the design level. The **Summary** tab shows your design's estimated power consumption and temperature information.

The power estimation reported in the **Summary** tab is the total static and dynamic power consumption of your design. For a more detailed view of this power consumption, click the **Analysis** tab. To estimate the junction temperature:

- 1. Verify your package. You cannot change your package directly in SmartPower, because it may render your place-and-route information (and thus it may severely impact the total power consumption). To choose another package, use **Designer > Tools > Device Selection**.
- 2. Click the **Summary** tab and select a **Cooling** style in the list. Thermal resistance changes automatically when you update the cooling style.
- 3. Specify an ambient temperature. Enter an **ambient temperature** (default value is 25°C) and click the **Set** button.

**Note:** The junction temperature value changes according to the package, cooling style, and ambient temperature values you choose.

### 4.16 Analyzing Results

The **Analysis** tab shows the estimated power consumption of individual blocks, gates, nets, I/Os, and memory, and allows you to make a hierarchical analysis of your power consumption.

The **Analysis** tab may also help you to improve your power consumption by identifying the components that consume a significant amount of power.

To identify the components consuming the most power:

1. Use the **Analysis** tab to expand the design hierarchy. The **Analysis** tab allows you to expand your design hierarchy and view a complete list of the blocks in your design. In the hierarchy window, click the **+** next to your design to view the items in the hierarchy. Click the **+** next to a sub-block to view its sub-elements.

Summary     Some Dom       Image: Summary     Image: Summary       Image: Summary     Image: Summary <th>P</th> <th>Consumption Block Nam Static Pow</th> <th>ne: WGT</th> <th>]</th> <th></th> <th></th>	P	Consumption Block Nam Static Pow	ne: WGT	]		
		Block Nan	ne: WGT			
IMDC/U IMDC/SL IG		Dynamic Pow akdown: By Ty	er: 0.014 mW		Show C Ch	art 💿 Grid
D PL D CTRL D CTRL D CTRL D CTRL		<b>Type</b> Net Gate	•	Power (mW) 0.003 0.011	20.3%	
SREG CLK CREG						3

- 2. Click to select a block. By default, SmartPower selects the design-level block, but you can always select another block in the hierarchical tree. The Report window displays the list of sub-elements of the selected block. Initially, this list includes all sub-elements. The grid in the Analysis window displays a breakdown of the power of the selected block by type. This breakdown provides you a good overview of which areas of your design you should optimize for power.
- 3. To find the components that use a significant amount of power, choose By Instance from the Breakdown drop-down list.
- Sort and filter the sub-elements to find the component that is using the most power. The Analysis window 4. displays the list of sub-elements of the selected block. By default, this list includes all sub-elements. The grid contains columns for name, type, power, driver, fanout, macro, I/O standard, output load, output drive, slew, port, domain and frequency. You can limit the list of sub-elements to a list of sub-blocks, nets, gates, I/Os, memories, or any combination of these five classes of sub-elements. You can sort the list according to any column by double-clicking the column header.

#### 4.17 SmartPower Calculation Equations

SmartPower calculates the static power and the dynamic power of your design, for given operating conditions and operating modes:

Static Power: summation of the static power consumed by each element of the design. SmartPower provides a static power consumption of the array. This value is die-dependent. This value is also a function of the operating mode. For some families, SmartPower also considers a static power contribution per I/O bank. For specific I/O technologies like voltage referenced I/Os or differential I/Os, SmartPower also considers a static power contribution per I/O.

Dynamic Power: summation of the dynamic power consumed by each element of the design (nets, modules, I/Os, RAMs, FIFOs, PLLs, etc.).

**Operating Conditions**: SmartPower calculates power consumption in Worst, Typical, or Best operating conditions. SmartPower uses the following as general guidelines:

It applies a voltage derating to dynamic power contributions. Higher voltage typically leads to higher power consumption.

- It applies a temperature derating to static power contributions. Higher temperature typically leads to higher power consumption.
- It applies no radiation derating.

**Operating Modes**: SmartPower calculates power consumption in Active, Static, Flash\*Freeze, Sleep, and Shutdown operating modes when applicable for your design.

## 4.18 Sample Equations:

The following examples are for general evaluation purposes only. They are not a precise representation of the actual calculations, since each calculation takes into account family-specific information.

• For a **net**,

 $P = C \cdot V^2 \cdot F$ 

where C is the total capacitive loading of the net (extracted from the routing topology), V is the net's voltage swing, and F is the average switching frequency.

**Note:** For the ProASIC<u>PLUS</u> family, SmartPower extracts the capacitive loading of a net from a Wire Load model.

• For a **module**, the power is computed using a characterized library (by family and die-size) describing a specific power model for each type of module. For example, the power model of a flip-flop is given by  $P = P_{CK} \cdot F_{CK} + P_{DOUT} \cdot F_{DOUT} + P_{Din} \cdot F_{Din}$ 

where FCK is the average clock-input frequency for this flip-flop, FDOUT is its average data-output frequency, and PCK, PDOUT, PDin are three constants estimated by electrical simulation and silicon characterization for this flip-flop module, and FDin is its average data-input frequency.

• For an **I/O**, the formula used for computing the power consumption depends on the I/O technology and the family. For example, for a TTL output, the dynamic power is given by  $P = P_{INT} \cdot F + C \cdot V^2 \cdot F$ 

where C is the output load (derived from what you have set in the I/O Attribute Editor GUI, typically 35 pF for TTL), V is the output's voltage swing (3.3 V for TTL), and PINT represents an internal power contribution dissipated in the pad, and F is the average switching frequency of the I/O.

• For a **complex block**, like a RAM, a FIFO, or a PLL, SmartPower uses a high-level power model that integrates design parameters.

SmartPower computes all the constant parameters of these equations automatically. However, the frequencies depend on the target frequencies of your design. Since it is impractical to enter each frequency manually, SmartPower has several flows that help you estimate the frequencies and calculate the power consumption.

## 4.19 Data Change History - SmartPower

The data change history report lists power data updates up to the current release that may impact the power consumption of the design.

To generate a data change history report, choose **Data Change History** from the **Help** menu to open a data change history report in text format.

## 5. SmartPower Tcl Commands

Refer to the following documents for detailed information about Tcl commands supported by SmartPower:

- SmartFusion2, IGLOO2, RTG4 Tcl Commands Reference Guide
- PolarFire FPGA Tcl Commands Reference Guide

# 6. Revision History

Revision	Date	Description
В	04/2021	<ul> <li>The following changes are made in this revision:</li> <li>Updated section Export Report for Microchip Power Estimator (MPE).</li> <li>Added section Freeze/Unfreeze Calculations.</li> </ul>
A	11/2020	Document converted to Microchip template. Initial Revision.

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