Welcome to Edition 31 of Microchip's Space Brief newsletter. Written for design engineers and design managers, system engineers and system architects, component engineers, radiation effects scientists and program managers in the space industry, Space Brief is a quarterly newsletter in which we aim to bring you the latest news about our radiation-tolerant and radiation-hardened products. Space Brief provides information about new products, updates on qualification and radiation testing, links to formal customer notifications, and news about workshops and conferences at which Microchip will be presenting or exhibiting.

Please forward Space Brief to your colleagues, and let them know they can register to receive this newsletter directly to their email inbox every three months by clicking here.

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PRODUCT NEWS

New Technical Brief for RTG4™ QML and Sub-QML FPGAs

We recently published a single document titled RTG4 FPGAs Technical Brief to replace two separate documents: RTG4 FPGAs Product Brief and RTG4 Plastic Product Brief. The new technical brief includes information about the RTG4 FPGA family overview, product features and benefits, ordering information, marking specifications and screening flows for both RTG4 QML and Sub-QML FPGAs.

Sub-QML FPGAs combine the radiation tolerance of QML components with our spaceflight heritage that permits lower screening requirements to provide lower costs and shorter lead times for demanding space missions. Although Sub-QML FPGA options are available for all our RT FPGA families, RTG4 FPGAs have the most screening flow options as shown in Figure 1. The lowest-cost option is RTG4 FPGAs in the 1657 Ball Grid Array (BGA) plastic package, which is well suited for small satellite or constellation applications. The RTG4 Sub-QML plastic package is currently going through JEDEC qualification and is targeted for completion in April 2021.

Flow	Purpose	Package	Qualification	Screening			
				Burn-In	Temp Test	Life Test	DPA
V	NSS, NASA Class1	Hermetic Ceramic	QML-V	Static Dynamic	-55°C – 125°C	Wafer-Lot	Assy Lot
E	Advanced Traditional Space	Hermetic Ceramic	QML-Q	Static Dynamic	-55°C – 125°C	Generic Group C	Optional
B	Entry Level Traditional Space	Hermetic Ceramic	QML-Q	Dynamic	-55°C – 125°C	Generic Group C	None
R	New Space, Strategic Programs	Hermetic Ceramic	MIL-STD-883 Class B	Dynamic	-55°C – 125°C	None	None
Mil Ceramic	New Space, Strategic Programs	Hermetic Ceramic	MIL-STD-883 Class B	None	-55°C – 125°C	None	None
PROTO	Prototyping	Ceramic (Hermeticity not Guaranteed)	MIL-STD-883 Class B	None	-55°C – 125°C	None	None
Mil Plastic	New Space, Strategic Programs	Plastic Non-Hermetic	JEDEC	None	-55°C – 125°C	None	None

Figure 1: RTG4™ FPGA Screening Flows

The technical brief has a new Screening Flows section with a detailed description of each of the QML (V, E, B), Sub-QML (R, Mil-Ceramic, Mil-Plastic) and even PROTO screening flows. An example of the screening flow description is shown in Figure 2.

Table 5-6. RTG4 Mil-Plastic Flow (Microchip Sub-QML Flow)

Step	Screen	Test Method	Requirement
1	Final Electrical Test	In accordance with applicable Microchip device specification, which includes a, b, and c:	100%
	a. Static Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3	
	b. Functional Tests (1) 25 °C (2) –55 °C and +125 °C	— 5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b	
	c. Switching Tests at 25 °C	5005, Table 1, Subgroup 9	
2	External Visual	2009	QA Sample

Figure 2: RTG4™ Mil-Plastic Flow in RTG4 FPGAs Technical Brief

The RTG4 FPGAs Technical Brief complements the RTG4 FPGAs data sheet, which was also updated recently and has all the timing and power data specifications for the family. Please check out these new documents and reach out to your local Microchip sales team if you have a need for QML, Sub-QML FPGAs, or radiation-tolerant FPGAs in higher volume and at lower cost than traditional space applications.

For further information, contact minh.nguyen@microchip.com

New Radiation Reports for RTG4 FPGAs

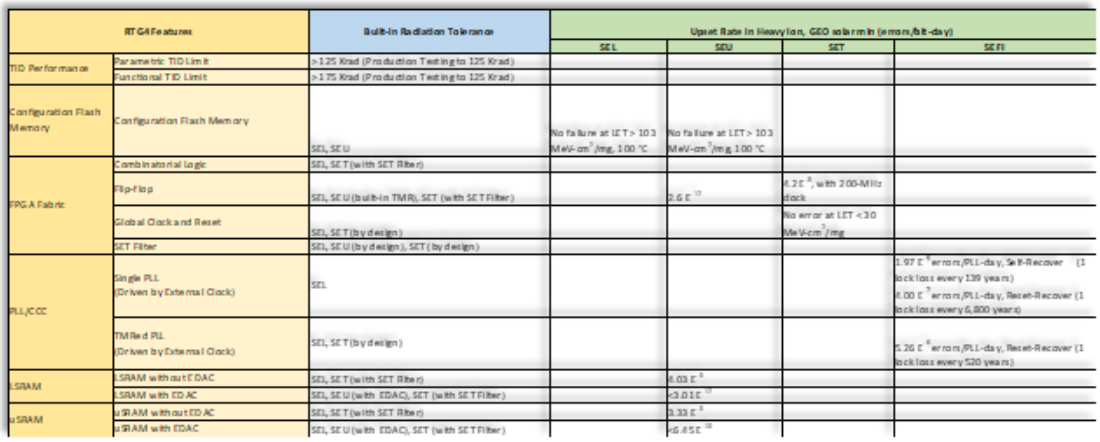
The following reports have recently been posted on our RT FPGAs Radiation and Reliability web page:

RTG4 SERDES Heavy Ion LBNL Report

RTG4 Proton DDR SERDES POR Programming UCD Report

RTG4 Radiation-Tolerant Features Summary

The RTG4 FPGAs radiation-tolerant features spreadsheet provides a summary of radiation performance for features and blocks available in the RTG4 radiation-tolerant FPGA. For radiation test details and results, please refer to the reference radiation reports on the RT FPGAs Radiation and Reliability webpage.



RTG4 Features		Built-In Radiation Tolerance	Upset Rate in Heavy Ion, GEO solar min (errors/bit-day)			
			SEL	SEU	SET	SEFI
TID Performance	Parametric TID Limit	>125 Krad (Production Testing to 125 Krad)				
	Functional TID Limit	>175 Krad (Production Testing to 125 Krad)				
Configuration Flash Memory	Configuration Flash Memory	SEL, SEU	No failure at LET > 103 MeV-cm²/mg, 100 °C	No failure at LET > 103 MeV-cm²/mg 100 °C		
FPGA Fabric	Combinatorial Logic	SEL, SET (with SET Filter)				
	Flip-Flop	SEL, SEU (built-in TMR), SET (with SET Filter)		2.6 E⁻¹⁵	4.2 E⁻⁸, with 200-MHz clock	
	Global Clock and Reset	SEL, SET (by design)			No error at LET <30 MeV-cm²/mg	
	SET Filter	SEL, SEU (by design), SET (by design)				
PLL/CCC	Single PLL (Driven by External Clock)	SEL				1.97 E⁻⁶ errors/PLL-day, Self-Recover (1 lock loss every 139 years) 8.00 E⁻⁷ errors/PLL-day, Reset-Recover (1 lock loss every 6,800 years)
	TMRed PLL (Driven by External Clock)	SEL, SET (by design)				5.26 E⁻⁶ errors/PLL-day, Reset-Recover (1 lock loss every 520 years)
LSRAM	LSRAM without EDAC	SEL, SET (with SET Filter)		8.03 E⁻⁵		
	LSRAM with EDAC	SEL, SEU (with EDAC), SET (with SET Filter)		<3.01 E⁻¹⁰		
uSRAM	uSRAM without EDAC	SEL, SET (with SET Filter)		3.33 E⁻⁴		
	uSRAM with EDAC	SEL, SEU (with EDAC), SET (with SET Filter)		<6.45 E⁻¹⁰		

Figure 3: RTG4™ FPGAs Radiation-Tolerant Features Summary

For further information, contact minh.nguyen@microchip.com

Floating Point Unit (CoreFPU) IP for RTG4 and RT PolarFire® FPGAs

We are delighted to introduce the Core Floating Point Unit (CoreFPU) IP for RTG4, PolarFire SoC and PolarFire FPGAs. This new IP core is designed for floating-point arithmetic and conversion operations for single-precision floating point numbers. CoreFPU supports fixed-point to floating-point and floating-point to fixed-point conversions and floating-point addition, subtraction and multiplication operations.

The Core Floating Point Unit (CoreFPU) IP supports the following features:

- Supports single-precision floating numbers per the IEEE® 754 standard
- Conversions
    - Fixed-point to floating-point conversion
    - Floating-point to fixed-point conversion
- Arithmetic operations
    - Floating point addition
    - Floating point subtraction
    - Floating point multiplication
- Provides flags for Overflow, Infinity, and Not-a-Number (NaN) for floating point numbers
- Fully pipelined implementation of arithmetic operations
- Provision to configure the core for design requirements

CoreFPU is not license locked and can be downloaded from the Libero® SoC Design Suite IP catalog on the web repository. Once it is listed in the catalog, the core can be instantiated using the SmartDesign flow.

After configuring and generating the core instance, you can simulate the basic functionality using the test bench supplied with the CoreFPU. The testbench parameters automatically adjust to the CoreFPU configuration. The CoreFPU can be instantiated as a component of a larger design.

For information on using SmartDesign to configure, connect, and generate cores, refer to the *Libero SoC Design Suite's online help.*

For further information, please contact:
Puneet.Kumar@microchip.com

Microchip's Early Access Program: High-Level Synthesis Targeting RT PolarFire FPGAs

High-Level Synthesis (**HLS**) is an FPGA design methodology that starts with a C++ software algorithmic description and generates an equivalent digital hardware block. We are excited to offer this new design methodology for RT PolarFire FPGAs.

FPGA design with C++ and LegUp HLS offers two to five times better design productivity when compared to designing in RTL. The resulting C++ code typically has five to ten times fewer lines of code than an equivalent RTL code design. HLS software-based verification and testing saves significant design effort compared to RTL verification. HLS also enables easier design space exploration and FPGA device portability.

The LegUp HLS compiler is an Eclipse-based Integrated Development Environment (IDE) that takes C++ software code as input and generates a SmartDesign IP component (Verilog HDL) that can be instantiated into the SmartDesign canvas available in the Libero SoC Design Suite to build an FPGA system.

We are running an Early Access Program (EAP) for the LegUp HLS compiler software targeting RT PolarFire FPGAs. This program enables you to evaluate a beta version of the LegUp HLS software and provide us with valuable feedback.

To participate in the early access program, please fill out the LegUp Software Request Form and we will contact you to support your evaluation. This program is primarily for users who have prior experience with other HLS software tools. To learn about our HLS tool, visit the LegUp HLS Compiler web page.

For further information, please contact: DivipalaBasava.Rajesh@microchip.com

RT PolarFire FPGA Single Event Latch-Up Report

Over the course of 2019 and 2020, our radiation effects team conducted a series of single event latch-up tests on RT PolarFire FPGAs. Tests were performed in heavy ions with linear energy transfer (LET) up to 80 MeV-cm^2/mg in facilities at Texas A&M University and Lawrence Berkeley National Laboratory. It was found that the single event latch-up threshold for RT PolarFire FPGAs exceeds 80 MeV-cm2/mg when operating with general-purpose I/Os configured for operation at 1.8V nominal. Details of the tests, including run logs and results, are documented in a new report which has been posted on the Microchip website.

For further information, contact Ken O'Neill: ken.oneill@microchip.com

LX7720 Rad-Hard-by-Design Motor Controller Achieves QML Certification

We are pleased to announce our radiation-hardened LX7720 motor controller with position sensing IC has achieved certification by the U.S. Defense Logistics Agency (DLA) and is listed on the Qualified Manufacturers List (QML) for both Class V and Q. These qualifications are vital for design-ins for many space programs and validate quality assurance and reliability of the device.

The LX7720 is used in various motor control applications such as space robotics and solar array or optical instruments positioning. It supports motor driver servo control, linear actuator servo control and driving stepper, Brushless Direct Current (BLDC), and Permanent-Magnet Synchronous (PMSM) motors.

The LX7720 is offered in a 132-pin ceramic quad flatpack as well as a 160-pin plastic quad flatpack. Ordering part numbers for the IC and development platform are:

Operating Temperature	Package Type	Package	Part Number	SMD Number	Flow
-55°C to 125°C	Hermetic Ceramic	CQFP 132L	LX7720MFQ-EV	5962-2120201VXC	MIL-PRF-38535 Class V
			LX7720MFQ-EQ	5962-2120201QXC	MIL-PRF-38535 Class Q
	Ceramic		LX7720-ES	-	Engineering Samples
	Plastic	QFP 160L	LX7720MLF	-	JEDEC
	Dev Board		LX7720-DB	-	Includes soldered LX7720-ES

Please visit the product web page, where you will find the updated data sheet cross-referencing the SMD numbers along with the latest radiation test results and conference papers. Check out our other mixed signal solutions for space.

Please contact dorian.johnson@microchip.com for more information.

SST38LF6401RT COTS Radiation-Tolerant 64 Mbit Parallel SuperFlash® Memory

We are now sampling a new radiation-tolerant device, a 64 Megabit (Mbit) parallel-interface SuperFlash memory device with unrivaled Total Ionizing Dose (TID) tolerance for maximum reliability and robustness in the harsh radiation environment of space missions. It is an ideal companion to our space-ready microcontrollers (MCUs), microprocessors (MPUs) and Field Programmable Gate Arrays (FPGAs). It offers the vital protection required by space systems for the most reliable digital processing where companion Flash memory is required to store the critical software code or bitstream that drives the complete system.

SST38LF6401RT is a 4M x16, radiation-tolerant device manufactured with our proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST38VF6401RT writes (Program or Erase) with a 3.0 to 3.6V power supply and conforms to JEDEC standard pinouts and command sets for x16 Flash memories.

Latch up immune and radiation-tolerant up to 50 kilorad (Krad) TID, even while the Flash is still biased and operating, the SST38LF6401RT device enables systems to operate in a broad range of space applications where they cannot afford any loss of code execution that could lead to severe defects and system loss. It is an ideal companion to our SAMRH71 Arm® Cortex®-M7-based radiation-hardened SoC processor and can also be used with RT PolarFire® and RTG4® FPGAs to support in-flight system reconfiguration. This COTS radiation-tolerant memory has pinout distribution compatibility with its industrial version for easy transition to the space-qualified plastic or ceramic versions at the Printed Circuit Board (PCB) level.

The SST38LF6401RT SuperFlash device is sampling now in a ceramic version and supported by an evaluation board and demonstration software, available upon request. Also available upon request is an FPGA flight programming reference case for combining the SuperFlash device with an FPGA and a SAMRH71 processor with supporting software. Voltage operation ranges from 3.0 to 3.6V .

- Ordering part number SST38LF6401RT Radiation-Tolerant 64 Mbit Parallel SuperFlash® Memory
  - SST38LF6401-90-RT/3YB-E Ceramic prototype

Ceramic-qualified flight models in QMLQ or QMLV equivalent flow are planned to be available before summer 2021. A “Hirel Plastic” qualified version is also planned in the same timeframe to support high-volume “New Space” demand.

Visit the SST38LF6401RT product page for additional information.

Please contact Nicolas.Ganry@microchip.com or Brian.Langedyk@microchip.com for more information.

Looking for the Correct Reference Clock to Drive ATmegaS128 Radiation-Tolerant Microcontrollers?

Application note AN3658 is located on our Hi-Rel Clock Oscillators web page. This application note lists the Vectron® high-reliability oscillator model numbers that have been characterized for use as the external clock for the ATmegaS128 series of radiation-tolerant microcontrollers. These oscillators are the only recommended external frequency sources for use as the ATmegaS128's external clock. While other suppliers may offer clocks that meet the specifications, they are not approved reference designs by Microchip, and, as such, you must complete your own qualification and analysis for fitness of use. Please find below the Vectron space-qualified clock oscillators that have been characterized and are recommended for use with ATmegaS128 microcontrollers.

The ATmegaS128 has five clock source options. This application note specifically addresses the external crystal oscillators that are recommended for use with the external clock. Two oscillator frequencies, 4 MHz and 8 MHz, are recommended in the application note, though any frequency below 8 MHz may be used per Table 30-3 of the ATmegaS128 data sheet. Four different reliability levels of the microcontroller are available. For each of these reliability levels, you need to ensure that the corresponding reliability level of the crystal oscillator is correctly specified to match the application. Eight individual oscillator model numbers are defined in Table 1 (one for each combination of frequency and reliability level). These oscillators are directly coupled to the XTAL1 pad.

The models chosen are the most cost-effective solutions that meet the requirements of ATmegaS128 and the required reliability level. The 1157 series oscillators recommended are from the Vectron Hi-Rel Oscillator standard OS-68338. All the devices listed are 3.3V, CMOS, surface mount, 7 mm × 5 mm, ceramic leadless chip carrier oscillators. The subsequent paragraphs after Table 1 are provided for reference and compliance purposes.

TABLE 1: RECOMMENDED VECTRON HIGH RELIABILITY OSCILLATOR MODELS AT TWO EXTERNAL CLOCK FREQUENCIES

MCU Model	Reliability Level	External Clock Frequency	Oscillator Model Number
ATmegaS128-ZC-E	Prototype (-E)	4 MHz	1157D4M00000BX
ATmegaS128-ZC-MQ	QML-Q equivalent	4 MHz	1157B4M00000BE
ATmegaS128-ZC-SV	QML-V equivalent	4 MHz	1157R4M00000BS
ATmegaS128-MD-HP	HiREL Plastic	4 MHz	1157C4M00000BB
ATmegaS128-ZC-E	Prototype (-E)	8 MHz	1157D8M00000BX
ATmegaS128-ZC-MQ	QML-Q equivalent	8 MHz	1157B8M00000BE
ATmegaS128-ZC-SV	QML-V equivalent	8 MHz	1157R8M00000BS
ATmegaS128-MD-HP	HiREL Plastic	8 MHz	1157C8M00000BB

Due to differences in the requirements listed in MIL-PRF-38535 (for radiation hardened electronics) and MIL-PRF 55310 (for crystal oscillators), exact matches in quality flow vs. screening levels and component pedigrees are not available. Table 2 summarizes available quality flows for the ATmegaS128 radiation-tolerant microcontroller and the recommended corresponding screening and pedigree levels for OS-68338 oscillators. We encourage you to review applicable specifications for mission-critical applications to ensure full compliance.

TABLE 2: ATMEGAS128 QUALITY FLOW REQUIREMENTS VS. OS-68338 OSCILLATOR SCREENING AND PEDIGREES

MCU Quality Flow	Oscillator Screening	Oscillator Component Pedigree	Description
Prototype (-E)	X	D	Engineering Model Hardware using high reliability design with commercial grade components and non-swept quartz.
QML-Q equivalent	E	B	Military Grade Hardware using high reliability design with military grade components and swept quartz.
QML-V equivalent	S	R	Space Grade Hardware with 100 kRad die, space grade components, and swept quartz.
Hirel Plastic (-HP)	B	C	Military grade die and plastic packaging. Oscillator use military grade components and non-swept quartz.

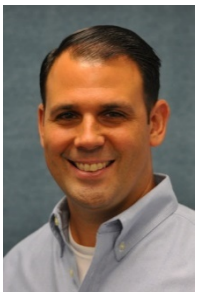
Electrical performance requirements for the external clock oscillator are defined in Table 30-3 and Table 30-2 of the ATmegaS128 data sheet. Additional requirements have been derived from customer use cases. These requirements are listed in Table 3, along with the corresponding electrical parameter specification from OS-68338.

TABLE 3: ELECTRICAL COMPLIANCE MATRIX FOR THE EXTERNAL CLOCK OSCILLATOR

Specification	ATmegaS128 Microcontroller Requirement	OS-68338 Oscillator Specification
Operating Temperature	–55°C to +125°C	–55°C to +125°C
20-year Total Stability (Note 1)	Not Defined	±100 ppm
Supply Voltage (V_S)	3.3VDC	3.3VDC
Supply Voltage Tolerance	±0.3VDC	±0.33VDC
Voltage Low Logic Min.	–0.5V	0V
Voltage Low Logic Max.	V_S x 0.1	V_S x 0.1
Voltage High Logic Min.	V_S x 0.7	V_S x 0.9
Voltage High Logic Max.	V_S + 0.5V	V_S
Duty Cycle	40% to 60%	45% to 55%
Rise and Fall Time Max.	1600 ns	5 ns
Total Ionized Dose	30 kRad	100 kRad
Single Event Latch-Up	62.5 MeV-cm^2/mg	120 MeV-cm^2/mg

Note 1: The ATmegaS128 data sheet does not specify a frequency stability requirement for the reference oscillators. The recommended oscillators in this application note will maintain a fractional frequency error of ±100 ppm under all conditions for a 20 year operational life. Table 4 provides details on the frequency budget. Note that while OS-68338 specification lists ±5 ppm for first-year aging, and ±2 ppm/year after year one, due to the logarithmic nature of the aging curves, oscillators will comply with ±31 ppm total aging over 20 years.

The OS-68338 oscillators listed in Table 1 have been characterized and are recommended for use as the external clock for the ATmegaS128 radiation-tolerant microprocessor. The oscillators meet all required performance parameters per the ATmegaS128 data sheet and expected use cases. The oscillators are rated to similar radiation levels as the microcontroller. Multiple alternate enclosure options are available, and alternate frequencies below 8 MHz can be provided.



For further information, please contact Scott Murphy, Space and Hi-Rel Product Line Manager at Microchip's Vectron Oscillator Products Division at scott.murphy@microchip.com.

Back to Basics: Understanding the Switching Power Converter Part 2: Topology and Transfer Function

In our last installment we discussed the front end of a switching power supply. We took a brief ride through Middlebrook stability criteria, ampacity, fusing, filtering and UVLO impact. In this second installment of that work, we will now continue up the power path to the topologies and transfer functions. To consider the large signal transfer function, we have to consider how the energy is stored and moved around in the circuit. This brief work will focus on mapping and analyzing the energy storage and transfer of many switching topologies.

I was once asked to train an elite group of analog IC designers on switching power supplies. These are the ladies and gents who designed the 32-bit references, the instrumentation amplifiers with 130 dB CMRR, op amps with incredible gain, bandwidth, noise and input offset performance. I knew this would be a daunting task. These are folks that can design a long-tail diff pair or a gilbert cell multiplier in seconds. What I chose to do was to take a different approach. I started with a simple buck converter. I asked the room about the parts.

"Well, that MOSFET needs to have really good linear mode SOA. Wait, hold on. Let's erase those MOSFETs and replace them with switches operating at D and 1-D."

"Why would that work? That has to be incredibly noisy!" the team responded.

"Bear with me," I said. "What then if we put this inductor in series with the output and then this capacitor?"

"Oh, gosh, the poles, the filtering—RESONANCE!" was the response.

Buck Converter

I continued, ”Hang on, let’s say we look at this differently? Where you want to see jwL and 1/jwC, let’s consider V = -Ldi/dt and then E = LI^2/2. When I close the high-side switch, I ramp up the current in the inductor as per V = -Ldi/dt. Energy is stored in that inductor as per E = LI^2/2. When I open the high-side switch, the low-side switch turns on. The inductor current then circulates and decays through the low-side switch and the parallel combination of the output capacitor and the load. I’m pumping energy from an inductor to a capacitor.”

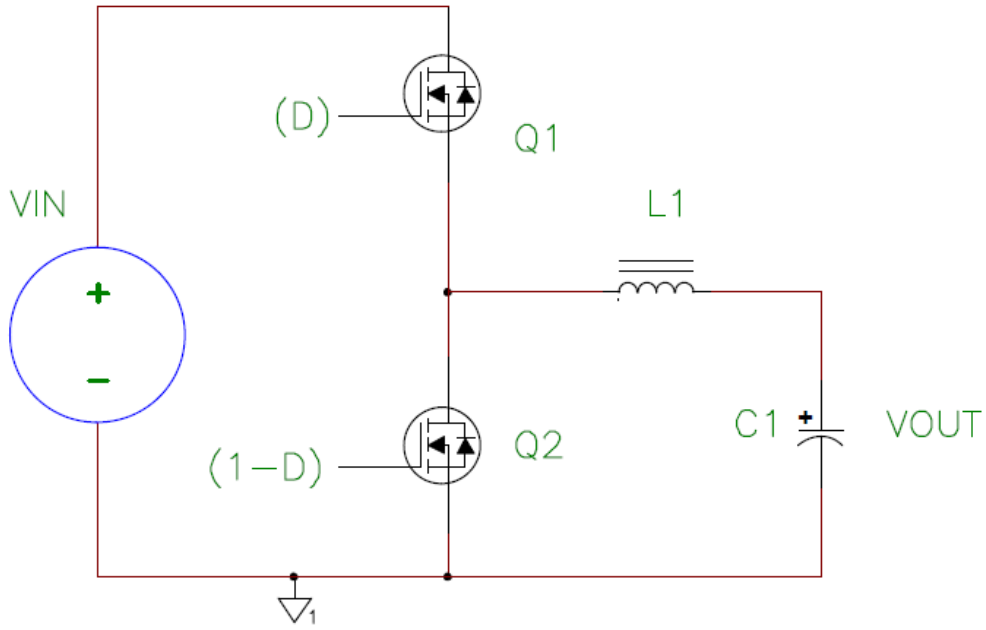


Figure 1: Buck Converter Power Train Schematic

This was the breakthrough! The response was amazing. I had easily a thousand years of hard core, DEEP-dive process, analog design, test engineering in front of me and I had piqued their interest with a silly four-node circuit.

“How does that inductor not saturate,” asked one of the very senior experts, not in a condescending way, but out of curiosity.

With this, I stopped the presentation, turned off my PC and went to the white board. “The volt time product across the inductor has to balance for it to stay out of saturation.” He looked more puzzled and curious. “Let’s set up a simple converter. Let’s say we have 10V input, 5V output and we are switching at 100 kHz. We know that the volt time product across the inductor in each state (driven and freewheel) has to balance to avoid saturation. Saturated inductor stores little energy and has little use here.”

His OK prompted me to continue. “OK, then, let’s lay that out as an equation:

D*(Vin-Vout)=(1-D)*Vout

This converter can deliver an output voltage less than that of the input voltage. What then is the transfer function of the converter with respect to duty cycle? We can rearrange such that D=Vout/Vin. This is the transfer function of the buck converter in simplest form.”

The room had never seen this before, but at the same time I was standing in front of at least a thousand years of analog experience—folks that could chase phase noise down to −160 dB or so.
Let’s then complete the idea. We had 10V input, 5V output, switching at 100 kHz. We know that the high side switch is on for 5 us, the lowside is on for 5 us. We haven’t talked about deadtime, body diode conduction, reverse recovery or any of that stuff yet, but let’s go to the load.

The load is 2A. Is it possible that the inductor can be in continuous conduction mode to deliver this 2A? Sure. We have to consider V = -Ldi/dt. For the charge state, V = Vin-Vout, di is the ripple current, for continuous conduction mode the ripple current is much less than 2A, dt is the interval, or 5us. By this, the CCM inductor can be calculated:

Lccm>>V*dt/di or Lccm>>12.5uH

But in terms of energy storage can this inductor source enough energy to the output to regulate? If we check, with E=LI^2/2, we get a stored energy of E>>(12.5 uH*2A^2)/2 or E>>25 uJ stored in the inductor, discharged at a rate of 100 kHz to deliver 2.5W. Yes, a CCM inductor can deliver enough energy to support the output.

But what then if we drop the inductor value substantially? At some point the inductor current discharges completely into the load before the discharge cycle is over. This is called Discontinuous Conduction Mode or DCM. For this to deliver 2A to the load the peak current in the inductor has to be much larger than 2A. The constraints to achieve DCM are converse to CCM:

Ldcm<<V*dt/di or Ldcm<<12.5uH

Clearly the higher currents in DCM will store enough energy to hold up the load.
In terms of voltage stresses on the power switches, both the charge cycle power switch (shown operating at D) and the discharge cycle power switch have to block the full maximum input voltage.
Then there are the caveats to the buck converter like deadtime, switching loss and freewheel path considerations, diode emulations mode, pre-bias startup. This work need not get into that, but I’ll gladly answer any questions on the matter.

Boost Converter

These energy storage elements can be rearranged a few different ways. The very same analysis can be applied to each of them to determine the transfer function. For the boost converter, we rearrange the energy storage elements by putting the inductor in series with the input. D is the duty cycle of the low-side power switch, 1-D is the duty cycle of the freewheel switch.

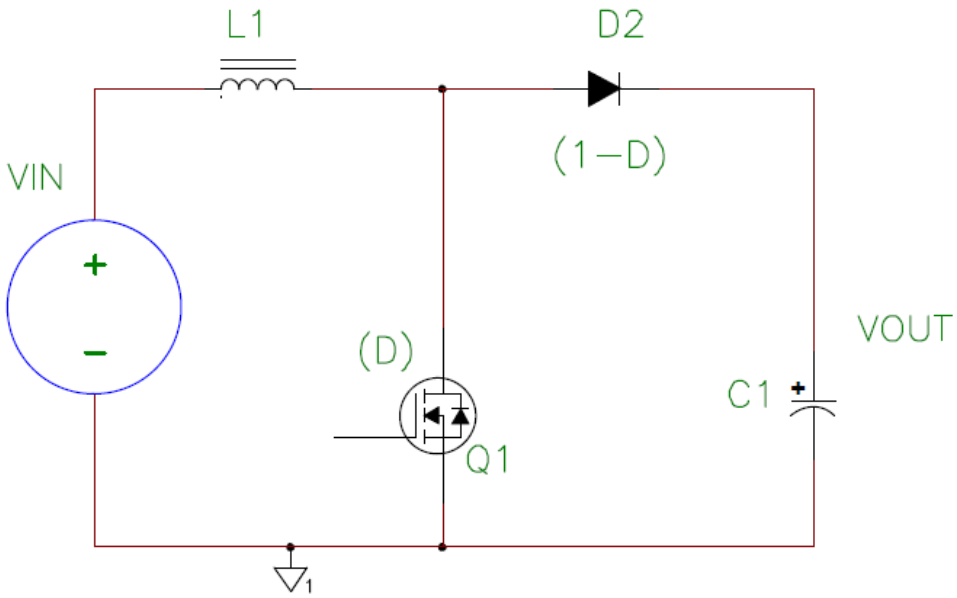


Figure 2: Boost Converter Power Train Schematic

If we apply the same volt*time equations for the inductor, during the charge cycle and discharge cycle, we get D*Vin=(1-D)(Vout-Vin), which reduces to Vout/Vin=1/(1-D). This converter can deliver an output voltage that is greater than the input voltage.

Flyback

The flyback converter also places the power switch in series with the inductor, but the positions are reversed. The power switch ties to the input source, the inductor terminates to return. This arrangement allows for the delivery of a negative output voltage with a positive input voltage. The volt*time product of the charge cycle of the inductor is the same as the boost: D*Vin.

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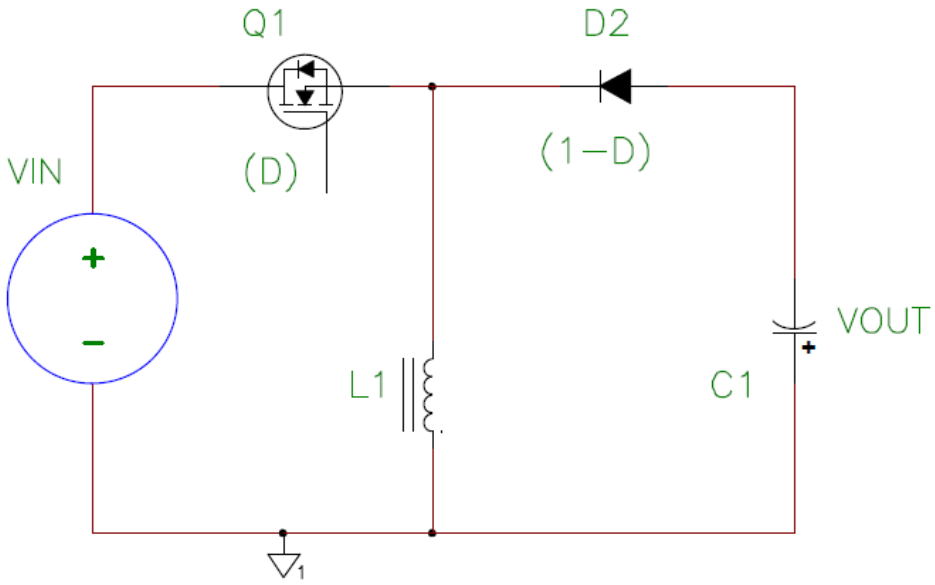

Figure 3: Flyback Power Train Schematic

The discharge cycle is slightly different in that it inverts. The feewheel cycle is then (1-D)*(-Vout).

If we set the two equal and reduce, we get Vout/Vin=-D/(1-D). This converter can deliver a negative output having a magnitude that is less than, equal to or greater than the magnitude of the input voltage.

Isolated Flyback

For the isolated flyback, a transformer is added to provide galvanic isolation between the output and the input.

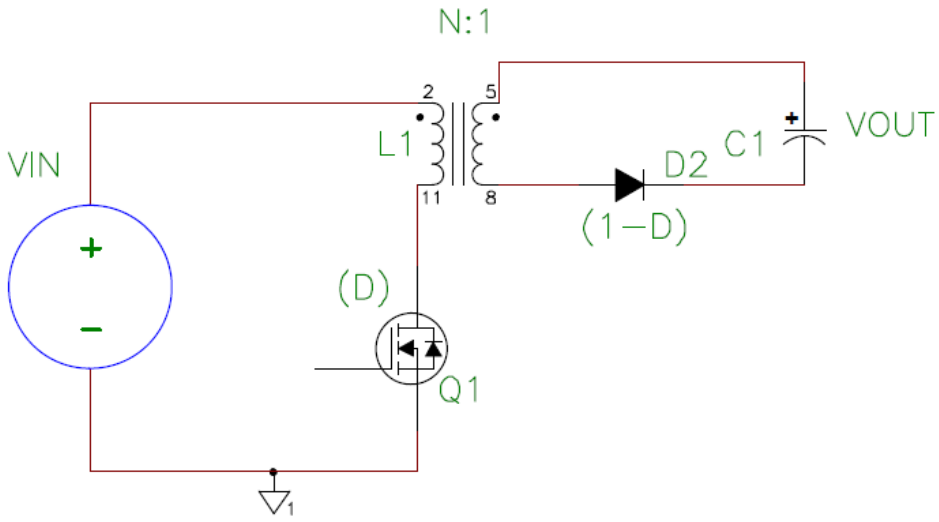

Figure 4: Isolated Flyback Power Train Schematic

The primary inductance of the transformer is the energy storage element. If the turns ratio of the transformer is primary/secondary = N/1, the volt time product on the primary and secondary can be analyzed as D*Vin=(1-D)(Vout*N) or Vout/Vin=D/N(1-D).

Conclusion

What started out as a horrifying task of training a room full of analog experts on power ended with long-term relationships and product definitions. Along those same lines, Microchip has many power solutions for space comprised of

- Rad-hard MOSFETs
- Linear ICs including PWM, supervisor, reference
- Linear regulators
- Switching POL converters
- Isolated switching DC to DC converters
- Discrete small signal and power transistors, diodes, Schottkies

Basic analysis of how the energy is transferred in a switching power converter is a powerful tool. Clearly these techniques can be expanded to cover topologies like SEPIC, Buck-Boost, Cuk, Forward, Half Bridge, Full Bridge and many others. When validating these converters on the bench, it's important to keep these relationships at hand and understand the commutation and current flow.

Stay tuned for a discussion of power supply control loops, control methods and caveats in part three of this series in our next installment. May your electrons continue to flow as intended.

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