



[Newsletter Archive](#) | [Feedback](#)

Edition 30: November 2020

Welcome to Edition 30 of Microchip's Space Brief newsletter. Written for design engineers and design managers, system engineers and system architects, component engineers, radiation effects scientists and program managers in the space industry, Space Brief is a quarterly newsletter in which we aim to bring you the latest news about our radiation-tolerant and radiation-hardened products. Space Brief provides information about new products, updates on qualification and radiation testing, links to formal customer notifications, and news about workshops and conferences at which Microchip will be presenting or exhibiting.

Please forward Space Brief to your colleagues, and let them know they can register to receive this newsletter directly to their email inbox every three months by clicking [here](#).

Table of Contents

- RTG4™ CQFP-352 FPGAs Have Achieved QML Class V Qualification
- RTG4 Sub-QML FPGAs in Plastic Package
- Introducing Mechanical Samples for RT FPGAs in CQFP Packages
- Integrated Joint Microchip Space Webinar with ASIC Design Services
- Joint Webinar Microchip RT FPGAs and 3D Plus
- FPGA Software Static Timing Analysis Customer Notification
- Space-Qualified Radiation-Tolerant Ethernet SAM3X8ERT MCU and VSC8540RT and VSC8541RT PHY Devices
- Looking for the Correct Reference Clock to Drive VSC8540RT and VSC8541RT Ethernet Transceivers?
- Rad-Hard LX7720 Motor Control IC with Position Sensing Moves to QML Class V Production
- LX7714 Radiation Hard Quad Power Switch Array - New Datasheet Available
- Back to Basics: Understanding the Switching Power Converter Part 1: The Input

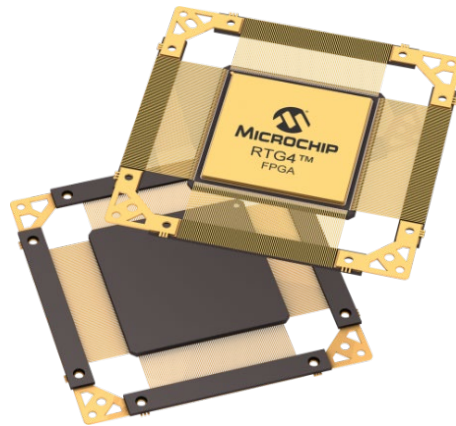
PRODUCT NEWS

RTG4™ FPGAs in CQFP-352 Package Have Achieved QML Class V Qualification

We are delighted to announce RTG4 FPGAs in the 352-pin ceramic quad flat pack (CQFP package) have achieved QML Class V qualification, the highest reliability standard for space integrated circuits, in October 2020. RTG4 FPGAs in the CQ352 package provide a more cost-effective integration than higher-pin-count packages. CQFP is the industry-standard package for space applications with its well-established board integration and inspection procedures. The RTG4 device in the CQ352 package is immediately available in the Libero® SoC software tool set, allowing you to design with this new device-package combination. We recommend you download the latest version of Libero SoC Design Suite to take advantage of these recent RTG4 FPGA product family updates. The latest RTG4 FPGA product brief has also been updated to include the RTG4 CQ352 FPGA.

[SMD part numbers](#) are as follows:

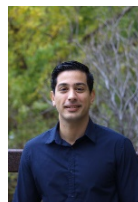
RT4G150-CQ352E	5962-1620822QYC
RT4G150-1CQ352E	5962-1620823QYC
RT4G150L-CQ352E	5962-1620824QYC
RT4G150-CQ352V	5962-1620825VYC
RT4G150-1CQ352V	5962-1620826VYC
RT4G150L-CQ352V	5962-1620827VYC



Please reach out to your local Microchip sales team if you have a need for QML class V FPGAs, or contact Microchip's space marketing team:



Ken O'Neill, Director of Marketing, Space and Aviation:
Ken.ONeill@microchip.com



Julian Di Matteo, Senior Engineer, Product Marketing, Space and Aviation:
Julian.DiMatteo@microchip.com



Minh Nguyen, Principal Engineer, Product Marketing, Space and Aviation:
Minh.Nguyen@microchip.com

RTG4™ Sub-QML FPGAs in Plastic Package

We recently introduced our [Sub-QML FPGAs](#) that combine the radiation tolerance of QML components with our spaceflight heritage that permits lower screening requirements to provide lower costs and shorter lead times for demanding space missions. Because Sub-QML FPGAs are radiation-tolerant without full QML screening, these products meet very high standards for reliability and radiation protection. Although Sub-QML FPGA options are available for all our RT FPGA families, [RTG4 FPGAs](#) have the most screening flow options. The lowest-cost option is RTG4 FPGAs in the 1657 ball grid array plastic package, which is well suited for small satellite or constellation applications.

Flow	Purpose	Package	Qualification	Screening			
				Burn-In	Temp Test	Life Test	DPA
V	NSS, NASA Class1	Hermetic Ceramic	QML-V	Static Dynamic	-55°C – 125°C	Wafer-Lot	Assy Lot
E	Advanced Traditional Space	Hermetic Ceramic	QML-Q	Static Dynamic	-55°C – 125°C	Generic Group C	Optional
B	Entry Level Traditional Space	Hermetic Ceramic	QML-Q	Dynamic	-55°C – 125°C	Generic Group C	None
R	New Space, Strategic Programs	Hermetic Ceramic	MIL-STD-883 Class B	Dynamic	-55°C – 125°C	None	None
Mil Ceramic	New Space, Strategic Programs	Hermetic Ceramic	MIL-STD-883 Class B	None	-55°C – 125°C	None	None
PROTO	Prototyping	Ceramic (Hermeticity not Guaranteed)	MIL-STD-883 Class B	None	-55°C – 125°C	None	None
Mil Plastic	New Space, Strategic Programs	Plastic Non-Hermetic	JEDEC	None	-55°C – 125°C	None	None

Figure 1: RTG4™ FPGA Screening Flows

The RTG4 FPGA Sub-QML plastic package is currently going through JEDEC qualification following JESD-47 guidelines. The qualification of the RTG4 FPGA plastic package is targeted for completion by early 2021. Once completed, RTG4 Sub-QML FPGAs will be offered in both lead solder (FC1657) and lead-free solder (FCG1657) package options. The flight units will be screened to the full military temperature range (–55°C to 125°C). Prototyping units, which are also tested to the full military temperature range and available in small quantities, will also be offered. The RTG4 FPGA plastic daisy chain package will also be available to help facilitate the qualification of the package board assembly practices without using flight-quality parts.

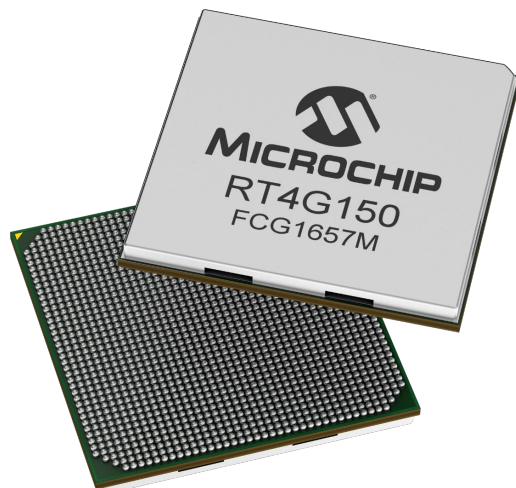


Figure 2: RTG4™ Sub-QML FPGAs in Plastic Package

Here are the reference RTG4 FPGA Plastic documents:

[RTG4 FPGA Plastic Product Brief](#)

[RTG4 FPGA Datasheet Including Plastic Package](#)

[RTG4 FPGA Package Drawing](#), [Pin Assignment Table](#) and [Daisy Chain Package](#)

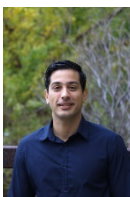
[Sub-QML Screening Flow](#)

Please reach out to your local Microchip sales team if you have a need for Sub-QML FPGAs, or radiation-tolerant FPGAs in higher volume and at lower cost than traditional space applications.



Ken O'Neill, Associate Director
of Marketing, Space and
Aviation:

Ken.ONeill@microchip.com



Julian Di Matteo, Senior Engineer,
Product Marketing, Space and
Aviation:

Julian.DiMatteo@microchip.com



Minh Nguyen,
Principal Engineer, Product Marketing, Space
and Aviation:

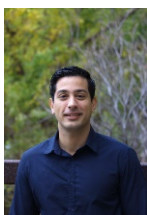
Minh.Nguyen@microchip.com

Introducing Mechanical Samples for RT FPGAs in CQFP Packages

We are planning to support mechanical samples of the Ceramic Quad Flat Packages (CQFP) we use for our radiation-tolerant FPGAs. This will enable you to evaluate our packages in your production set-up, such as practicing board assembly and inspection and package lead trim and form. Our tentative schedule is to support the mechanical samples in early 2021.

Mech Sample Part #	Package	Heat-Sink	Device Family*	Device Name
MECH-SAMPLE-CQ84	CQ84		RTSX-SU	RTSX32SU
MECH-SAMPLE-CQ208NHS	CQ208		RTSX-SU, RTAX	RTSX32SU
				RTAX250S
MECH-SMAPLE-CQ208HS	CQ208	Yes	RTSX72SU	RTSX72U
MECH-SAMPLE-CQ256NHS	CQ256		RTSX-SU,RTAX, RT3P	RTSX32SU
				RTAX2000S
				RT3PE600L
				RT3PE3000L
MECH-SAMPLE-CQ256HS	CQ256	Yes	RTSX72SU	RTSX72SU
MECH-SAMPLE-CQ352TB	CQ352		RTAX	RTAX250S
				RTAX1000S
				RTAX2000S
				RTAX4000S
				RTAX2000D
				RTAX4000D
MECH-SAMPLE-CQ352BB	CQ352		RTG4	RT4G150

*Please note that each mechanical sample part number may support multiple device families. Each part number will have the same package body size as the device families listed but, the lid size may be different. We chose the largest lid size for each package that supports multiple device families.



For further information, contact Julian Di Matteo, Sr. Product Marketing Engineer, Space and Aviation, FPGA Group. Julian.DiMatteo@microchip.com

Integrated Joint Microchip Space Webinar with ASIC Design Services

Microchip's RT FPGAs bring together 60 years of space flight heritage and the industry's lowest-power FPGA family to enable new capabilities for space applications. Our radiation-tolerant RT PolarFire® FPGAs enable higher computing and connectivity throughput for mission-critical systems at 40 to 50% lower power than competing SRAM FPGAs while delivering greater immunity to configuration Single Event Upsets (SEUs).

In collaboration with our partner, ASIC Design Services, we have introduced Deep Learning solutions and a Core Deep Learning (CDL) IP Framework. The CDL Framework is a scalable and flexible Convolutional Neural Network (CNN) solution that allows your trained Machine Learning (ML) inference engine to be run in RT FPGAs.

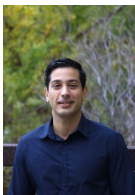
CDL accelerates a wide range of layers typically associated with CNNs. The configurable nature, small real estate and low-power properties of RTG4 and RT PolarFire FPGAs allow for computationally expensive CNNs to be moved to the node. CDL can be scaled to fit into an RT FPGA design to meet your unique requirements. Its key features include:

- Support for TensorFlow and Caffe Framework
- Full pipeline from the convolutional neural network to FPGA implementation
- Network quantization for memory footprint minimization
- Support for different network layers:
 - Convolution
 - Depthwise separable
 - Concatenation
 - Pooling
 - Activation
 - Fully connected
 - Batch normalization
 - Residual layer

Do You Want to Learn How to Accelerate Your AI/ML Design with Our RT FPGAs?

We are scheduling an upcoming webinar with our partner ASIC Design Services (ADS) where you will learn about the integrated Core Deep Learning (CDL) Framework solution that allows your trained ML inference engine to be run on Microchip RT FPGAs

Stay tuned!



For further information, please contact Julian.DiMatteo@microchip.com and Puneet.Kumar@microchip.com

Joint Webinar Showcasing Microchip RT FPGAs and 3D Plus RT DDR Memories

RTG4™ and RT PolarFire FPGAs bring together 60 years of space flight heritage and the industry's lowest power FPGA family to enable new capabilities for space applications.

With up to 480K logic elements, 33 Mbits of embedded SRAM, 1480 DSP blocks, and 24 lanes of 10 Gbps transceivers, our next generation radiation-tolerant FPGA enables higher computing and connectivity throughput for mission-critical systems at 40 to 50% lower power than competing SRAM FPGAs while delivering greater immunity to configuration Single Event Upsets (SEUs) and maintaining the resistance to radiation-induced configuration upsets in the harshest radiation environments, such as space flight (LEO, MEO, GEO, HEO, deep space); high altitude aviation, medical electronics, and nuclear power plant control. No background scrubbing or reconfiguration of the FPGA is needed in order to mitigate changes in configuration due to radiation effects.

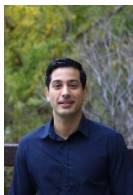
3D Plus is a world leader in providing high-density 3D microelectronics products in a small form factor to meet the high-reliability and high-performance requirements of current and future electronic systems that are used in aerospace and defense, industrial and medical applications. 3D Plus offers a full line up of radiation-tolerant memories that offer state-of-the art stacking technology. These devices feature:

- High performance, high density, high speed and excellent signal integrity
- High reliability to extremely harsh environments and space applications
- Small form factor
- Space qualification and extensive flight heritage

Want to accelerate our design with space qualified DDR memories with Microchip RT FPGAs?

If you would like to learn how to accelerate your design with 3D Plus' space-qualified DDR memories and our RT FPGAs, we are scheduling an upcoming joint webinar where engineers from Microchip and 3D Plus will demonstrate the benefits and advantages of integrating radiation-tolerant DDR memories with our RT FPGAs.

Stay tuned!



For further information, please contact Julian.DiMatteo@microchip.com and Puneet.Kumar@microchip.com

FPGA Software Static Timing Analysis Customer Notification (CN)

[Customer Notification \(CN\) 20022](#) has been released to inform customers that ongoing software quality testing on Libero® SoC Design Suite has found a Static Timing Analysis coverage issue for specific scenarios for SmartFusion® 2, IGLOO® 2, RTG4 and PolarFire® FPGA product families.

Space-Qualified Radiation-Tolerant Ethernet MCU and PHY Devices

To support the growing demand for Ethernet connectivity in space and high reliability applications, we have completed QML-equivalent qualification for three new rad-tolerant devices:

- [VSC8540RT Ethernet Transceiver](#), 100 Mbps version, and
- [VSC8541RT Ethernet Transceiver](#), 1 Gbps version
- [SAM3X8ERT](#), a space-qualified Arm® Cortex®-M3 based microcontroller (MCU) with an embedded Ethernet controller

Ethernet is being used more frequently in space applications. This connectivity technology is chosen for most human flight missions, such as Deep Space Gateway which is an international spaceport program for human and robotic exploration to the Moon and beyond.

With these devices, Microchip extends its Radiation-Tolerant portfolio. The combination of an Ethernet transceiver with a MCU that includes an Ethernet controller and FPGAs featuring Ethernet IP creates a total system solution for using Ethernet in space applications.

The VSC8540RT and VSC8541RT Ethernet transceivers are immune to radiation-induced Single Event Latch-up (SEL) to LET 78 MeV-cm²/mg, and the SAM3X8ERT MCU is immune to SEL to LET 62 MeV-cm²/mg.

Regarding Total Ionizing Dose (TID), VSC8540RT and VSC8541T transceivers are qualified up to 100 Krad and the SAM3X8ERT MCU is qualified up to 30 Krad.

Final and full radiation reports are available for the VSC8540RT, VSC8541RT and SAM3X8ERT, including TID qualification results and complete Single Event Effect (SEE) characterization for all functional blocks. Some applications notes are also available to help with system mitigation techniques when needed. Products data sheets and applications notes are available on the product web pages. Radiation report are available on request. Please contact your local Microchip sales organization.

The VSC8540RT, VSC8541RT and SAM3X8ERT are available in ceramic packages and are now qualified at space-grade levels equivalent to QML class Q and QML class V. Full qualification and release to production activities have been completed. You can now order the following MQ and SV flight models with a qualification data package. This package includes screening description, electrical data, Wafer Lot Acceptance (WLA), Scanning Electron Microscopy (SEM) and qualification certificates. For hermetic devices, the data package also includes pre-encapsulation report, Particle Impact Noise Detection (PIND) test report and final source inspection report.

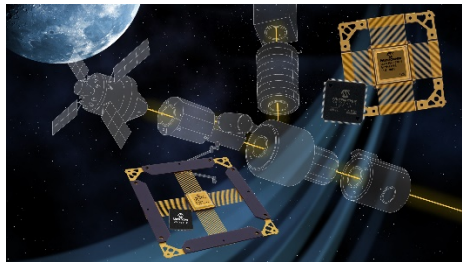
- Ordering part number SAM3X8ERT Arm Cortex-M3 Based Radiation Tolerant MCU
 - SAM3X8ERT-DHB-E Ceramic prototype
 - SAM3X8ERT-DHB-MQ Ceramic qualified flight model QML class Q equivalent
 - SAM3X8ERT-DHB-SV Ceramic qualified flight model QML class V equivalent
- Ordering part number VSC8540RT Radiation-Tolerant 100 Mbps Ethernet transceiver
 - VSC8540WZBRT-E Ceramic prototype
 - VSC8540WZBRT-MQ Ceramic qualified flight model QML class Q equivalent
 - VSC8540WZBRT-SV Ceramic qualified flight model QML class V equivalent

- Ordering part number VSC8541RT Radiation-Tolerant 1 Gbps Ethernet transceiver
 - VSC8541WZBRT-E Ceramic prototype
 - VSC8541WZBRT-MQ Ceramic qualified flight model QML class Q equivalent
 - VSC8541WZBRT-SV Ceramic qualified flight model QML class V equivalent

Those devices are also available with a Hi-Rel Plastic qualification flow to support volume programs

- SAM3X8ERT-H8X-HP Hi-Rel Plastic qualified flight model
- VSC8540XMVRT-HP Hi-Rel Plastic qualified flight model
- VSC8541XMVRT-HP Hi-Rel Plastic qualified flight model

Visit our [Aerospace and Defense](#) design center for more information. Please contact nicolas.ganry@microchip.com for more information.



Looking for the Correct Reference Clock to Drive VSC8540RT and VSC8541RT Ethernet Transceivers?

Our application note AN3503 was revised in September 2020 and is located at <https://www.vectron.com/products/space/space.htm>. This application note lists the Vectron high-reliability clock source specifications and the custom part numbers that have been characterized for use as reference clocks (REFCLK) for the VSC8540RT and VSC8541RT radiation-tolerant Ethernet PHYs. These clocks are the only recommended frequency sources for use with the VSC854(x)RT PHYs. Other suppliers may offer clocks that meet the specifications, but they are not the approved devices used in our reference designs. You must complete your own qualification and analysis for fitness of use if an alternate supplier's oscillator is chosen. Please find below the Vectron space-qualified clock oscillators that have been characterized and are recommended for use with VSC854(x)RT REFCLK receivers.

The VSC854(x)RT series has an on-chip oscillator that may be used by connecting a 25 MHz crystal across the Xtal1/Xtal2 pins or by connecting a CMOS clock oscillator to the Xtal1 pin. AN3503 specifically addresses the CMOS clock oscillators. The requirements are detailed in paragraph 8.4.1 of the VSC854(x)RT datasheet. The PHY is compatible with 25 MHz, 50 MHz, or 125 MHz frequencies. Four different PHY reliability options are available. For each of these reliability levels, you must ensure that the corresponding reliability level of the REFCLK is correctly specified to match the application. Twelve individual oscillator model numbers are defined in Table 1-1 (one for each combination of frequency and reliability level).

Table 1-1. Recommended Vectron® High-Reliability Oscillator Models at Three Primary Reference Clock Frequencies

PHY Model	Reliability Model	REFCLK Frequency (MHz)	Oscillator Specification ¹	Oscillator Model Number ¹	Oscillator Supply Voltage (V)	Termination Circuit
VSC854(x)WZBRT-E	Prototype (-E)	25	OS-68338/PX-709	PX-709-0025-25M0000000	3.3	Figure 1-1
VSC854(x)WZBRT-MQ	QML-Q	25	OS-68338/PX-709	PX-709-0026-25M0000000	3.3	Figure 1-1
VSC854(x)WZBRT-SV	QML-V	25	OS-68338/PX-709	PX-709-0027-25M0000000	3.3	Figure 1-1
VSC854(x)XMVRT-HP	Hirel Plastic (-HP)	25	OS-68338/PX-709	PX-709-0028-25M0000000	3.3	Figure 1-1
VSC854(x)WZBRT-E	Prototype (-E)	50	OS-68338/PX-709	PX-709-0029-50M0000000	3.3	Figure 1-1
VSC854(x)WZBRT-MQ	QML-Q	50	OS-68338/PX-709	PX-709-0030-50M0000000	3.3	Figure 1-1
VSC854(x)WZBRT-SV	QML-V	50	OS-68338/PX-709	PX-709-0031-50M0000000	3.3	Figure 1-1
VSC854(x)XMVRT-HP	Hirel Plastic (-HP)	50	OS-68338/PX-709	PX-709-0032-50M0000000	3.3	Figure 1-1
VSC854(x)WZBRT-E	Prototype (-E)	125	DOC204900/PX-489	PX-489-0059-125M0000000	2.5	Directly coupled
VSC854(x)WZBRT-MQ	QML-Q	125	DOC204900/PX-489	PX-489-0060-125M0000000	2.5	Directly coupled
VSC854(x)WZBRT-SV	QML-V	125	DOC204900/PX-489	PX-489-0061-125M0000000	2.5	Directly coupled
VSC854(x)XMVRT-HP	Hirel Plastic (-HP)	125	DOC204900/PX-489	PX-489-0062-125M0000000	2.5	Directly coupled

Note: 1. The PX-709 models listed in Table 1-1 are customized versions of the 1157 series oscillators from the OS-68338 specification. The PX-489 models are customized versions of the 1403 series oscillators from the DOC204900 specification.

The models chosen are the smallest and most cost-effective solutions that meet the requirements of paragraph 8.4.1 of the VSC854(x)RT data sheet and the required reliability level. These oscillators are custom part numbers that have minor design or test modifications from standard OS-68338 or DOC204900 oscillators. The modifications were required to be compliant with the REFCLK requirements. Table 1-2 provides the definition of these part numbers. The listed PX-709 series oscillators require the termination circuit of Figure 1-1 to be placed between the oscillator and the VSC854(x)RT. The resistor values recommended for use are: R1 = 220Ω ±5% and R2 = 75Ω ±5%. These values differ from those listed in VSC854(x)RT but ensure the full compliance to the specified REFCLK input specifications. The PX-489 series oscillators may be directly coupled to the REFCLK input.



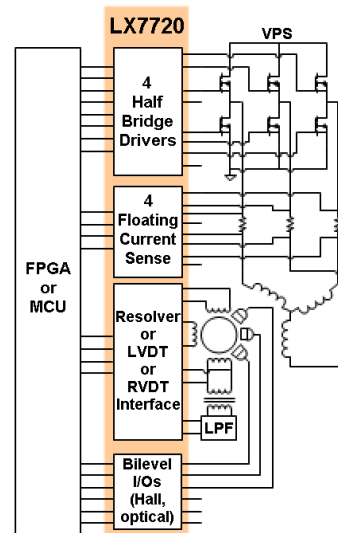
For further information, please contact Scott Murphy, Space and Hi-Rel Product Line Manager at Microchip's Vectron Oscillator Products Division at scott.murphy@microchip.com

Radiation-Hard LX7720 Motor Control IC with Position Sensing Moves to QML Class V Production

The LX7720 Motor Control IC for space applications has successfully completed all qualification requirements for the MIL-PRF-38535 Class V flow. The device is radiation hardened by design and integrates many circuit elements that until now were implemented discretely, thus offering a tremendous savings in board space and weight and a significant increase in reliability.

LX7720 Key Features:

- Four half-bridge N-channel MOSFET drivers
- Four floating differential current sensors
- Pulse modulated resolver transformer driver
- Three differential resolver sense inputs
- Six bi-level logic inputs
- Fault detection
- Supports both PMSM and Stepper motors
- Radiation-tolerance: 100 krad TID, 50krad ELDRS, and single event immune
- Packaged in a 132-pin hermetic CQFP and in a 208 pin plastic QFP with reduced screening



The LX7720 operates as a motor interface in conjunction with Microchip radiation-hard MOSFETs and the user's choice of either an FPGA or MCU device. Evaluation platforms are offered for both. The QML class Q flow product completed qualification and was released to production in November 2019. With all qualifications complete, we are seeking QML certification for both flows with the Defense Logistics Agency (DLA).

For information on the LX7720 and other mixed signal ICs for space, visit our [Radiation-Hardened Mixed-Signal ICs](#) page on our website.



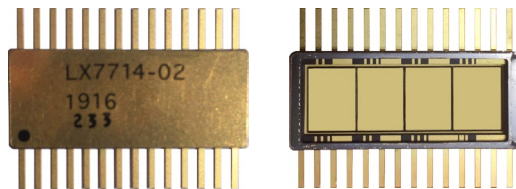
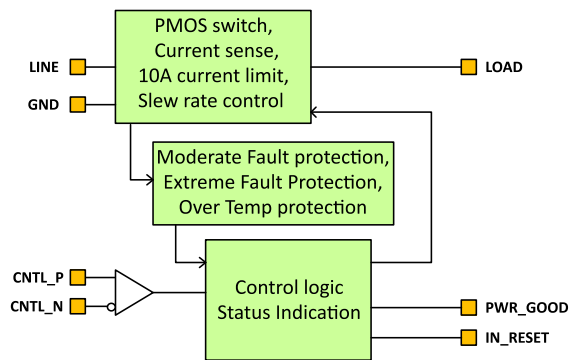
Please contact dorian.johnson@microchip.com for more information.

LX7714 Radiation Hard Quad Power Switch Array - New Data Sheet Available

The new LX7714 data sheet includes comprehensive updates to package drawings and thermal properties, ordering information and pin descriptions. The LX7714 is a quad power switch with line protection that is radiation-hardened by design and is used for spacecraft power distribution. It provides a means to turn on and off four independent DC loads with continuous currents up to 2.5A. There are four independent protected power switch sections per device with each capable of driving a load up to 1.25A or 2.5A, depending on the user's preference.

LX7714 Features:

- Four internal 2.5A or 1.25A rated power switches; power switches can be paralleled up to 10A
- Switches voltages to 46V
- Built-in fuse-like I^2t current limiting
- Safe management of soft overload faults
- Automatic hiccup retry timer to clear faults
- Power Good and Fault status outputs
- Differential on and off control inputs
- Low-power switch voltage drop
- Over temperature shutdown
- Load current slew rate control
- Small hermetic 28 lead ceramic flatpack package
- Radiation tolerant: 100 krad TID, 50 krad ELDRS and single event immune



Please contact dorian.johnson@microchip.com for more information.

Back to Basics: Understanding the Switching Power Converter Part 1: The Input

Is it possible that the engineer or team designing the power supply is either new to the game or perhaps from a software background or some other discipline outside of power electronics? It's not impossible, therefore, it will surely happen. The power burden may well have been assigned or delegated. It's also conceivable that the "old power expert" moved on leaving a hole in the org chart that was shored-up by necessity and urgency.

In an environment like this, a little knowledge can go a long way. This series will provide a brief overview of how the power supply works and how to make power related decisions without guesswork. The first part of this series is on the front end of the power supply. It will explore the input impedance of the converter, Middlebrook stability criteria, front end design, filter design, ampacity, fusing and Undervoltage Lockout (UVLO). Subsequent installments of this series will include a power train discussion including switching and transfer function, the output stage of the power supply, control and interface.

Middlebrook Stability Criteria

I was working on a large telecom rectifier design many moons ago and I had a colleague ask me, "So what's the big deal with all of this switching power supply stuff anyway?" He was a software engineer wholeheartedly dedicated to the "ones and zeros" by his own introduction. I decided to show him.

I had many things running on the bench including a linear regulator delivering about 10W and a DC to DC converter delivering about 10 KW. Taking some efficiency measurements, I showed that the efficiency of the linear regulator was basically V_{out}/V_{in} with some added loss for quiescent current. I went to the benchtop power supply feeding the linear regulator and turned the voltage up. The current stayed the same. Then I went to the LARGE power supply that was supplying the 10KW prototype. I turned the voltage up and the current dropped. Then I turned the voltage down and the current went up. I computed the efficiency as the software engineer freaked out. "That's NEGATIVE INPUT impedance---you can't control that, it MUST be unstable!" And yet the prototype was working right along, delivering 10 KW to a massive resistor bank that I had assembled. But the interaction was memorable. He saw that an incremental change in input voltage caused a negative incremental change in input current and vice versa. While the converter was doing real work, the incremental input impedance to the converter was negative. This drove me to a couple of additional experiments. What I found was that when I put enough series resistance in line with the input power supply, my converter was in fact hopelessly unstable. The instability was beyond anything that my PID loop and feedforward could compensate and the whole thing would bounce into and out of UVLO until I dropped the load. But with a "stiff" input supply, which is to say an ideal voltage source, very low Thevenin resistance, the converter was as stable as my PID loop commanded it to be.

This is the definitive Middlebrook story (see reference 1; more available [here](#)), before I knew it as such. The concept is very simple. A switching power converter has a negative incremental input impedance.

When the Thevenin impedance of the source approaches this negative incremental input impedance, instability is guaranteed and assured. I had the luxury of learning this from Dr. Middlebrook himself at a local Unitrode seminar. I later worked with him for a couple of years.

In practice, the output impedance of a large earthbound transformer or genset is usually a very small number. Usually on the order of 2 to 5% Per Unit or PU. By this a 100 KW generator at 480 VAC line to line output voltage; delivering three phase mains would have a Thevenin output impedance of $5\%(277V/120.3A)$ or 0.115 ohms. In most applications, this is nowhere near a Middlebrook stability criteria problem

But there are applications where the Thevenin output impedance can be much higher. If we consider perhaps a large solar array in a satellite, if the output current is 10A into a short circuit and the output voltage is 120V nominal, the Thevenin impedance is then approximately 12 ohms. The maximum power that the array can deliver is then 300W. Let's say we connect a reasonable load to this bus, perhaps three SA50-120 DC to DC converters to deliver a galvanically isolated total power of 150W to the platform. The efficiency of the converters is approximately 86%. The 150W output then requires 174.3W of input power. This is a switching converter. At 120V nominal, the converter will then draw 0.484A. At 125V, the converter will draw 0.465A. At 115V, the converter will draw 0.505A. The negative incremental input impedance of the converter is then $(115V-125V)/(0.505A-0.465A)$ or -250 ohms. Three converters running in parallel will have a negative incremental input impedance of -83.3 ohms. In this case, the Thevenin output impedance of the source is reasonably lower than the negative incremental input impedance of the converter at DC. But there is more in play. The impedance must be considered up to the switching frequency of the power supply.

It has also been argued that the impedances only need consideration up to the dominant pole of the converter, but the built-in feedforward in peak current mode control does in fact include line voltage information at a rate that is refreshed at the switching frequency of the converter. By this, most aerospace customers will ask for an input impedance plot up to and including the switching frequency as a matter of good practice.

If we consider the input impedance of the switching power supply, let's use a simple buck converter as the example. In closed-loop mode the converter delivers constant power. At DC the impedance then simply reflects the output power and efficiency. It's a fixed value at fixed voltage. The output capacitor of the converter is the next element to have an effect on the input impedance. It causes a negative slope in the input impedance. This slope stops at the resonant frequency of the LC output filter and then turns positive. The next large downturn is caused by the input capacitance of the converter and it extends well out beyond fsw. This can be measured on the bench and in SPICE with much the same technique. On the bench, we would add a current injection transformer and use a VNA. We would inject AC current and then measure the current and voltage. Divide the two to get input impedance ($Z=V/I$). In SPICE, the operation is similar. The measurement is usually taken from DC to something beyond the switching frequency, perhaps 2 fsw.

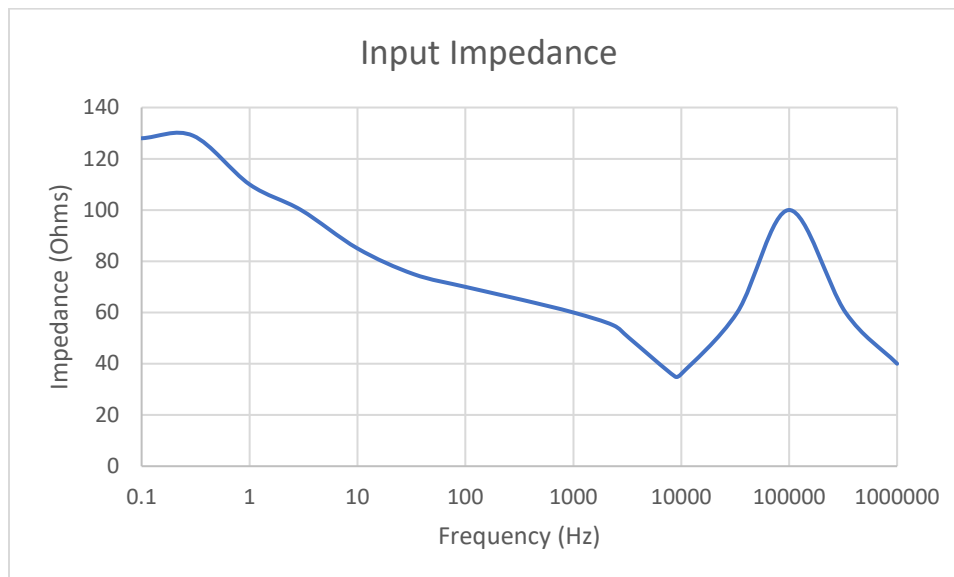


Figure 1: Input impedance plot: 50W Buck converter, 80V input, $C_{in}=47 \mu F$, $C_{out}=22 \mu F$, $L=15 \mu H$

The next measurement should then be the complete Thevenin impedance of the source. This would include any filter blocks or added filtering to the input of the power supply. Same measurement technique and instrumentation only looking back at the source.

It is required that the Thevenin impedance of the source be much less than the input impedance of the converter from DC up to fsw. I've often seen a factor of 5 used: $Z_{inpower\ supply} < Z_{thevenin\ source} * 5$

The impedance of the filter block or any input filter must add to the Thevenin output impedance of the source.

Front End Design

With input stability reasonably addressed, we should have a look at the front end design attributes. For a smaller POL converter or switching power supply design, the currents are much lower and easier to deal with. We may be dealing with traces on a PWB that may see a few amperes. Use the POL or DC to DC converter manufacturer's recommendations on external input and output capacitors. They have made proper ripple current and capacitance considerations.

In the absence of manufacturer's recommendations, Multilayer Ceramic Capacitors (MLCCs) are often used in applications like this with tantalum capacitors if larger capacitance is needed. Low tan (delta) capacitors are desired due to the low ESR and ESL of the structure and the low heating losses $(rms\ ripple\ current)^2 * ESR$. On the matter of sizing the bus or input capacitors, the RMS ripple current must be known and the capacitor array sized properly to meet this. Recall, the input capacitor is both sourcing current to the power converter to discharge and sinking current

must be known and the capacitor array sized properly to meet this. Recall, the input capacitor is both sourcing current to the power converter to discharge and sinking current from the line to charge. There is often an additional holdover requirement where the capacitor bank must sustain the output of the converter for a short period of time. This often comes up because the input source can be switched and the transfer time is nonzero. Almost any good capacitor vendor has the tools to size the capacitors, calculate the losses, temp rise, MTBF in situ, etc.

EMI Filter

The design of the EMI filter is fairly complex, but the guesswork is gone. The noise spectra in conducted or radiated mode is fixed—the limit line doesn't move. It doesn't vary with the size of the converter. A larger converter makes more switching noise, therefore, it needs more filtering and attention to detail. The filter is not a magic cure. If the layout of the switching circuitry is poor, with large loops areas, fast edges to excite oscillations and large copper pours moving at high dv/dt , the filter won't solve everything. The nearfields will couple into and around the filter. There is a lot of discussion and varying design methodology on where to put the dominant poles. We know the bandwidth of switching converter emissions is enveloped by the rise and fall times as well as the maximum and minimum duty cycles. This can be expressed as $1/\pi \cdot tr$ and $1/\pi \cdot ton \cdot min$ (see reference 2, 3).

For perhaps a Si Power MOSFET in a switching power converter, the rise and fall times may be in the 100 ns range, the switching frequency may be in the 500 kHz range, the minimum duty cycle may be down around 10% or 200 ns. The dominant poles of the conducted and or radiated emissions from the converter are then at 3.2 MHz and 1.6 MHz, respectively. Any filter design must consider the noise coupling mode (common mode or differential), the roll off frequencies, the attenuation required and then the damping of the filter elements. Model the input source to the filter as having a Thevenin impedance of zero. Model the converter as having the measured impedance on the VNA. When you excite the system with a small AC voltage to measure, look for underdamped oscillations. I've caught many instances of this and had to fix them by adding resistance in parallel to inductors, RC series damping, etc.

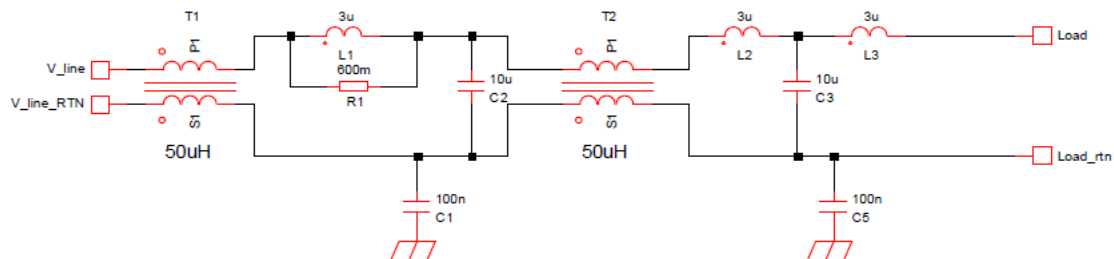


Figure 2: SF-200 block diagram

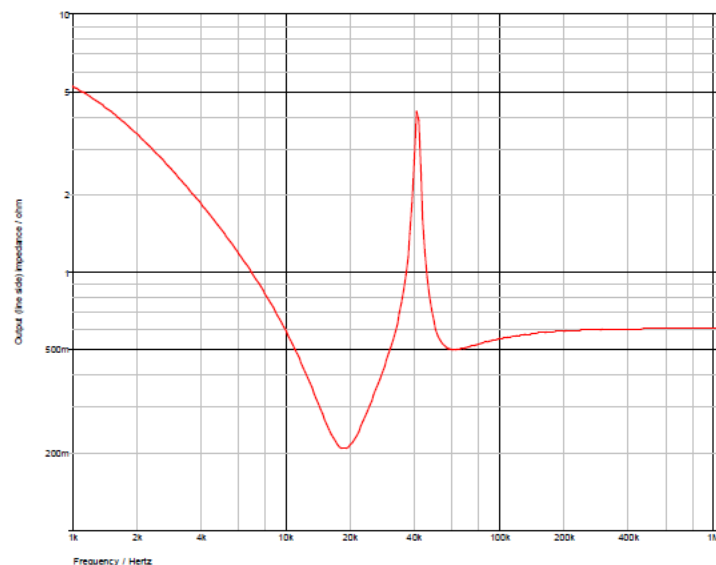


Figure 3: A look at the SF-200 EMI filter (designed for use with SA50 modules)

Ampacity (yes, it's really a word)

In that we are discussing the front end of a power supply, a discussion on ampacity must be included. How much current can a conductor carry? What if the conductor is a flat trace on a PWB? What if it's raw copper in free air? In a wind tunnel? With a heavy jacket? All of these attributes impact ampacity. There is no single right answer, but it is entirely possible to temper the discussion with common sense. When discussing ampacity, it is useful to develop a language. Current, cross section, current density. The simplest discussion I've found on this matter is to use US standards including American Wire Gauge (AWG), Circular Mils (CM) and then current density as CM/A or circular mils per ampere. Note that circular mils is a derivation based completely on the diameter of a solid, round conductor. If the solid round conductor has a diameter of 0.100" or 100 mils, the cross section is then 10,000 CM. CM simply squares the diameter of the round wire (thereby the area is 4/pi times greater than the true cross section in square mils).

If I tear into a couple of "lab stock" fuses, designed to blow at 3A quickly, I find that the fuse cartridge or housing is 1.25" x 0.25" diameter. The conductor is 1.25" long and it is 0.0062" diameter with round cross section. The glass tube on the outside of the fuse serves to contain the fused material on a fault along with the arc. The cross section of the fuse is then 39 CM or circular mils, which is simply the diameter of the round wire squared (in mils where 1 mil=0.001"). The fusing current density at 3A is then about 13 CM/A

Further, we know that a 12 AWG extension cord is good for 20A in most any environment, including our home as per UL, IEC, NFPA, your insurance company and many other safety-minded organizations, as well as the nameplate on the cable. The cross section of a single 12 AWG conductor is 6530 CM, and the current density is then 326 CM/A.

As a last boundary, when I used to design transformers for completely sealed environments, we kept the current densities up around 500 CM/A to 1000 CM/A depending on max ambient conditions. With this, we could usually make the required UL Class B insulation systems.

To boil this down to common sense, if your trace has less cross section than the fuse, you are in trouble. In practice on FR4 PWB builds, I've found that a surface trace of any appreciable length with a current density much below 100 CM/A is risking browning the board and the resultant delamination and failure. I've always targeted as much copper as possible for a power path. Interleaving is a great option due to the lumped capacitance in all of the layers and minimal inductance. I use the attached table to get from AWG to trace width and size traces for safe current density.

Paul L. Schimele PE
psl@schimeleinc.com
(224) 227-3076

COPPER WIRE

AWG #	Solid Wire Diameter (mil)	Cross Section Cir mil	Cross Section Square mil	Cross section square mm	Equivalent Cross section in 1/2 oz copper 1/2oz Cu: 7 mil Width (mil)	Equivalent Cross Section in 2 oz copper 1oz Cu: 1.4 mil Width (mil)	Equivalent Cross Section in 4 oz copper 2oz Cu: 0.7 mil Width (mil)	Equivalent Cross Section in 8 oz copper 4oz Cu: 0.35 mil Width (mil)	Equivalent Cross Section in 16 oz copper 8oz Cu: 0.17 mil Width (mil)	30 or mil/A Current	100 or mil/A Current	300 or mil/A Current	500 or mil/A Current	1000 or mil/A Current	ohm/foot 24 deg c	ohm/foot 105 deg c
40	1.16	9.8	7.78	0.0069	11.11	6.66	2.78	1.39	0.69	0.33	0.10	0.03	0.02	0.01	0.0007772248	1.5847722248
39	3.54	12.5	9.82	0.0063	14.02	7.51	3.51	1.75	0.87	0.42	0.13	0.04	0.03	0.01	0.0488320089	1.044635621
38	3.96	15.7	12.33	0.0080	17.62	8.81	4.40	2.20	1.10	0.52	0.16	0.05	0.03	0.02	0.0734388605	0.8796032085
37	4.45	19.8	16.55	0.0100	22.22	11.11	5.55	2.78	1.39	0.68	0.20	0.07	0.04	0.02	0.0939893995	0.8973886124
36	5.00	25.0	19.63	0.0127	28.05	14.02	7.01	3.51	1.75	0.83	0.25	0.08	0.05	0.03	0.1229196044	0.6523317910
35	5.61	31.5	24.74	0.0160	35.34	17.67	8.84	4.42	2.21	1.05	0.32	0.11	0.06	0.03	0.1386650479	0.4383885564
34	6.31	39.8	31.26	0.0202	44.66	22.33	11.16	5.58	2.79	1.33	0.40	0.13	0.08	0.04	0.2656530179	0.3469420735
33	7.08	50.1	39.35	0.0254	56.21	28.11	14.05	7.03	3.51	1.67	0.50	0.17	0.10	0.05	0.2110377287	0.2756146612
32	7.95	63.2	49.64	0.0320	70.91	35.45	17.73	8.86	4.43	2.11	0.63	0.21	0.13	0.06	0.1672941473	0.2148656729
31	8.93	79.7	62.60	0.0404	89.42	44.71	22.36	11.18	5.59	2.66	0.80	0.27	0.16	0.08	0.1326598508	0.1732533818
30	10.05	101	79.39	0.0512	113.32	56.66	28.33	14.17	7.09	3.37	1.01	0.34	0.20	0.10	0.1046880704	0.1387167874
29	11.27	127	99.75	0.0644	142.49	71.25	35.62	17.81	8.91	4.23	1.27	0.42	0.25	0.13	0.0832518904	0.1087267286
28	12.65	158	125.66	0.0811	179.52	89.75	44.88	22.44	11.22	5.33	1.60	0.53	0.32	0.16	0.0660118842	0.0863018408
27	14.21	202	158.65	0.1024	226.64	113.32	56.66	28.33	14.17	6.73	2.02	0.67	0.40	0.20	0.0523415352	0.0683278937
26	15.94	254	199.49	0.1287	284.99	142.49	71.25	35.62	17.81	8.47	2.54	0.85	0.51	0.25	0.0416289463	0.0543633643
25	17.89	320	251.33	0.1621	359.04	179.52	89.75	44.88	22.44	10.67	3.20	1.07	0.64	0.32	0.0330405941	0.0431509204
24	20.10	404	317.30	0.2047	453.29	226.64	113.32	56.66	28.33	13.47	4.04	1.35	0.81	0.40	0.0261707676	0.0341759468
23	22.56	509	399.77	0.2579	571.10	285.55	142.77	71.39	35.69	16.97	5.09	1.70	1.02	0.51	0.0207720837	0.0271282000
22	25.34	642	504.23	0.3253	720.32	360.16	180.08	90.04	45.02	21.40	6.42	2.14	1.28	0.64	0.0164688319	0.0215082469
21	28.45	810	636.17	0.4104	908.82	454.41	227.20	113.60	56.80	27.00	8.10	2.70	1.62	0.81	0.0130530742	0.0170472772
20	31.84	1020	801.11	0.6188	1144.44	572.22	286.11	143.06	71.53	34.00	10.50	3.40	2.04	1.02	0.0108868796	0.0136876407
19	35.52	1290	1013.16	0.8537	1447.38	723.69	361.84	180.92	90.46	42.00	12.50	4.20	2.50	1.25	0.0091961154	0.0120701043
18	40.25	1620	1272.34	0.8009	1817.63	908.82	454.41	227.20	113.60	54.00	16.20	5.40	3.24	1.62	0.0065265371	0.0086236396
17	45.28	2050	1610.06	1.0387	2300.09	1150.05	575.02	287.51	143.76	68.33	20.50	6.83	4.10	2.05	0.0051575562	0.0067357534
16	50.79	2580	2026.33	1.3073	2894.75	1447.38	723.69	361.84	180.92	86.00	25.80	8.60	5.16	2.58	0.0040980582	0.0053520521
15	57.10	3250	2560.40	1.6519	3657.51	1828.75	914.43	457.22	228.61	106.67	32.50	10.67	6.42	3.21	0.0032432485	0.0042356732
14	64.11	4110	3227.98	2.0826	4611.41	2305.70	1152.85	576.43	288.28	137.00	41.10	13.70	8.22	4.11	0.0026725037	0.0033958624
13	71.97	5180	4069.36	2.6247	5811.94	2905.97	1447.38	723.69	361.84	172.67	51.80	17.27	10.36	5.18	0.0020411178	0.0026656939
12	80.81	6530	5128.65	3.3088	7226.64	3663.32	1831.66	915.83	457.92	217.67	65.30	21.77	13.06	6.53	0.0016191409	0.0021459333
11	92.30	8230	6463.82	4.1702	9234.03	4617.02	2308.51	1154.25	577.13	271.67	82.30	27.17	16.46	8.23	0.0012384690	0.0016191409
10	101.88	10400	8168.15	6.3988	11688.76	5843.38	2917.19	1458.00	729.00	345.67	104.00	34.57	20.85	10.40	0.0010168337	0.0013277204
9	114.45	13100	10288.71	8.6375	14588.16	7345.08	3674.54	1837.27	918.54	435.67	131.00	43.67	26.20	13.10	0.0008070593	0.0010540583
8	128.45	16500	12959.06	8.3607	18512.94	9256.47	4628.24	2314.12	1157.06	550.00	165.00	55.00	33.00	16.50	0.0006407873	0.0008368663
7	144.22	20800	16336.27	10.5395	23337.53	11668.76	5834.38	2917.19	1458.00	693.33	208.00	69.33	41.80	20.80	0.0005083169	0.0006638603
6	162.17	26100	20856.95	13.3264	29505.51	14754.25	7377.13	3688.56	1844.04	876.67	261.00	87.67	52.60	26.30	0.0004020148	0.0005303032
5	181.93	33100	25996.66	16.7720	37138.08	18569.04	9284.52	4642.26	2321.13	1103.33	331.00	110.33	66.20	33.10	0.0003194257	0.0004171690
4	204.21	41700	32751.08	21.1297	46787.25	23393.63	11695.81	5848.41	2921.13	1390.00	417.00	139.00	83.40	41.70	0.0002554589	0.0003311342
3	229.35	52600	41311.51	26.8528	59017.01	29508.51	14754.25	7377.13	3688.56	1753.33	526.00	175.33	105.20	52.60	0.0002010074	0.0002625151
2	257.68	66400	52150.39	33.6453	74500.55	37250.28	18625.14	9315.27	4658.54	2213.33	664.00	221.33	132.80	66.40	0.0001593318	0.0002079562
1	289.31	83700	65737.77	42.4114	93911.10	46955.55	23477.78	11739.89	5895.93	2790.00	837.00	279.00	167.40	83.70	0.0001263201	0.0001649737
ought (0)	326.68	108000	83262.14	63.7108	118931.82	59486.81	29732.91	14880.46	7393.93	3533.33	1080.00	353.33	212.00	108.00	0.0000987452	0.0001302888
2ought (00)	364.69	133000	104457.87	67.3920	149225.53	74612.76	37306.38	18653.19	9323.46	4433.33	1330.00	443.33	266.00	133.00	0.0000749462	0.0001082189
3ought (000)	409.88	168000	131946.78	85.1268	188495.40	94247.70	47123.85	23561.93	11707.95	5600.00	1680.00	560.00	336.00	168.00	0.0000629345	0.0000821922
4ought (0000)	462.43	212000	166504.27	107.4219	237863.34	118931.62	59486.81	29732.91	14880.46	7066.67	2120.00	706.67	424.00	212.00	0.0000488724	0.0000641335

1.) FOR THE SAME RUN IN ALUMINUM WIRE, TO GET THE SAME CONDUCTOR RESISTANCE REQUIRES 160% OF THE CROSS SECTION OF COPPER. (Al=(CuAWG-2))
2.) THE TEMPO FOR AI AND CU ARE VERY SIMILAR, SO THIS APPLIES OVER ALL TEMP.

Additional Notes:

Resistivity of Cu:

$R(T) = (1.7241 \times 10^{-4}) \cdot [1 + 0.0038(T - 20)]$

T is temp in deg C

S is Resistivity in Ohm*centimeters (cm)

Resistance= $[S(T) \cdot \text{Length}(cm)] / \text{Cross Section}(cm^2)$

Temperature Classification (per UL1448)	
Designator	Hot spot temp (deg C)
B	130
F	165
H	180
N	200
R	220
S	240

In the IC and the module, ampacity is a slightly different matter. The conductors still conduct, but things are MUCH closer together. For example, in a large power module, with an 80°C nameplate current rating of 750A, we might find a total of 36 bondwires connecting all of the paralleled die to form the composite power switch. The bondwires are 12 mil diameter, 144 CM cross section. This comes out to a total conducting cross section of 5184 CM. At 750A this is a current density of roughly 7 CM/A. But in this module, the longest distance traversed is perhaps 125 mil, the longest bondwire is perhaps 150 mil. The bondwires are immersed in vacuum filled silicone gel. But the current density in the module is lower than that of a 3 AG cartridge fuse!

Further, that same module may be used in an inverter with output terminations that are available to the end user (read as: bolted fault short circuit event is possible). In this case, the module may see a short circuit on the order of 3800A (usually roughly 5x nameplate rating). The ISC or short circuit current specification for the module usually allows 2 to 10 us total in this heavy pulse condition. What that means for the inverter designer is that they have to sense this fault event and shut down the PWM pulses well within this time period. Should anyone ever ask if a 12 AWG extension cord can handle 750A, you might say yes if, and only if, the cord is reduced to about 1/8" in total length!

As a last required item in an ampacity discussion, we have to consider AC effects in current carrying conductors. The primary mechanism for this is skin effect. The physics behind this are fairly simple. At DC, a given current flows through a given conductor uniformly. There is no distribution; each smaller cross section sees the same current density as any other. However, this changes at AC. We can recall that an AC current produces a varying magnetic field. That magnetic field induces currents in the conductor that oppose the flow of current (read as self-inductance). If we look at the cross section of a single conductor, we see that high-frequency AC current tends to oppose in the core of the conductor. This pushes the current out to the edges. For a round, solid copper conductor, $D_{pen} = 7.6 / \sqrt{f}$, where D_{pen} is in cm and f is in Hertz (see reference 4). This is the thickness of the current-carrying part of the cross section of the wire. Stated differently, it is the depth of penetration of the current into the conductor. We can improve this by using Litz wire, which is a bundle of individually enameled conductors of much smaller diameter, allowing higher utilization of each conductor. This is often done in transformers.

On a PWB we can specify the copper thickness. Our conductors are generally large, flat sheets. The thickness varies. 1 ounce per square foot copper is 1.4 mil thick, 2 ounce is 2.8, 4 ounce is 5.6 mil and so forth. At 500 KHz, D_{pen} is 0.0107 cm or 4.2 mil. For a 4 ounce PWB trace in a compact DC to DC converter design, the conductor thickness is slightly larger than D_{pen} . A little more cross section might be advantageous, but on a wide trace, the AC impedance will be close to that of the DC resistance.

Proximity effect is simply skin effect compounded. Individual conductors are stacked on top of each other in layers, such that the fields add up exponentially toward the middle. This is primarily a design concern in transformers. The Dowell curves model this as R_{ac}/R_{dc} at various layer stack-ups and depth of penetrations (see reference 4). The curves were later corrected for square wave excitation (and the added harmonic content) as in most SMPS waveforms.

I²t discussion

If we imagine the fuse as a low-value resistor, the power in that resistor is ultimately what makes it fuse open. Once the local power dissipation causes enough localized heating, such that the heat can't be removed from a given area or space, the fuse develops a hotspot and melts. This is driven by the power dissipation in the fuse element and then, of course, ambient temperature. If the fuse is hotter, it doesn't take as much added heat to make it open. Numerically we can compute the power in this resistor as $I^2 \cdot R$. The power in the fusible element varies with the square of the current.

But power isn't the whole story. Power is just the rate at which the heat is delivered to the element. The element can withstand a certain energy at a given ambient temperature before it fuses open. Energy is the timewise integral of power. This is where I^2t value comes from for a given fuse element. Higher-current drives exponentially higher power, but the timewise integral of the power pulse tells us where the fuse will blow. In larger power matters, the characteristic curve that describes this is often referred to as the "let-through" curve.

In the module example above, with the given ratings, we might expect to see an I^2t rating on the order of $144A^2s$. In reality, this is guard-banded to assure the module survives the 5x nameplate rating short-circuit event.

To see how the I^2t value works for a fuse, we can look at almost any fuse. In this case a 1.25" × 0.25" 3AG type fuse is shown.

Ampacity:

3A, 3AG type fuse, 1.25" long, 0.25" OD Glass Envelope

Current	Time	I^2t
A	s	(A^2s)
4	0.009	0.144
5	0.006	0.15
6	0.004	0.144
7	0.003	0.147
8.5	0.002	0.1445
12	0.001	0.144

Figure 5: Let-through curve for 3AG cartridge fuse

To go beyond the utility of the fuse, the LX7712 depicted above is a superb electronic circuit breaker. Great current adjustments, telemetry, and programmable modality from one shot to retry to foldback.

Undervoltage Lockout (UVLO)

UVLO isn't in the front end of the power supply, however it impacts it heavily. Imagine the SA50 example above, only without UVLO. (Note, this is for discussion only, SA50 can't be delivered or built without UVLO.) If the SA50 were to try and deliver 50W output, at 10V input (assuming ideal power switches, etc) the input current would be greater than 5A. The input impedance would be less than 2.0 ohms. With the Thevenin output impedance of the source being much larger than this, the converter could only oscillate (read as Middlebrook stability problem). Then there would be the matter of ampacity. The conductors to a 50W converter for 120V mains would have to handle over 5A! The filters would be much larger, conductors, fuses, etc., not to mention the added scaling for telemetry. While it seems remedial, UVLO in a switching converter is actually fairly important, not just from an ampacity standpoint but from a stability standpoint as well.

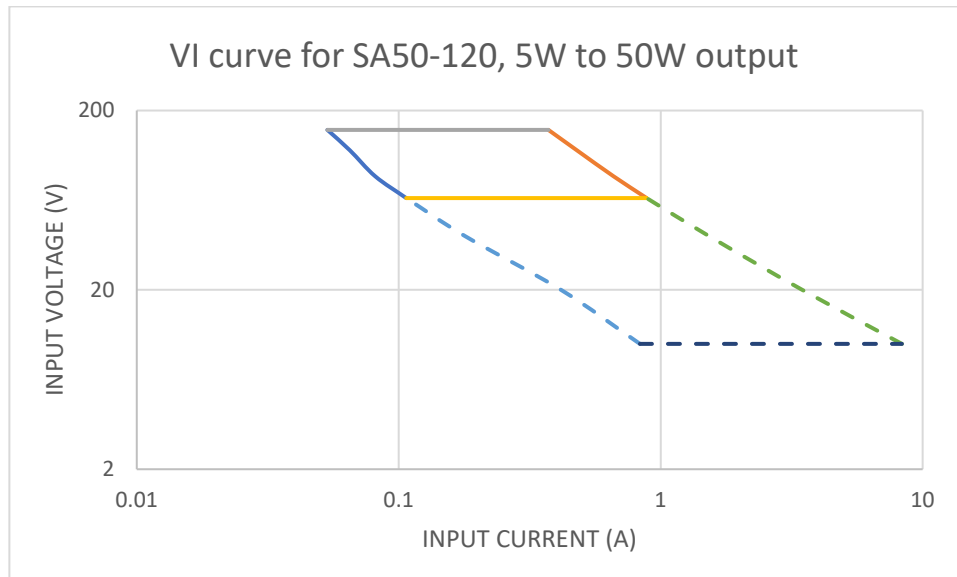


Figure 6.) VI curve for SA50-120 radiation-hard converter, 5W to 50W output. Dotted line represents input without UVLO (not possible in design). Note the much higher input currents (much lower input impedance) that would have to be considered without UVLO.

The hysteresis in UVLO is often what causes the hiccup operation when the source impedance gets too high. The hiccup comes from the converter trying to power up, pulling down the mains voltage, then shutting down, then the voltage rising and trying again.

Conclusions

I hope the holiday finds you well. Perhaps we can take off the mask and enjoy a little family time, unwind a bit, bring back a little balance. My hope is that this brief tour of the input of a power supply provides some utility. Middlebrook stability criteria is an important part of a high reliability design as is the input impedance measurement and that of the source. The front end may be as simple as a large capacitor bank; it may also be complex and include differential and common mode filtering. In my experience, one of the most often overlooked design attributes is ampacity. I've seen a lot browned traces, heated wire jackets and, in some cases, fused traces and conductors. It's a large topic with no single right answer, but the wire table is a good start along with the common-sense asymptotes presented. UVLO is determined by the controller, but it does have an impact on the front end design in terms of ampacity and stability. If there were no UVLO, most switching converters would have tremendous problems at very low voltages.

Happy Holidays and Stay tuned for our next edition where we discuss the second part of this five-part series: the topology and the transfer function.

References:

- 1.) Stability Testing and Analysis of a PMAD DC Test Bed for the Space Station Freedom, NASA-TM-105846; pp 1-3.
- 2.) M. Mardiguian, *Controlling Radiated Emissions By Design*. Second ed. Boston MA, KAP, 2001
- 3.) H. Ott, *Noise Reduction Techniques in Electronic Systems*. Second ed. New York NY, Wiley, 1998.
- 4.) Lloyd Dixon, *Magnetics Design Handbook*. <https://www.ti.com/seclit/ml/slup132/slup132.pdf>

Scrap Iron Creation Quiz: Common Mode or Differential Noise?



Figure x.) Is the data (crosshatched expanded metal) flowing out of the page from one bulldog face (common mode) or is it flowing from two bulldogs mashed together from left to right (differential)?



For further information contact Paul.Schimel@microchip.com.