Welcome to Edition 29 of Microchip's Space Brief newsletter. Written for design engineers and design managers, system engineers and system architects, component engineers, radiation effects scientists and program managers in the space industry, Space Brief is a quarterly newsletter in which we aim to bring you the latest news about our radiation-tolerant and radiation-hardened products. Space Brief provides information about new products, updates on qualification and radiation testing, links to formal customer notifications, and news about workshops and conferences at which Microchip will be presenting or exhibiting.

Please forward Space Brief to your colleagues, and let them know they can register to receive this newsletter directly to their email inbox every three months by clicking here.

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PRODUCT NEWS

SAMRH71 Rad-Hard Arm® Cortex®-M7 Based SoC
Ceramic Flight Models and Plastic Samples Available

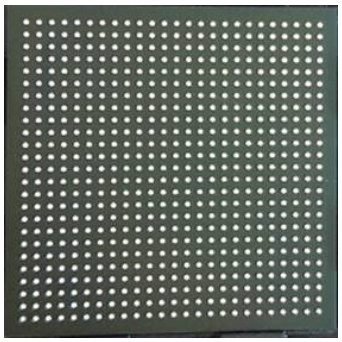
The SAMRH71 is a unique Rad-Hard processor targeting space applications, derived from the SAMV71Q21 Commercial Off-the-Shelf (COTS) automotive microcontroller. The SAMRH71 supports SpaceWire, Mil-Std 1553, CAN FD, and Ethernet TSN interfaces and provides high levels of radiation performance, including:

- Accumulated TID of more than 100 Krad (Si)
- SEL latch up immune up to 62 MeV.cm^2/mg
- No Single Event Upset (SEU) at Linear Energy Transfer (LET) up to 20 MeV.cm²/mg, without system mitigation
- Designed for No Single-Event Functional Interrupts (SEFI) to secure integrity of all memories

Here is some information about the package options for the SAMRH71:

- Ceramic-qualified MQ flight models are now available, and the ordering part number is SAMRH71F20C-7GB-MQ. The MQ screening flow is equivalent to QML class Q.
- SAMRH71 ceramic-qualified SV flight models are expected to be available before the end of 2020.
- To support volume programs for space applications, we are offering a Hi Rel plastic BGA625 version. Samples are now available for design purposes, and the ordering part number is SAMRH71F20C-HFB-E.
- Plastic-qualified flight model versions, based on the Hi Rel Plastic (HP) qualification flow, are expected to be available by the end of 2020. The HP flow targets low-cost and high-volume requirements, and typically meet the requirements of Low Earth Orbit (LEO) constellations.
- We also provide devices based on the SN flow, which is a high-reliability plastic package extended quality flow with a higher screening level, including Wafer Lot Acceptance, serialization, 100% thermal cycling, 100% burn-in and PDA.

Read about our qualification flow in our AEQA0242 Reference Document.



For further information, contact **Nicolas Ganry**, Product Marketing Manager, Nicolas.Ganry@microchip.com

Space CSAC Applications in Low Earth Orbit

The market opportunity for LEO space applications is growing quickly. Many commercial, scientific and defense programs are seeking precision timing solutions with shorter lead times and lower costs to meet the current demand. Launched in June 2018, our SA.45s commercial space Chip-Scale Atomic Clock (CSAC) is the industry's first commercially available radiation-tolerant CSAC. Ideally suited for LEO applications, the device provides the accuracy and stability of atomic clock technology while achieving significant breakthroughs in reduced size, weight, and power consumption.

Space CSAC LEO applications include:

- Satellite timing and frequency control
- Satellite cross linking
- Optical time transfer (between satellites and between ground and satellite)
- Earth observation
- Radio Frequency (RF) geolocation
- Interferometry

I'll describe these applications in future issues of *Space Brief*, but here are summaries about the first two:

Application: Ionosphere Plasma Monitoring

Variability in the Earth's ionosphere affects radio-frequency and GNSS communication systems. Measuring the phenomenon to understand and predict ionospheric variability can enhance the reliability and accuracy of these systems.

Space Precision Atomic-clock Timing Mission (SPATIUM) is a collaboration between the Satellite Research Center at Nanyang Technological University, Singapore, and Kyutech – Kyushu Institute of Technology, Japan, to develop high-resolution, near-real-time ionosphere plasma monitoring using a constellation of cubesats at different LEO altitudes that are precisely time-synchronized between each satellite and with multiple ground stations.

Modeling of the ionosphere plasma density is achieved using a combination of multipoint measurement of phase shift in satellite clock signal and in situ plasma density measurement from a constellation of nanosatellites This application requires CSAC low SWaP and precise atomic clock performance.

Application: Radio Frequency (RF) Geolocation

RF detection and location from LEO space is a growing Geospatial Intelligence (GEOINT) application that has multiple commercial, scientific and defense intelligence applications including ocean transportation and activity tracking from space, GNSS spoof detection to detect illicit shipping, emergency response, interference detection and geolocation, and spectrum management.

Compared to RF geolocation from aircraft, geolocation from LEO space requires a cluster of satellites flying in formation that are precisely time synchronized and can have co-visibility of the signal of interest to compare frequency and time of arrival. Each satellite has a GPS Disciplined Oscillator (GPSDO) and local CSAC and is synchronized using GPS receivers. GPS and clock stability time and frequency error contribute to signal position and velocity accuracy. This application can leverage Low-Noise CSAC (LNCSAC) with its low SWaP and precise atomic clock performance.

Conclusions

With many spacecraft manufacturers turning to COTS parts to meet performance, schedule, and cost requirements, the space CSAC offers a solution for many commercial and defense LEO satellite missions and applications.

The space CSAC is available now with the part number 090-02984-007. Delivery is 4 weeks, ARO. A developer kit is also available with part number 990-00123-000.

For further information, contact **Stewart Hampton**, Product Line Manager, Stewart.Hampton@microchip.com

Vectron® Response to DLA Release of MIL-PRF-55310, Revision F (Amendment 1) and MIL-PRF-38534, Revision L

MIL-PRF-55310 and MIL-PRF-38534 are the two primary governing authorities for hybrid crystal oscillator quality assurance and test requirements. Both documents recently received official makeovers that QPL suppliers must comply with. As a result of recent DLA revisions, MIL-PRF-55310, Revision F, Amendment 1 (March 2020) and MIL-PRF-38534, Revision L (December 2019) are now in effect and must be adhered to when the applicable MIL standards are invoked. Please find below a list of the most significant changes to MIL-PRF-55310, Revision F:

- Device Screening Amendments
  - Addition of Random Vibration test (MIL-STD-883, Method 2026, Test Condition I-B)
  - Temp Cycle test condition change from B (-55°C to +125°C) to C (-65°C to +150°C)
  - PIND test condition change from B to A
  - Seal tests (Fine/Gross) now mandate MIL-STD-883, Method 1014 (Kr-85 mandate for Gross Leak test)
  - Additional delta limit considerations apply to burn-in

- Group B Aging Amendments
  - Added 15-day aging option if drift does not exceed one-half of the 30-day limit

- Group C Inspection Amendments
  - Random Vibration test (36.6g rms) added to SG1
  - Seal tests must also comply with MIL-STD-883, Method 1014 requirements
  - Life test (1,000 hours @ +125°C) added as SG5 on 25% of test specimens

The release of MIL-PRF-38534, Revision L highlights many significant changes to the Class K element evaluation requirements for EEE components. These changes largely mimic Aerospace TOR requirements for element evaluation that you would typically find in North American space defense applications. Although these changes most notably affect passive elements, microcircuit and semiconductor requirements have also been revised.

In July 2020, Microchip responded to these changes by revising and re-releasing all fifteen Hi-Rel Standards to offer fully compliant Class S and Class K platforms to the industry. All of our Vectron Hi-Rel Standards eliminate the need for the creation of OEM Source Control Drawings. The most up-to-date revision of each standard is:

OS-68338, Rev Q
Hybrid Clock Hi-Rel Standard, ACMOS and TTL Output

DOC200103, Rev I and DOC207139, Rev C
Hybrid TCXO Hi-Rel Standard, CMOS/Sinewave or LVDS Output

DOC203679, Rev G and DOC203810, Rev F
Hybrid Clock Hi-Rel Standard, LVDS or LVPECL Output

DOC204898, Rev E and DOC204899, Rev E
Hybrid VCXO Hi-Rel Standard, LVPECL or LVDS Output

DOC204900, Rev F
Hybrid Clock Hi-Rel Standard, High Frequency ACMOS Output

DOC206218, Rev D
Hybrid VCXO Hi-Rel Standard, ACMOS Output, 9 × 14 mm J-lead

DOC206379, Rev C and DOC206903, Rev C
300krad Hybrid Clock Hi-Rel Standard, ACMOS and LVDS Output

DOC206559, Rev D and DOC206906, Rev D
Hybrid VCSO Hi-Rel Standard, Sinewave or LVPECL Output

DOC207753, Rev B
Hybrid VCXO Hi-Rel Standard, High Frequency Sinewave Output

DOC207975, Rev A
Hybrid Clock Hi-Rel Standard, High Frequency Sinewave Output

In an effort to capture all newly enhanced Class K element evaluation requirements of MIL-PRF-38534, Revision L, we have created and released DOC208191, Rev A. For catalog devices where Design Pedigree "E" is invoked as the fifth digit of the part number string (i.e. 2102E24M00000TAF and 1219E156M2500BS), all "enhanced" element evaluation requirements as listed within DOC208191, Rev A will be met:

DOC208191, Rev A
Enhanced Element Evaluation (MIL-PRF-38534, Rev L compliant for Class K devices)

All of these updated Hi-Rel standards can be found on the Vectron Space and Hi-Rel page.

For further information, contact **Scott Murphy**, Space and Hi-Rel Product Line Manager at Microchip's Vectron Oscillator Products Division, Scott.Murphy@microchip.com

Qualified Space Clock Solutions Recommended for the SAMRH71 MCU and VSC854xRT Ethernet Transceiver

Our new Crystal Oscillators for SAMRH71F20 Rad-Hard Microcontroller Main Clock (MAINCK) Input application note recommends the best crystal oscillators to use with the SAMRH71 SoC. The recommended OS-68338 oscillators have been characterized and can be used as the external oscillator for the Main Clock for the SAMRH71. These oscillators meet all required performance parameters per the SAMRH71 data sheet and expected use cases. They are rated to similar radiation levels as the SoC. Multiple alternate enclosure options are available, and alternate frequencies in the range of 3 MHz to 20 MHz can be provided.

A similar application note, Reference Clocks for VSC854(x)RT Radiation Tolerant Ethernet Transceiver Family, is also available for using the SAMRH71 with the VSC8540RT Ethernet Transceiver to create an Ethernet application. This document recommends several types of OS-68338 or DOC204900 oscillators based on the target application.

For further information, contact **Yohann Bricard**, Applications Manager, Yohann.Bricard@microchip.com

Simplify Your Evaluation Platform Designs

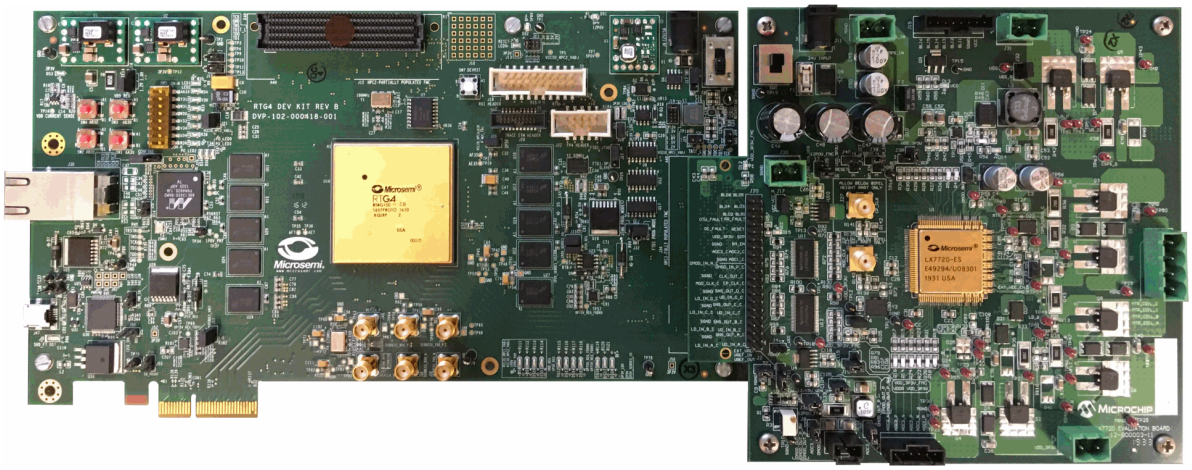
We offer several board level options allowing you to evaluate our mixed-signal ICs for space applications. These options include solutions related to our highly integrated LX7720 and the LX7730 Space System Manager companion ICs. These devices work in conjunction with an FPGA or MCU, and we have development platforms allowing you to integrate with both.

LX7720 Rad-Hard-By-Design Motor Controller IC Evaluation Solutions:

For Designs Using an FPGA:

The LX7720 Daughter Board uses the LX7720MFQ-ES and operates by default from a supplied 24V AC adapter. There are four on-board NFET half-bridges that directly drive up to four windings (such as 3-phase BLDC + brake, stepper motor). The LX7720-DB connects directly via an FMC connector to the RTG4™ FPGA Development Kit (shown below) or the PolarFire® FPGA Evaluation Kit revision B.

For more details, check out the updated LX7720 Daughter Board User Guide on our website.

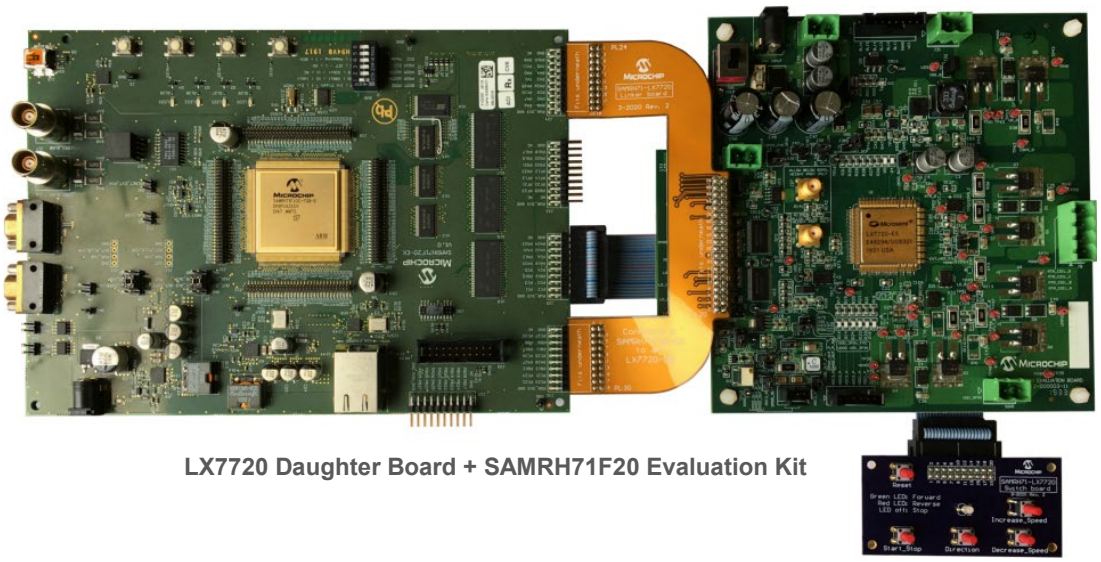


LX7720 Daughter Board + RTG4™ FPGA Development Kit

For Designs Using an MCU:

The LX7720 Daughter Board can also connect to the SAMRH71F20 Evaluation Kit (shown below) via a connector kit that includes a flexible circuit and a small PCB with switches.

For more details, check out the new LX7720 Daughter Board to SAMRH71EVB User's Manual on our website.

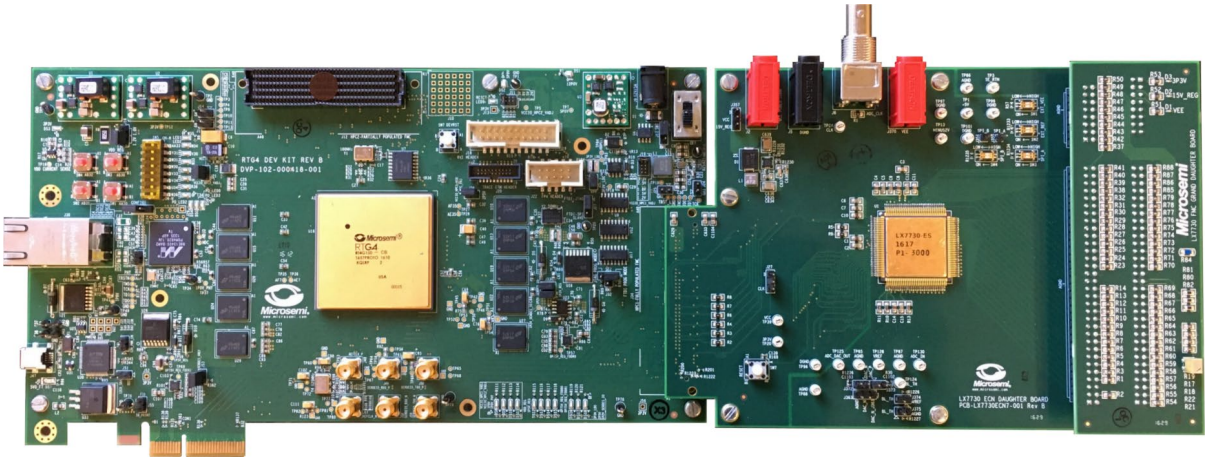


LX7720 Daughter Board + SAMRH71F20 Evaluation Kit

LX7730 Rad-Hard-By-Design Telemetry Controller IC Evaluation Solutions:

The LX7730 Daughter Board uses the LX7730MFQ-ES and connects directly via an FMC connector to the RTG4 FPGA Development Kit (shown below) or the PolarFire FPGA Evaluation Kit revision B. RTG4 FPGA firmware instantiates the LX7730 serial and parallel interfaces.

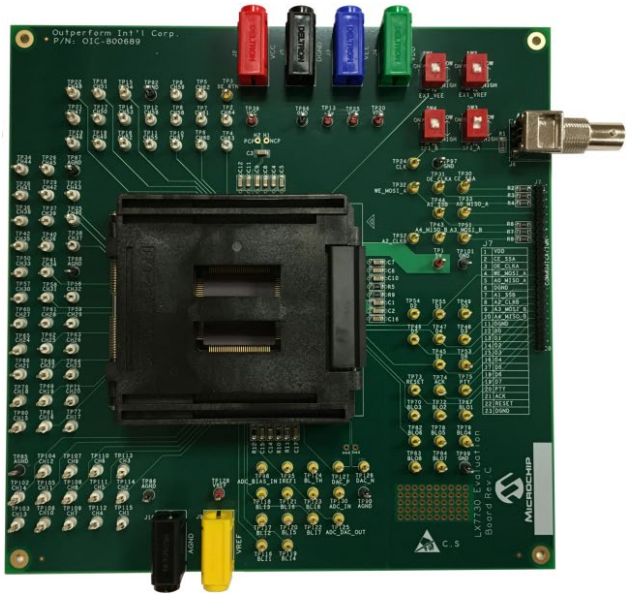
For more details, check out the updated LX7730 Daughter Board User Guide on our website.



LX7730 Daughter Board + RTG4™ FPGA Development Kit

The LLX7730 Evaluation Board accommodates the LX7730MFQ-ES via a socket. It provides full access to all analog and digital I/Os with the user providing all supplies and the ADC clock.

For more details, check out the updated LX7730 EVB Get Started Guide on our website.



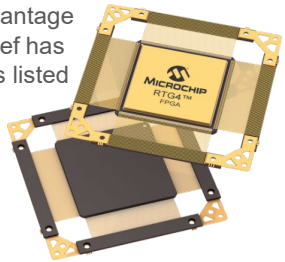
LX7730 Evaluation Board

For further information, contact **Dorian Johnson**, Product Marketing Manager, Dorian.Johnson@microchip.com

RTG4™ FPGA CQFP-352 QML Class V Qualification Update

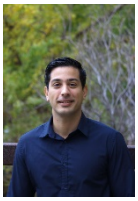
RTG4™ FPGAs in the 352-pin Ceramic Quad Flat Pack (CQFP) package are currently undergoing QML Class V qualification with a target date of October 2020. RTG4 FPGAs in the CQ352 package provide a more cost-effective integration than higher-pin-count packages. CQFP is the industry-standard package for space applications with well-established board integration and inspection procedures. The RTG4 FPGA in the CQ352 package is immediately available in the Libero® SoC software tool set, allowing you to design with this new device-package combination. When the CQ352 QML class V qualification is granted, this will complete the QML qualification for the RTG4 FPGA family. The CQ352 is already qualified to QML class Q, and the original 1657-column grid array package is already qualified to QML class Q and class V.

We recommend you download the latest version of Libero SoC Design Suite to take advantage of these recent RTG4 FPGA product family updates. The latest RTG4 FPGA product brief has also been updated to include the RTG4 CQ352. Please stay tuned to find SMD numbers listed on the DLA website once qualification is completed.



Please reach out to your local Microchip sales team if you have a need for RTG4 FPGAs in the CQ352 package with QML qualification or contact our space marketing team:

Ken O'Neill, Director of Marketing, Space and Aviation:
Ken.ONeill@microchip.com



Julian Di Matteo, Senior Engineer, Product Marketing, Space and Aviation:
Julian.DiMatteo@microchip.com

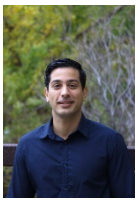
RTG4™ FPGA Sub-QML FPGA Qualification

We are currently expecting to complete the JEDEC qualification for RTG4™ Sub-QML FPGAs in the 1657 ball grid array plastic package. The target date for qualification completion is October 2020. Our Sub-QML FPGAs bridge the gap between QML and COTS components. Until now, the two main component options have been COTS products, which usually come with no radiation and limited reliability data, or QML class Q and class V components which are radiation-hardened but more expensive and have longer lead times. Our Sub-QML FPGAs are ideal components for New Space applications where commercial satellite constellations using large quantities of components require lower unit costs and faster service entry.

Please continue to check our new Sub-QML page, where you will find important documentation for Sub-QML FPGAs. In the Documents tab, we have uploaded the RTG4 Plastic Product Brief and Plastic RTG4 Package Mechanical Drawings. We have also uploaded Sub-QML screening flows which apply to all our RT FPGAs. Stay tuned for the RTG4 FPGA Plastic data sheet and pin assignment document.

Please reach out to your local Microchip sales team if you have a need for Sub-QML FPGAs or radiation-tolerant FPGAs in higher volumes and at lower cost than traditional space applications or contact our space marketing team:

Ken O'Neill, Director of Marketing, Space and Aviation:
Ken.ONeill@microchip.com



Julian Di Matteo, Senior Engineer, Product Marketing, Space and Aviation:
Julian.DiMatteo@microchip.com

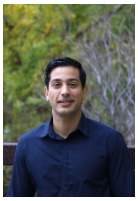
RTG4™ FPGA Production Data Sheet Rev 7 Update

The latest RTG4™ FPGA data sheet (rev 7) is posted here. Several updates were completed on the following sections and tables:

- AC Switching Characteristics for Transmitter
- LVDS25 and LVDS33 DC Voltage Specifications
- Fabric PLL Output Clock Jitter Specification
- Received and Transmitter Parameters (PCIE, SRIO, XAU)
- Added RTG4 Global Network – Max Period Jitter Table

These changes were previously discussed in customer notifications CN20006 and CN19009B. Please reach out to your local Microchip sales team if you have questions about RTG4 FPGAs or contact our space marketing team:

Ken O'Neill, Director of Marketing, Space and Aviation:
Ken.ONeill@microchip.com



Julian Di Matteo, Senior Engineer, Product Marketing, Space and Aviation:
Julian.DiMatteo@microchip.com

Understanding FPGA and Processor Current Draw

When considering practical physics and working with electricity, current must be mentioned in any discussion about power. You may know current as (the curl of the magnetic field * the cross section in space); (dQ/dt); Amperes, MMF, "Weldin' Juice", (Coulombs/s); (volume flow rate of electrons) or perhaps Watts/Volt. Remember power is work. To do work with electricity, whether you're using a pump jack or a processor, you need both a potential (voltage) and a current (Amperes) present in some DC or coherent time-varying form and/or phase. Without current, we can't do ANYTHING with electricity.

As a few fun milestones, without current, "Watson, come here, I need you," would have never been heard by Watson or uttered by Mr. A. G. Bell from the adjacent room over a DC carrier in the analogue. Thermionic emission, transconductance, HFE would be moot. Nipper, the RCA dog would have never been fooled by a recording and amplified playback of his master's call. Nikola Tesla's tower would have never pumped up to inception. There would be no data storage either in the magnetic or electrostatic domain. The telegraph would have had no MMF to pull in the solenoid to make a dot or dash. A motor would be a paperweight having never had a Q axis from which to make torque. Electromagnetic waves wouldn't exist, propagate or stand. RADAR would have never been applicable. D'Arsonval would have never moved the needle. Maxwell would have done taxes for a living. Fuses of all shapes, sizes and colors would have no utility. Service panels and thermomagnetic breakers would be repurposed as ant traps, having never had the current to heat the bimetallic thermal strip or generate the MMF in the solenoid to trip the sear.

But what then of software engineering? This has been with us since punch cards, but the focus is usually not on current consumption, but rather on wonderful, innovative and glorious machine code that enables applications that were otherwise impossible.

With respect to modern processors and FPGAs, IC designers have done a fabulous job keeping currents down to very small values. Our Rad-Hard and Rad-Tolerant processors and FPGAs have some of the lowest currents in their respective classes. But again, we have to recall, if the ammeter said "0.000000000000000000 A", the circuit wouldn't be doing anything, whether in machine code or in the analog, at tectonic rates or approaching Planck's constant.

To help bridge the current consumption gap, we have wonderful current estimator tools where the user can enter utilization and clocking parameters and compute the current required by the FPGA or processor. But is that enough? If you were coding for perhaps a mission-critical system, where you had to deal with validation, qualification, FMECA and possibly worst-case analysis, would a calculation of current draw be enough? (Hint: No).

In general, as part of any validation and verification operation, it is a good idea (and often a requirement) to measure both the time averaged or DC current drawn by the various processor rails and then the worst-case peak current. To better understand this, a simple example is in order.

First, we have to estimate the current draw of each respective rail. For an RTG4™ FPGA we can use the RTG4 Power Estimator. The tool will ask for basic design inputs and yield current estimates for each rail.

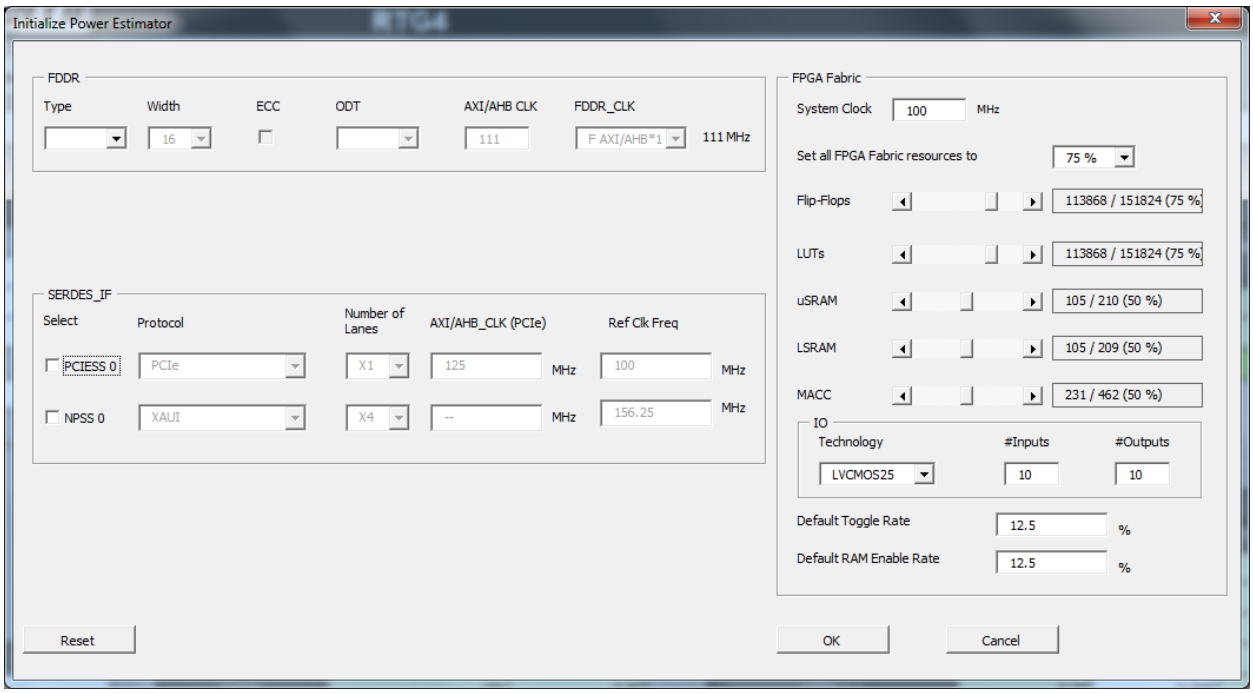


Figure 1: RTG4™ Power Estimator Screenshot

Alternately, we could simply begin the prototype effort with Point-of-Load (POL) solutions that will support known worst-case loading.

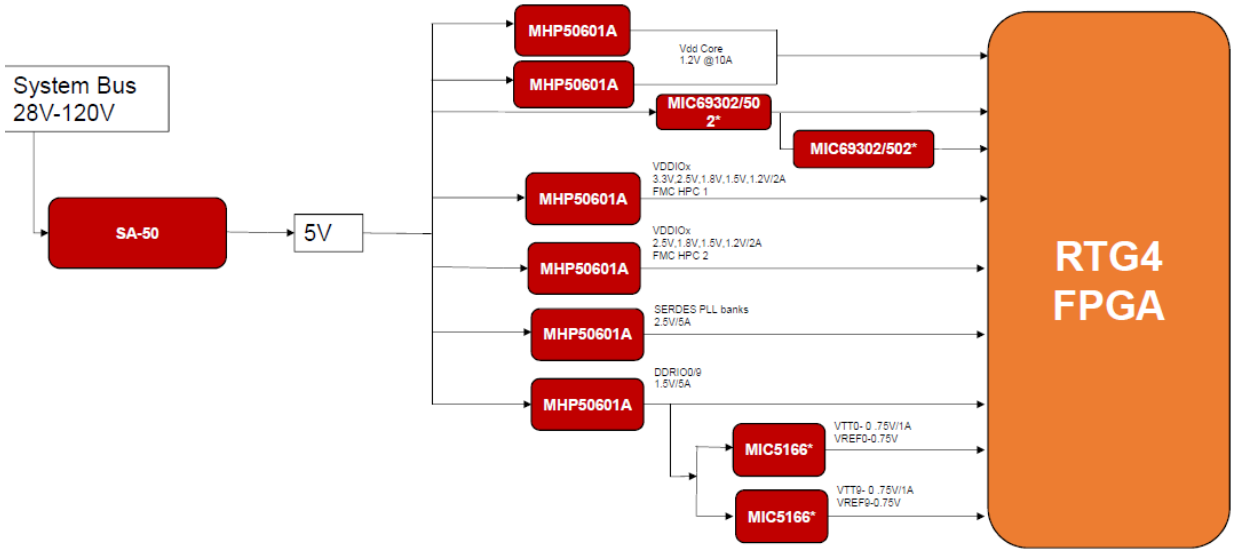


Figure 2: Block Diagram Showing POL Solutions for RTG4™ FPGAs

From this point, we assemble the prototype board with POL solutions that are perhaps slightly larger than the estimated power values. Headroom in a prototype is a good idea, whether electrical, thermal, or mechanical. Use the recommended output capacitors with each rail, whether an LDO, Linear Dropout Regulator or switching POL converter. Leave a little physical room to get an ammeter in line with each rail and a current loop for a high-speed

Mag/Hall current probe. Leave a little more room to attach a good probe interface or test point right at the pins of the FPGA or processor.

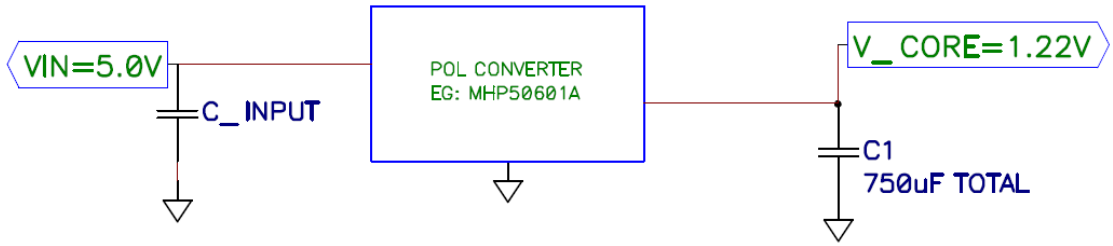


Figure 3: Schematic of POL Circuit

Verify basic operation and functionality, observe and or design proper sequencing. Once the design is known stable, take those voltage current measurements. Note: worst case is at highest temperature.

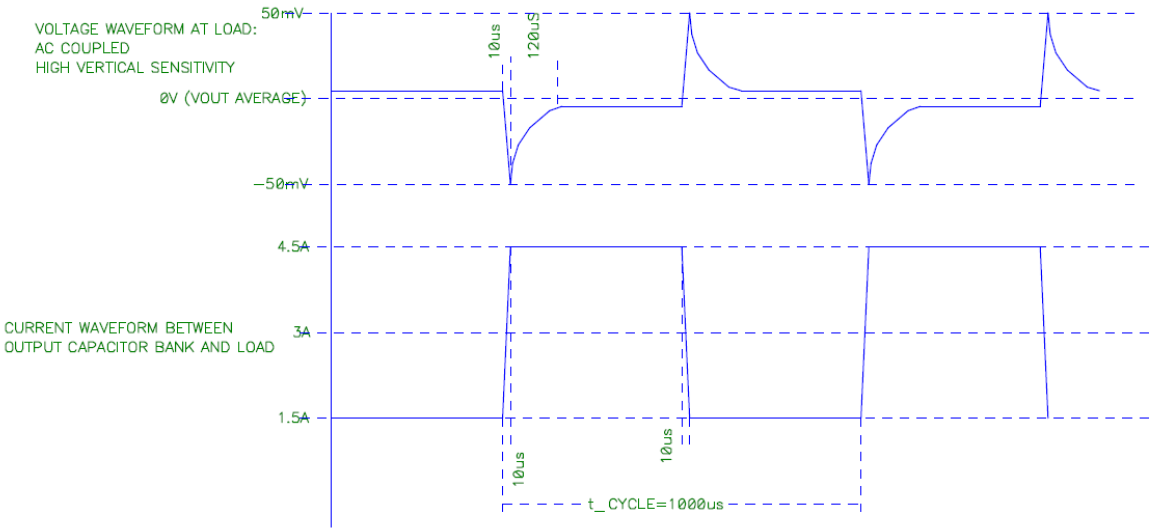


Figure 4: Worst-Case Current/Voltage Measurement Sketch (at Maximum Temperature)

With a little basic analysis, it's easy to see that this waveform has an average value of 3.0A, the maximum peak to peak excursion is 3.0A, the maximum current is 4.5A and the transition from lowest to highest current occurs in 80 us. This is then a maximum dI/dt of 0.0375 A/us.

The voltage waveform shows a worst-case voltage droop of 50 mV incident with the rising edge. The worst case overshoot is 5 0mV at the falling edge of the load step. The DC voltage (not depicted, capacitive coupling takes this to zero) was 1.22V. The max/min is then 1.27V and 1.17V respectively. This is within the worst case ±60 mV value for the core supply in the RTG4 FPGA data sheet.

The time constant of the exponential envelope (e^{-at}) is on the order of a = 1/120 us. From a dominant pole approximation, the dominant pole of the converter is then at around 8300 Hz.

With this information, it appears that the POL converter is doing a great job. The worst-case ripple voltage is well above the data sheet's specified minimum voltage.

From the POL converter's perspective, there are a few common questions. One of the first is, "Why are capacitors specified as being located right at the [respective] power pins on the PWB?" From the software side, this seems like a

nuisance that adds tremendous expense to the BOM plus the effort of populating and reflowing. But we have to remember what the capacitor does. We can recall I = Cdv/dt from almost any early engineering discussions. For a large value capacitor, the device can source or sink substantive current with minimal voltage droop or rise respectively. When we got into power electronics, this statement was simplified to “a big capacitor looks like a constant voltage source.” Same equations, same meaning. Switching power converters simply supply energy at a faster refresh rate, thereby the voltage across the output capacitor looks constant. To locate this “constant voltage source” right at the FPGA or processor power pins is the best solution possible. We also know that the capacitor stores energy in the dielectric as $E = CV^2/2$. That stored energy can be delivered to the load during a fast transient. The path of least resistance to the load is indeed right at the power pins on the board.

But that’s not the whole story. The POL solution operates in a closed loop, whether digital or analog, switch mode or linear. The loop then has an error amplifier that sees a perturbation at the output and commands the regulator to correct the perturbation. The speed of the control loop is not infinite nor can it be as per Nyquist. While a fast, momentary load condition may sink energy from the capacitor array at the power pins, a larger load condition has to be addressed by the feedback loop.

The traces on the PWB may also have a slight voltage droop due to their nonzero resistance. This is why ALL power designers recommend keeping the POL solution as close to the load as possible: a POINT OF LOAD power converter locates AT POINT OF LOAD.

From the example above, most of the current in the rising edge of the load step comes from the lumped output capacitor array (the sum of all of the capacitors in parallel). For the 3A load step occurring over 10 us, we would expect approximately a 40 mV drop given the lumped total output capacitance of 750 uF. The 10 mV discrepancy is due to the non-zero ESR of the capacitor and the voltage drop of the power planes leading to the power pins.

The layout of the POL solution must take advantage of power planes and interleaved layers at higher current levels. The concept behind this is to use the PCB dielectric to store energy in the local E-field as a capacitor; doing so also dramatically reduces the inductance. Viewed as a transmission line, the impedance approaches zero (sqrt (L/C)) where L approaches zero and C is maximized by interleaved, alternating ± layers to the processor pins and/or vias. This provides the best voltage response to the load.

Our FPGAs and processors come with a long legacy and heritage of design and support excellence. Designing the power solution for these or other devices comes with some responsibility somewhat outside of the compilers and VHDL tools. We have to supply enough current to the FPGA or processor to keep the voltage rails within the data sheet values. The responsibility is then to:

1. Use the load calculator tools for the processor or FPGA to estimate the load currents
2. Use the recommended bypassing and decoupling capacitors
3. Measure the actual currents and voltages on the prototype and communicate that information with the power designers
    a. . Take DC current measurements, Hall/Mag probe current measurements and voltage ripple measurements
4. Specify the correct POL converters
5. Validate the system over temperature; high temperature is worst case

We are glad to help with any questions you may have on pairing the right POL solution with your load FPGA or processor load base, layout, bypassing and noise reduction techniques.

For further information, contact **Paul Schimel**, Product Marketing Manager, Paul.Schimel@microchip.com

Events

Due to the global Covid-19 pandemic, almost all of the space conferences planned through August 2020 have been either canceled or postponed. Some event organizers have moved to a virtual event format. By the time you receive this newsletter, Microchip will have supported the SmallSat conference (August 1–6) with on-line activities including a virtual exhibition booth.

The IEEE® Nuclear and Space Radiation Effects Conference (NSREC) is also moving to a virtual format for 2020. At the time of writing this newsletter, details are still being worked out, however you can access the latest information directly from the NSREC web site.

The Microelectronic Workshop (MEWS) hosted by the Japan Aerospace Exploration Agency (JAXA) is also moving to partially virtual format. Details will be provided on the MEWS web site.

Microchip Technology Inc.
2355 West Chandler Blvd. Chandler,
Arizona, USA 85224-6199
(480) 792-7200 | www.microchip.com