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Total Ionizing Dose Test Report

No. 20T-RTAX4000D-CQ352-DGQYM1

February 2021

Table of Contents

I. Summary Table	3
II. Total Ionizing Dose (TID) Testing	3
A. Device-Under-Test (DUT) and Irradiation Parameters	4
B. Test Method.....	5
C. Design and Parametric Measurements	6
III. Test Results	8
A. Functionality.....	8
B. Power Supply Current (ICCA and ICCI)	8
C. Single-Ended 3.3 V LVTTTL Input Logic Threshold (VIL/VIH).....	12
D. Output-Drive Voltage (VOL/VOH).....	13
E. Propagation Delay.....	14
F. Transition Time.....	15
Appendix A: DUT Bias Diagram.....	27
Appendix B: Functionality Tests.....	30

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December 8, 2020

I. Summary Table

The TID tolerance for each tested parameter is summarized below in Table 1. The overall tolerance is limited by the standby power-supply current (ICC). The room temperature annealing allowed by 1019.8 to anneal down ICC is performed for approximately 7 days. Every DUT passes the major specifications listed in the table for 300 krad (SiO₂) of irradiation.

Table 1 Tolerances for Each Tested Parameter

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO ₂)
2. Power Supply Current (ICCA/ICCI)	Passed 300 krad (SiO ₂)
3. Input Threshold (VIL/VIH)	Passed 300 krad (SiO ₂)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO ₂)
5. Propagation Delay	Passed 300 krad (SiO ₂) for 10% degradation criterion
6. Transition Time	Passed 300 krad (SiO ₂)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the basis of an extensive database (see, for example, TID data of antifuse-based FPGAs at <http://www.klabs.org> and <http://www.microsemi.com/soc>) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 2 lists the DUT and irradiation parameters. During irradiation all inputs are grounded except for the inputs Burnin, oe_EAQ, enable_HSB and the utilized clocks (Rclock1-3 and Hclock1-4). The inputs Burnin, oe_EAQ and enable_HSB are set high to 3.3 V and a 1 KHz clock is provided to all clocks in order for the design to remain stable during irradiation. During anneal each input and output is tied to ground or VCCI through a 4.7 kΩ resistor. Appendix A contains the schematics of irradiation-bias circuits.

Table 2 DUT and Irradiation Parameters

Part Number	RTAX4000D
Package	CQFP352
Foundry	United Microelectronics Corp.
Technology	0.15 μm CMOS
DUT Design	MASTER_RTAX4000S_DESIGN_80_SP1
Die Lot Number	DQYM1
Quantity Tested	6
Serial Number	300 krad: 8733, 8750 200 krad: 8731, 8732 100 krad: 8713, 8714
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad (SiO ₂)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V / 1.5 V
I/O Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

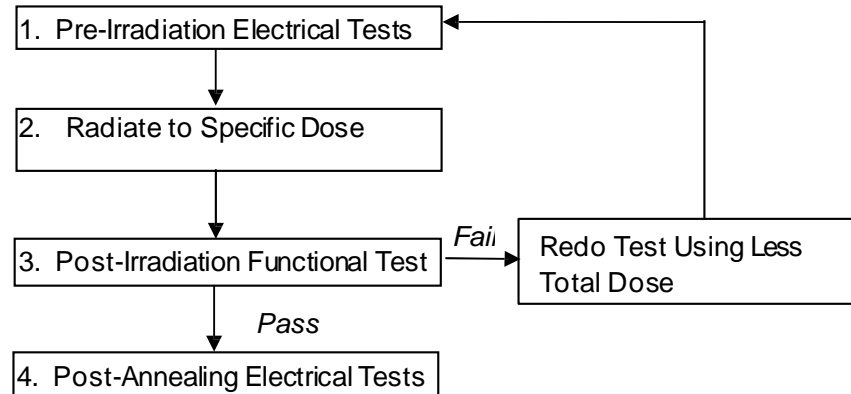


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8, is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi SoC Products Group products manufactured by sub-micron CMOS technology. Elevated temperature annealing actually reduces the effects originated from radiation-induced leakages. As indicated by testing data in the following sections, the predominant radiation effects in RTAX4000S are due to radiation-induced leakages.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

The DUT uses a high utilization generic design (RTAX4000S_CQ352_MASTER) to evaluate total dose effects for typical space applications. The schematics of this design are documented in Appendix B.

The functionality is measured at 1 MHz and 50 MHz using the minimum and maximum power specifications shown in Table 3.

Table 3 Minimum and Maximum Power Specifications for RTAX-D Devices

Supply Voltage	Minimum	Recommended	Maximum
1.5 V Core	1.4 V	1.5 V	1.6 V
3.3 V I/O	3.0 V	3.3 V	3.6 V
3.3 V VCCDA I/O	3.0 V	3.3 V	3.6 V

The functionality test design is subdivided into two blocks, the EAQ (Enhanced Antifuse Qualification) and the QBI (Qualification Burn-In). The EAQ block includes three 1458-bit shift registers and tests the I/Os (1560 I/O registers and 520 I/Os) and RAM (1x16384 RAM). The QBI block tests all offered macros and I/O standards. The results from the functional tests are obtained from the following outputs: IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI. Details on the Functionality Test are shown in Appendix B.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic threshold (VIL/VIH) is tested on single-ended inputs Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Reseth, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, and A_Pattern_Length_0. The output-drive voltage (VOL/VOH) is measured on single-ended outputs Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8.

The propagation delays are measured on the outputs of five delay strings; each one comprises of 1,170 NAND4-inverters. There are 6 delay measurements: one measurement for each delay string and a total delay measurement obtained from cascading all the delay strings. The propagation delay is defined as the time delay from the triggering edge at the HClock1 input to the switching edge at the output. The delay measurements are taken for both rising and falling edges, the average reading of the two measurements is reported. The transition characteristics, measured on the output delay_out_SEU4, are shown as oscilloscope captures.

Table 4 lists measured electrical parameters and the corresponding logic design.

Table 4 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Single ended inputs (Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, A_Pattern_Length_0)
4. Output Drive (VOL/VOH)	Single-ended outputs (Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8)
5. Propagation Delay	String of NAND4-inverters. Measured from output delay_out_SEU4
6. Transition Characteristic	NAND4-inverter output (delay_out_SEU4)

III. Test Results

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing.

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

The logic-array power supply (VCCA) is 1.5 V, and the IO power supply (VCCI) is 3.3 V. Their standby currents, ICCA and ICCI, are monitored influx. Figure 2-7 show the influx ICCA and ICCI versus total dose for the DUTs.

Referring to TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICC, should be defined as the addition of highest ICCI, ICCDA, and ICCDIFFA values in Table 2-4 of the *RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs datasheet* posted on the Microsemi SoC Products Group website:

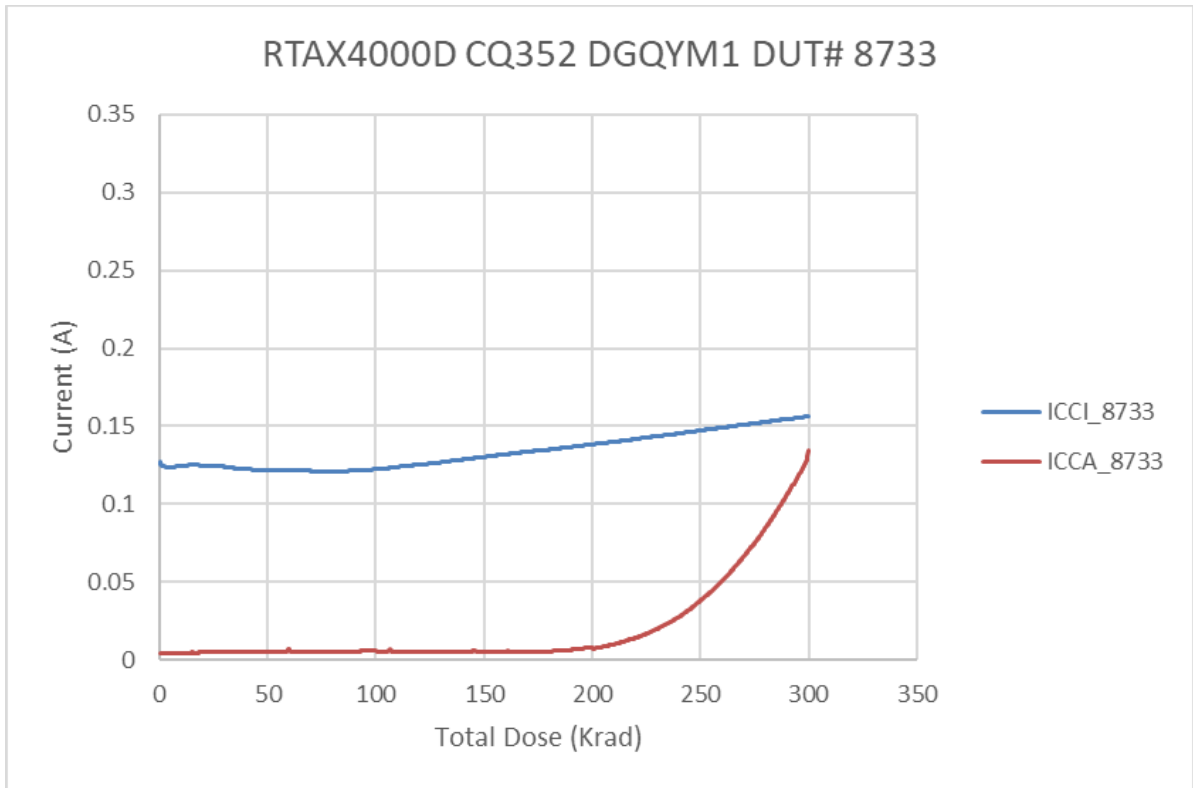
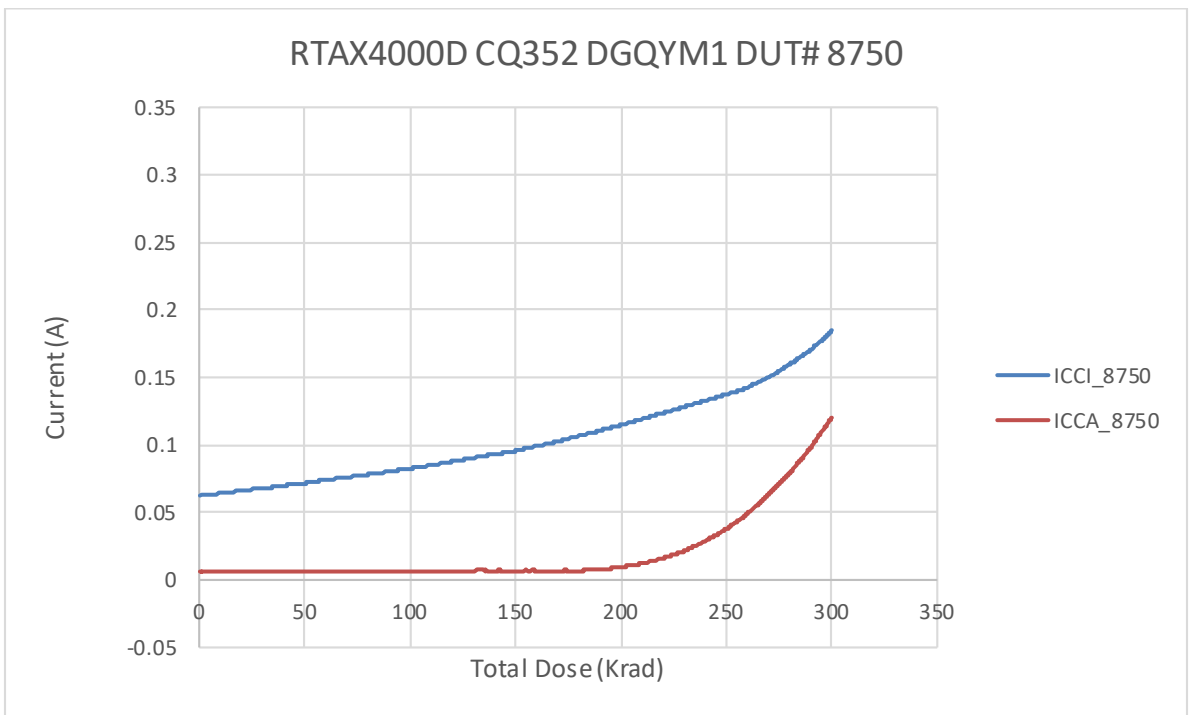
http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

Therefore, the PIPL for ICCA is 600 mA, and the PIPL for ICCI is 60 mA.

Table 5 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 5 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-Irrad.	Post-Irrad.	Post-Ann.	Pre-Irrad.	Post-Irrad.	Post-Ann.
8713	100 krad	5	5.60	4	14	16.6	15
8714	100 krad	5	5.90	5	14	16.1	15
8731	200 krad	6	6.80	6	14	178	29
8732	200 krad	5	9.30	5	14	172	32
8733	300 krad	4	118	11	14	155	56
8750	300 krad	6	115	12	14	184	64


Figure 2 DUT 8733 Influx ICCI and ICCA

Figure 3 DUT 8750 Influx ICCI and ICCA

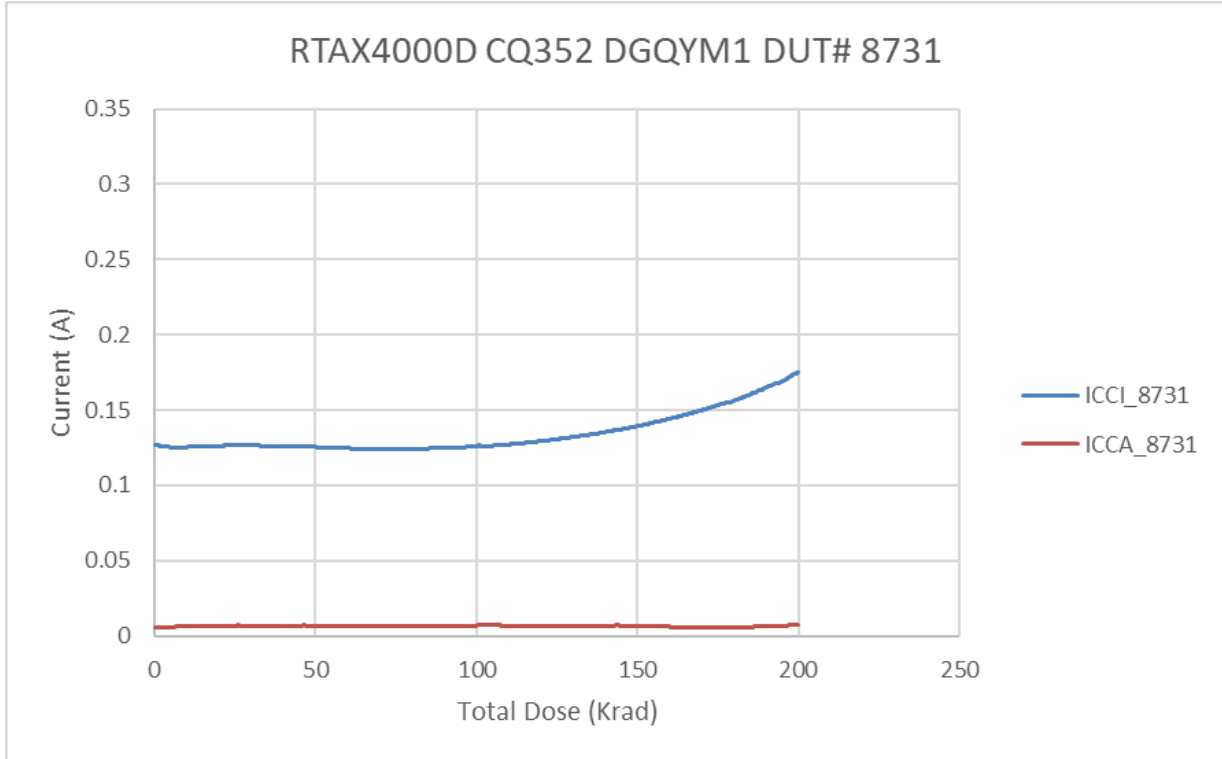


Figure 4 DUT 8731 Influx ICCI and ICCA

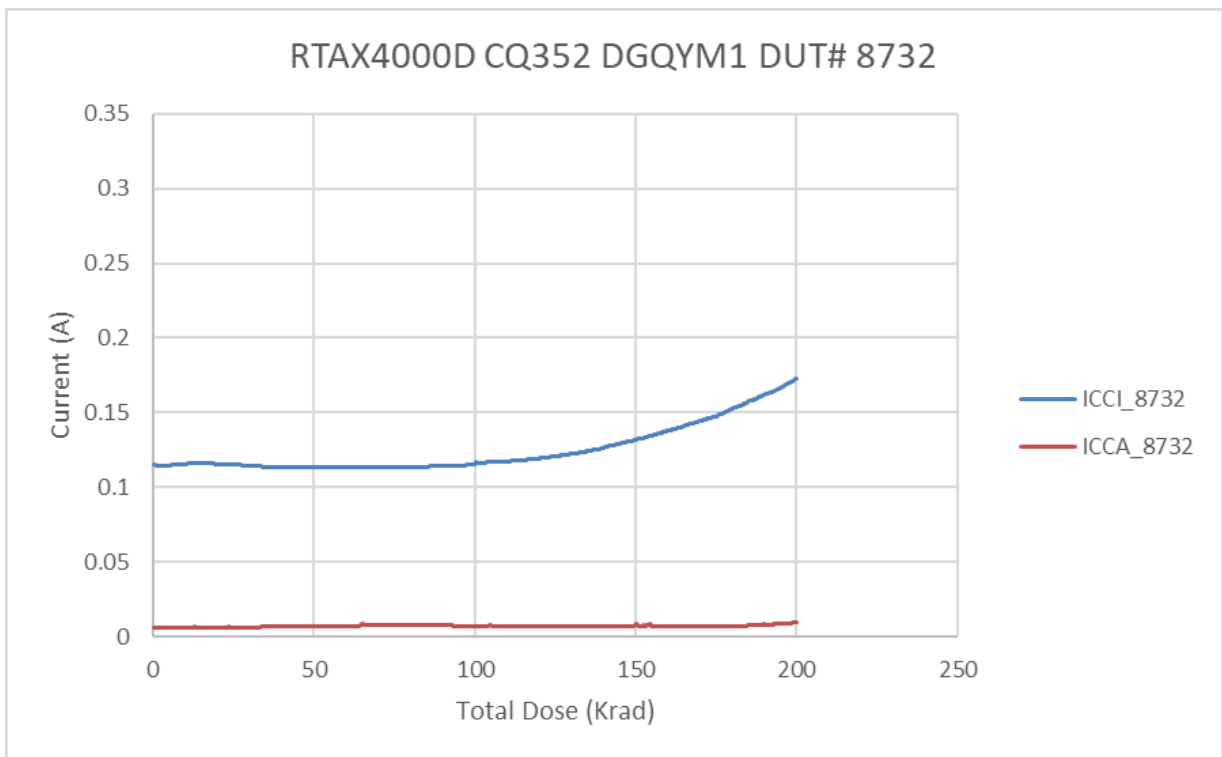


Figure 5 DUT 8732 Influx ICCI and ICCA

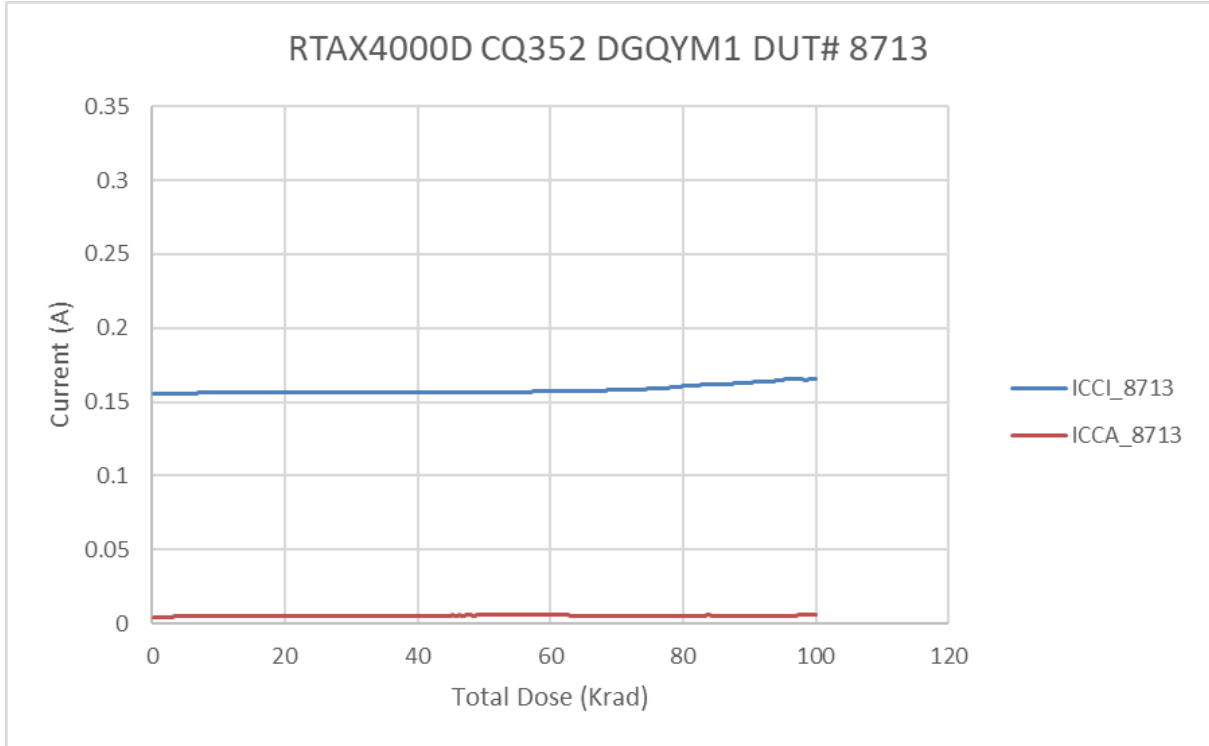


Figure 6 DUT 8713 Influx ICCI and ICCA

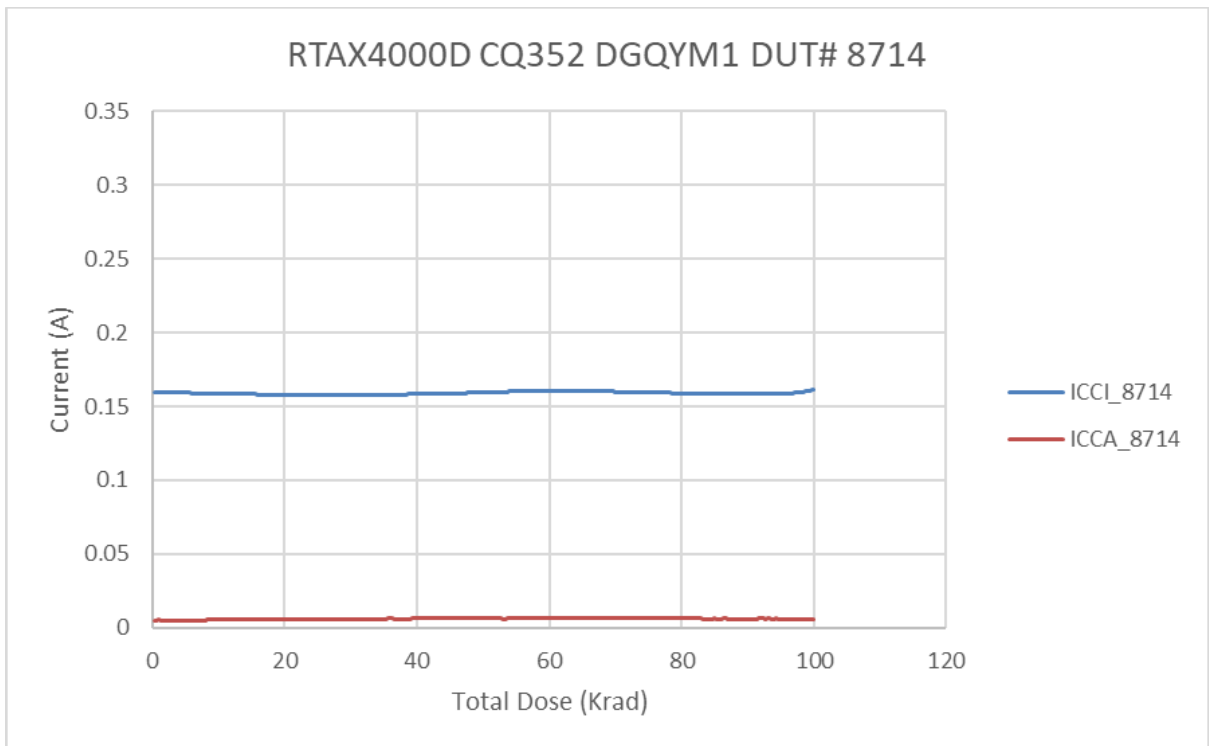


Figure 7 DUT 8714 Influx ICCI and ICCA

C. Single-Ended 3.3 V LVTTTL Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design, often just input and output buffers, starts to switch: VIH is the input trip point when the input is going high to low; VIL is the input trip point when the input is going low to high. They are listed in Tables 6 and 7. The difference between the pre-irradiation and post-annealing data is usually negligibly small.

Table 6 Pre-Irradiation and Post-Annealing Input Thresholds (VIL)

Pin \ DUT(Dose)	8733 (300 krad)		8750 (300 krad)		8731 (200 krad)		8732 (200 krad)		8713 (100 krad)		8714 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
SEU_sel	1.345	1.325	1.345	1.325	1.345	1.330	1.345	1.330	1.350	1.345	1.350	1.345
zoom_sel_n_0	1.350	1.330	1.350	1.330	1.350	1.335	1.350	1.335	1.355	1.350	1.355	1.345
zoom_sel_n_1	1.345	1.325	1.345	1.325	1.345	1.330	1.345	1.330	1.345	1.340	1.350	1.345
zoom	1.345	1.325	1.345	1.325	1.340	1.330	1.340	1.330	1.350	1.345	1.350	1.340
TOG_n	1.360	1.355	1.360	1.355	1.360	1.355	1.360	1.355	1.360	1.355	1.370	1.365
Set_n	1.345	1.335	1.345	1.335	1.345	1.335	1.345	1.335	1.345	1.340	1.350	1.345
Resetn	1.345	1.345	1.350	1.345	1.350	1.345	1.350	1.350	1.355	1.355	1.360	1.360
oe_EAQ	1.360	1.355	1.365	1.350	1.360	1.355	1.370	1.360	1.365	1.360	1.375	1.365
enable_HSB	1.350	1.345	1.350	1.345	1.350	1.345	1.350	1.345	1.350	1.350	1.355	1.355
IO_Pattern_Length_1	1.355	1.350	1.360	1.355	1.355	1.355	1.360	1.355	1.360	1.360	1.360	1.360
IO_Pattern_Length_2	1.355	1.350	1.360	1.350	1.360	1.350	1.360	1.350	1.360	1.355	1.360	1.360

Table 7 Pre-Irradiation and Post-Annealing Input Thresholds (VIH)

Pin \ DUT(Dose)	8733 (300 krad)		8750 (300 krad)		8731 (200 krad)		8732 (200 krad)		8713 (100 krad)		8714 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
SEU_sel	1.635	1.610	1.635	1.610	1.630	1.610	1.635	1.615	1.640	1.625	1.640	1.625
zoom_sel_n_0	1.625	1.600	1.625	1.600	1.625	1.605	1.625	1.605	1.630	1.620	1.630	1.615
zoom_sel_n_1	1.630	1.610	1.635	1.610	1.635	1.615	1.635	1.615	1.635	1.620	1.640	1.625
zoom	1.630	1.610	1.630	1.610	1.630	1.610	1.630	1.615	1.640	1.625	1.635	1.625
TOG_n	1.645	1.640	1.645	1.640	1.645	1.640	1.650	1.640	1.645	1.640	1.655	1.650
Set_n	1.630	1.620	1.635	1.615	1.630	1.615	1.635	1.620	1.630	1.625	1.635	1.630
Resetn	1.625	1.620	1.630	1.625	1.625	1.620	1.630	1.625	1.635	1.630	1.635	1.630
oe_EAQ	1.635	1.625	1.635	1.620	1.635	1.625	1.645	1.630	1.640	1.630	1.650	1.640
enable_HSB	1.635	1.625	1.635	1.630	1.635	1.625	1.635	1.630	1.635	1.630	1.640	1.635
IO_Pattern_Length_1	1.645	1.635	1.655	1.645	1.645	1.640	1.645	1.640	1.650	1.645	1.650	1.645
IO_Pattern_Length_2	1.630	1.620	1.635	1.620	1.635	1.625	1.635	1.625	1.635	1.625	1.635	1.630

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 6 and 7. The post-annealing data are within the specification limits; in each case, the radiation-induced degradation is within 10%.

Table 6 Pre-Irradiation and Post-Annealing VOL (mV)

Pin \ DUT(Dose)	8733 (300 krad)		8750 (300 krad)		8731 (200 krad)		8732 (200 krad)		8713 (100 krad)		8714 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	163.31	157.96	157.96	157.96	157.96	162.88	163.35	163.35	162.88	163.31	164.79	164.79
Array_out_EAQ_1	179.7	171.2	181.5	173.0	180.5	171.8	182.2	173.6	182.2	174.2	180.4	172.5
Array_out_EAQ_2	196.95	172.55	172.55	172.63	172.63	178.88	178.88	178.88	178.88	196.95	198.28	198.28
Global_Monitor_EAQ	187.24	183.86	191.93	185.03	187.32	174.56	187.55	176.05	186.70	177.14	191.07	188.23
Shiftout3	18.13	17.40	18.28	17.32	17.89	17.40	17.66	16.93	17.66	17.40	18.44	17.87
Shiftout7	18.51	17.78	19.06	18.10	18.12	17.24	18.59	17.63	18.59	17.70	19.37	18.17
Shiftout8	187.2	177.8	188.0	177.5	185.5	177.4	184.7	176.1	184.6	178.4	194.1	183.1
RAM_Monitor_EAQ	18.43	17.38	17.38	17.23	17.23	17.38	17.46	17.46	17.38	18.43	18.50	18.50
RAM_out_EAQ_0	19.81	16.54	16.54	16.85	16.85	17.48	17.32	17.32	17.48	19.81	19.88	19.88
RAM_out_EAQ_4	17.41	17.46	17.46	16.60	16.60	16.99	17.30	17.30	16.99	17.41	17.25	17.25
RAM_out_EAQ_8	191.6	198.5	194.5	200.9	189.7	182.7	192.0	182.8	190.9	187.9	195.7	204.8

Table 7 Pre-Irradiation and Post-Annealing VOH (V)

Pin \ DUT(Dose)	8733 (300 krad)		8750 (300 krad)		8731 (200 krad)		8732 (200 krad)		8713 (100 krad)		8714 (100 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	2.740	2.739	2.744	2.742	2.736	2.737	2.737	2.737	2.740	2.742	2.739	2.742
Array_out_EAQ_1	2.73	2.73	2.73	2.73	2.73	2.73	2.73	2.73	2.73	2.73	2.73	2.73
Array_out_EAQ_2	2.731	2.723	2.733	2.725	2.726	2.720	2.727	2.721	2.728	2.712	2.727	2.711
Global_Monitor_EAQ	2.723	2.717	2.721	2.717	2.721	2.726	2.722	2.726	2.722	2.728	2.724	2.721
Shiftout3	2.959	2.957	2.959	2.958	2.959	2.958	2.959	2.958	2.959	2.960	2.960	2.959
Shiftout7	2.960	2.958	2.960	2.958	2.960	2.959	2.959	2.959	2.960	2.960	2.960	2.960
Shiftout8	2.722	2.722	2.723	2.723	2.722	2.723	2.724	2.725	2.723	2.726	2.718	2.725
RAM_Monitor_EAQ	2.959	2.957	2.959	2.957	2.959	2.958	2.959	2.958	2.959	2.959	2.959	2.959
RAM_out_EAQ_0	2.959	2.956	2.959	2.956	2.958	2.958	2.959	2.958	2.958	2.958	2.959	2.957
RAM_out_EAQ_4	2.959	2.959	2.960	2.957	2.959	2.958	2.959	2.958	2.959	2.960	2.959	2.960

E. Propagation Delay

Table 8 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case, the percentage change is well below 10%.

Table 8 Radiation-Induced Propagation Delay Degradations

Delay (μ s)							
	DUT	Total Dose	Pre-rad	100 krad	200 krad	300 krad	Post-ann
	8733	300 krad	7.58	7.57	7.71	7.85	7.49
	8750	300 krad	7.35	7.31	7.48	7.61	7.22
	8731	200 krad	7.49	7.51	7.56	-	7.37
	8732	200 krad	7.38	7.39	7.54	-	7.24
	8713	100 krad	7.43	7.42	-	-	7.33
	8714	100 krad	7.44	7.44	-	-	7.34
Radiation Δ (%)							
	DUT	Total Dose	Pre-rad	100 krad	200 krad	300 krad	Post-ann
	8733	100 krad	-	-0.13%	1.65%	3.50%	-1.25%
	8750	100 krad	-	-0.61%	1.77%	3.47%	-1.77%
	8731	200 krad	-	0.20%	0.87%	-	-1.67%
	8732	200 krad	-	0.14%	2.10%	-	-1.90%
	8713	300 krad	-	-0.07%	-	-	-1.35%
	8714	300 krad	-	0.00%	-	-	-1.41%

F. Transition Time

Figure 8a to Figure 19b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

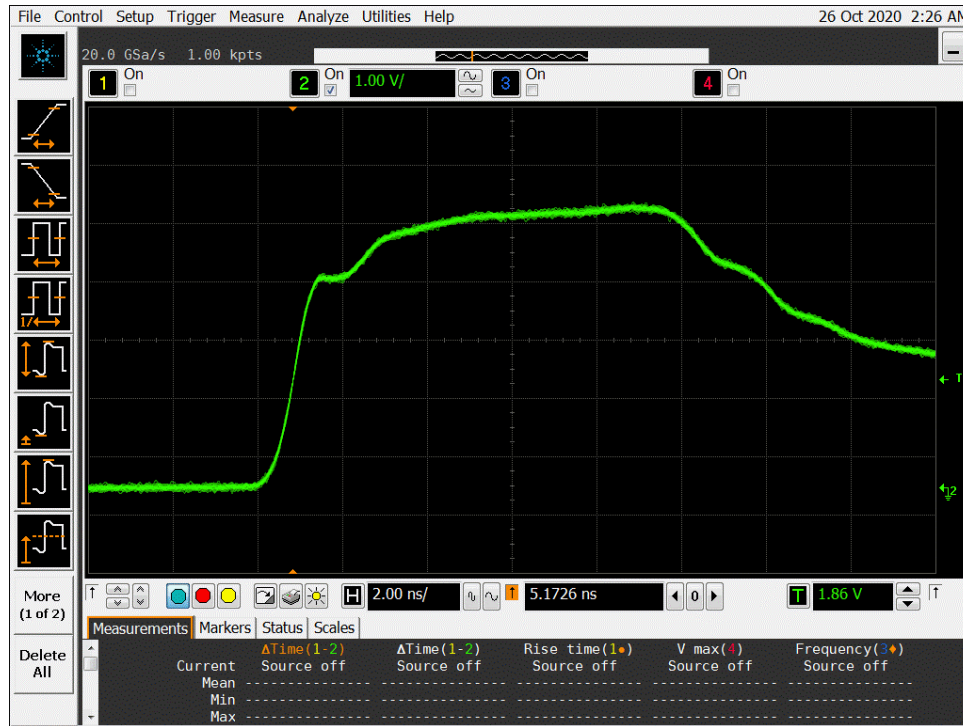


Figure 8a DUT 8733 Pre-Irradiation Rising Edge.



Figure 8b DUT 8733 Post-Annealing Rising Edge.

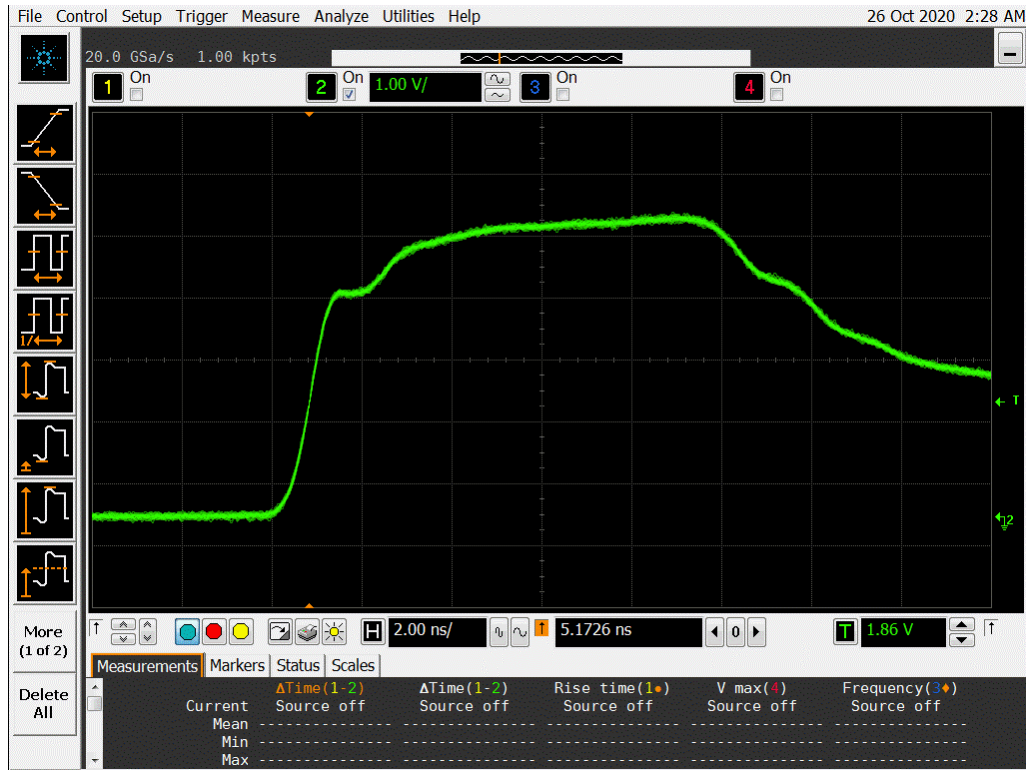


Figure 9a DUT 8750 Pre-irradiation Rising Edge.



Figure 9b DUT 8750 Post-Annealing Rising Edge.

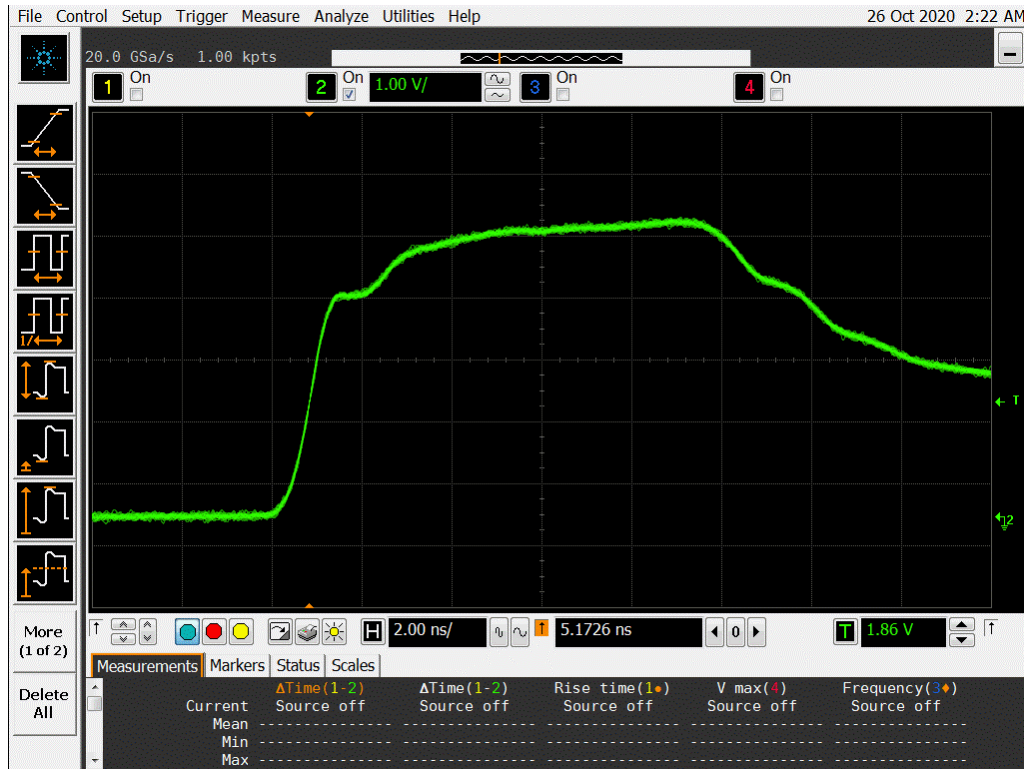


Figure 10a DUT 8731 Pre-Irradiation Rising Edge.



Figure 10b DUT 8731 Post-Annealing Rising Edge.

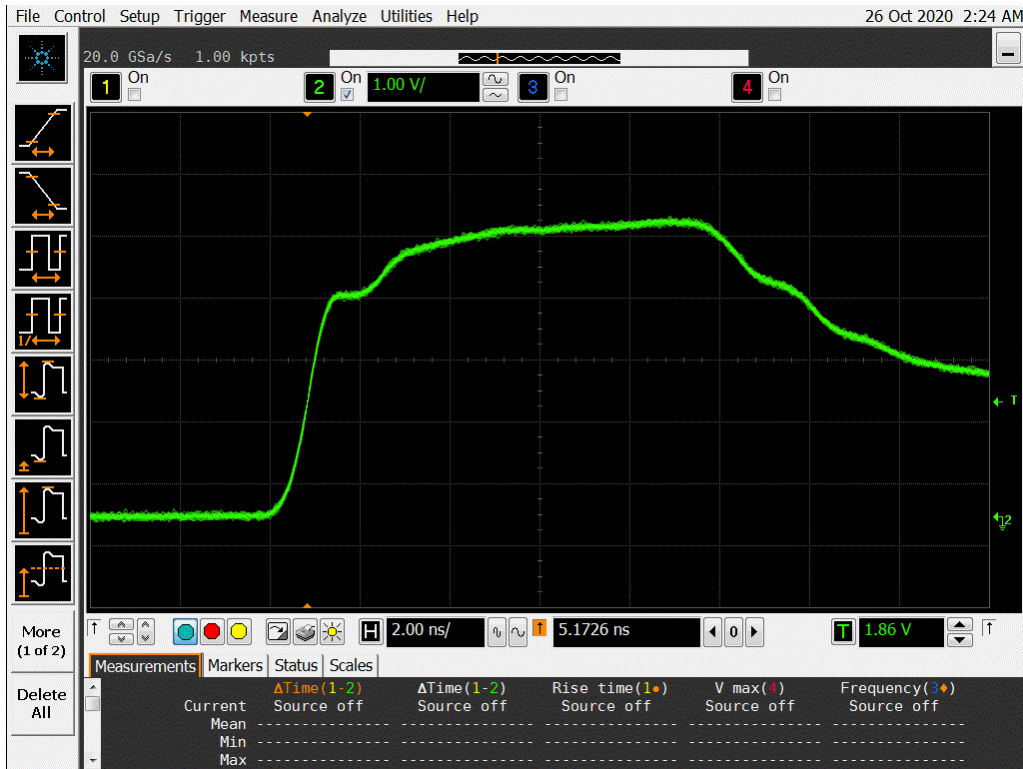


Figure 11a DUT 8732 Pre-Irradiation Rising Edge.

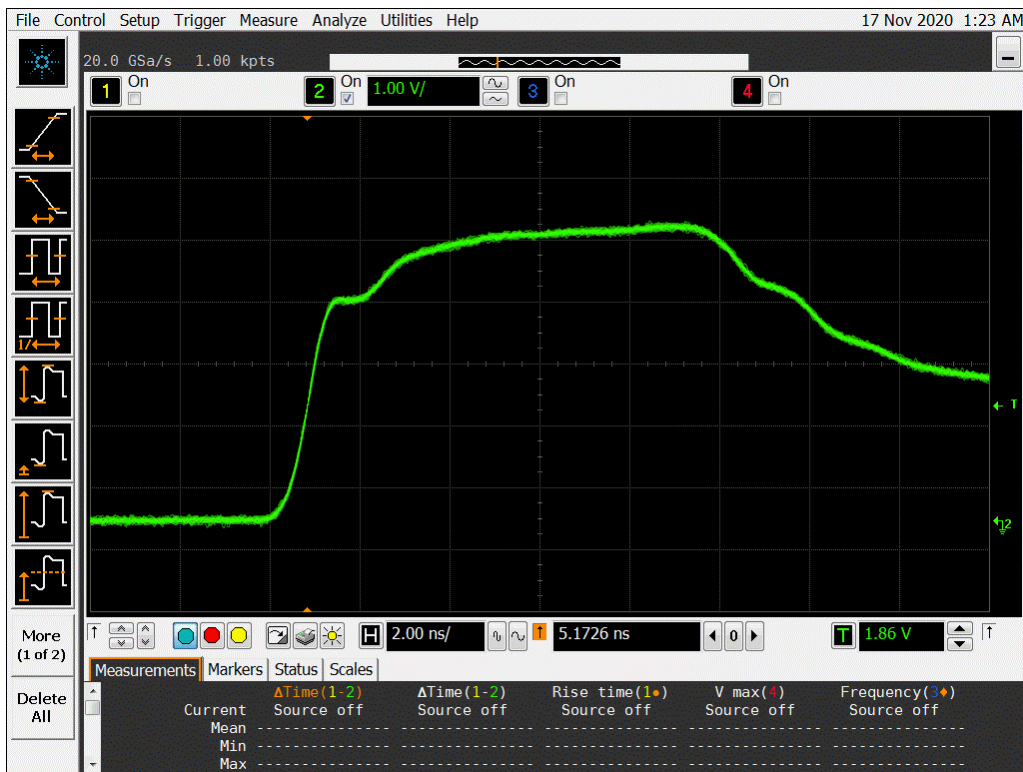


Figure 11b DUT 8732 Post-Annealing Rising Edge.

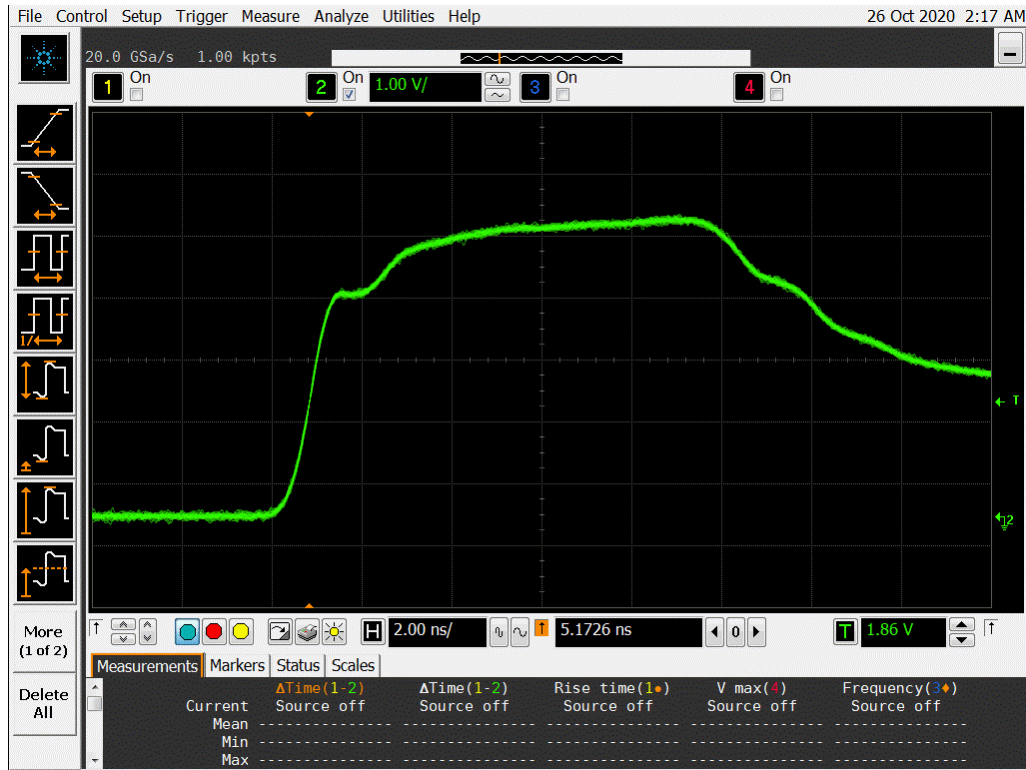


Figure 12a DUT 8713 Pre-Irradiation Rising Edge.

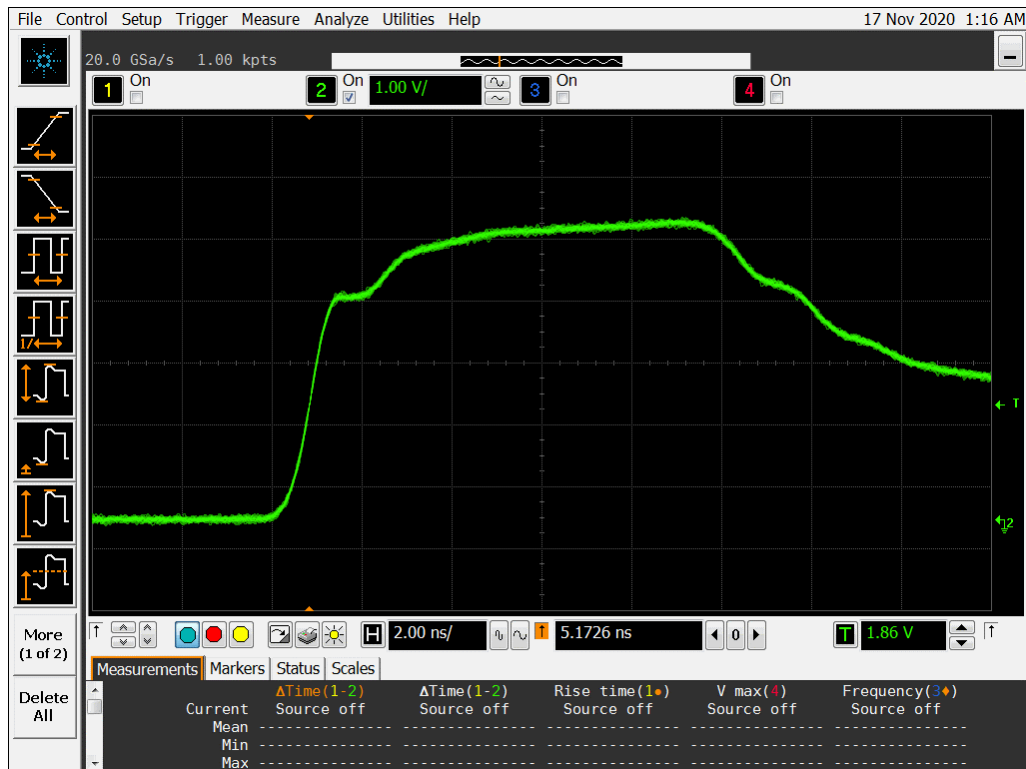


Figure 12b DUT 8713 Post-Annealing Rising Edge.

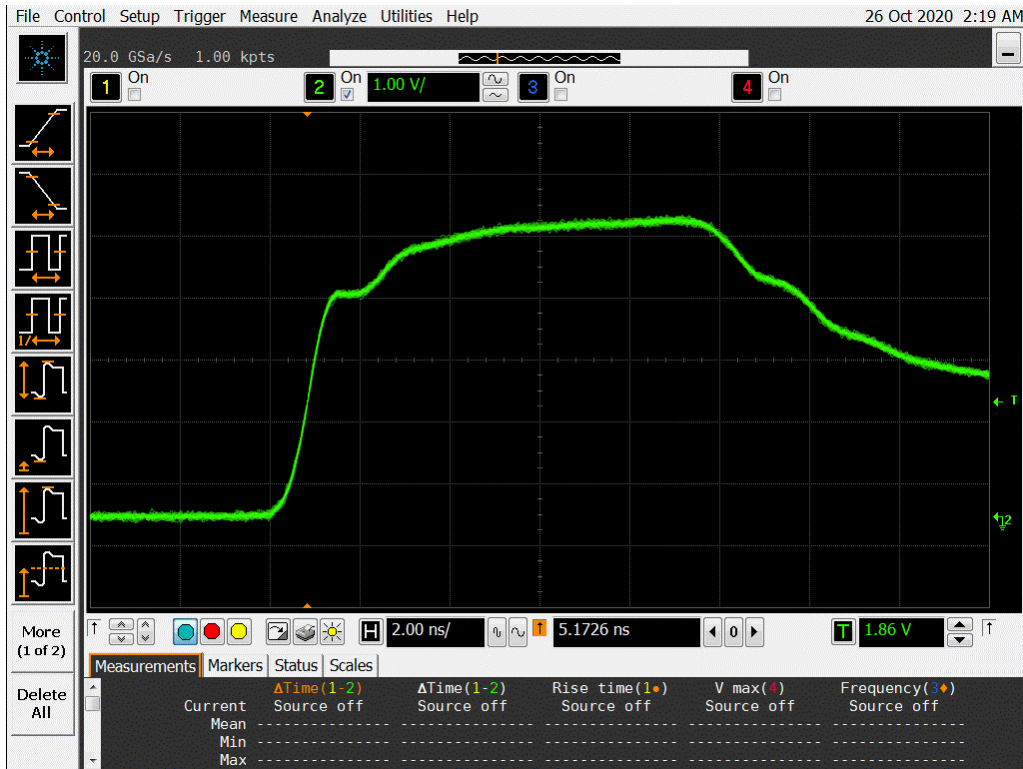


Figure 13a DUT 8714 Pre-Irradiation Rising Edge.



Figure 13b DUT 8714 Post-Annealing Rising Edge.

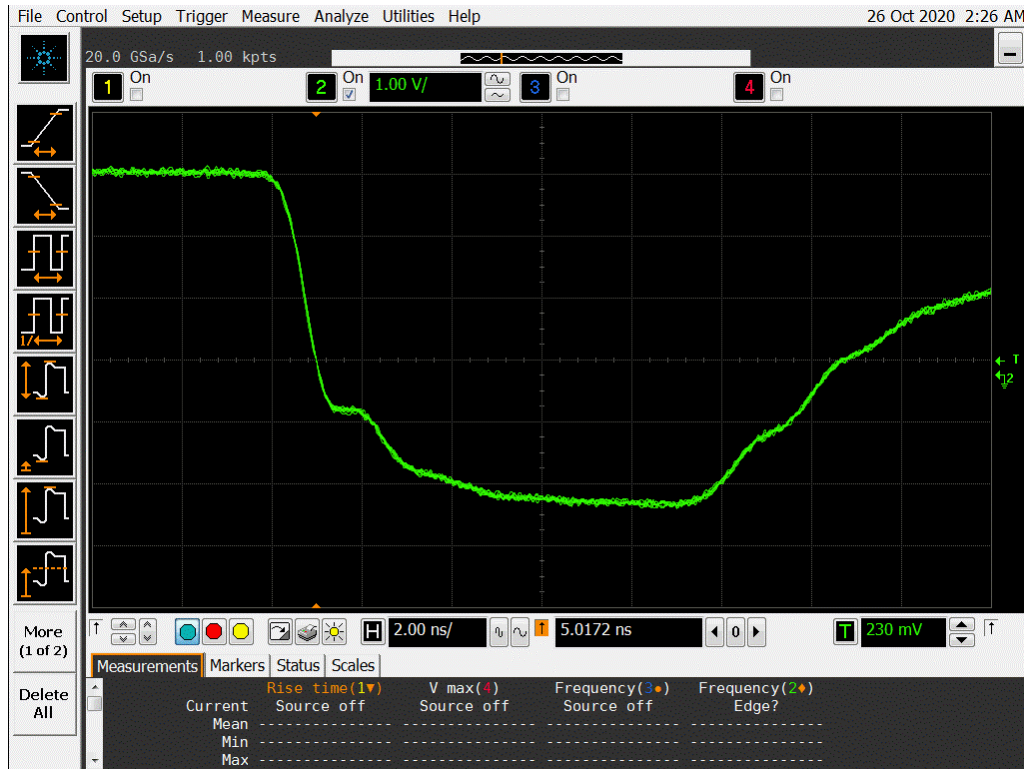


Figure 14a DUT 8733 Pre-Irradiation Falling Edge.

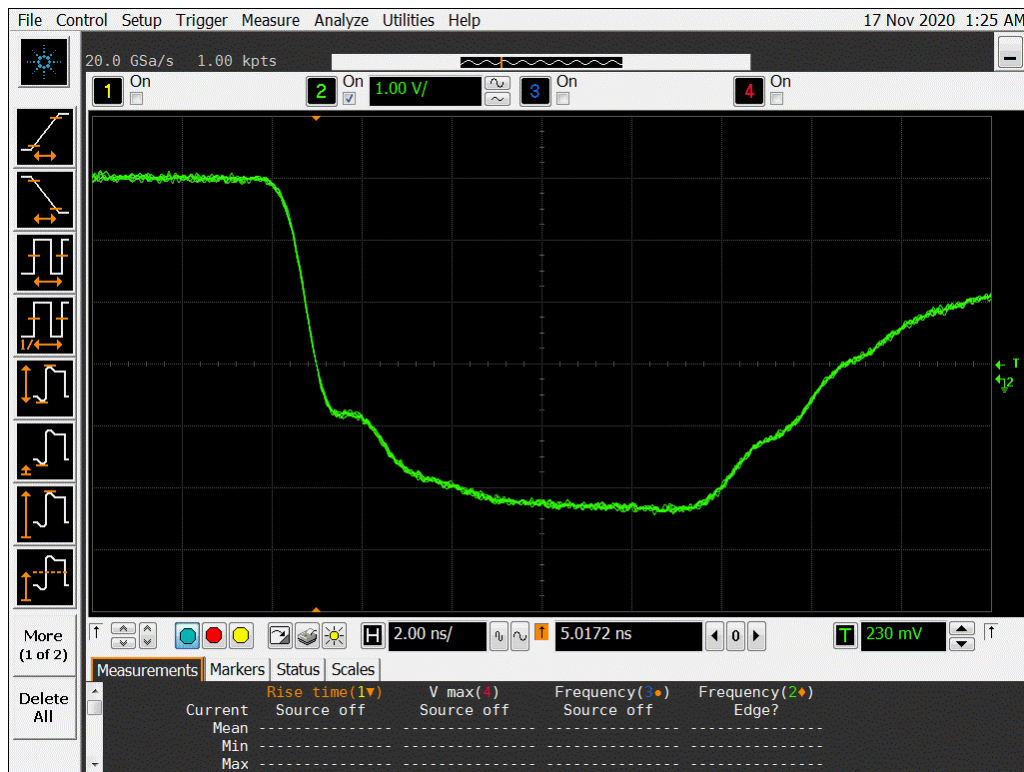


Figure 14b DUT 8733 Post-Annealing Falling Edge.

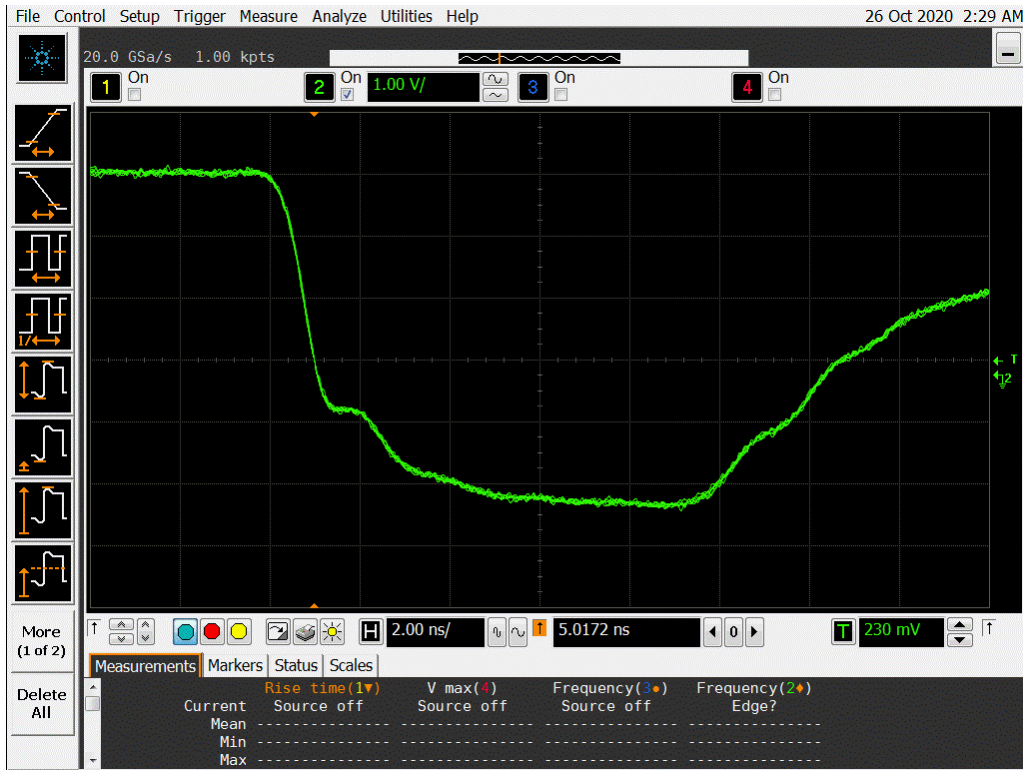


Figure 15a DUT 8750 Pre-Irradiation Falling Edge.

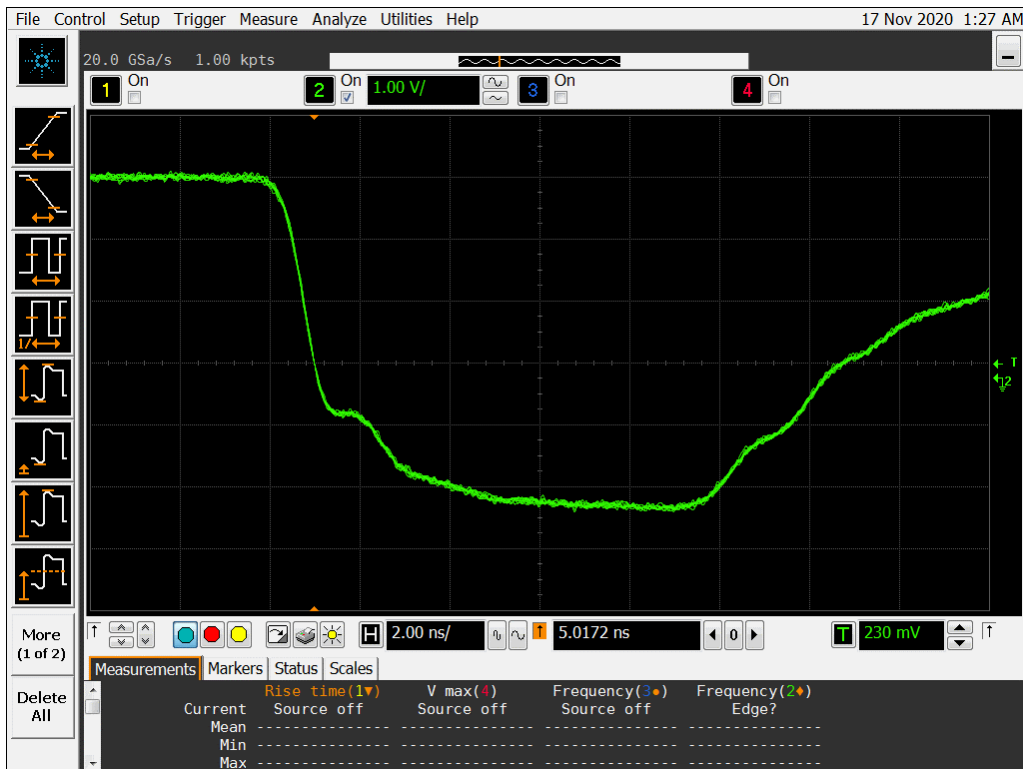


Figure 15b DUT 8750 Post-Annealing Falling Edge.

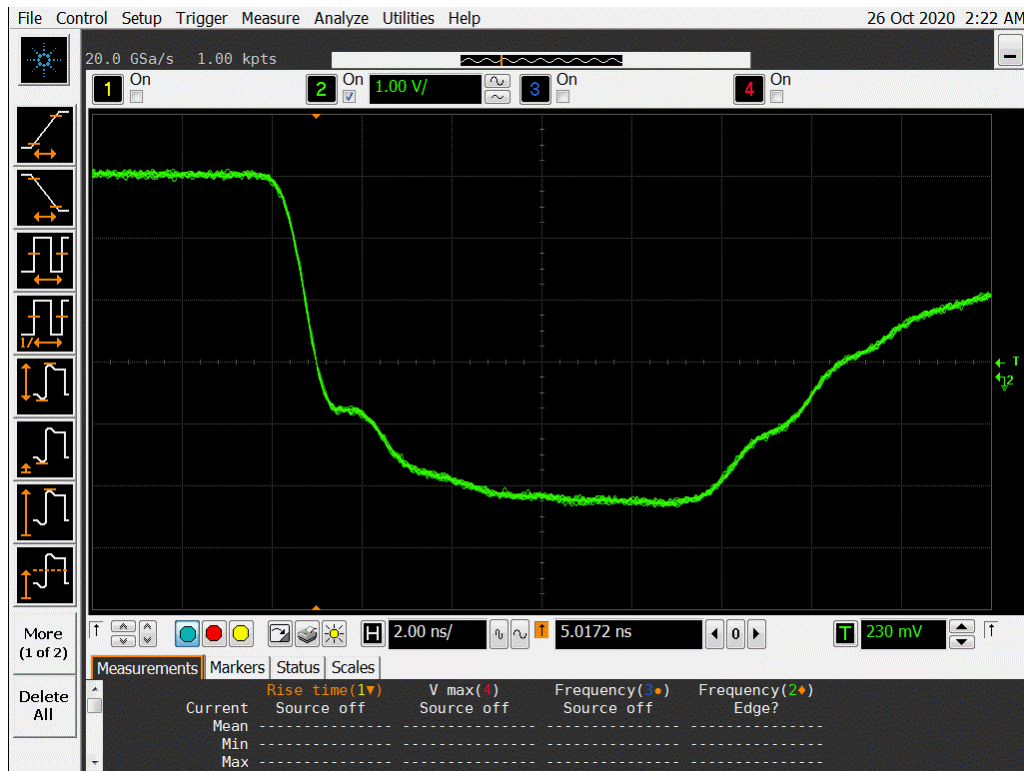


Figure 16a DUT 8731 Pre-Irradiation Falling Edge.

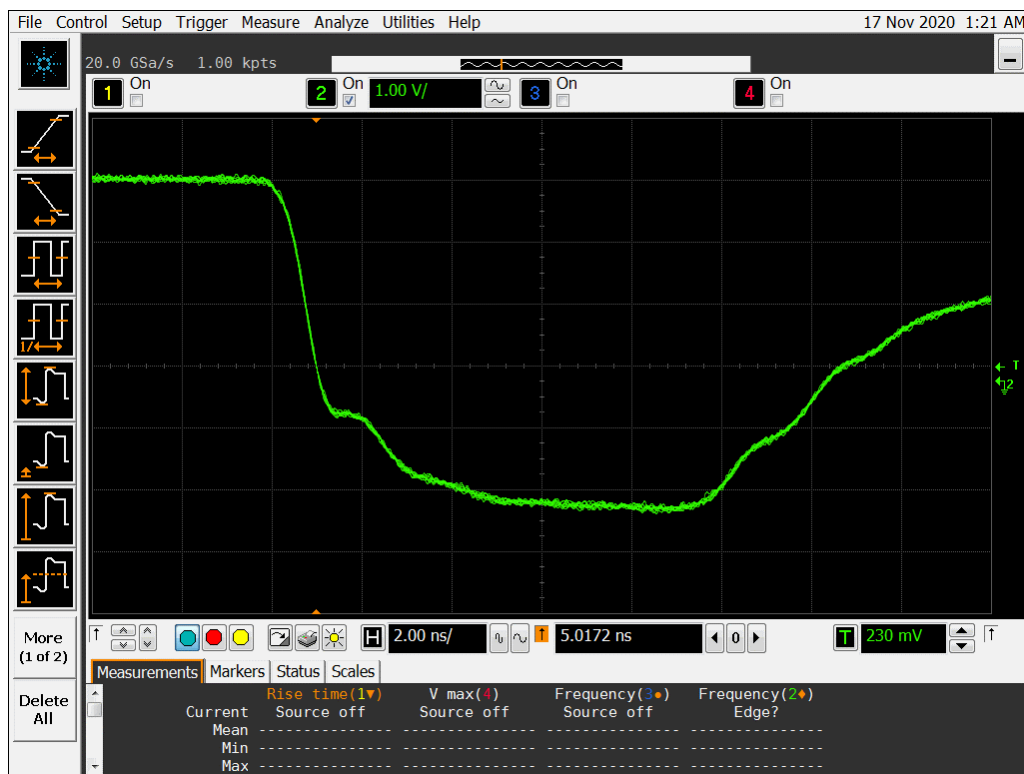


Figure 16b DUT 8731 Post-Annealing Falling Edge.

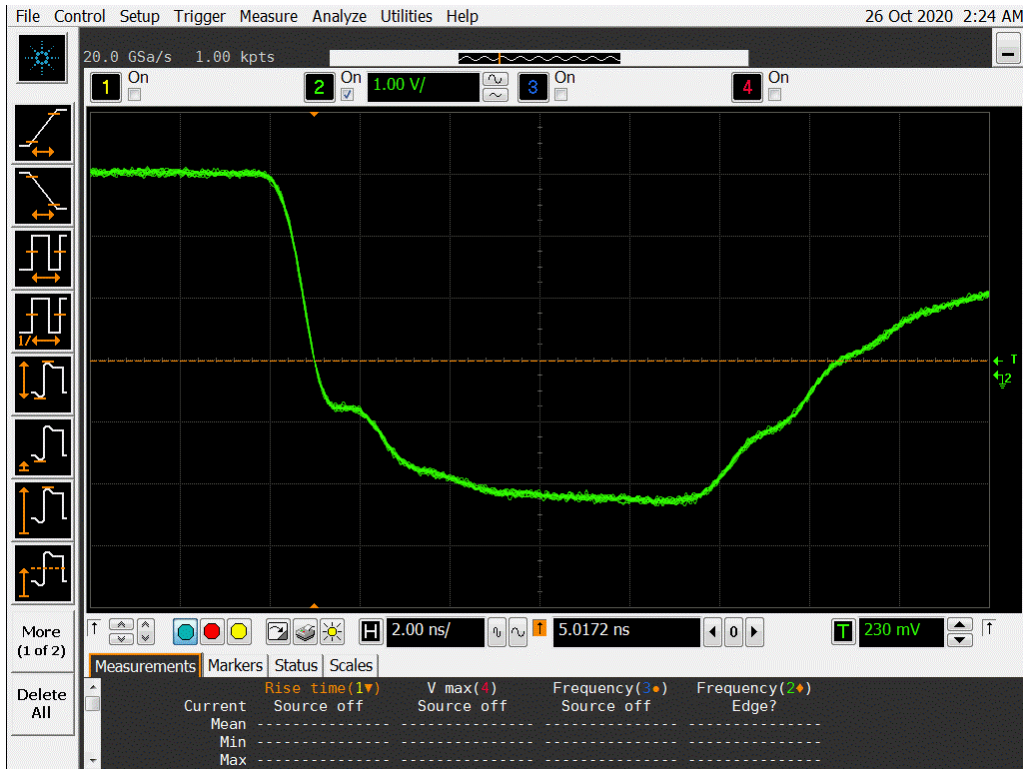


Figure 17a DUT 8732 Pre-Irradiation Falling Edge.

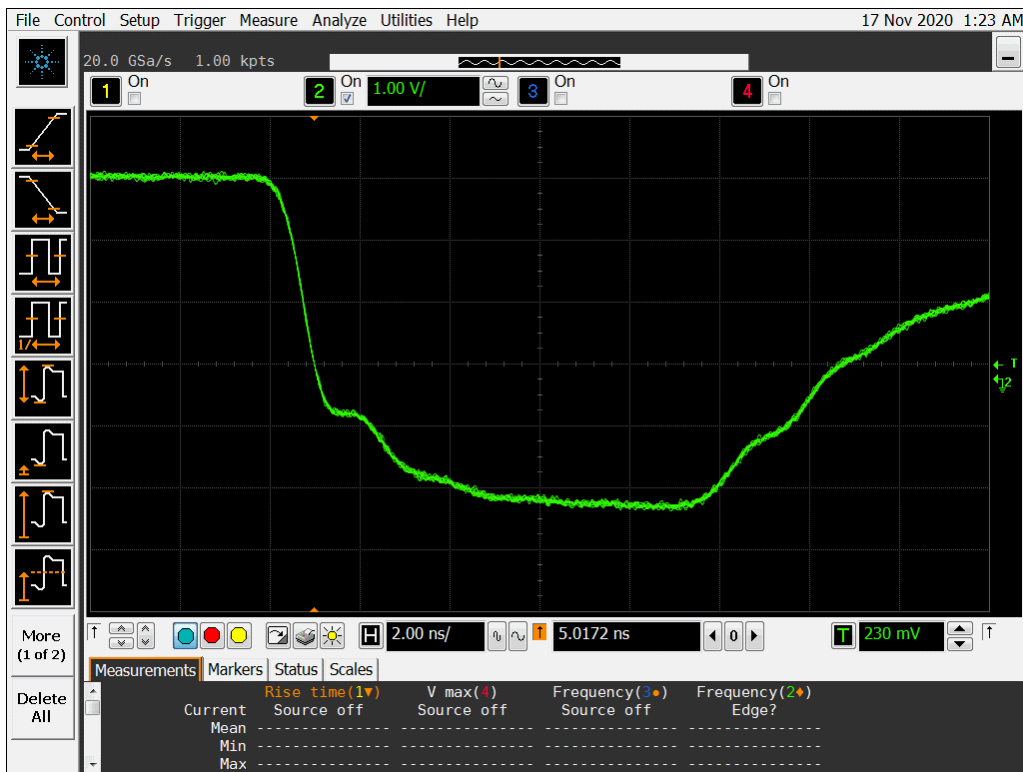


Figure 17b DUT 8732 Post-Annealing Falling Edge.

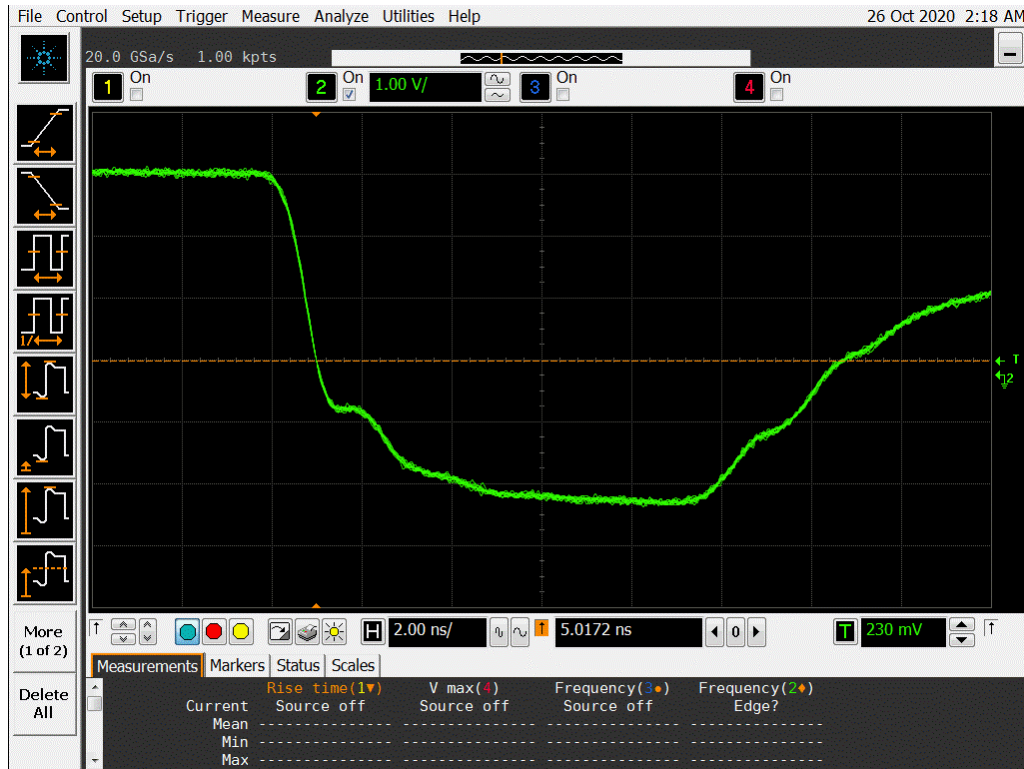


Figure 18a DUT 8713 Pre-Irradiation Falling Edge.

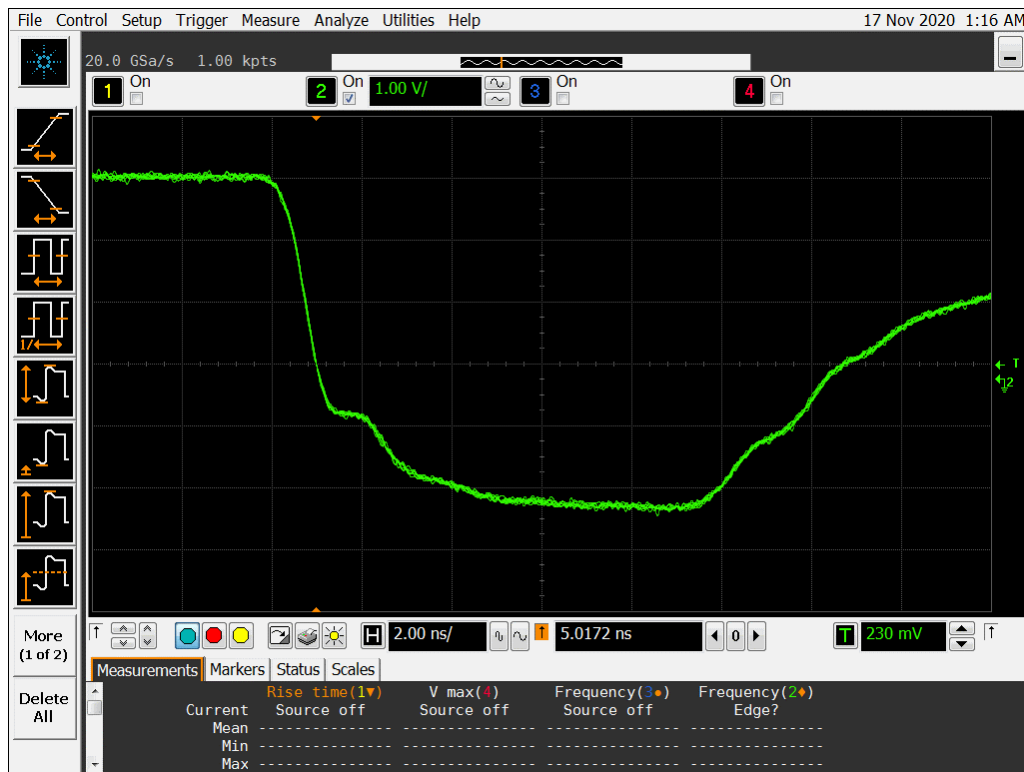


Figure 18b DUT 8713 Post-Annealing Falling Edge.

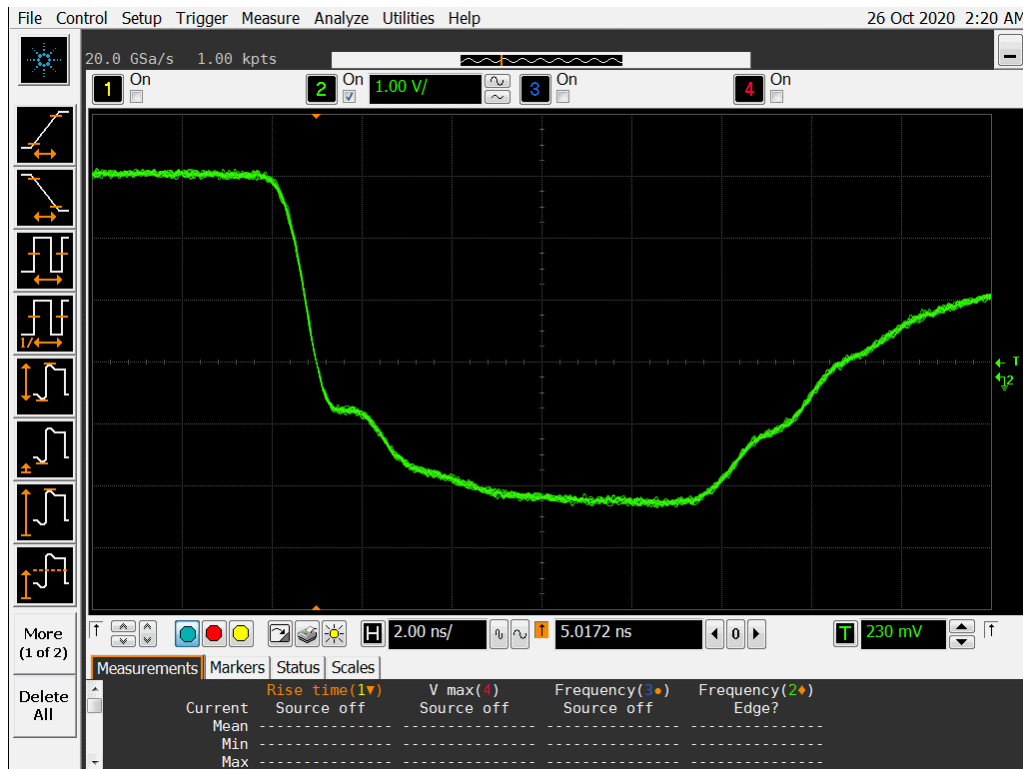


Figure 19a DUT 8714 Pre-Irradiation Falling Edge.

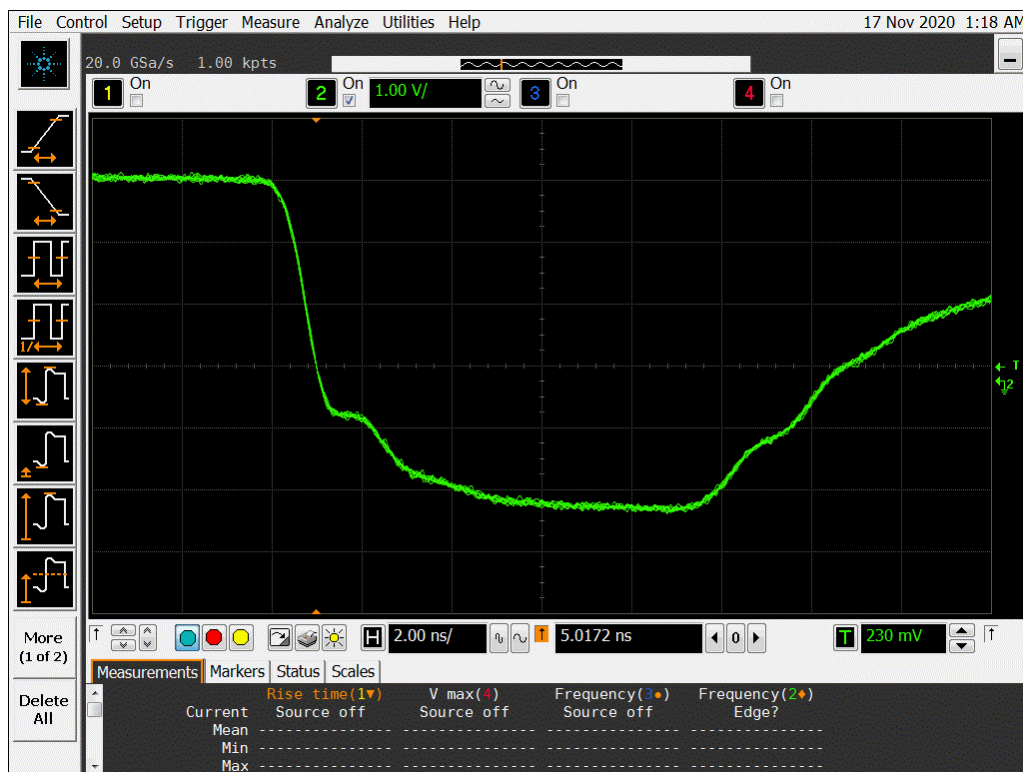


Figure 19b DUT 8714 Post-Annealing Falling Edge.

Appendix A: DUT Bias Diagram

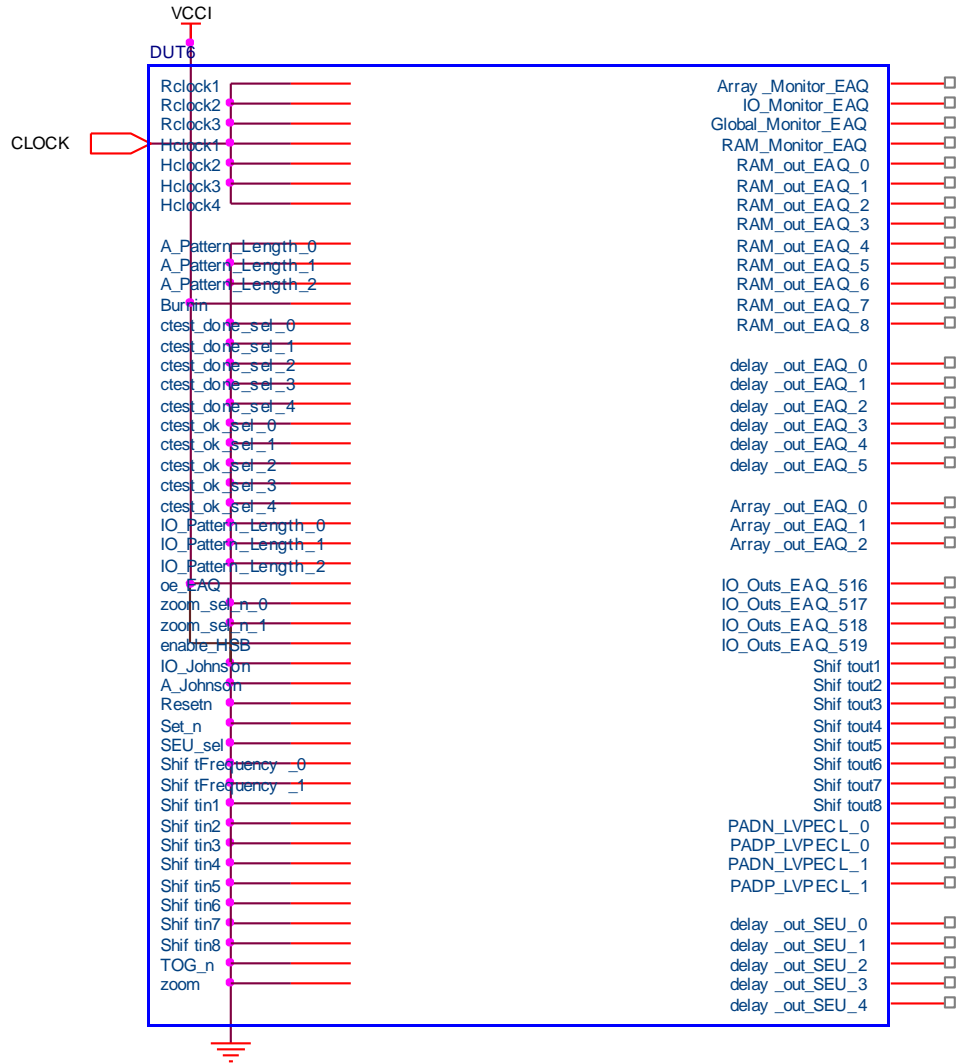


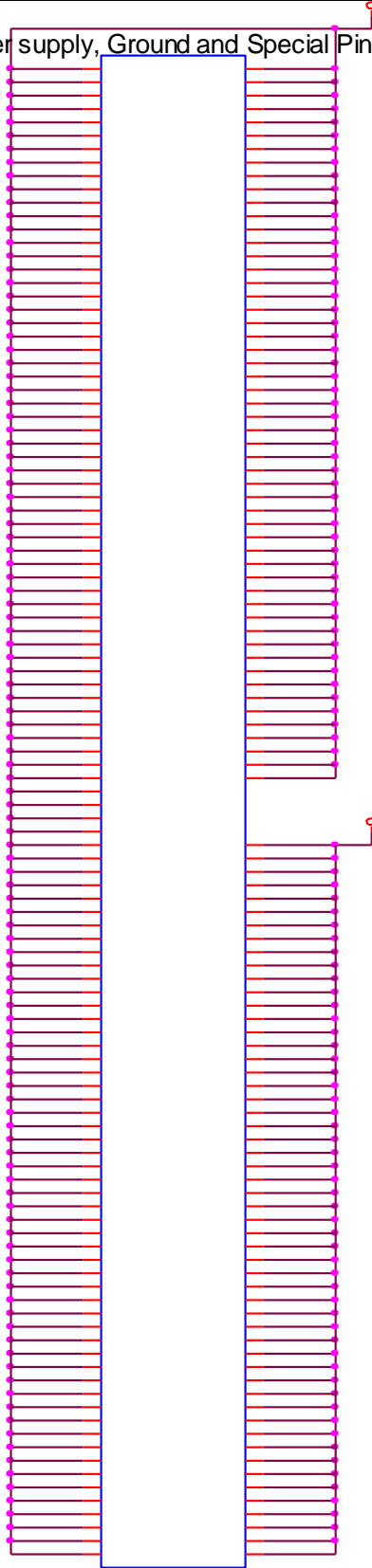
Figure A1 I/O Bias During Irradiation

VCCI_3.3

DUT1D		
B11		AB10
B14	VCCI 1	VCCR AB27
B17	VCCI 1	VCCR AF19
B5	VCCI 1	VCCR AH29
B8	VCCI 1	VCCR AJ9
F11	VCCI 1	VCCR AK30
F14	VCCI 1	VCCR AK7
F17	VCCI 1	VCCR AM31
F8	VCCI 1	VCCR F19
K11	VCCI 1	VCCR G31
K14	VCCI 1	VCCR G6
K17	VCCI 1	VCCR H29
N15	VCCI 1	VCCR L18
N17	VCCI 1	VCCR R10
B20	VCCI 1	VCCR V11
B23	VCCI 2	VCCR V26
B26	VCCI 2	VCCR E5
B29	VCCI 2	VPP1 F31
B32	VCCI 2	VPP10 C21
F20	VCCI 2	VPP11 J29
F23	VCCI 2	VPP12 G30
F26	VCCI 2	VPP13 E24
F29	VCCI 2	VPP14 H28
K20	VCCI 2	VPP15 AL30
K23	VCCI 2	VPP16 AM24
K26	VCCI 2	VPP17 AM32
N20	VCCI 2	VPP18 AJ28
N22	VCCI 2	VPP19 E13
E35	VCCI 3	VPP2 AP21
H31	VCCI 3	VPP21 AE22
H35	VCCI 3	VPP22 AN21
K27	VCCI 3	VPP23 AF18
L31	VCCI 3	VPP24 AN16
L35	VCCI 3	VPP25 AM6
P27	VCCI 3	VPP26 AP16
P31	VCCI 3	VPP27 AM5
P35	VCCI 3	VPP28 AH8
R24	VCCI 3	VPP29 AM13
U24	VCCI 3	VPP3 E6
U27	VCCI 3	VPP3 AL6
U31	VCCI 3	VPP30 N13
U85	VCCI 3	VPP4 C16
AB24	VCCI 3	VPP5 L19
AC27	VCCI 4	VPP6 D16
AC31	VCCI 4	VPP7 M22
AC35	VCCI 4	VPP8 D21
AF31	VCCI 4	VSV A19
AF35	VCCI 4	VSV AE12
AG27	VCCI 4	VSV AL32
AJ31	VCCI 4	VSV AL5
AJ35	VCCI 4	VSV AT18
AM35	VCCI 4	VSV J30
Y24	VCCI 4	VSV M12
Y27	VCCI 4	VSV W33
Y31	VCCI 4	
Y35	VCCI 4	
AD20	VCCI 5	
AD22	VCCI 5	
AG20	VCCI 5	VCC AA14
AG23	VCCI 5	VCC AA16
AG26	VCCI 5	VCC AA18
AL20	VCCI 5	VCC AA20
AL23	VCCI 5	VCC AA22
AL26	VCCI 5	VCC AB15
AL29	VCCI 5	VCC AB17
AR20	VCCI 5	VCC AB19
AR23	VCCI 5	VCC AB21
AR26	VCCI 5	VCC AB23
AR29	VCCI 5	VCC AC14
AR32	VCCI 5	VCC AC16
AD15	VCCI 6	VCC AC18
AD17	VCCI 6	VCC AC20
AG11	VCCI 6	VCC AC22
AG14	VCCI 6	VCC AF3
AG17	VCCI 6	VCC AP34
AL11	VCCI 6	VCC C3
AL14	VCCI 6	VCC C34
AL17	VCCI 6	VCC P15
AL8	VCCI 6	VCC P17
AR11	VCCI 6	VCC P19
AR14	VCCI 6	VCC P21
AR17	VCCI 6	VCC P23
AR5	VCCI 6	VCC R14
AR8	VCCI 6	VCC R16
AB13	VCCI 6	VCC R18
AC10	VCCI 7	VCC R20
AC2	VCCI 7	VCC R22
AC6	VCCI 7	VCC T15
AF2	VCCI 7	VCC T17
AF6	VCCI 7	VCC T19
AG10	VCCI 7	VCC T21
AJ2	VCCI 7	VCC T23
AJ6	VCCI 7	VCC U14
AM2	VCCI 7	VCC U16
Y10	VCCI 7	VCC U18
Y13	VCCI 7	VCC U20
Y2	VCCI 7	VCC U22
Y6	VCCI 7	VCC V15
E2	VCCI 7	VCC V17
H2	VCCI 8	VCC V19
H6	VCCI 8	VCC V21
K10	VCCI 8	VCC V23
L2 L6	VCCI 8	VCC W14
P10	VCCI 8	VCC W16
P2	VCCI 8	VCC W18
P6	VCCI 8	VCC W20
R13	VCCI 8	VCC W22
U10	VCCI 8	VCC Y15
U13	VCCI 8	VCC Y17
U2	VCCI 8	VCC Y19
U6	VCCI 8	VCC Y21
	VCCI 8	VCC Y23

VCCA_1.5

Figure A2 Power supply, Ground and Special Pins Bias During Irradiation



Appendix B: Functionality Tests

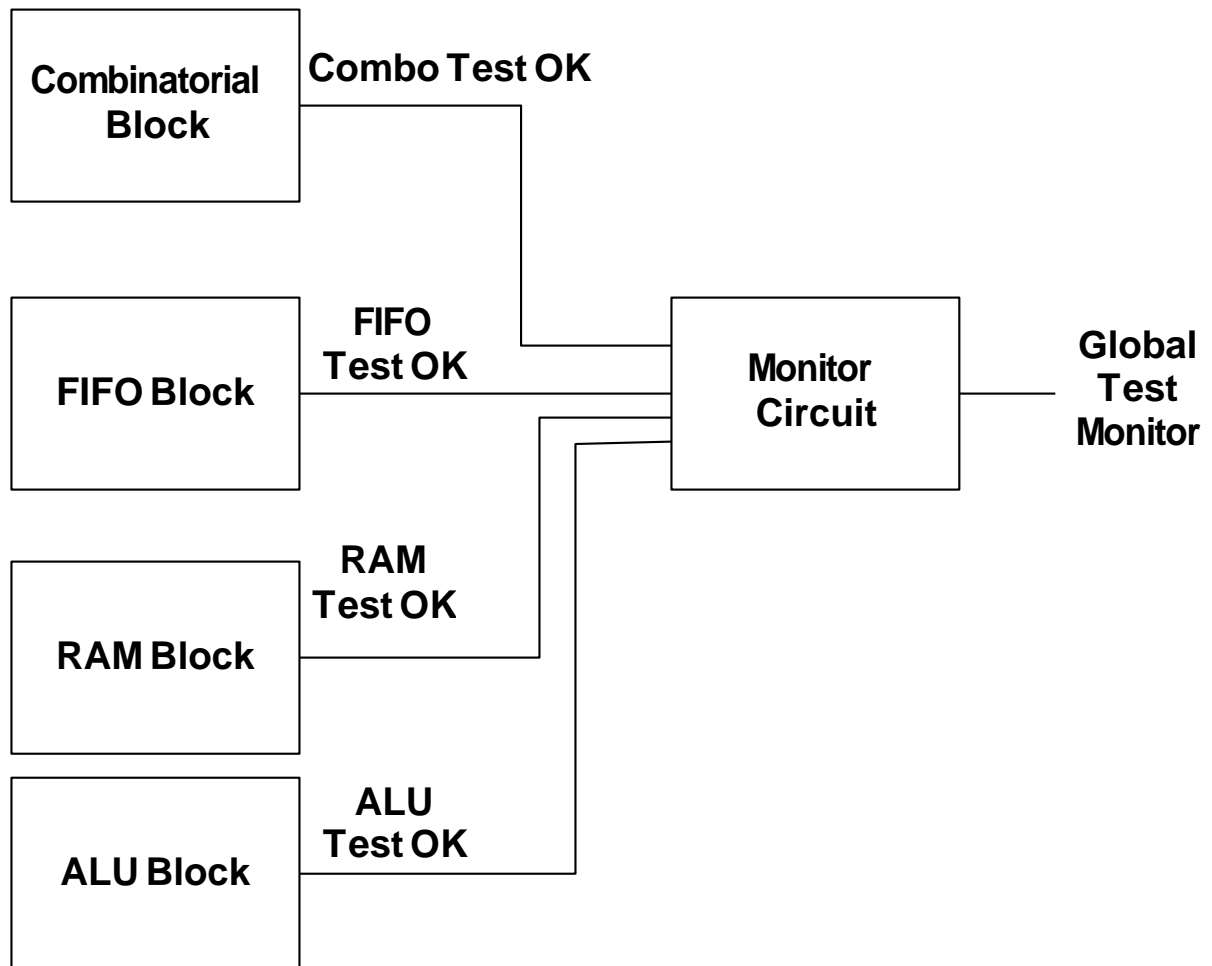


Figure B1 QBI Block – Top-Level Design

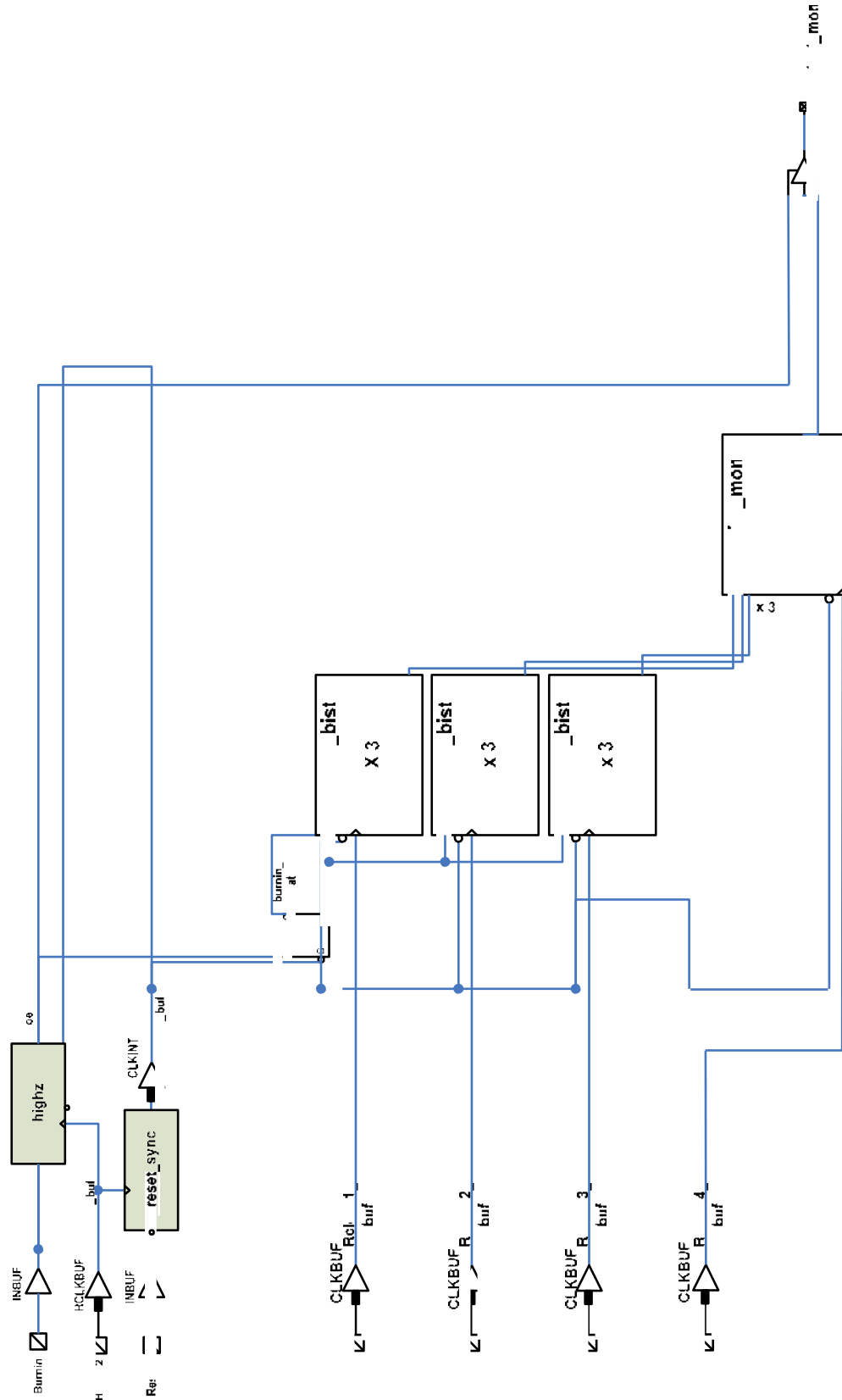


Figure B2 QBI Block – Combinatorial Test (Top Level)

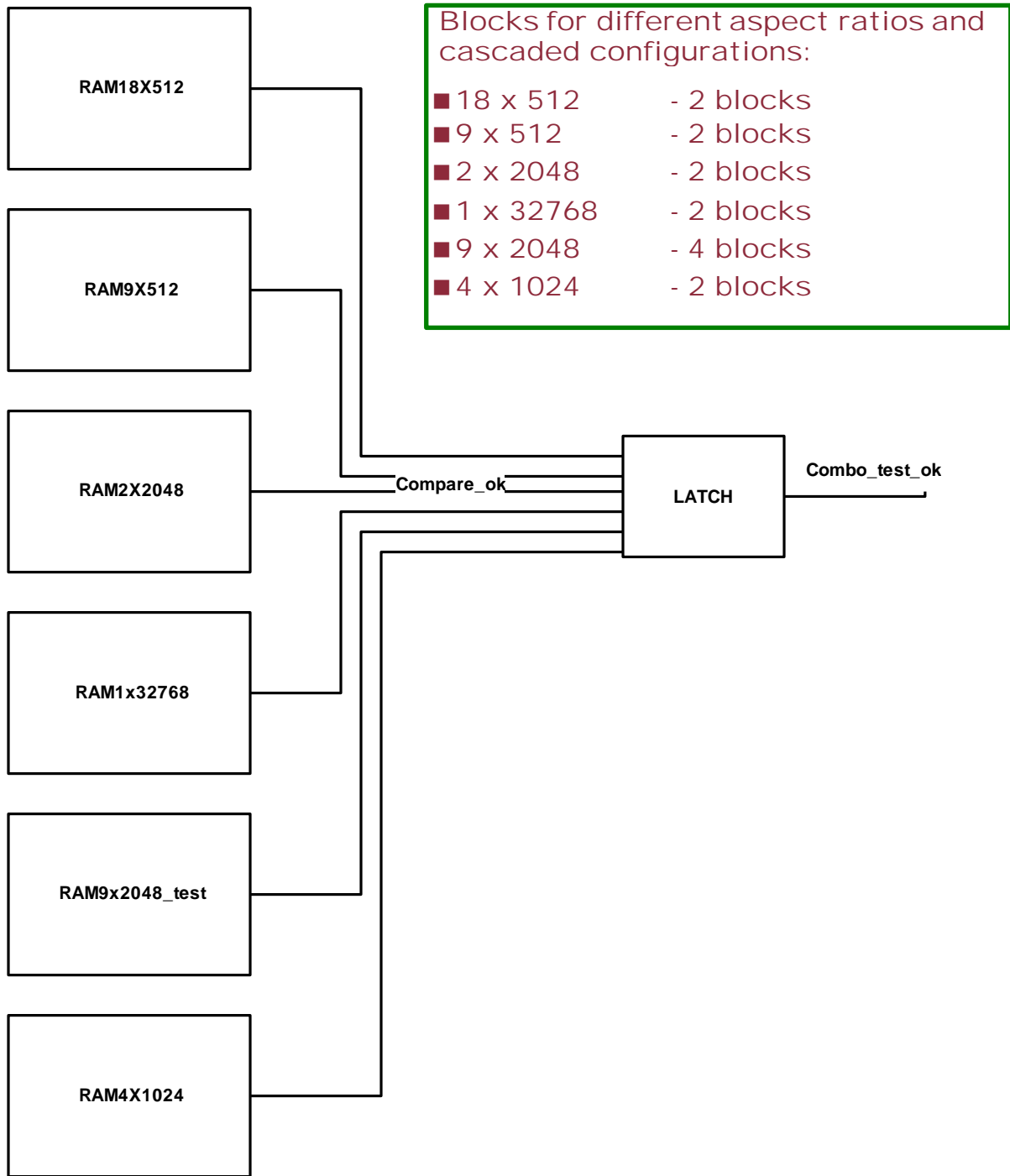


Figure B3 QBI Block – RAM Test (Top Level)

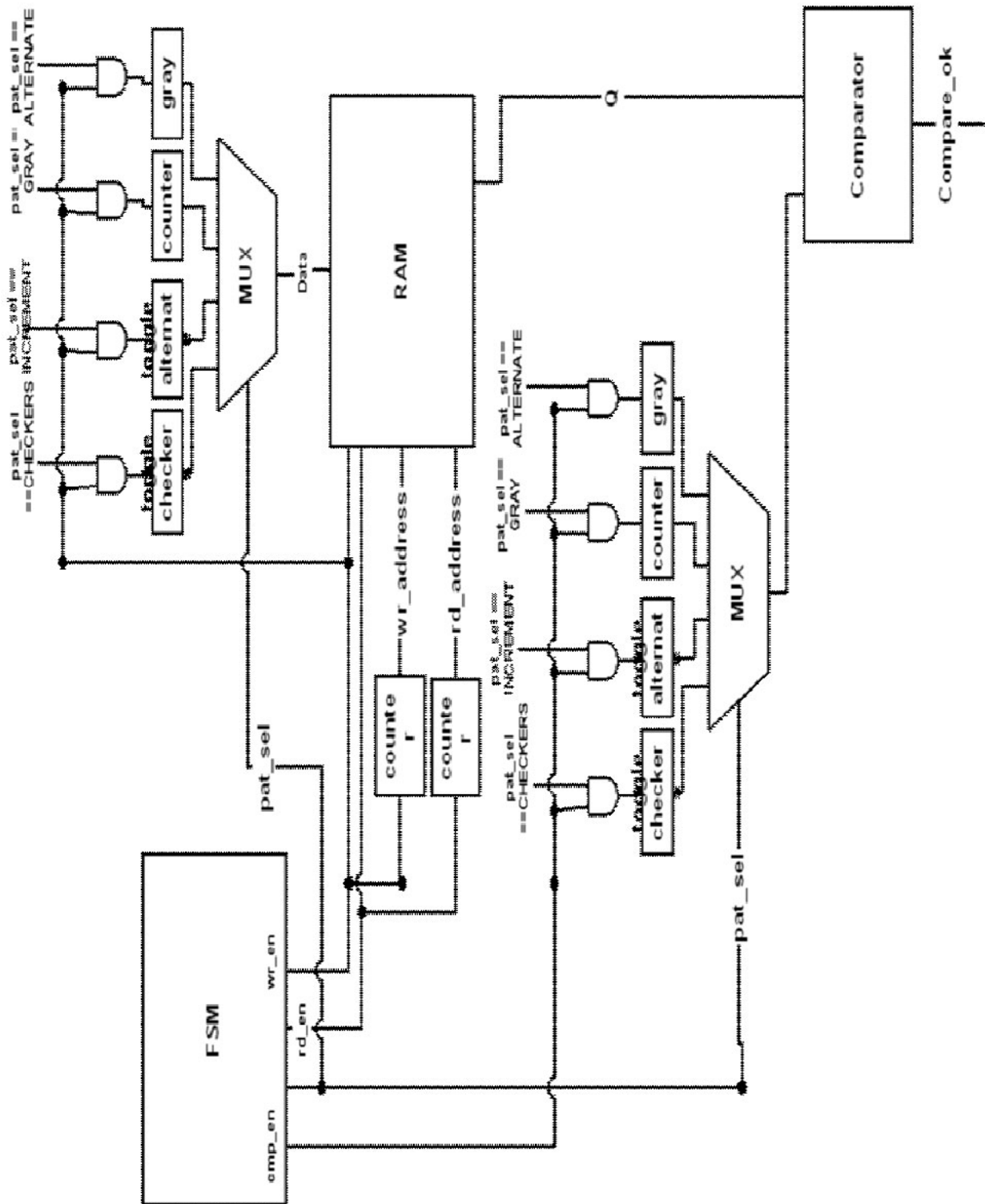


Figure B4 QBI Block – RAM Block

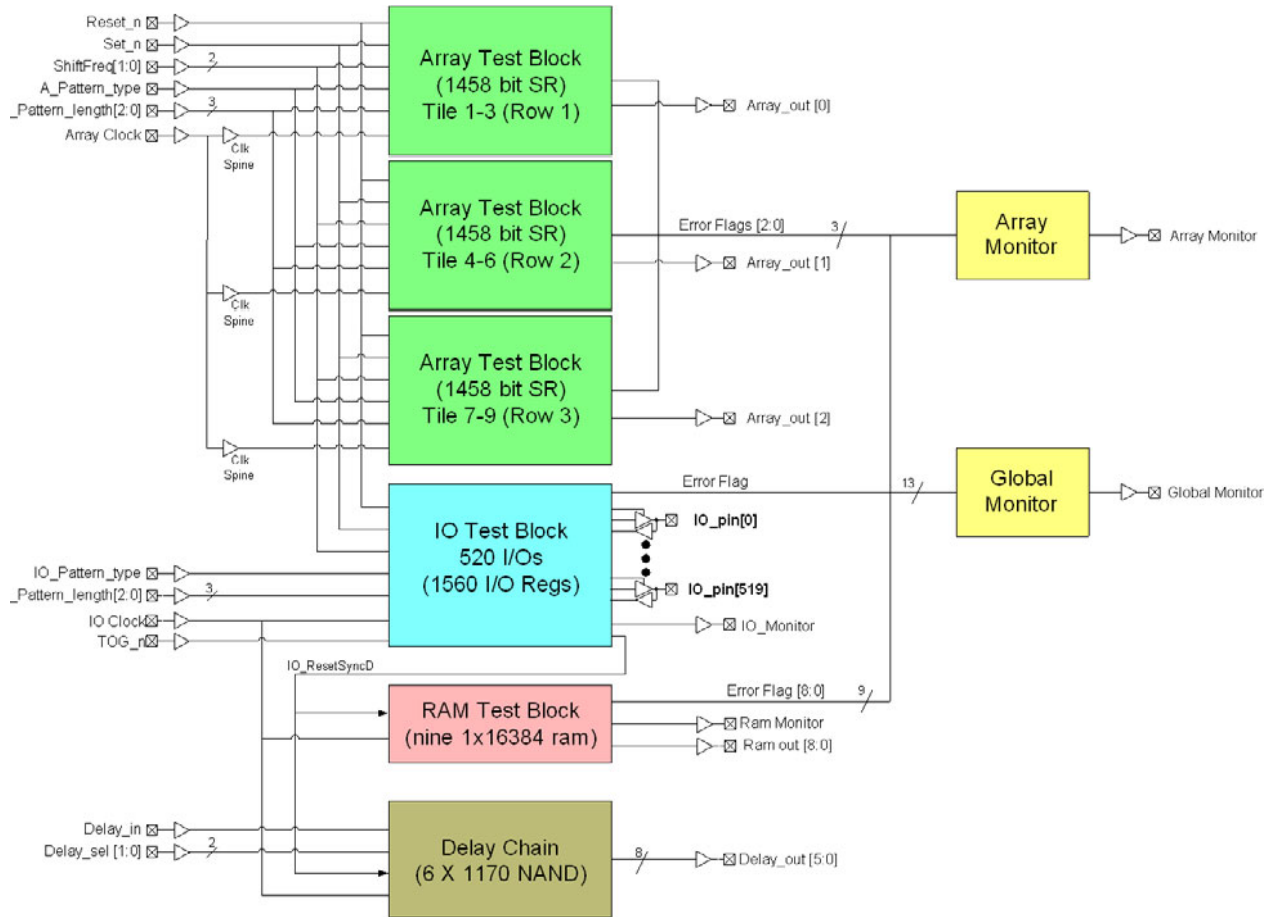


Figure B5 EAQ Block – Top Level

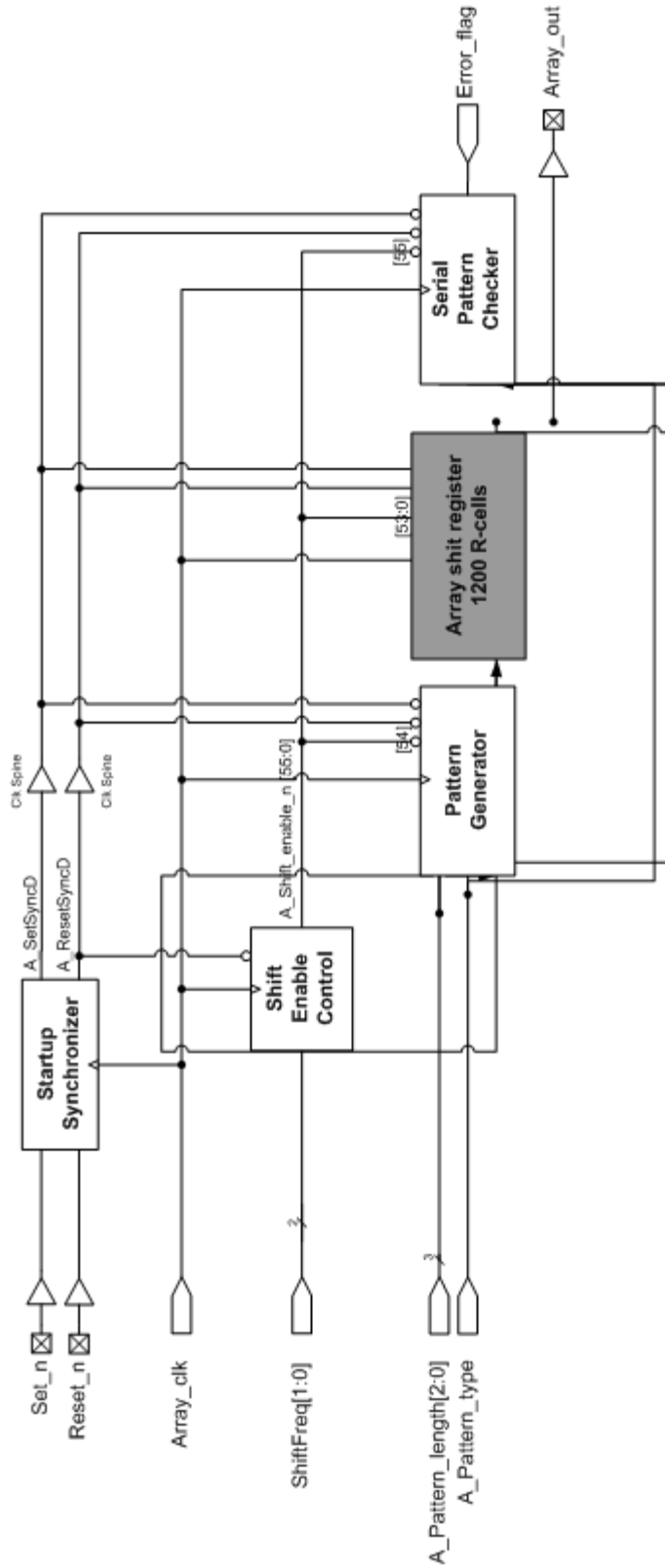


Figure B6 EAQ Block – Array Test (Shift Register)

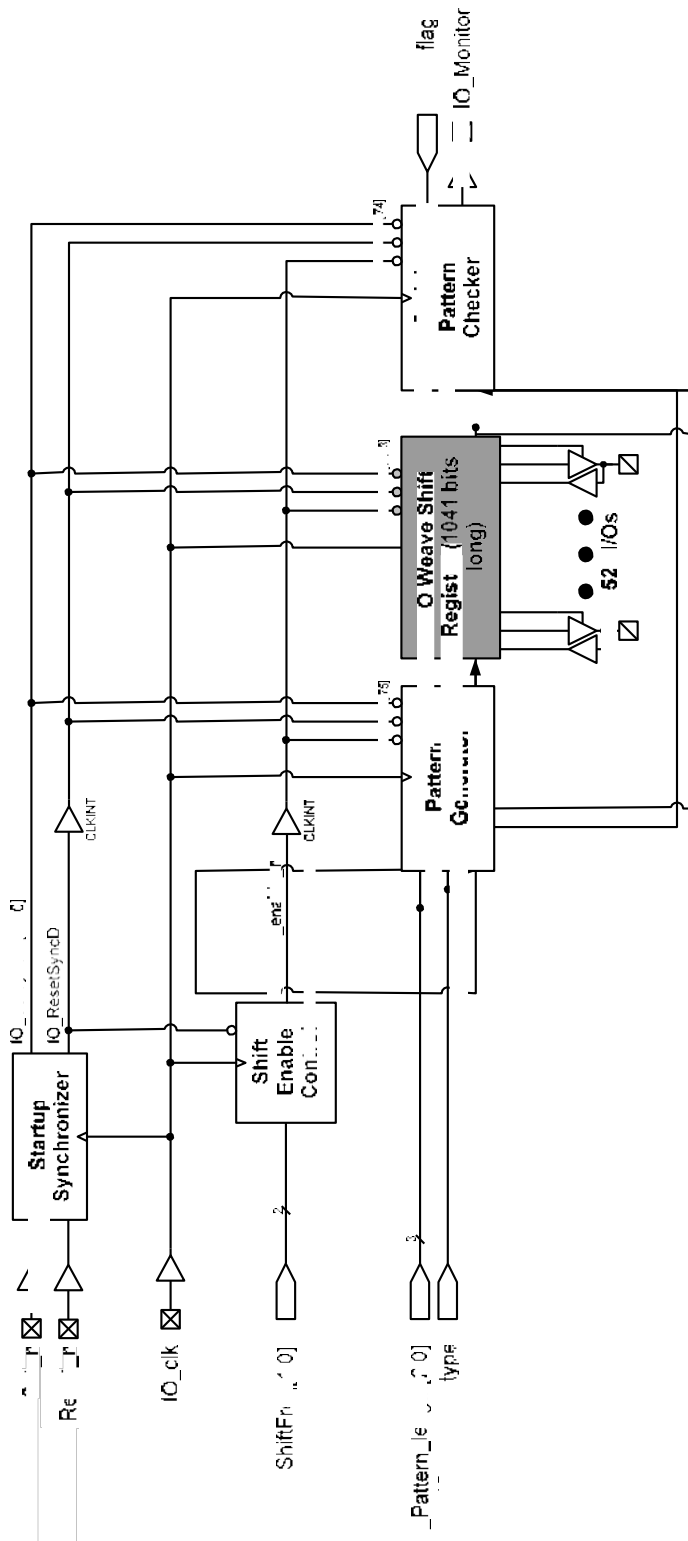


Figure B7 EAQ Block – I/O Test (Top Level)

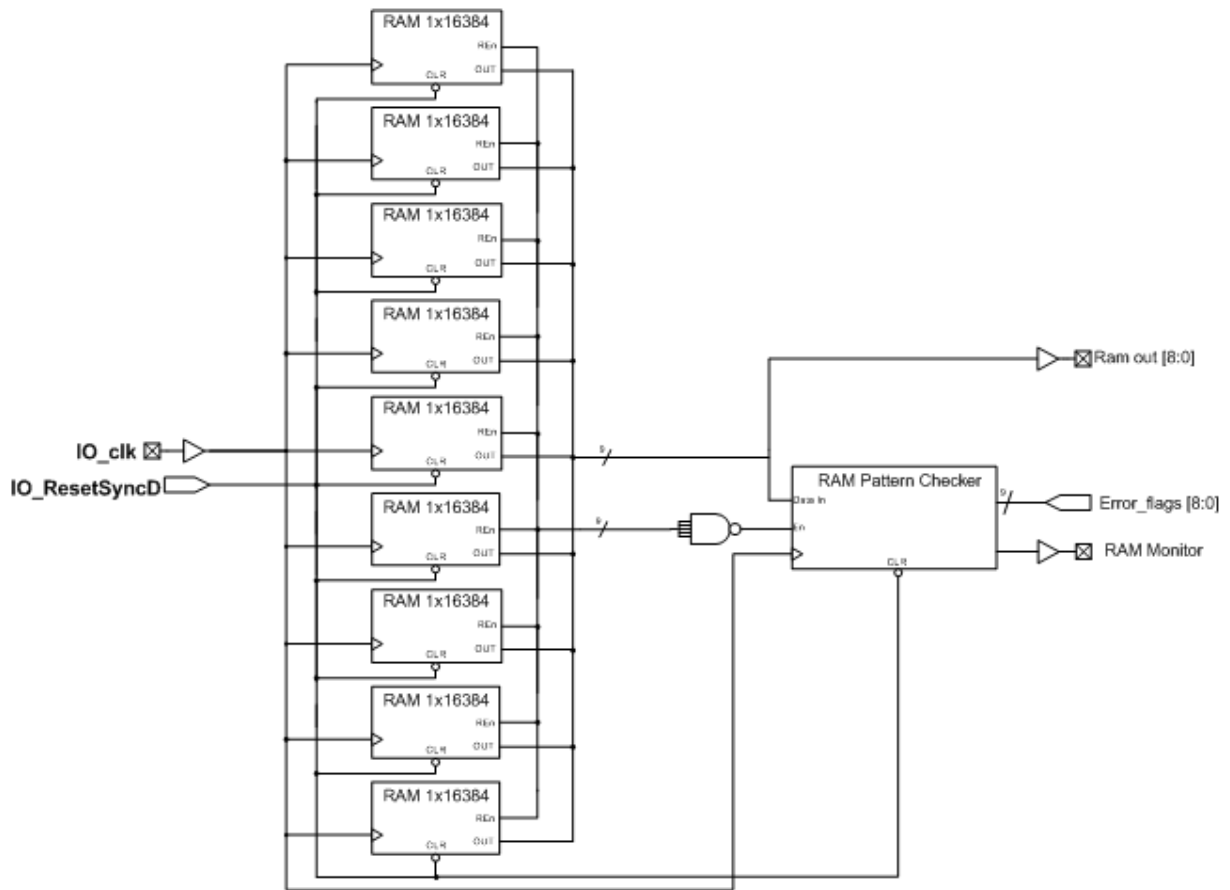


Figure B8 EAQ Block – SRAM Test (Top Level)



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