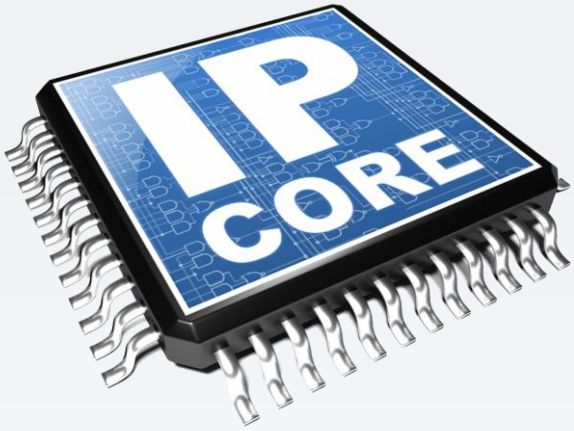
SpaceFibre CODEC IP Core

SpaceFibre is the ESA standard (ECSS-E-ST-50-11C) for very high-speed serial communication links between the units of the satellite. It is compatible with SpaceWire at packet level, but the data-link and physical layers are completely re-defined in order to have advanced Quality-of-Service (QoS) and Fault Detection, Isolation and Recovery (FDIR) features. The SpaceFibre CODEC IP core is the full implementation of the SpaceFibre standard (ECSS-E-ST-50-11C) for point-to-point links. QoS and FDIR mechanisms foreseen by the standard are built-in in the hardware CODEC. The IP core also supports multi-lane functionality and is technology independent as far as the core is concerned. Since the standard implementation is based on the usage of Serializer/Deserializer (SERDES) devices, which are normally hard IPs on the target technology, that part is technology dependent. IngeniArs IP core supports the most relevant SERDES devices for space applications (Xilinx, Microsemi / Microchip, TLK2711, …) and support for additional SERDES devices can be implemented upon request.

Key Features

- SpaceFibre CODEC IP core suitable to implement SpaceFibre point-to-point links(encoder-decoder specification)
- Supports a wide range of SERDES devices
- Technology independent core implementation
- Configurable number of Virtual Channels
- Configurable number of lanes
- Available with reduced footprint to allow more efficient implementation (still compatible with the full implementation of the standard)



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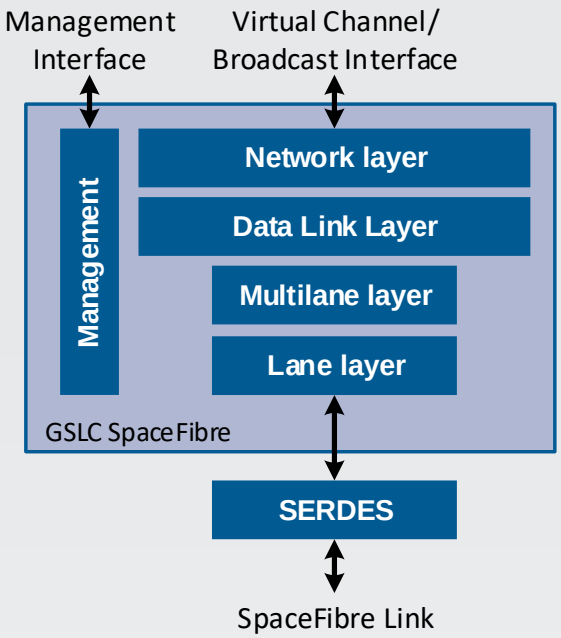
Block Diagram



Additional Features

The IP core was **verified with 100% code coverage** by using a comprehensive **SystemVerilog** test-environment and has been **validated with FPGA implementations** on different technologies also proving interoperability with third-party implementations of the standard.

Since SpaceFibre is a quite complex standard (especially vs SpaceWire), **a reduced version of SpaceFibre CODEC IP** core may come at hand. This configuration was designed for simple high speed point-to-point communication and is still compatible to the full SpaceFibre implementation, meaning that it can communicate with a remote node supporting the full standard. Some features were removed in order to have a smaller footprint, such as frame re-transmission and broadcast services. The reduced SpaceFibre CODEC can save up to 40% hardware resources with respect to the full SpaceFibre CODEC.

Synthesis results on RTAX2000S and RTG4 FPGA

	Combinational	Registers	RAM blocks
RTAX2000S 4 VCs	29 %	20 %	25 %
RTG4 4 VCs	7.5 %	4.2 %	2 %

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