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Total Ionizing Dose Test Report

No. 20T-RT4G150-LG1657- K924T

December 28, 2020

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I. SUMMARY TABLE

Table. 1. Summary

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO_2)
2. Power Supply Current	Passed 125 krad(SiO_2)
3. Input Threshold (VIL/VIH)	Passed 125 krad(SiO_2)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO_2)
5. Propagation Delay	Passed 125 krad(SiO_2) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the Automatic Test Equipment (ATE) program. The report summarizes sample pins.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters.

Table. 2. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	K924T
Quantity Tested	5
Serial Number (Dose)	10759 (125 krad), 10765 (125 krad), 10772 (125 krad), 10807 (125 krad), 10822 (125 krad)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

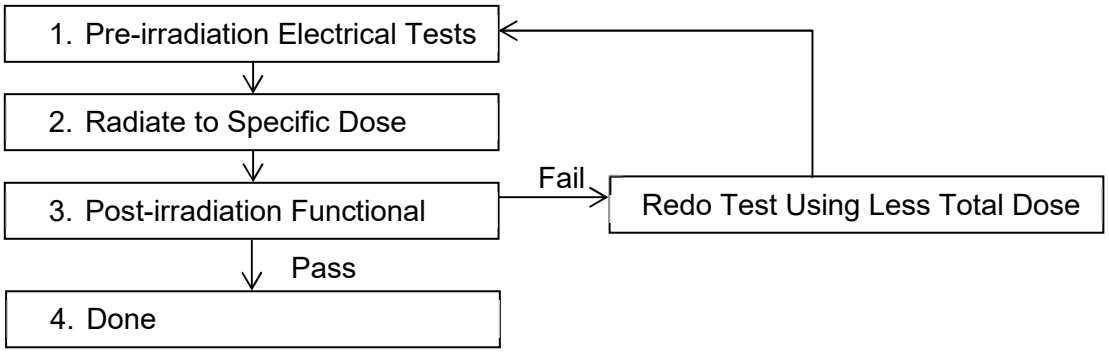

Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 3. Fabric Functional Coverage

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump and PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design. LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents are reported.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-25 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL.

Table. 4. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
10759	125 krad	0.4079	0.4198	2.92
10765	125 krad	0.3060	0.3201	4.61
10772	125 krad	0.3690	0.3810	3.25
10807	125 krad	0.4259	0.4433	4.09
10822	125 krad	0.3561	0.3661	2.81

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI\_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
10759	125 krad	0.0091	0.0116	27.47
10765	125 krad	0.0086	0.0109	26.74
10772	125 krad	0.0086	0.0109	26.74
10807	125 krad	0.0100	0.0125	25.00
10822	125 krad	0.0085	0.0107	25.88

Table. 6. Pre-irradiation and Post-irradiation $I_{DDI\_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
10759	125 krad	0.0334	0.0367	9.88
10765	125 krad	0.0338	0.0368	8.88
10772	125 krad	0.0331	0.0361	9.06
10807	125 krad	0.0338	0.0370	9.47
10822	125 krad	0.0334	0.0364	8.98

Table. 7. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
10759	125 krad	0.0152	0.0191	25.66
10765	125 krad	0.0155	0.0215	38.71
10772	125 krad	0.0153	0.0211	37.91
10807	125 krad	0.0151	0.0185	22.52
10822	125 krad	0.0153	0.0170	11.11

The following figures (2-21) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

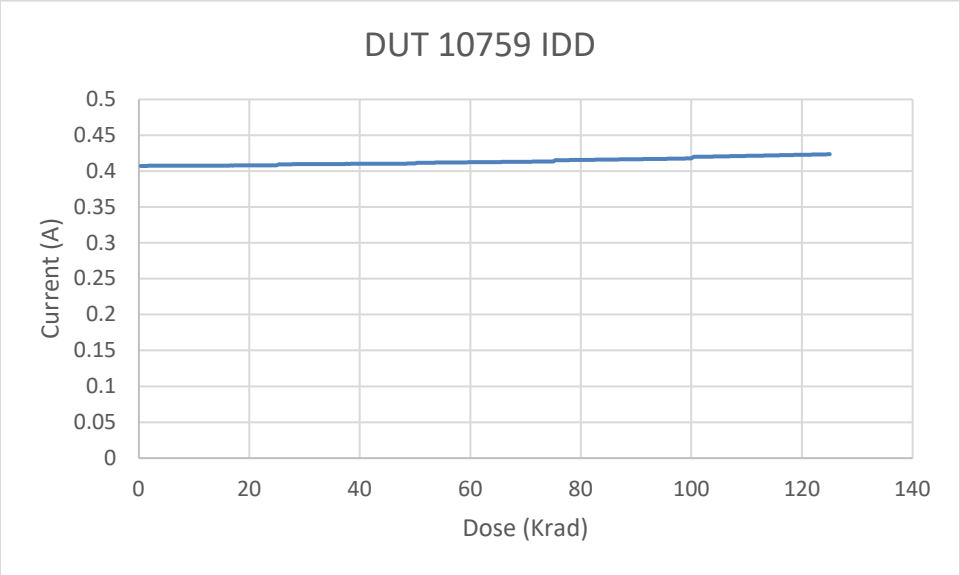

Fig. 2. DUT 10759 core power supply current (I_{DD}) versus TID

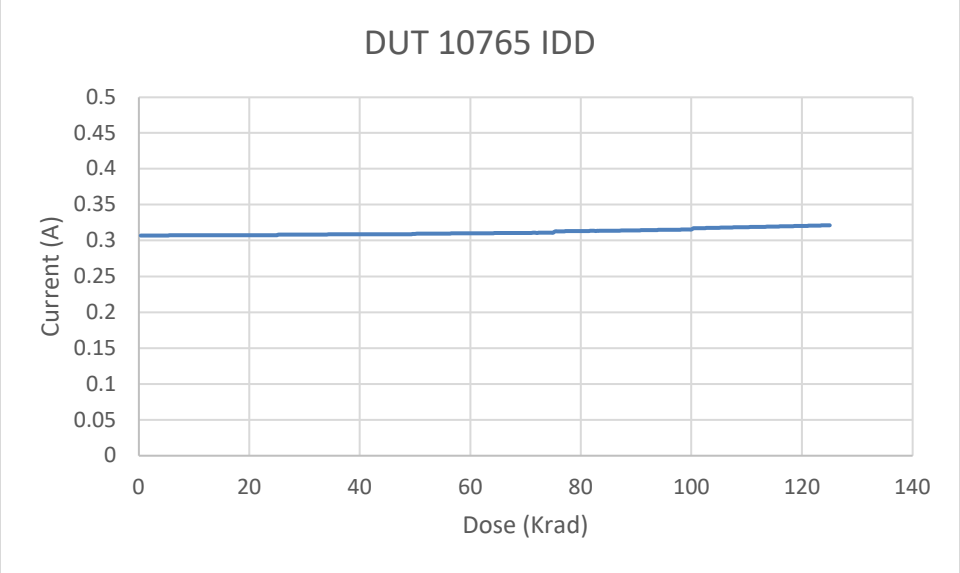

Fig. 3. DUT 10765 core power supply current (I_{DD}) versus TID

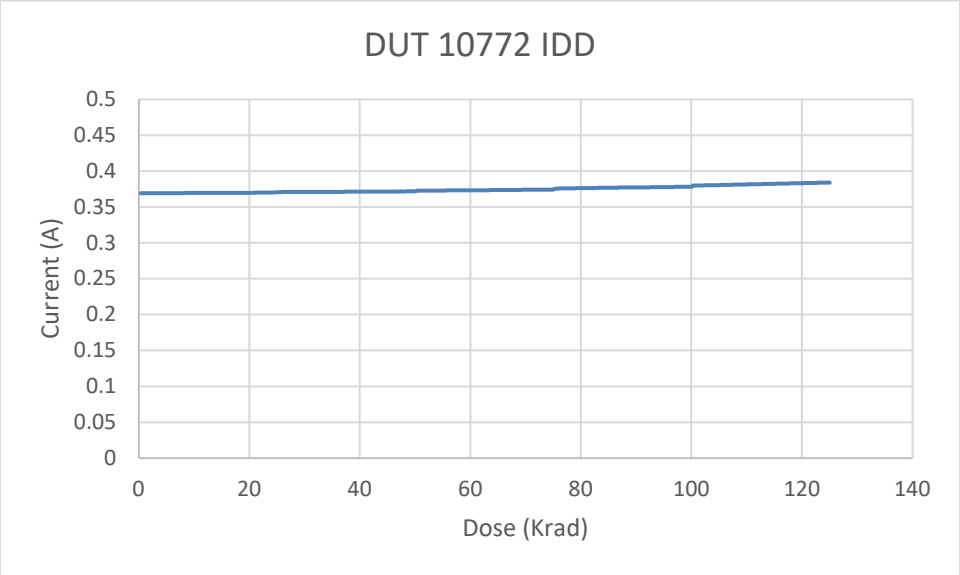

Fig. 4. DUT 10772 core power supply current (I_{DD}) versus TID

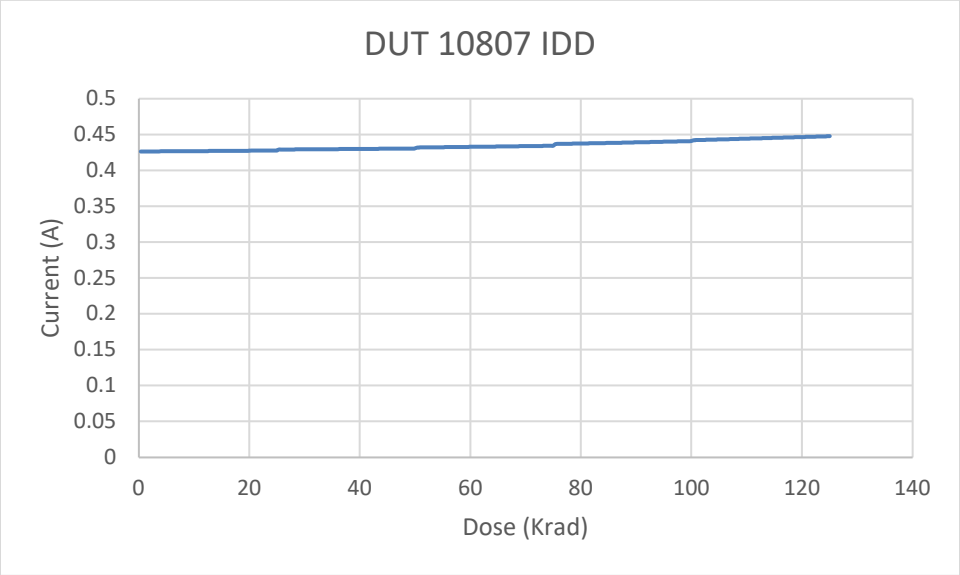

Fig. 5. DUT 10807 core power supply current (I_{DD}) versus TID

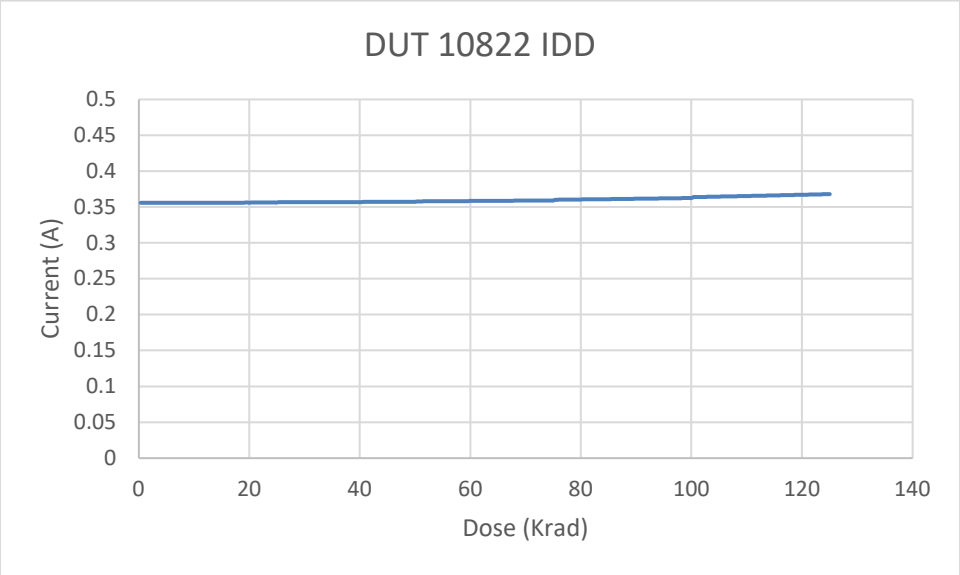

Fig. 6. DUT 10822 core power supply current (I_{DD}) versus TID

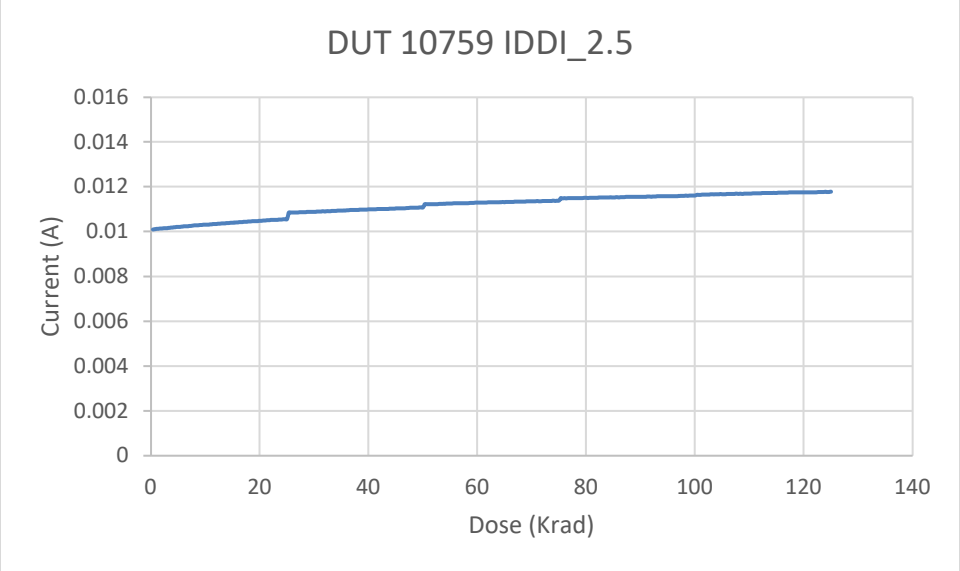

Fig. 7. DUT 10759 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

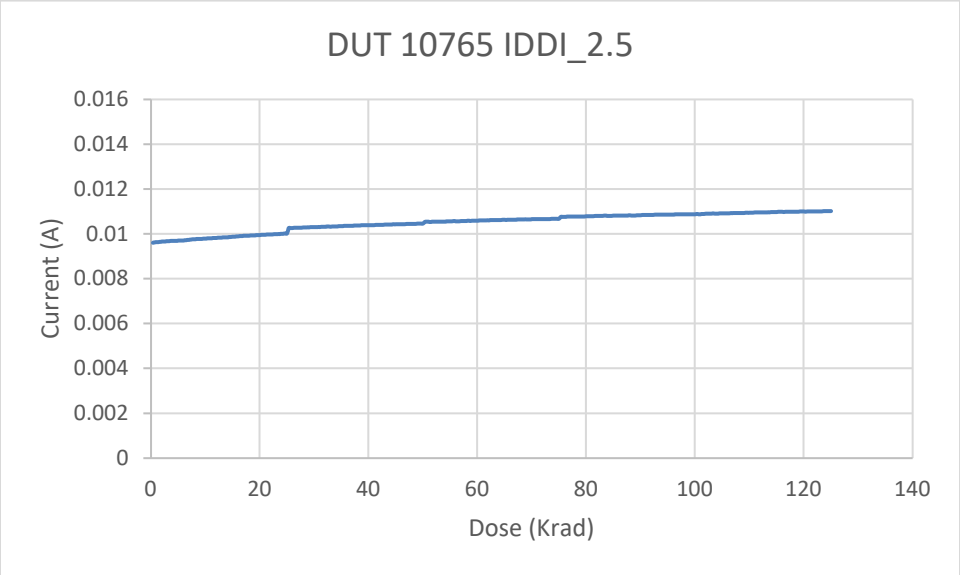

Fig. 8. DUT 10765 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

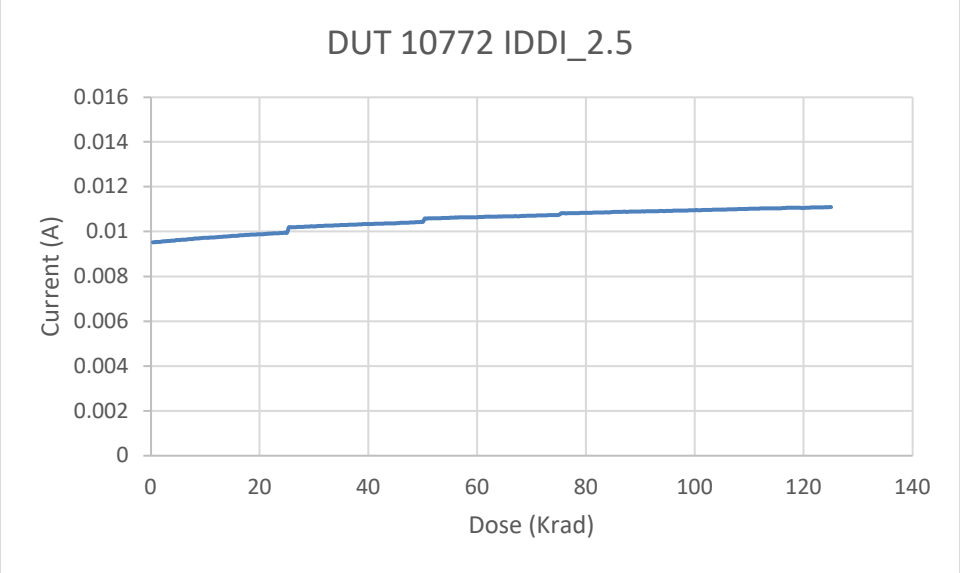

Fig. 9. DUT 10772 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

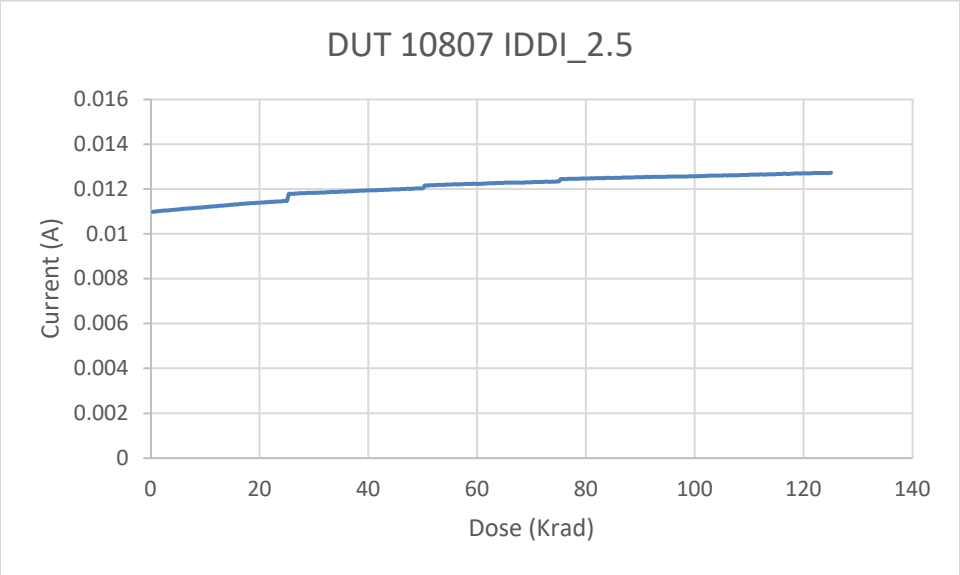

Fig. 10. DUT 10807 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

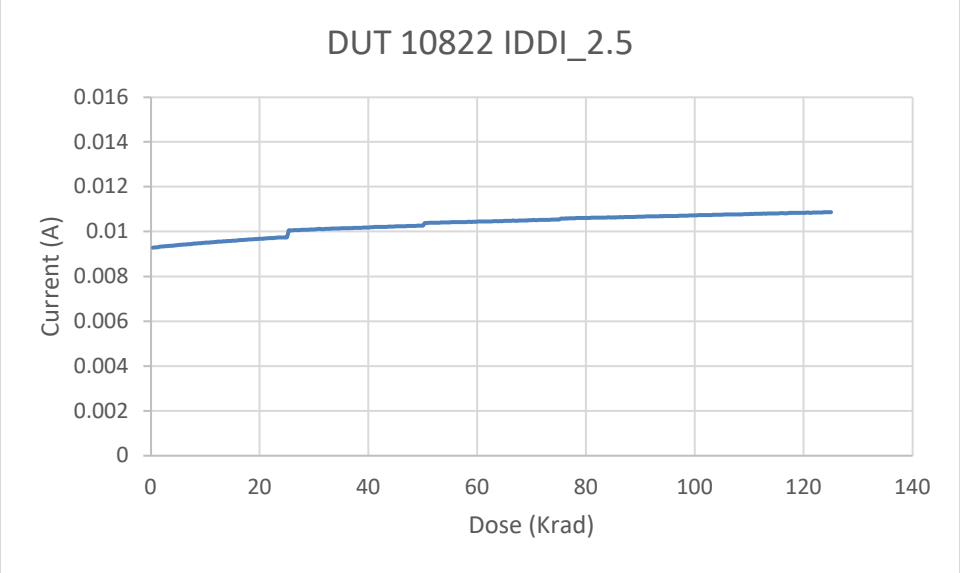

Fig. 11. DUT 10822 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

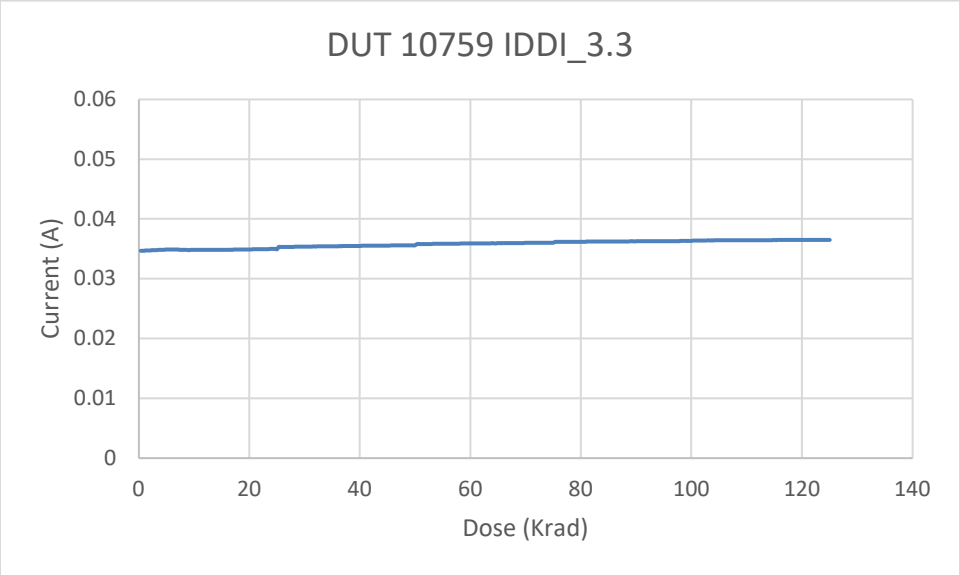

Fig. 12. DUT 10759 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

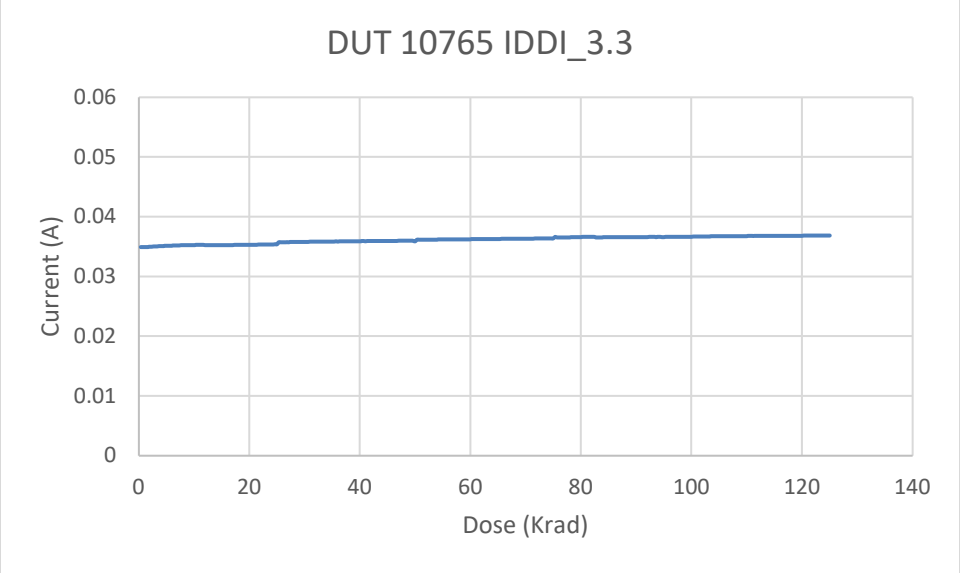

Fig. 13. DUT 10765 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

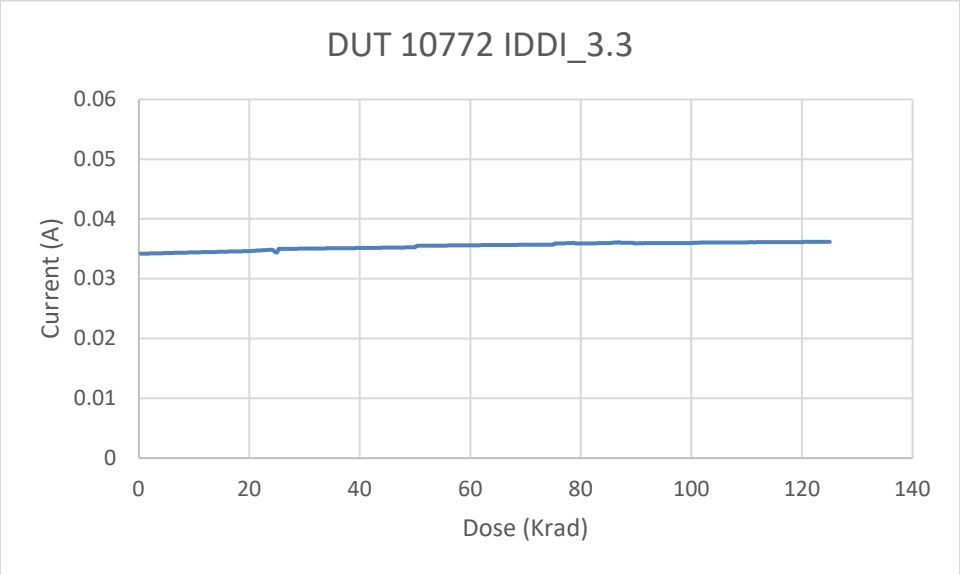

Fig. 14. DUT 10772 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

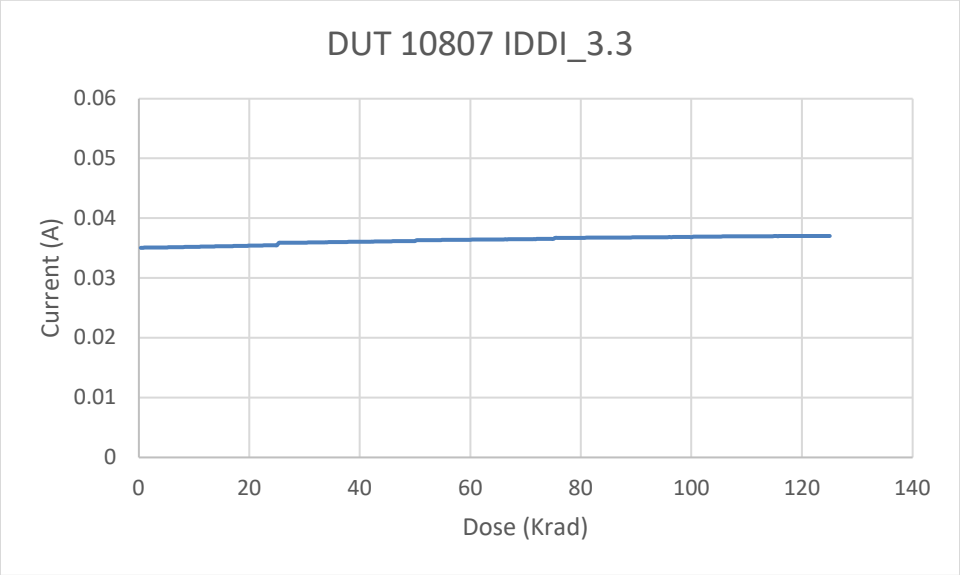

Fig. 15. DUT 10807 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

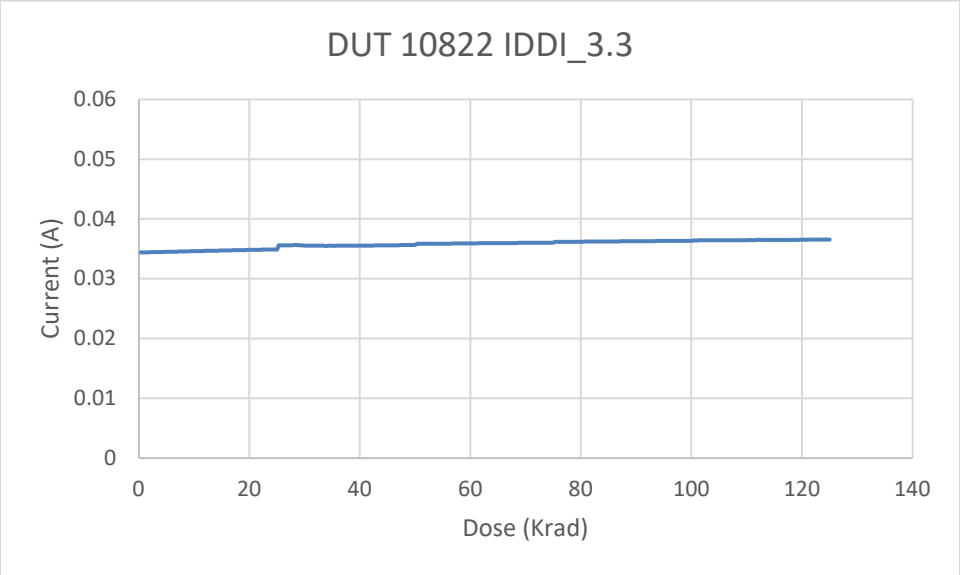

Fig. 16. DUT 10822 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

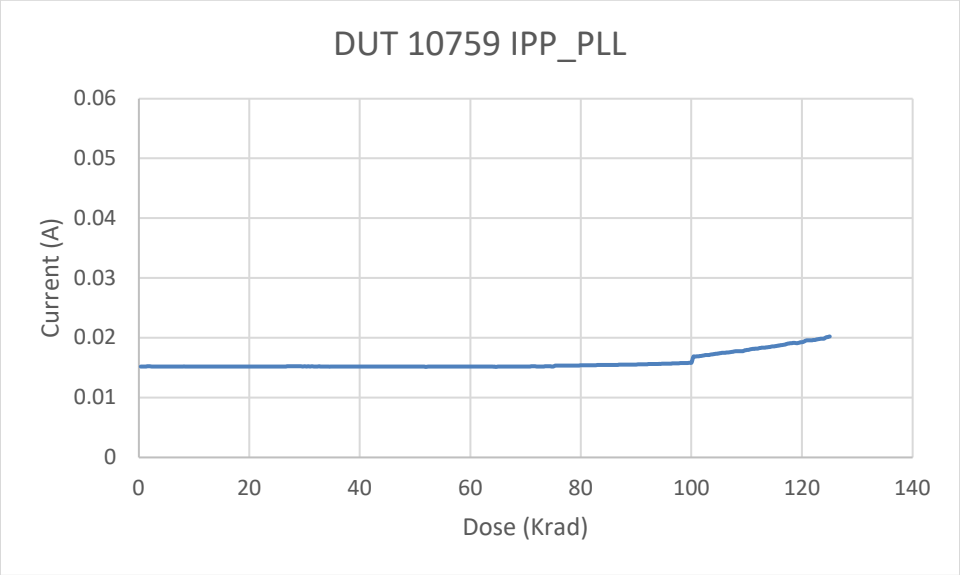

Fig. 17. DUT 10759 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

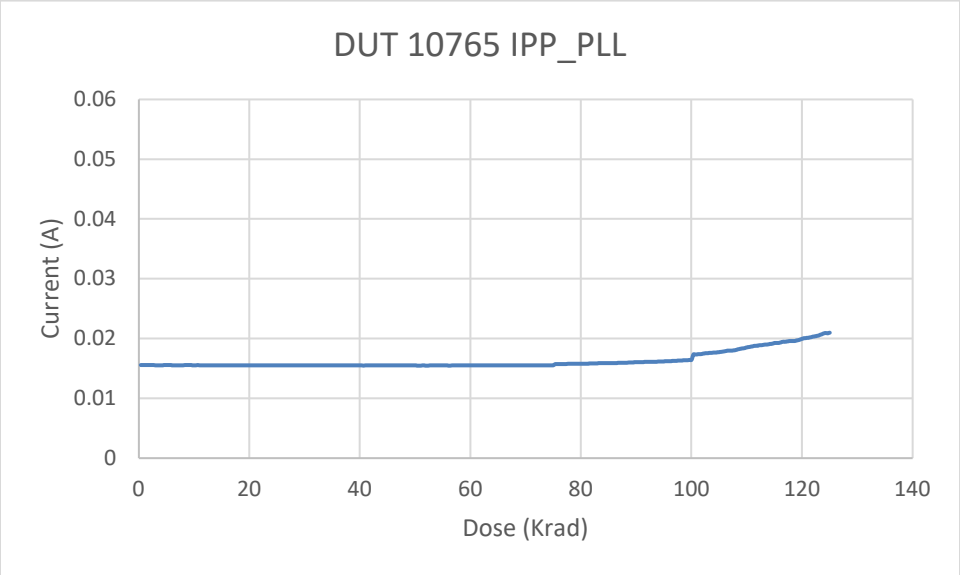

Fig. 18. DUT 10765 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

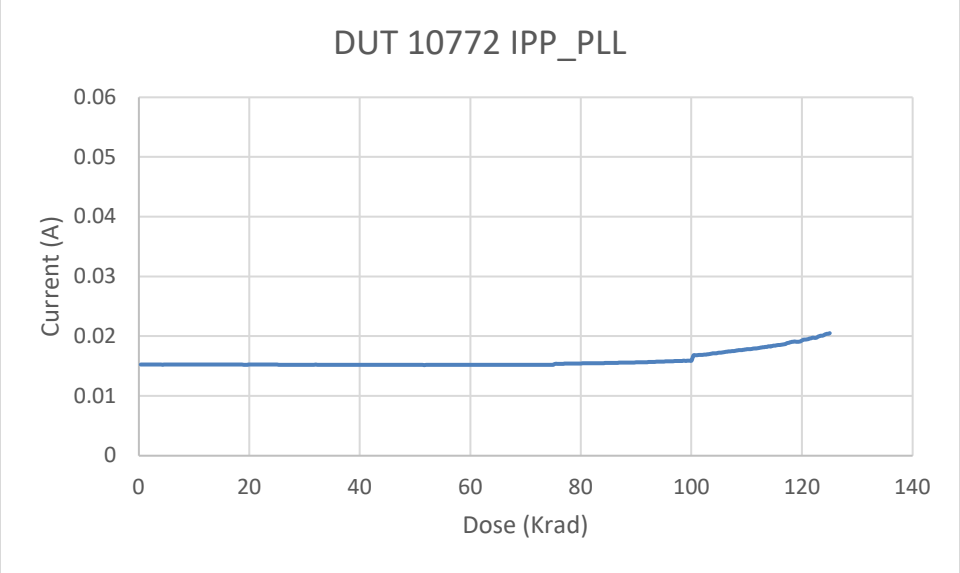

Fig. 19. DUT 10772 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

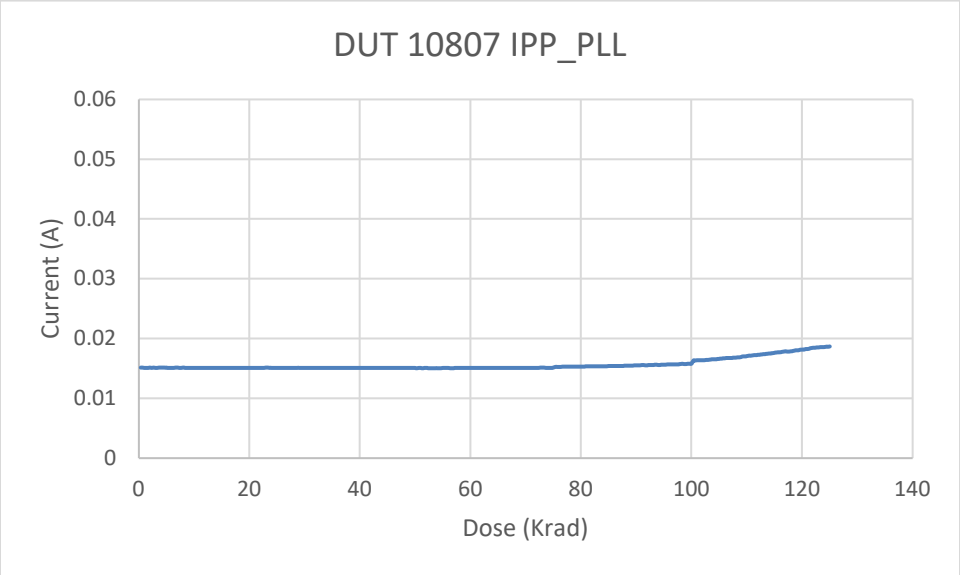

Fig. 20. DUT 10807 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

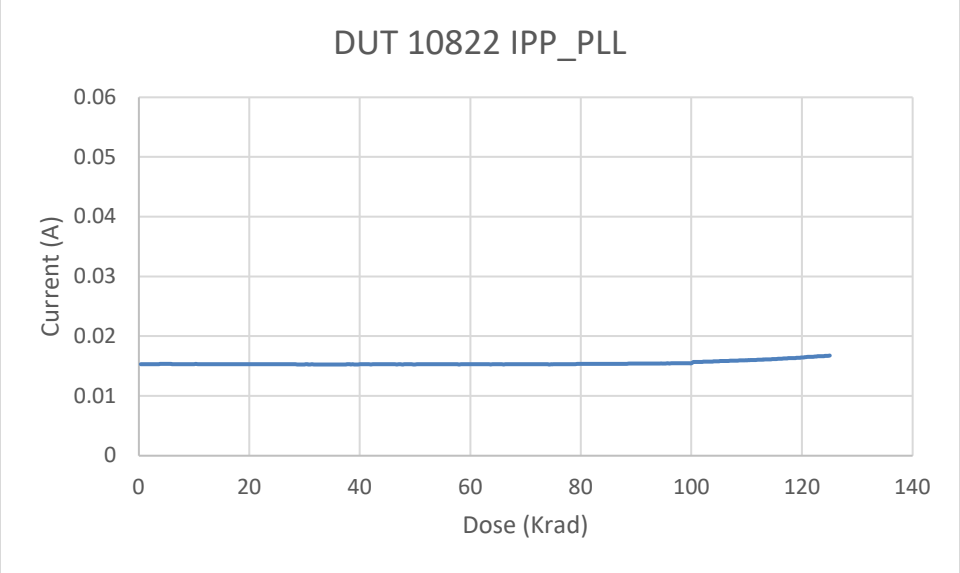

Fig. 21. DUT 10822 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 8. VIH Summary

DUT	Pre-irradiation	Post-irradiation
10759	Passed	Passed
10765	Passed	Passed
10772	Passed	Passed
10807	Passed	Passed
10822	Passed	Passed

Table. 9. VIL Summary

DUT	Pre-irradiation	Post-irradiation
10759	Passed	Passed
10765	Passed	Passed
10772	Passed	Passed
10807	Passed	Passed
10822	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 10 through 29 are sampled on several pins used in the burn in design.

Table. 10. LVCMOS 25 VOH – DUT 10759

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.135	2.133	2.203	2.202	2.174	2.173	2.153	2.152	2.121	2.119	2.107	2.106
EPCSRST_N_0	B31	2.135	2.134	2.202	2.201	2.173	2.172	2.152	2.150	2.119	2.117	2.105	2.103
EPCSRST_N_1	B32	2.134	2.134	2.201	2.203	2.171	2.173	2.150	2.152	2.115	2.120	2.100	2.105
EPCSRST_N_2	B34	2.135	2.134	2.203	2.203	2.175	2.174	2.155	2.154	2.123	2.122	2.109	2.108
EPCSRST_N_3	B35	2.135	2.135	2.204	2.204	2.175	2.176	2.155	2.157	2.124	2.126	2.110	2.113
EPCSRST_N_4	B36	2.133	2.134	2.199	2.201	2.169	2.171	2.147	2.150	2.111	2.116	2.096	2.101
EPCSRST_N_5	B37	2.135	2.134	2.203	2.203	2.174	2.174	2.154	2.154	2.122	2.121	2.108	2.108
MONITOR	K23	2.134	2.132	2.202	2.199	2.174	2.169	2.154	2.148	2.123	2.113	2.109	2.099
PLL_MON	L20	2.135	2.135	2.206	2.205	2.179	2.178	2.162	2.161	2.133	2.132	2.122	2.120
TOGGLE_MON	L22	2.136	2.134	2.205	2.204	2.178	2.177	2.160	2.158	2.130	2.128	2.118	2.116

Table. 11. LVCMOS 25 VOH – DUT 10765

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.133	2.132	2.202	2.201	2.173	2.172	2.152	2.150	2.119	2.118	2.106	2.104
EPCSRST_N_0	B31	2.134	2.133	2.202	2.201	2.173	2.172	2.152	2.150	2.119	2.117	2.105	2.103
EPCSRST_N_1	B32	2.133	2.134	2.200	2.201	2.170	2.172	2.148	2.152	2.113	2.118	2.097	2.104
EPCSRST_N_2	B34	2.134	2.133	2.203	2.202	2.174	2.173	2.154	2.153	2.121	2.120	2.107	2.106
EPCSRST_N_3	B35	2.135	2.135	2.204	2.204	2.175	2.175	2.155	2.156	2.123	2.125	2.110	2.112
EPCSRST_N_4	B36	2.133	2.133	2.199	2.200	2.168	2.171	2.147	2.150	2.111	2.116	2.095	2.102
EPCSRST_N_5	B37	2.135	2.134	2.203	2.202	2.174	2.173	2.154	2.153	2.121	2.120	2.107	2.107
MONITOR	K23	2.134	2.133	2.202	2.202	2.174	2.174	2.155	2.155	2.122	2.123	2.109	2.110
PLL_MON	L20	2.136	2.134	2.206	2.205	2.179	2.178	2.162	2.160	2.134	2.132	2.122	2.120
TOGGLE_MON	L22	2.135	2.134	2.205	2.204	2.178	2.176	2.159	2.158	2.130	2.128	2.118	2.116

Table. 12. LVCMOS 25 VOH – DUT 10772

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.132	2.131	2.201	2.200	2.172	2.171	2.151	2.150	2.118	2.116	2.104	2.102
EPCSRST_N_0	B31	2.132	2.131	2.201	2.200	2.172	2.171	2.151	2.149	2.118	2.116	2.104	2.102
EPCSRST_N_1	B32	2.132	2.132	2.199	2.201	2.168	2.171	2.146	2.151	2.110	2.117	2.095	2.103
EPCSRST_N_2	B34	2.132	2.132	2.201	2.201	2.173	2.172	2.152	2.151	2.120	2.119	2.106	2.105
EPCSRST_N_3	B35	2.133	2.132	2.202	2.202	2.174	2.174	2.154	2.154	2.122	2.123	2.108	2.110
EPCSRST_N_4	B36	2.131	2.131	2.198	2.199	2.167	2.169	2.145	2.148	2.108	2.113	2.092	2.099
EPCSRST_N_5	B37	2.133	2.132	2.201	2.201	2.172	2.172	2.152	2.152	2.120	2.120	2.106	2.106
MONITOR	K23	2.132	2.130	2.201	2.197	2.173	2.166	2.153	2.145	2.121	2.109	2.107	2.094
PLL_MON	L20	2.135	2.133	2.205	2.204	2.179	2.177	2.161	2.159	2.133	2.131	2.121	2.119
TOGGLE_MON	L22	2.134	2.133	2.204	2.203	2.176	2.175	2.158	2.157	2.128	2.127	2.116	2.115

Table. 13. LVCMOS 25 VOH – DUT 10807

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.132	2.131	2.201	2.201	2.172	2.172	2.151	2.150	2.118	2.118	2.105	2.104
EPCSRST_N_0	B31	2.132	2.130	2.201	2.196	2.171	2.165	2.150	2.141	2.117	2.104	2.103	2.088
EPCSRST_N_1	B32	2.132	2.132	2.199	2.200	2.169	2.171	2.148	2.150	2.113	2.116	2.097	2.102
EPCSRST_N_2	B34	2.133	2.133	2.202	2.202	2.173	2.172	2.152	2.152	2.120	2.120	2.107	2.106
EPCSRST_N_3	B35	2.133	2.133	2.202	2.203	2.173	2.174	2.154	2.155	2.121	2.123	2.108	2.110
EPCSRST_N_4	B36	2.131	2.131	2.198	2.200	2.167	2.170	2.145	2.149	2.109	2.115	2.093	2.101
EPCSRST_N_5	B37	2.132	2.132	2.201	2.200	2.172	2.171	2.152	2.151	2.119	2.118	2.105	2.104
MONITOR	K23	2.133	2.132	2.202	2.201	2.173	2.173	2.153	2.153	2.121	2.121	2.108	2.107
PLL_MON	L20	2.135	2.134	2.205	2.205	2.179	2.178	2.161	2.160	2.133	2.131	2.121	2.120
TOGGLE_MON	L22	2.134	2.134	2.204	2.204	2.177	2.176	2.158	2.157	2.128	2.126	2.116	2.114

Table. 14. LVCMOS 25 VOH – DUT 10822

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.138	2.136	2.205	2.204	2.176	2.175	2.156	2.154	2.123	2.122	2.110	2.108
EPCSRST_N_0	B31	2.138	2.136	2.205	2.203	2.176	2.174	2.155	2.152	2.122	2.118	2.108	2.104
EPCSRST_N_1	B32	2.138	2.137	2.203	2.204	2.173	2.175	2.152	2.155	2.117	2.122	2.102	2.108
EPCSRST_N_2	B34	2.139	2.137	2.206	2.205	2.177	2.176	2.157	2.156	2.125	2.124	2.112	2.111
EPCSRST_N_3	B35	2.139	2.138	2.206	2.206	2.178	2.178	2.158	2.159	2.126	2.128	2.113	2.115
EPCSRST_N_4	B36	2.136	2.136	2.202	2.203	2.171	2.173	2.150	2.152	2.113	2.118	2.098	2.104
EPCSRST_N_5	B37	2.138	2.137	2.205	2.205	2.177	2.176	2.157	2.156	2.124	2.123	2.110	2.110
MONITOR	K23	2.138	2.136	2.205	2.204	2.176	2.176	2.156	2.156	2.124	2.124	2.111	2.111
PLL_MON	L20	2.139	2.138	2.208	2.208	2.182	2.181	2.165	2.163	2.137	2.135	2.125	2.123
TOGGLE_MON	L22	2.139	2.138	2.207	2.207	2.181	2.179	2.163	2.161	2.133	2.132	2.121	2.120

Table. 15. LVCMOS 25 VOL – DUT 10759

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	234.3	234.0	167.5	167.3	195.5	195.5	216.6	216.4	248.2	248.0	261.7	261.7
EPCSRST_N_0	B31	234.1	234.2	167.8	168.0	196.2	196.7	217.5	218.0	249.9	250.6	263.9	264.7
EPCSRST_N_1	B32	235.3	234.5	169.5	167.8	198.7	196.0	221.5	218.0	255.4	250.1	270.1	263.9
EPCSRST_N_2	B34	235.5	235.4	167.5	167.7	195.4	195.4	216.7	216.6	247.8	247.8	261.0	261.1
EPCSRST_N_3	B35	235.0	234.5	167.2	166.3	195.0	193.6	216.4	214.5	247.4	244.5	260.6	257.2
EPCSRST_N_4	B36	237.5	236.6	171.6	169.8	201.5	198.8	224.8	221.3	259.7	254.3	275.0	268.7
EPCSRST_N_5	B37	235.7	235.5	168.1	167.9	196.2	195.9	218.0	217.6	249.5	249.0	263.0	262.5
MONITOR	K23	235.4	236.6	167.7	170.3	195.6	199.5	217.3	222.4	248.0	255.8	261.0	270.1
PLL_MON	L20	232.9	232.9	163.5	163.8	189.6	190.1	209.5	210.0	236.7	237.3	247.8	248.8
TOGGLE_MON	L22	233.7	233.6	164.8	164.9	191.2	191.7	211.6	212.0	240.1	240.9	252.1	252.8

Table. 16. LVCMOS 25 VOL – DUT 10765

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	235.6	235.5	167.7	167.8	196.0	196.2	217.3	217.3	248.8	249.1	262.5	262.8
EPCSRST_N_0	B31	234.5	234.7	167.6	168.0	195.9	196.6	217.3	217.8	249.4	250.3	263.2	264.2
EPCSRST_N_1	B32	236.1	235.3	170.4	168.5	200.0	197.0	223.0	219.1	257.6	251.4	272.7	265.4
EPCSRST_N_2	B34	235.5	235.8	168.0	168.2	196.0	196.3	217.7	218.0	249.1	249.6	262.6	263.0
EPCSRST_N_3	B35	235.2	235.1	167.5	166.7	195.4	194.2	216.6	215.0	247.4	244.9	260.5	257.7
EPCSRST_N_4	B36	237.7	236.8	171.9	170.0	201.7	198.8	225.0	221.3	259.9	254.1	275.1	268.4
EPCSRST_N_5	B37	235.8	235.9	168.4	168.3	196.4	196.3	218.2	218.1	249.8	249.6	263.3	263.1
MONITOR	K23	235.6	235.2	167.4	166.8	195.4	194.4	216.9	215.7	247.5	245.5	260.6	258.2
PLL_MON	L20	232.8	233.1	163.2	163.7	189.2	189.9	209.3	210.0	236.3	237.2	247.6	248.7
TOGGLE_MON	L22	233.7	233.8	164.6	165.0	191.4	191.8	211.5	212.1	240.0	240.7	251.8	252.7

Table. 17. LVCMOS 25 VOL – DUT 10772

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	237.0	236.8	169.3	169.1	197.7	197.7	219.0	219.0	250.8	250.9	264.5	264.8
EPCSRST_N_0	B31	236.0	236.4	168.8	169.3	197.5	197.9	218.7	219.2	250.9	251.6	264.8	265.6
EPCSRST_N_1	B32	237.6	236.4	171.8	169.3	201.6	197.7	225.0	219.7	260.1	252.2	275.6	266.1
EPCSRST_N_2	B34	237.6	238.0	169.4	169.7	197.6	197.8	219.0	219.5	250.6	251.0	263.9	264.5
EPCSRST_N_3	B35	237.7	237.4	169.0	168.2	197.0	195.7	218.3	216.8	249.5	247.1	262.6	259.9
EPCSRST_N_4	B36	239.8	239.0	173.4	171.5	203.6	200.8	227.0	223.4	262.5	256.8	278.0	271.3
EPCSRST_N_5	B37	237.7	237.7	169.4	169.3	197.7	197.6	219.4	219.1	251.0	250.4	264.4	263.8
MONITOR	K23	237.1	239.0	168.6	172.2	196.7	202.0	218.4	225.6	249.2	259.7	262.3	274.6
PLL_MON	L20	233.9	234.1	164.1	164.6	190.5	191.0	210.2	211.1	237.5	238.7	248.6	250.0
TOGGLE_MON	L22	235.1	235.2	166.0	166.0	192.9	192.9	213.3	213.3	242.1	242.0	254.2	254.0

Table. 18. LVCMOS 25 VOL – DUT 10807

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	236.0	235.3	168.3	167.9	196.6	196.2	217.7	217.1	249.2	248.6	262.8	262.3
EPCSRST_N_0	B31	235.4	237.2	168.5	172.5	197.1	203.2	218.6	226.6	251.0	263.2	265.1	279.2
EPCSRST_N_1	B32	236.9	235.8	170.5	169.0	199.9	197.5	222.9	219.6	257.1	252.5	271.9	266.7
EPCSRST_N_2	B34	236.5	236.1	168.6	168.3	196.8	196.4	218.3	217.7	249.6	248.9	263.1	262.4
EPCSRST_N_3	B35	236.7	235.7	168.6	167.4	196.6	195.0	218.1	215.7	249.2	246.0	262.4	258.8
EPCSRST_N_4	B36	238.8	237.1	172.7	170.1	202.8	199.1	226.2	221.0	261.2	253.9	276.6	268.2
EPCSRST_N_5	B37	237.2	236.6	169.3	169.2	197.5	197.6	219.3	219.2	251.1	251.3	264.6	265.0
MONITOR	K23	236.2	235.4	168.0	167.6	195.9	195.3	217.6	216.5	248.4	247.3	261.4	260.2
PLL_MON	L20	232.9	232.4	163.4	163.5	189.5	189.5	209.3	209.7	236.4	237.1	247.8	248.7
TOGGLE_MON	L22	233.8	233.4	165.1	165.3	191.8	192.2	212.2	212.7	240.8	241.8	252.8	254.2

Table. 19. LVCMOS 25 VOL – DUT 10822

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	231.1	231.2	165.1	165.4	192.9	193.3	213.9	214.0	245.1	245.6	258.5	259.1
EPCSRST_N_0	B31	229.9	230.7	165.1	166.1	193.2	194.8	214.5	216.1	246.5	249.1	260.4	263.4
EPCSRST_N_1	B32	231.7	231.1	167.3	165.6	196.3	193.6	219.1	215.3	253.1	247.2	267.8	261.0
EPCSRST_N_2	B34	231.4	231.8	165.2	165.4	192.6	193.0	213.8	214.3	244.7	245.0	258.1	258.5
EPCSRST_N_3	B35	231.8	231.6	165.2	164.6	192.6	191.6	213.9	212.4	244.8	242.4	258.1	255.3
EPCSRST_N_4	B36	233.8	233.3	169.6	167.7	199.1	196.3	222.3	218.7	257.3	251.7	272.7	265.9
EPCSRST_N_5	B37	231.8	232.1	165.6	165.8	193.5	193.6	215.0	215.2	246.6	246.6	260.0	260.0
MONITOR	K23	231.5	231.5	165.4	165.1	193.1	192.6	214.8	214.1	245.7	244.6	259.0	257.6
PLL_MON	L20	228.9	229.1	160.6	161.0	186.2	186.7	205.9	206.5	232.9	233.8	244.1	245.2
TOGGLE_MON	L22	229.8	229.9	162.3	162.4	188.6	188.7	208.7	208.8	236.8	237.1	248.7	249.0

Table. 20. LVTTL VOH – DUT 10759

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.922	2.922	2.913	2.912	2.894	2.893	2.875	2.874	2.856	2.854
EPCSRST_N_0	B31	2.922	2.921	2.912	2.911	2.893	2.891	2.873	2.871	2.853	2.851
EPCSRST_N_1	B32	2.922	2.922	2.911	2.912	2.889	2.892	2.868	2.873	2.847	2.854
EPCSRST_N_2	B34	2.922	2.921	2.913	2.913	2.894	2.894	2.876	2.875	2.858	2.857
EPCSRST_N_3	B35	2.923	2.922	2.913	2.914	2.895	2.896	2.877	2.879	2.859	2.862
EPCSRST_N_4	B36	2.921	2.921	2.909	2.910	2.887	2.890	2.865	2.869	2.843	2.849
EPCSRST_N_5	B37	2.923	2.922	2.913	2.912	2.894	2.893	2.875	2.874	2.856	2.856
MONITOR	K23	2.921	2.919	2.912	2.908	2.893	2.887	2.875	2.866	2.857	2.846
PLL_MON	L20	2.923	2.921	2.915	2.914	2.901	2.899	2.886	2.884	2.872	2.870
TOGGLE_MON	L22	2.923	2.921	2.914	2.913	2.899	2.897	2.883	2.881	2.867	2.865

Table. 21. LVTTL VOH – DUT 10765

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.921	2.920	2.912	2.910	2.893	2.891	2.873	2.872	2.854	2.853
EPCSRST_N_0	B31	2.921	2.920	2.912	2.911	2.892	2.891	2.873	2.871	2.853	2.851
EPCSRST_N_1	B32	2.920	2.921	2.909	2.911	2.887	2.891	2.865	2.871	2.844	2.852
EPCSRST_N_2	B34	2.921	2.921	2.912	2.911	2.893	2.892	2.874	2.873	2.856	2.854
EPCSRST_N_3	B35	2.922	2.922	2.913	2.913	2.894	2.895	2.876	2.878	2.859	2.861
EPCSRST_N_4	B36	2.920	2.920	2.909	2.909	2.886	2.889	2.864	2.869	2.842	2.849
EPCSRST_N_5	B37	2.922	2.921	2.912	2.911	2.893	2.892	2.874	2.873	2.855	2.855
MONITOR	K23	2.921	2.920	2.911	2.911	2.893	2.893	2.875	2.876	2.857	2.859
PLL_MON	L20	2.922	2.921	2.915	2.913	2.900	2.899	2.885	2.884	2.872	2.870
TOGGLE_MON	L22	2.922	2.921	2.914	2.913	2.898	2.897	2.882	2.881	2.867	2.865

Table. 22. LVTTL VOH – DUT 10772

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.920	2.919	2.910	2.909	2.891	2.890	2.872	2.870	2.853	2.851
EPCSRST_N_0	B31	2.920	2.919	2.910	2.909	2.891	2.890	2.872	2.870	2.852	2.850
EPCSRST_N_1	B32	2.919	2.920	2.908	2.910	2.885	2.890	2.863	2.870	2.841	2.851
EPCSRST_N_2	B34	2.920	2.919	2.910	2.909	2.892	2.890	2.873	2.872	2.855	2.853
EPCSRST_N_3	B35	2.920	2.920	2.911	2.911	2.893	2.894	2.874	2.876	2.857	2.859
EPCSRST_N_4	B36	2.918	2.918	2.906	2.908	2.884	2.887	2.861	2.866	2.839	2.846
EPCSRST_N_5	B37	2.920	2.919	2.911	2.910	2.891	2.891	2.873	2.873	2.854	2.854
MONITOR	K23	2.919	2.917	2.910	2.906	2.892	2.884	2.873	2.862	2.856	2.841
PLL_MON	L20	2.922	2.921	2.914	2.913	2.900	2.898	2.885	2.883	2.871	2.869
TOGGLE_MON	L22	2.921	2.920	2.913	2.912	2.897	2.896	2.881	2.880	2.865	2.864

Table. 23. LVTTL VOH – DUT 10807

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.920	2.920	2.911	2.910	2.892	2.891	2.873	2.873	2.854	2.853
EPCSRST_N_0	B31	2.920	2.918	2.910	2.906	2.891	2.882	2.871	2.858	2.851	2.834
EPCSRST_N_1	B32	2.919	2.920	2.909	2.910	2.887	2.890	2.865	2.869	2.845	2.850
EPCSRST_N_2	B34	2.920	2.920	2.911	2.910	2.892	2.892	2.873	2.873	2.855	2.855
EPCSRST_N_3	B35	2.921	2.921	2.911	2.912	2.893	2.894	2.874	2.877	2.856	2.860
EPCSRST_N_4	B36	2.918	2.919	2.907	2.909	2.884	2.889	2.862	2.868	2.840	2.849
EPCSRST_N_5	B37	2.920	2.920	2.910	2.910	2.891	2.890	2.872	2.871	2.854	2.852
MONITOR	K23	2.920	2.919	2.910	2.910	2.892	2.892	2.874	2.874	2.856	2.856
PLL_MON	L20	2.922	2.921	2.915	2.914	2.900	2.899	2.885	2.884	2.872	2.870
TOGGLE_MON	L22	2.922	2.921	2.914	2.913	2.897	2.896	2.881	2.879	2.866	2.863

Table. 24. LVTTL VOH – DUT 10822

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.925	2.924	2.916	2.914	2.896	2.895	2.877	2.876	2.859	2.857
EPCSRST_N_0	B31	2.925	2.924	2.915	2.914	2.896	2.893	2.876	2.872	2.856	2.852
EPCSRST_N_1	B32	2.924	2.925	2.913	2.915	2.892	2.895	2.870	2.876	2.849	2.857
EPCSRST_N_2	B34	2.925	2.924	2.916	2.915	2.897	2.896	2.878	2.877	2.860	2.860
EPCSRST_N_3	B35	2.925	2.925	2.916	2.916	2.897	2.899	2.879	2.881	2.861	2.864
EPCSRST_N_4	B36	2.923	2.923	2.912	2.913	2.889	2.892	2.866	2.871	2.844	2.851
EPCSRST_N_5	B37	2.925	2.924	2.916	2.915	2.896	2.896	2.877	2.876	2.859	2.858
MONITOR	K23	2.924	2.923	2.914	2.914	2.896	2.895	2.877	2.877	2.859	2.859
PLL_MON	L20	2.926	2.925	2.919	2.918	2.904	2.903	2.889	2.888	2.876	2.873
TOGGLE_MON	L22	2.926	2.925	2.917	2.916	2.901	2.900	2.886	2.884	2.870	2.869

Table. 25. LVTTL VOL – DUT 10759

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	214.0	213.7	223.9	223.2	241.9	241.7	260.5	260.7	280.2	280.1
EPCSRST_N_0	B31	213.9	214.1	223.7	224.0	242.8	243.5	262.5	263.3	282.9	283.8
EPCSRST_N_1	B32	215.6	214.6	227.4	225.6	246.4	242.9	267.7	262.3	289.8	282.7
EPCSRST_N_2	B34	215.3	215.5	225.6	225.5	241.8	241.6	259.9	260.2	279.3	279.3
EPCSRST_N_3	B35	215.0	214.6	225.2	224.3	241.2	239.4	259.5	256.8	278.7	275.0
EPCSRST_N_4	B36	217.4	216.3	229.9	228.0	249.7	246.3	272.1	266.7	295.1	287.9
EPCSRST_N_5	B37	215.6	215.5	226.4	226.0	242.8	242.5	261.8	261.4	281.6	280.8
MONITOR	K23	215.3	216.3	225.9	228.5	242.0	247.3	260.1	268.0	279.3	289.7
PLL_MON	L20	213.2	213.2	222.8	222.6	234.4	235.0	248.8	249.5	264.2	265.1
TOGGLE_MON	L22	213.7	213.9	223.4	223.5	236.7	237.1	252.2	253.1	268.9	270.0

Table. 26. LVTTL VOL – DUT 10765

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	215.6	215.1	224.7	224.5	242.9	243.0	261.5	262.0	281.4	281.6
EPCSRST_N_0	B31	214.5	214.8	224.1	224.2	242.7	243.5	262.0	263.3	282.3	283.4
EPCSRST_N_1	B32	216.5	215.7	228.8	226.8	248.5	244.1	270.3	263.8	293.3	284.6
EPCSRST_N_2	B34	215.7	215.7	226.0	226.8	242.9	243.3	261.7	262.2	281.5	281.7
EPCSRST_N_3	B35	215.7	215.2	226.1	225.4	242.1	240.4	259.9	257.3	278.9	275.6
EPCSRST_N_4	B36	217.5	216.9	230.4	228.6	250.3	246.5	272.5	266.4	295.7	287.8
EPCSRST_N_5	B37	216.0	216.2	226.7	226.7	243.5	243.3	262.3	262.1	282.1	281.7
MONITOR	K23	215.6	215.4	226.0	225.4	241.9	240.4	260.0	257.8	279.0	276.3
PLL_MON	L20	213.5	213.4	222.7	222.6	234.7	234.8	248.8	249.6	264.2	265.2
TOGGLE_MON	L22	214.1	214.3	223.4	223.6	237.0	237.5	252.5	253.2	269.0	270.0

Table. 27. LVTTL VOL – DUT 10772

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	216.4	216.4	226.1	225.9	244.4	244.3	263.5	263.6	283.1	283.4
EPCSRST_N_0	B31	215.8	216.1	225.6	225.4	244.3	244.9	263.7	264.2	283.7	284.6
EPCSRST_N_1	B32	217.6	216.1	230.0	227.4	250.1	244.9	272.3	264.2	296.0	285.0
EPCSRST_N_2	B34	217.6	217.7	227.8	228.5	244.3	245.0	263.0	263.6	282.5	283.0
EPCSRST_N_3	B35	217.3	217.2	227.5	226.5	243.6	242.0	262.1	259.3	280.9	277.8
EPCSRST_N_4	B36	219.4	218.8	232.3	230.5	252.5	248.6	274.9	269.3	298.6	290.9
EPCSRST_N_5	B37	217.4	217.6	227.9	227.9	244.6	244.4	263.6	262.8	283.1	282.2
MONITOR	K23	216.8	218.5	227.4	230.7	243.4	250.4	261.4	271.8	280.6	294.4
PLL_MON	L20	213.9	214.2	223.3	223.4	235.2	236.1	249.4	250.7	265.0	266.5
TOGGLE_MON	L22	215.3	215.2	224.8	224.8	238.7	238.6	254.6	254.2	271.1	270.9

Table. 28. LVTTL VOL – DUT 10807

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	215.3	214.6	225.0	223.9	242.9	242.6	261.8	261.0	281.1	280.5
EPCSRST_N_0	B31	215.0	216.6	225.0	228.2	244.0	252.1	263.5	275.8	283.9	300.1
EPCSRST_N_1	B32	216.8	215.8	228.6	226.1	247.8	244.8	269.1	264.8	291.7	285.7
EPCSRST_N_2	B34	216.3	215.6	226.8	226.0	243.4	242.8	261.8	261.3	281.3	280.5
EPCSRST_N_3	B35	216.5	215.7	226.9	225.1	243.3	241.2	261.5	258.3	280.6	276.6
EPCSRST_N_4	B36	218.6	216.8	231.1	228.0	251.3	246.7	273.6	266.4	296.8	287.3
EPCSRST_N_5	B37	216.8	216.4	227.6	226.8	244.3	244.4	263.4	263.7	283.1	283.6
MONITOR	K23	215.7	215.2	226.2	225.0	242.0	241.4	260.4	259.4	279.4	278.2
PLL_MON	L20	212.8	212.4	222.2	221.9	233.8	234.5	248.3	249.0	263.7	264.8
TOGGLE_MON	L22	213.8	213.4	223.3	223.0	237.0	237.7	252.8	254.0	269.5	271.2

Table. 29. LVTTL VOL – DUT 10822

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	211.3	211.3	220.6	220.3	238.8	239.3	257.6	258.1	277.0	277.5
EPCSRST_N_0	B31	210.5	211.3	220.4	221.1	239.6	241.3	259.0	261.5	279.3	282.8
EPCSRST_N_1	B32	212.6	211.9	224.6	222.8	244.0	239.9	265.4	259.4	287.8	279.7
EPCSRST_N_2	B34	212.0	212.4	222.5	222.8	238.7	239.1	257.2	257.6	276.5	276.9
EPCSRST_N_3	B35	212.4	212.1	222.6	222.0	238.7	237.2	257.1	254.8	276.4	272.9
EPCSRST_N_4	B36	214.4	213.7	226.9	225.1	247.3	243.5	269.6	264.0	293.2	285.3
EPCSRST_N_5	B37	212.4	212.3	222.9	223.1	239.9	239.8	258.8	258.7	278.7	278.6
MONITOR	K23	212.0	212.0	223.0	222.7	239.1	238.4	257.9	256.9	277.5	275.9
PLL_MON	L20	209.7	209.8	218.4	218.4	230.5	231.1	245.1	245.8	260.5	261.5
TOGGLE_MON	L22	210.5	210.4	220.2	220.3	233.4	233.8	249.2	249.3	265.6	265.8

E. Propagation Delay

Table 30 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 30. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (µs)	Post-irradiation (µs)	Change Degradation (%)
10759	125 krad	0.457	0.457	0.00
10765	125 krad	0.47	0.471	0.21
10772	125 krad	0.461	0.462	0.22
10807	125 krad	0.482	0.486	0.83
10822	125 krad	0.457	0.456	-0.22

F. Transition Time

The figures below show the pre-irradiation and post-irradiation transitions edges. In each case the radiation induced transition degradation is not observable.

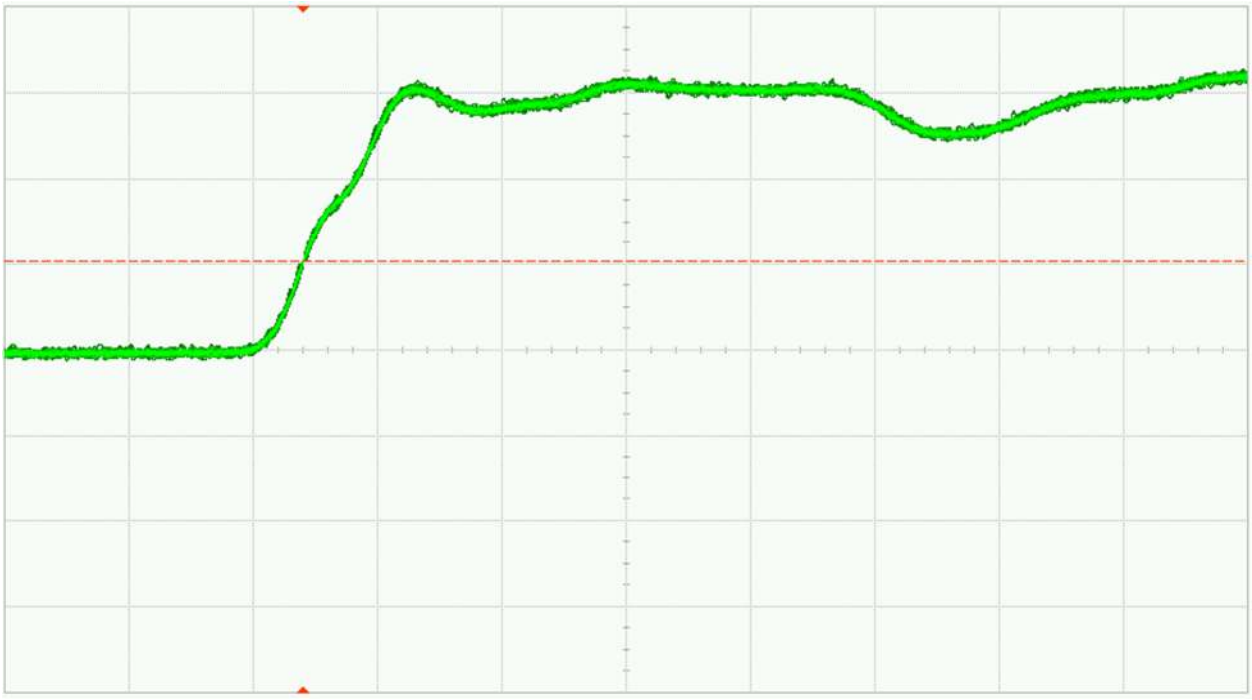

Fig. 22 (a). DUT 10759 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

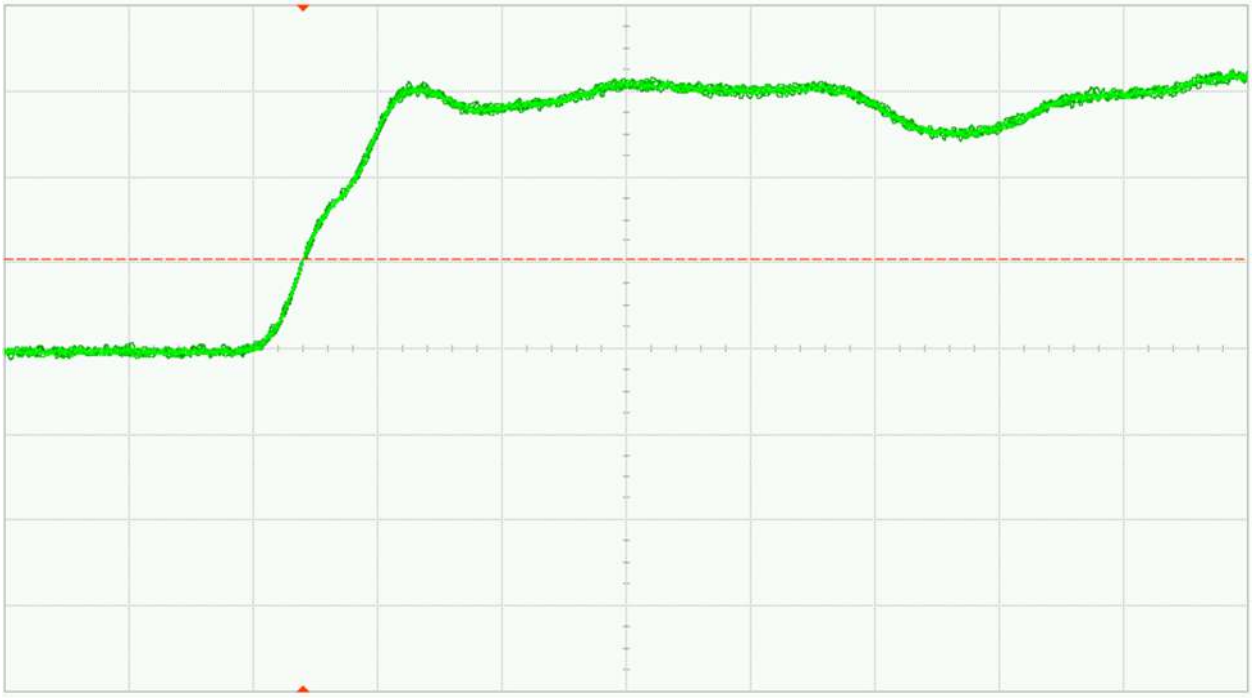

Fig. 22 (b). DUT 10759 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

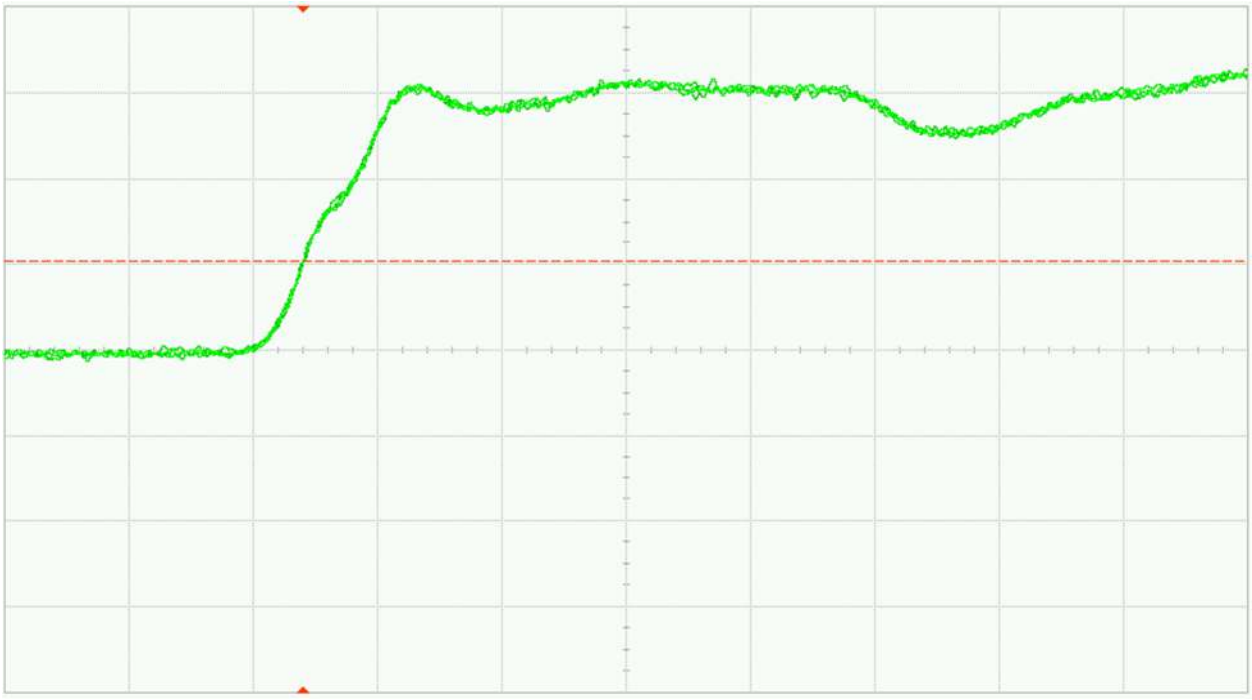

Fig. 23 (a). DUT 10765 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

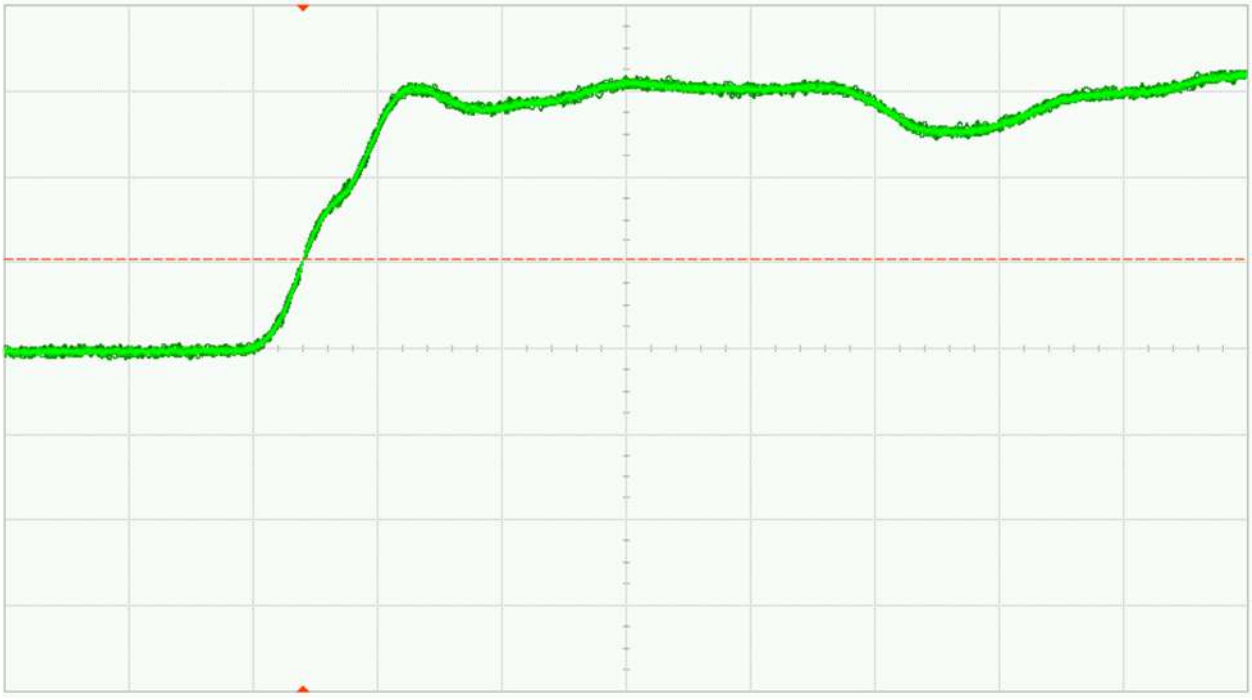

Fig. 23 (b). DUT 10765 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

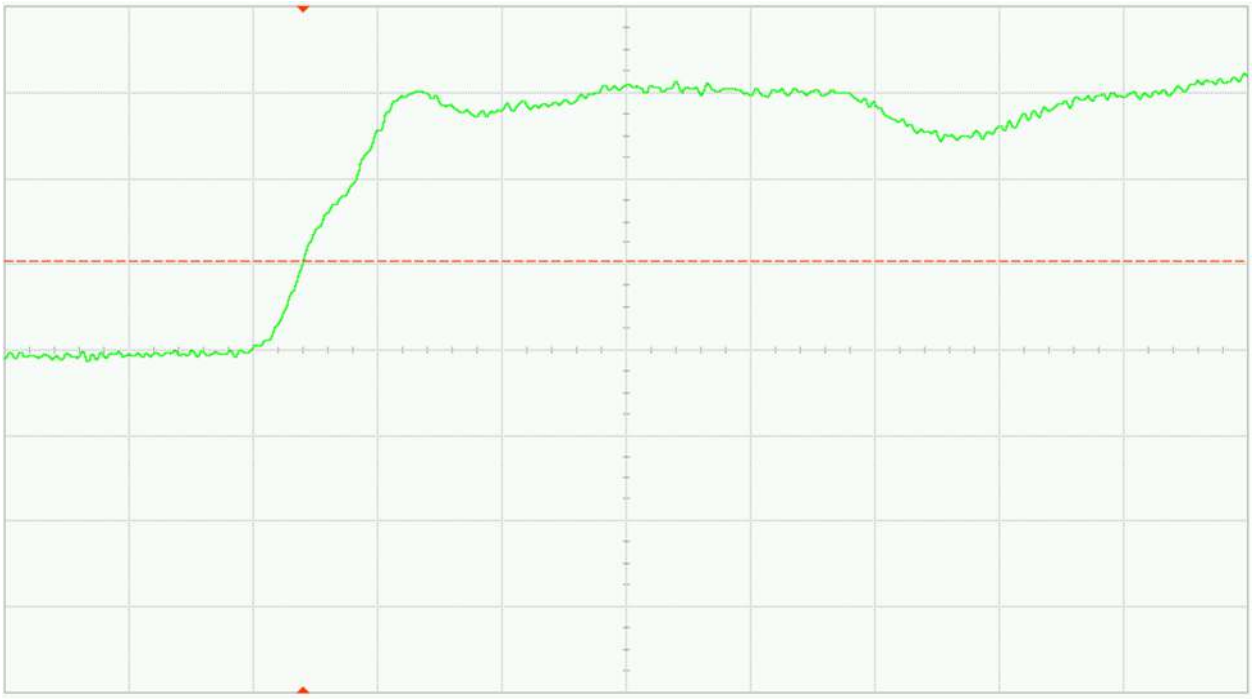

Fig. 24 (a). DUT 10772 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

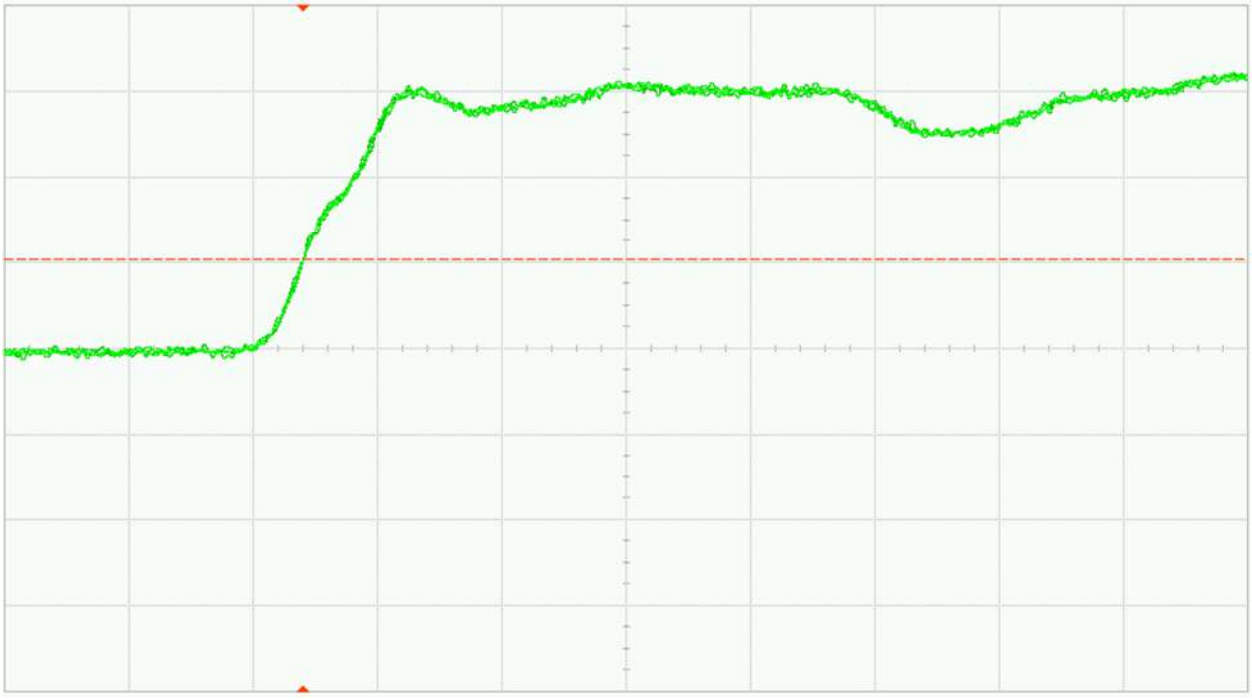

Fig. 24 (b). DUT 10772 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

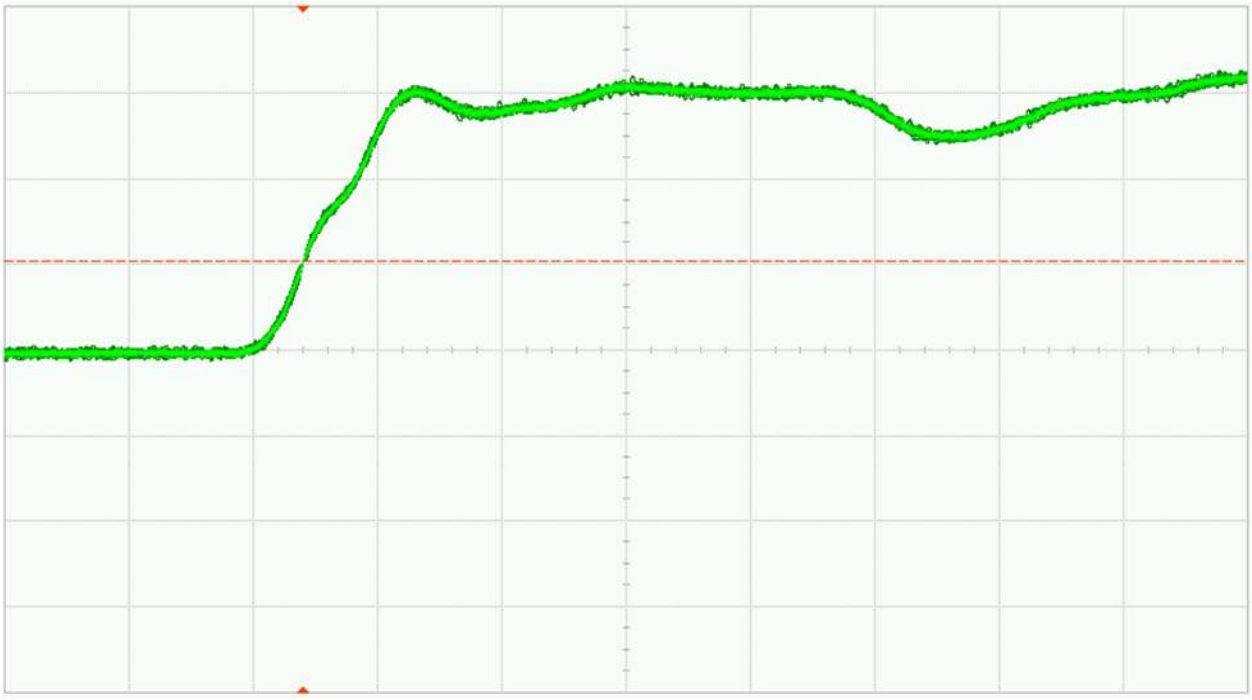

Fig. 25 (a). DUT 10807 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

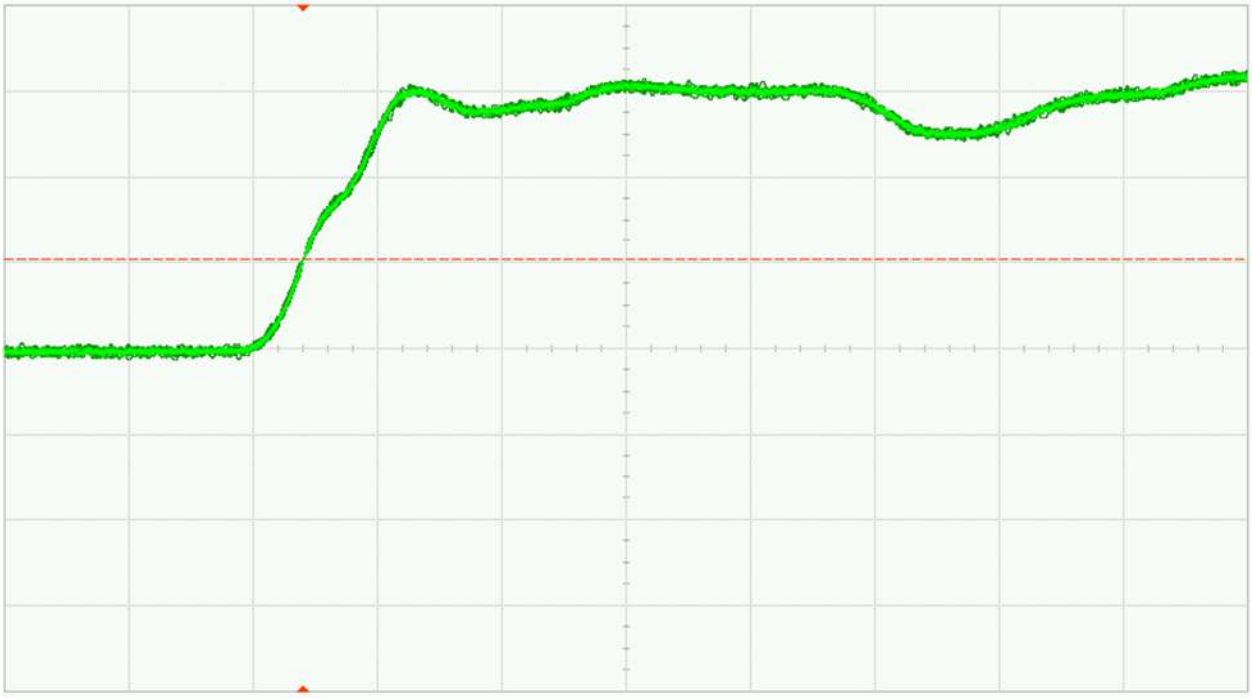

Fig. 25 (b). DUT 10807 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

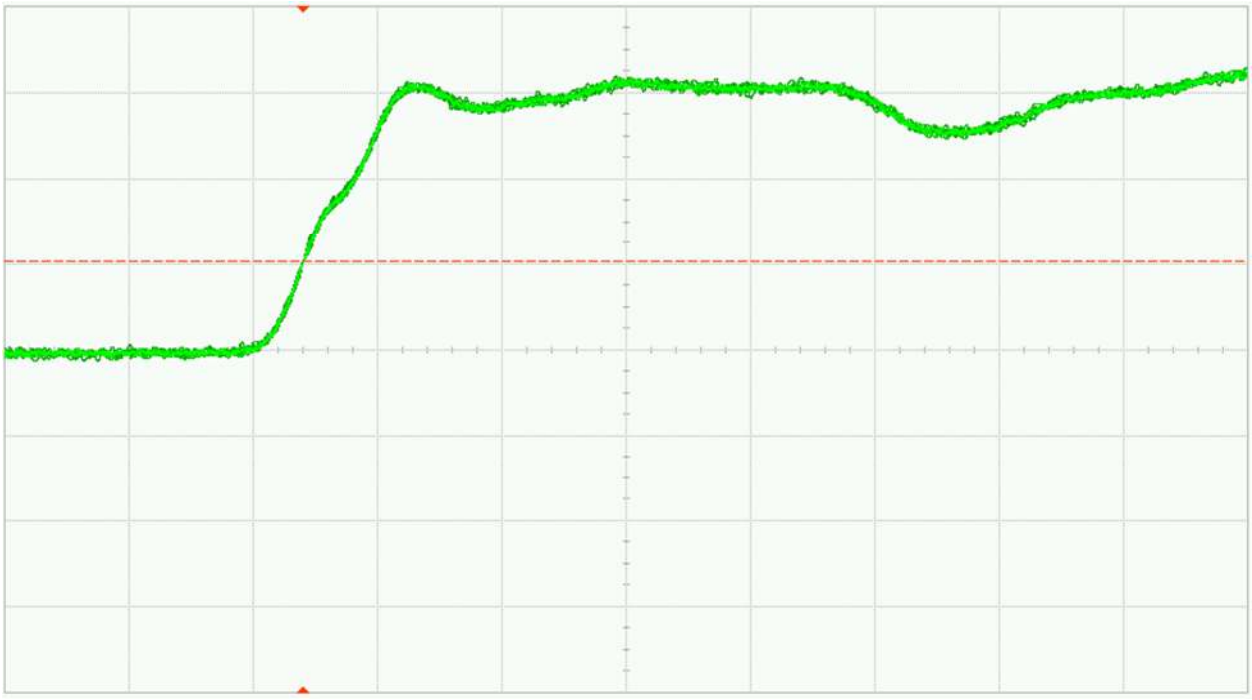

Fig. 26 (a). DUT 10822 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

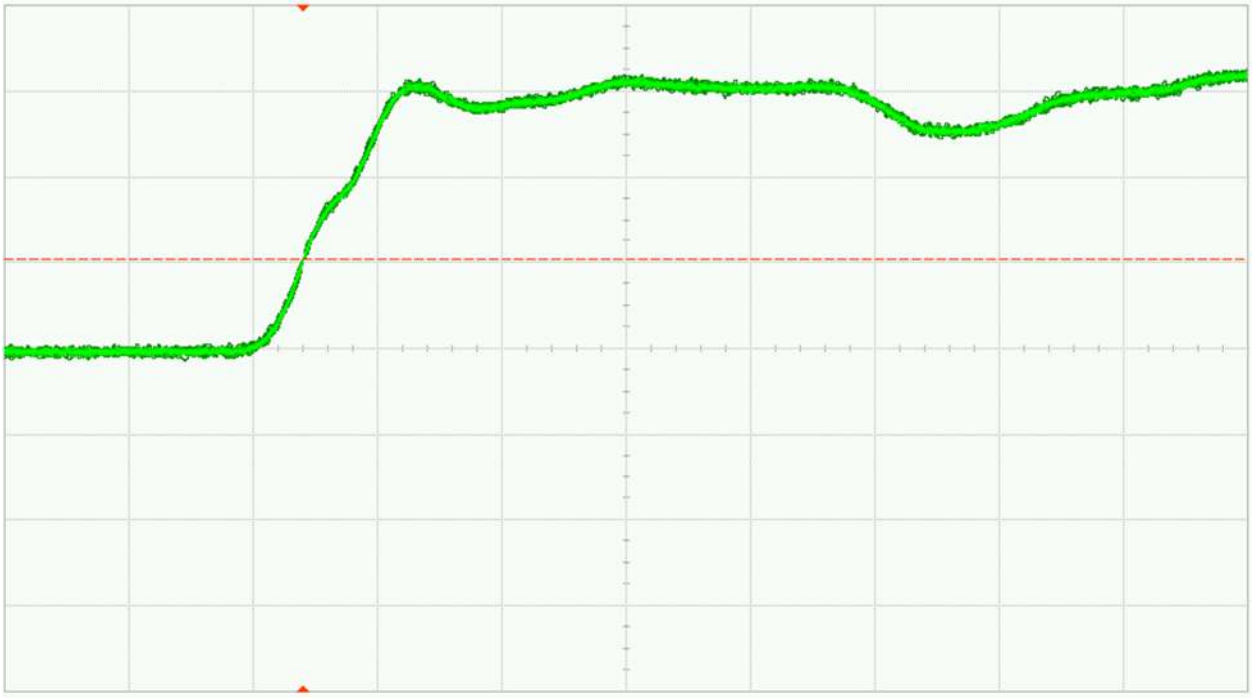

Fig. 26 (b). DUT 10822 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Fig. 27 (a). DUT 10759 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

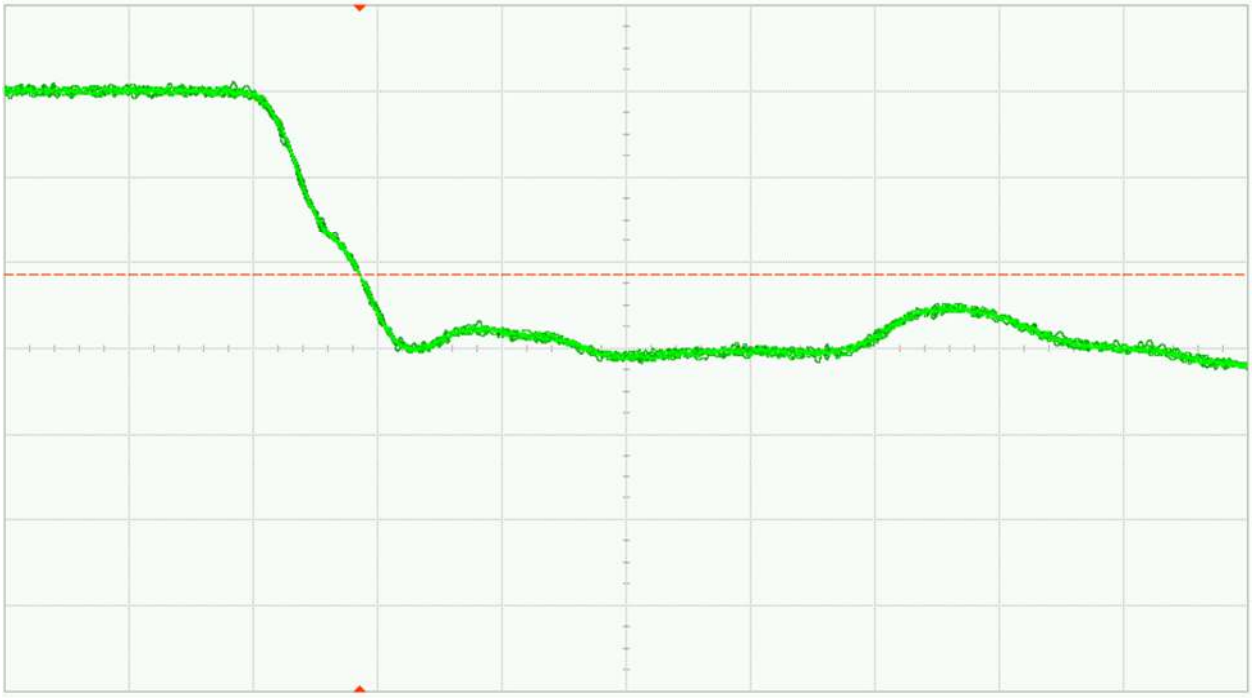

Fig. 27 (b). DUT 10759 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Fig. 28 (a). DUT 10765 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

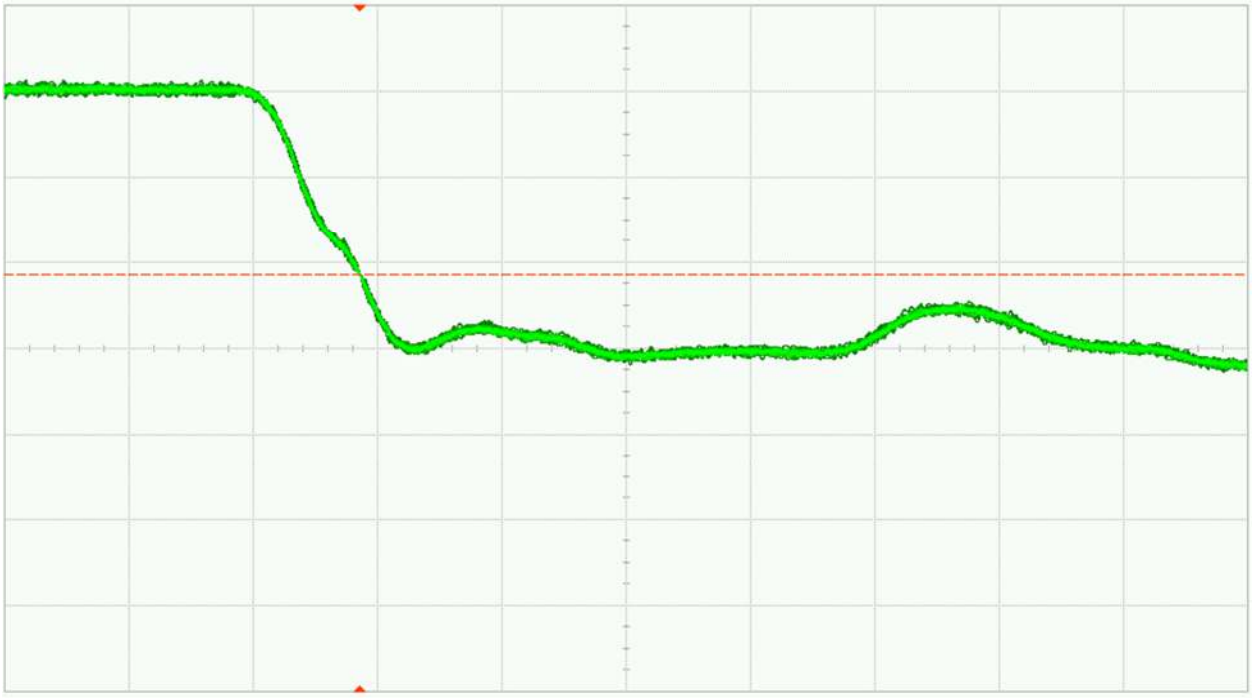

Fig. 28 (b). DUT 10765 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Fig. 29 (a). DUT 10772 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

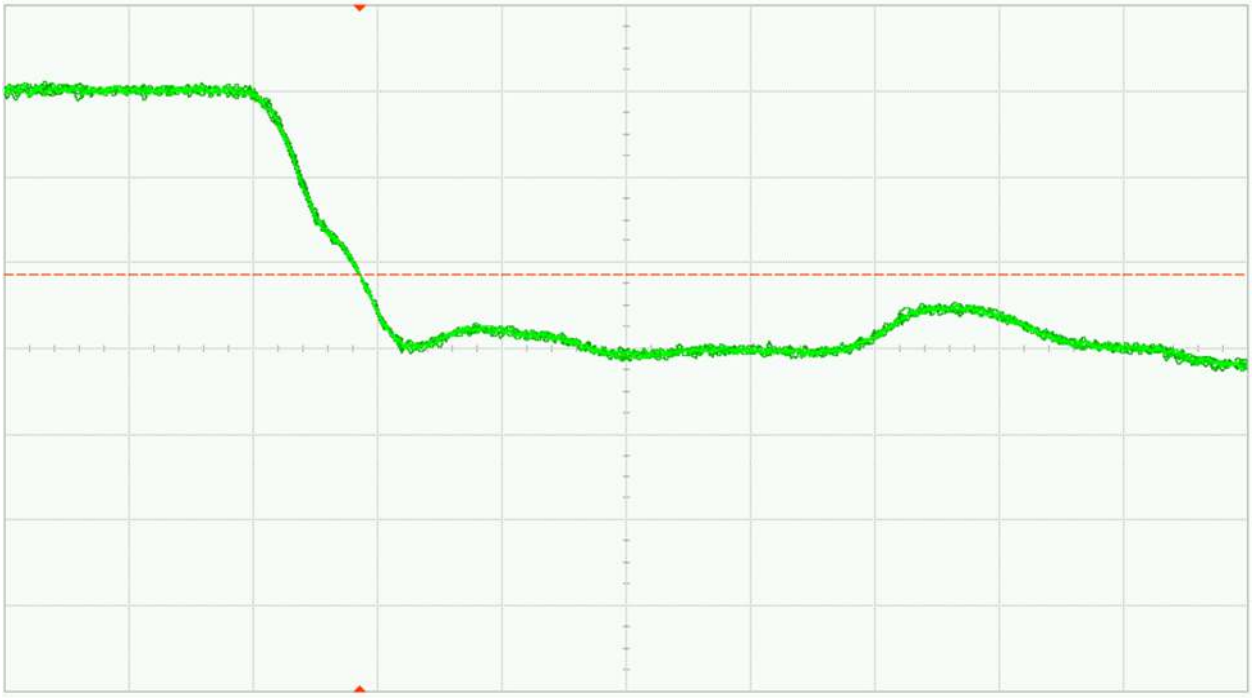

Fig. 29 (b). DUT 10772 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Fig. 30 (a). DUT 10807 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Fig. 30 (b). DUT 10807 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Fig. 31 (a). DUT 10822 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

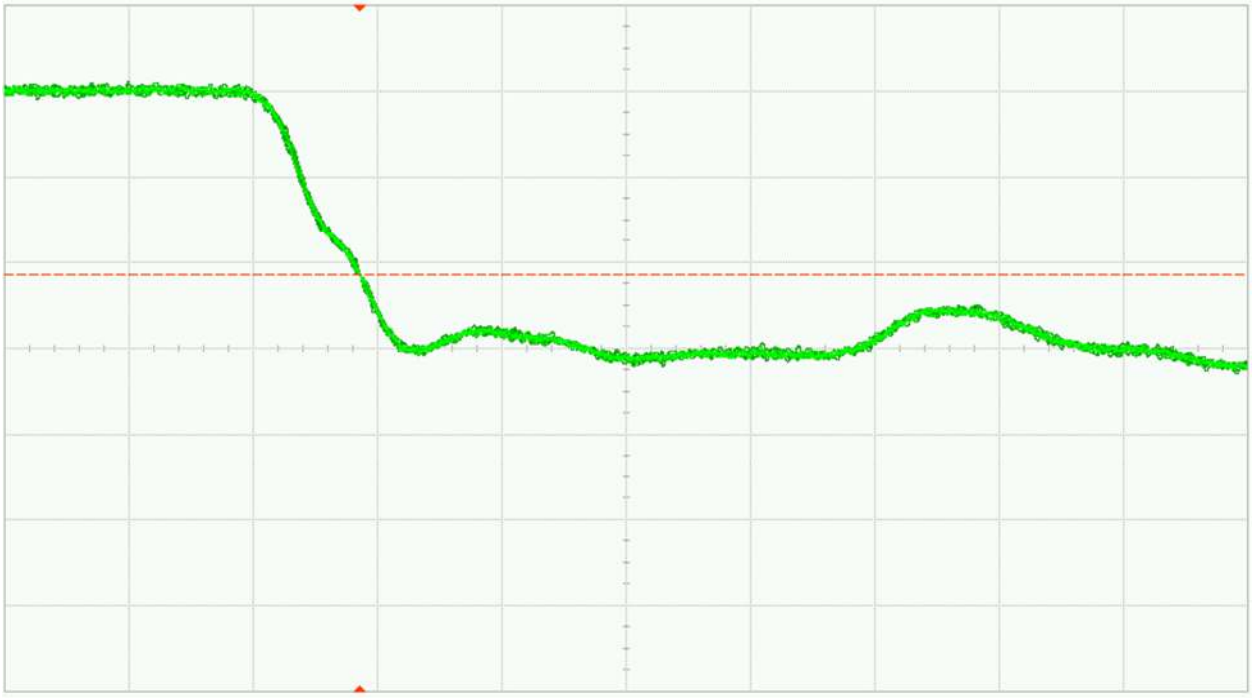

Fig. 31 (b). DUT 10822 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 35. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

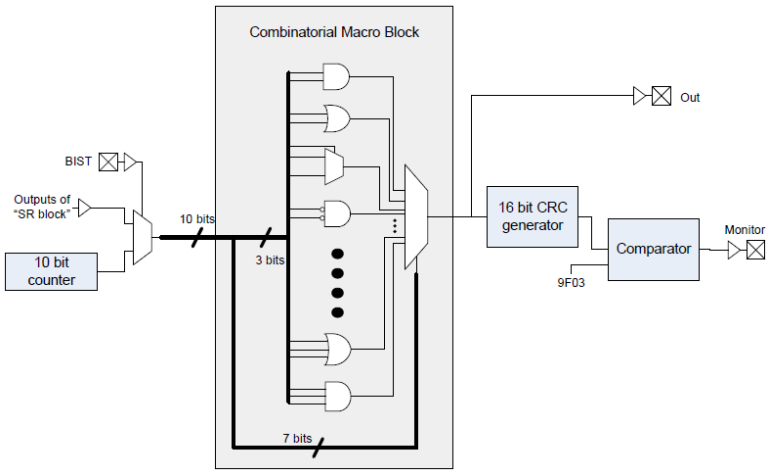

Fig. 38. Combo Block

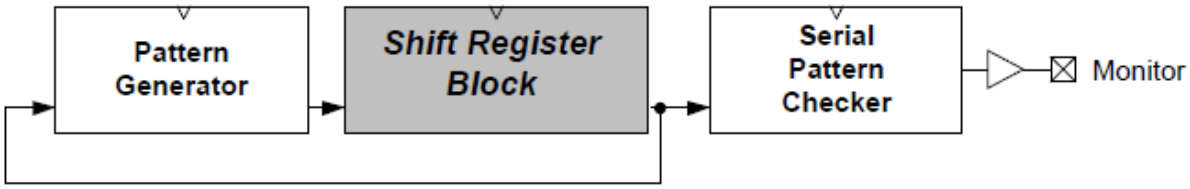

Fig. 39. Shift Register Block

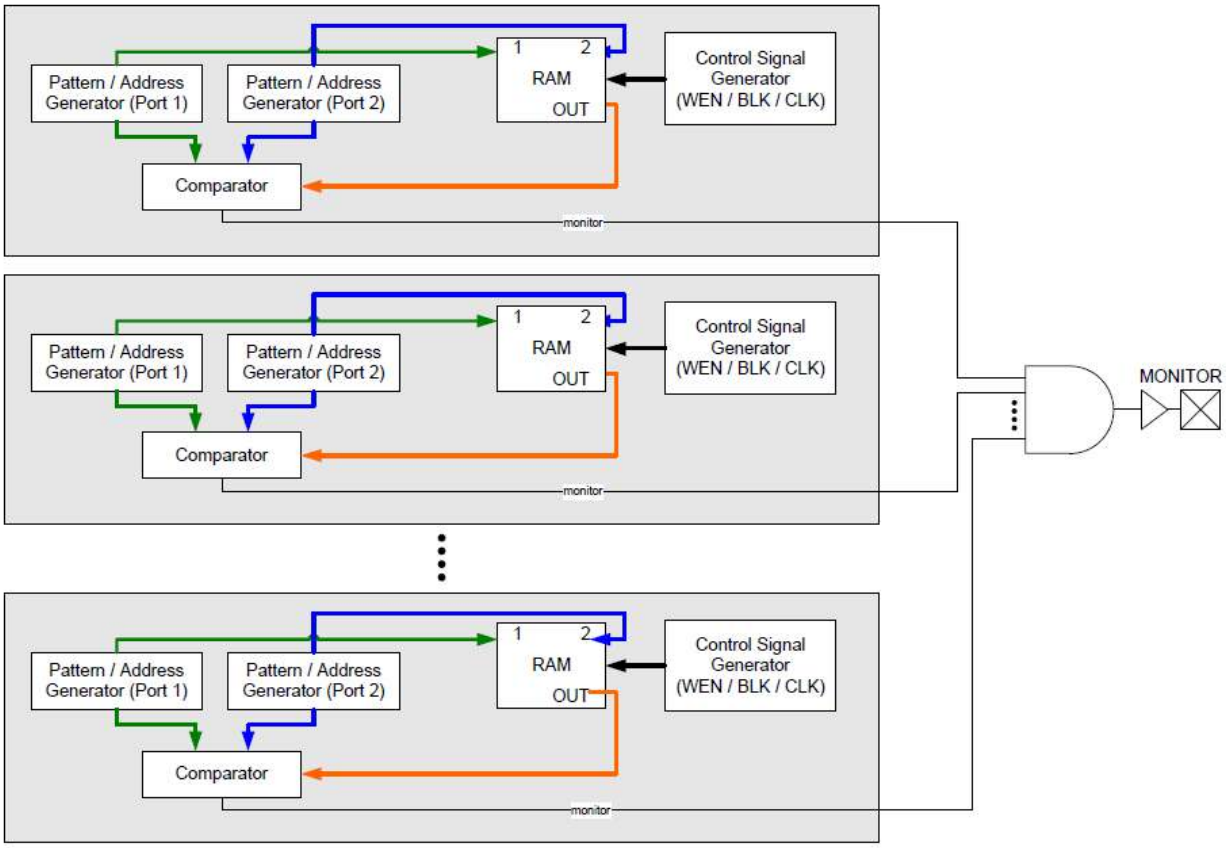

Fig. 40. Embedded Ram Blocks

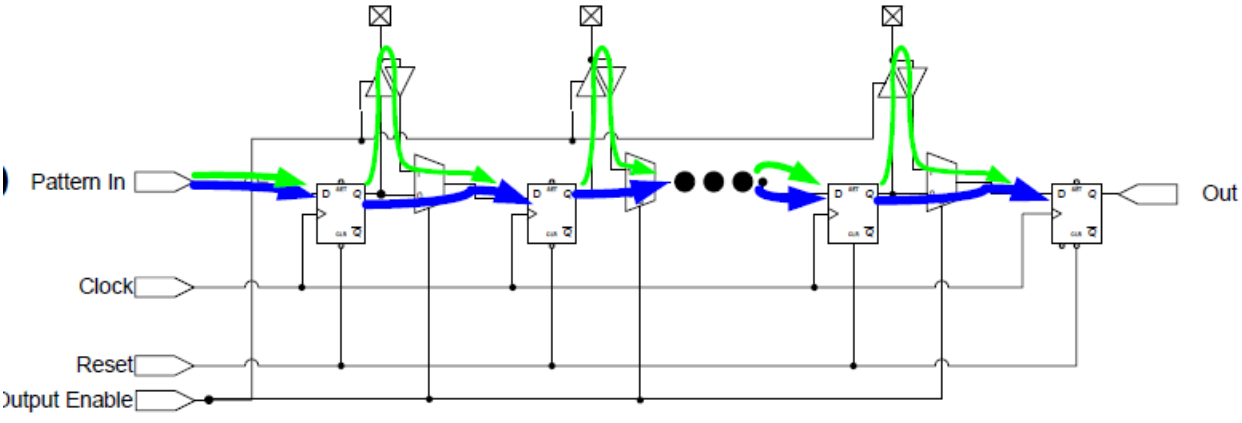

Fig. 41. IO Block

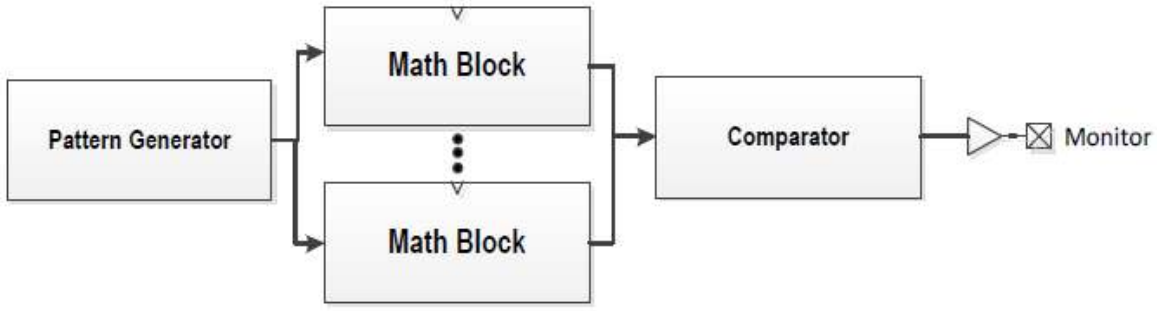

Fig. 42. Math Block

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