RTG4 Proton Testing Report

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Nadia Rezzak, J.J. Wang, Paco Mok, Connor Fraser

I. TEST OBJECTIVE

Proton testing was performed on RT4G150 device. The objectives are to test the single event effects (SEE) of FDDR and SERDES, and also perform two in-beam tests: Power-On-Reset (POR) and Program-Verify.

II. DEVICE UNDER TEST

One RT4G150 part was irradiated during the test. The sample was prepared by removing packaging material to expose the die. The testing was performed at room temperature and nominal bias using two RT4G150 evaluation boards: one master-controller board located off-beam, and one DUT board in-beam. Table 1 shows the testing configuration.

Table 1. Testing Configuration

Part Number	Revision/Lot ID	Design
RT4G150	C/KWMTM	SERDES+FDDR+POR+Program/Verify

High energy proton with approximate energy of 64 MeV is generated at Crocker Nuclear Laboratory (CNL) to bombard RT4G150 samples, which are de-capped to expose the bare silicon on the back side of the chip.

III. DUT DESIGN

1. Fabric DDR Controller (FDDRC)

The design instantiates the FDDR controller by the method documented in the RTG4 user guide. The transactions to and from the FDDR controller are handled through the AXI interface (refer to Microsemi Demo Guide DG0625)

The circuits-under-test include the following (referring to DG0625 for more details):

1) FDDRC_With_INIT
2) AXI_IF
3) FSMs responsible for Data Comparison (User Defined)

The demo design is modified to isolate the circuits-under-test as mentioned above. Additional logic blocks were moved to the master FPGA to facilitate remote user interaction and data collection.

a. Experimental Setup and Procedure:

Figure 1 shows the block diagram of the FDDR controller testing setup.

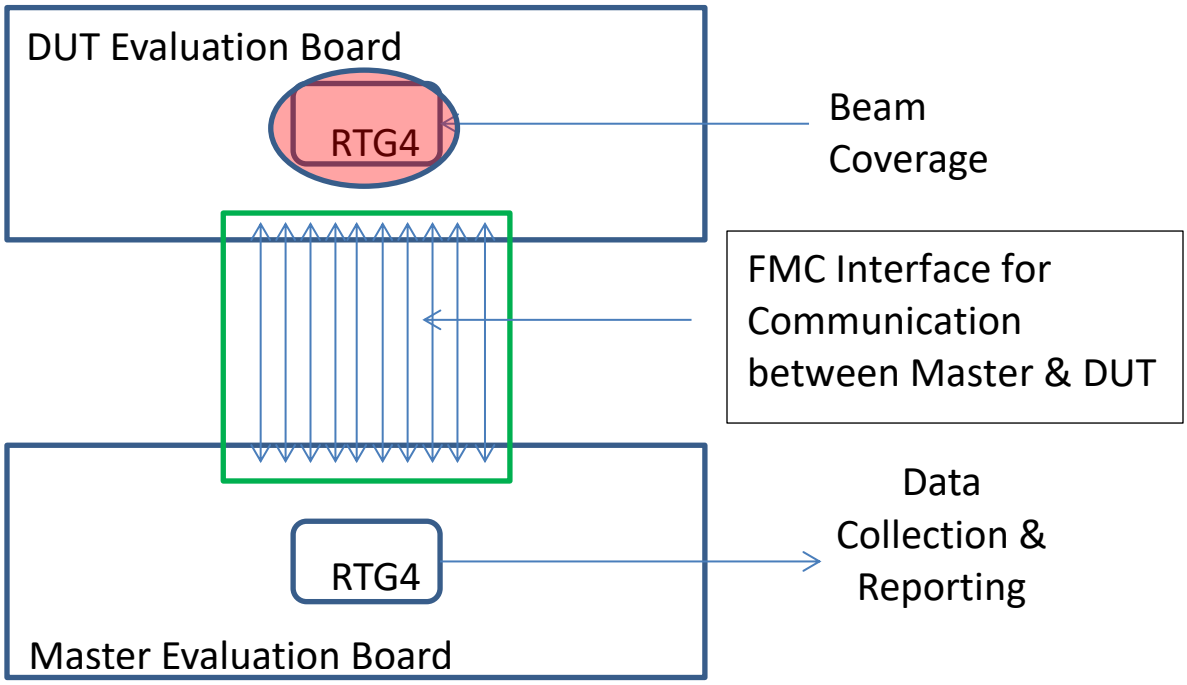

Figure. 1. Block diagram showing the DUT setup.

b. FDDR Controller Test Flow:

The Master FSMs will write the entire memory space, followed by reading and comparing. If a single event error is detected, the FSM will log the error and rewrite the entire memory. This type of error is registered when the return value of the read data does not equal the address (bad/corrupt data). If a lock up (SEFI) behavior occurs, the beam will be stopped and a reset is issued to recover the controller. In the event that the reset does not work, a power cycle will be applied. Throughout the entire test, no SEFI events were observed and no power cycle or reset were needed.

The following is a test flow for testing the FDDR controller:

1) Master controller fills DRAM with DATA = ADDRESS
2) Master controller reads and compares data with the address in sequence through the entire memory space.
3) Once the reading and writing is in progress the radiation beam is turned on.
4) If an error is detected the counter increments and the state machine reverts back to the fill state. This type of error is registered when the return value of the read data does not equal the address (bad/corrupt data)
5) Each memory address is read 3 times, the following shows how to determine the type of error:
    a. All 3 reads expected – pass
    b. All 3 reads different from expected but the read-back values are all same – write error
    c. Any of the 3 reads different from expected but not the same with each other – read error
6) If the operation locks up at any point, the beam will be stopped and resets will be issued by the user to reinitialize the test.
    d. When a lock up (SEFI) behavior is observed, the beam will be stopped immediately and a SEFI event will be recorded.

Figure 2 shows the testing flow chart.

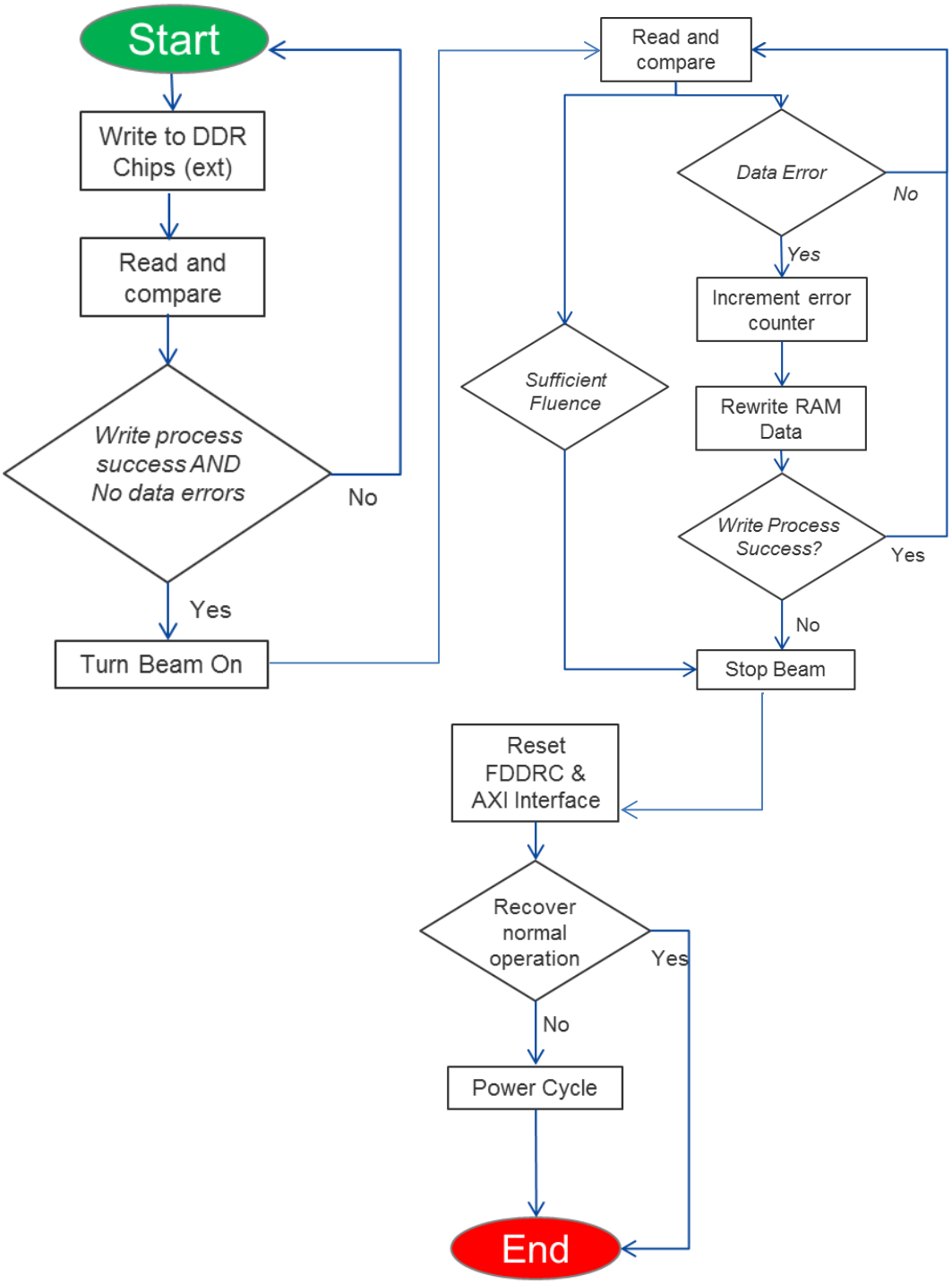

Figure. 2. FDDRC Testing flow chart

2. SERDES

The SERDES test was performed in 3 different configurations:
1) SERDES configured as RX/TX with external loop back
2) SERDES configured as Receiver (RX) only
3) SERDES configured as Transmitter (TX) only

The Demo design was used as the test design (refer to Microsemi Demo Guide DG0624), the main modification from previous design/test is the use of the SERDES internal PRBS generator and checker. Previous tests using the built-in RC oscillator and fabric generator/checker did not result in meaningful data. Testing of the RTG4 built-in RC oscillator by itself will be planned.

IV. RESULTS

1. FDDRC

No Read error, Write error or SEFI were observed during the test and an upper bound cross section is shown in Table 2.

Table 2. FDDRC Results Summary

Error Mode	# Errors	Fluence (p^+/cm^2)	σ (cm^2/FDDR)
Read Error	0	1.79×10^{11}	$<5.58\times10^{-12}$
Write Error	0	1.79×10^{11}	$<5.58\times10^{-12}$
SEFI	0	1.79×10^{11}	$<5.58\times10^{-12}$

2. SERDES

SERDES Lane data errors were observed for both Lane 0 and Lane 1 for RX/TX and RX modes only. No data errors were observed for the TX mode for both lanes because the TX circuit is much smaller in area compared to RX circuit. A large portion of the RX and TX PLL area represents a loop filter capacitor to keep the jitter low, and generally we would not expect a hit to most of that area to cause more than a very slight frequency variation that will migrate the frequency slowly and not be picked up as a TX issue, and may not be seen as an error on the receiving side. For the RX side, it has much more digital logic, thus is more susceptible to errors.

No Tx PLL loss of lock, Rx PLL loss of lock or Lock-to-data errors were observed. Rx PLL and Tx PLL lock signals represent the tolerance of the PLL and only go low if the PLL goes too fast or too slow. Lock-to-data compares the two output clocks of Rx PLL and Tx PLL. If any of the two output clocks frequency is beyond the allowed frequency band, Lock-to-data would show an error, which is consistent with the results summarized in Table 3. The JPSS-1 environment orbital error rate is summarized in Table 4.

Table 3. SERDES Results Summary

Config	Lane 0 errors	Lane 1 errors	Rx PLL	Tx PLL	Lock to data	Fluence (p^+/cm^2)	Lane 0 σ (cm^2/SERDES)	Lane 1 σ (cm^2/SERDES)
RX/TX	1	1	0	0	0	2.00×10^{11}	5.00×10^{-12}	5.00×10^{-12}
RX	2	0	0	0	0	2.00×10^{11}	1.00×10^{-11}	$<5.00\times10^{-12}$
TX	0	0	0	0	0	2.24×10^{11}	$<4.46\times10^{-12}$	$<4.46\times10^{-12}$

Table 4. SERDES JPSS-1 Orbital Upset Rate

Config	Lane 0 Upset Rate (Upset/SERDES Lane-day)	Lane 1 Upset Rate (Upset/SERDES Lane-day)
RX/TX	5.61×10^{-5}	5.61×10^{-5}
RX	1.23×10^{-4}	$<5.61\times10^{-5}$
TX	$<5.01\times10^{-5}$	$<5.01\times10^{-5}$

3. POR Test

The POR test consists of performing 10 consecutive power cycle of the part in-beam. The flux used to perform the POR test is 1.20×10^{6} $p^{+}/cm^{2}/s$. All 10 power cycles were performed successfully.

4. In-beam Program and Verify

The flux used to perform in-beam programming and verify is 1.20×10^{6} $p^{+}/cm^{2}/s$. In-beam programming passed 10 out of 10 times and after each programming success, a standalone verify was performed; all 10 out of 10 verify passed. The results are summarized in Table 5.

Table 5. In-beam Programming and Verify Summary

Attempt #	1	2	3	4	5	6	7	8	9	10
Program	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
Verify	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass

V. CONCLUSION

1. FDDRC test shows no Read errors, Write errors or SEFI.
2. SERDES results show Lane data errors for both lanes 0 and 1 in RX/TX and RX modes. No TX Lane data error, Tx PLL, Rx PLL or "Lock to data" errors were observed.
3. In-beam POR test and in-beam Programming/Verify successfully passed 10 out of 10 consecutive times.

REVISION HISTORY

Revision 1.0

Revision 1.0 was published in December 2020. It is the first publication of this document.