PolarFire® SoC

MSS Simulation User Guide

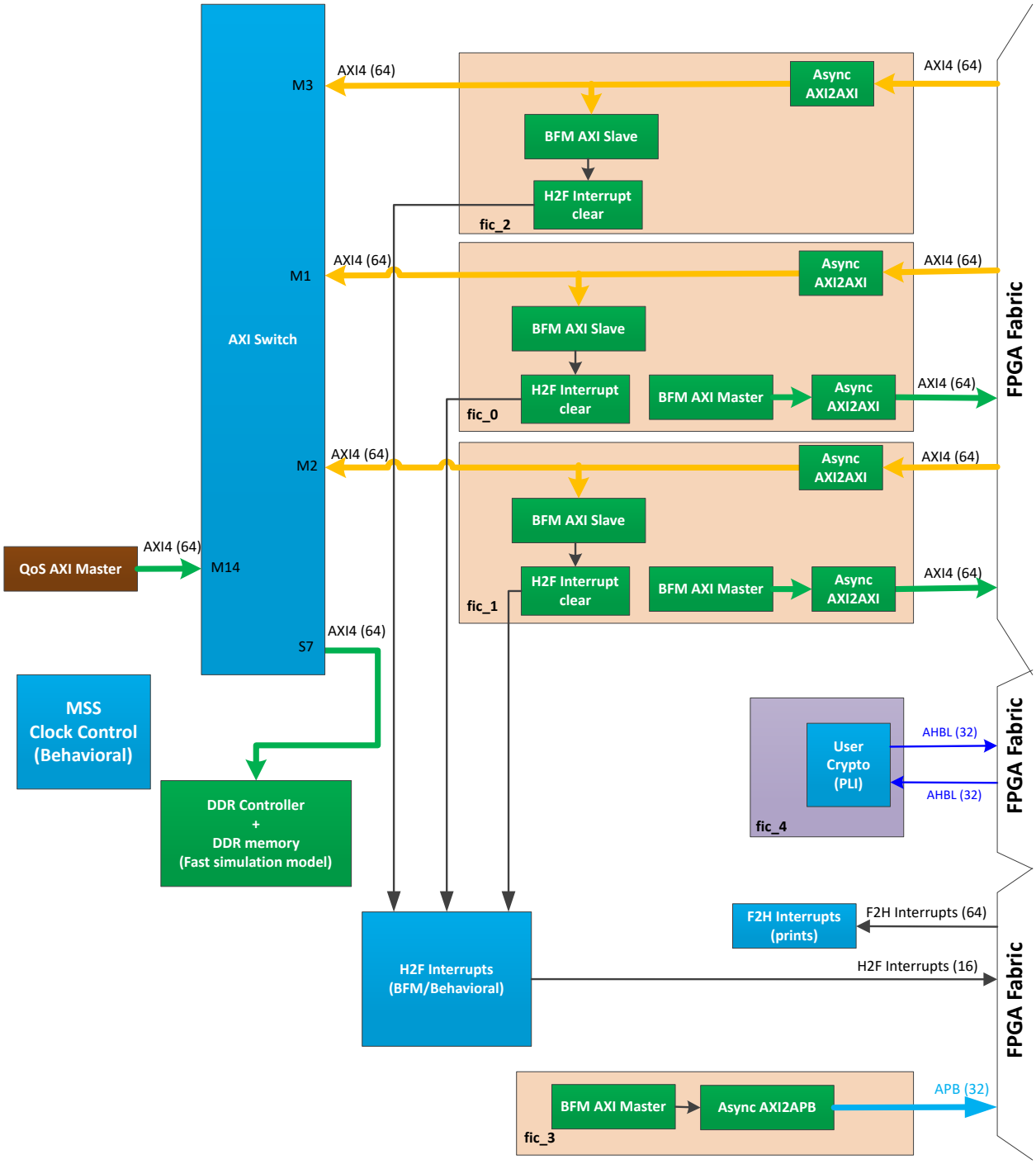
Introduction

The PolarFire SoC Microcontroller Subsystem (MSS) is modeled with Microchip's AMBA Bus Functional Model (BFM). For information about supported instructions and syntax of the BFM commands, see the DirectCore Advanced Microcontroller Bus Architecture - Bus Functional Model User's Guide.

Simulation can be useful in the following situations:

- Verifying the connectivity with the fabric logic.
- Addressing peripherals, memories etc. in the fabric that are connected to the MSS using the Fabric Interface Controllers (FICs).
- Accessing MSS-DDR from fabric master using the FICs.
- Accessing the Crypto from fabric.
- Generation of H2F and F2H interrupts.

Figure 1. Architecture of MSS Simulation Model



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1. Creating a Project

Use the MSS standalone configuration tool and Libero® SoC to create MSS-based designs. For more information, see the MSS Standalone Configurator User Guide.

1. Create the MSS configurator using the pfsoc_mss application by either creating a new configuration (`.cfg`) file or opening an existing one.
2. Configure the MSS subsystem with the required FIC interface and other necessary modules like DDR and Crypto.
3. Generate the MSS component file (`.cxz`).

After finishing with the MSS standalone configuration, import the MSS subsystem into Libero, and then design the entire system:

1. Open the Libero SoC Design Suite.
2. Create the project.
3. Invoke system builder to create your MSS block.
4. Import the MSS component file.
5. Design your entire system using MSS, AXI4 interconnect, fabric slaves, and fabric masters. The following figures show typical systems.

Figure 1-1. Example 1: Typical Smart Design Block

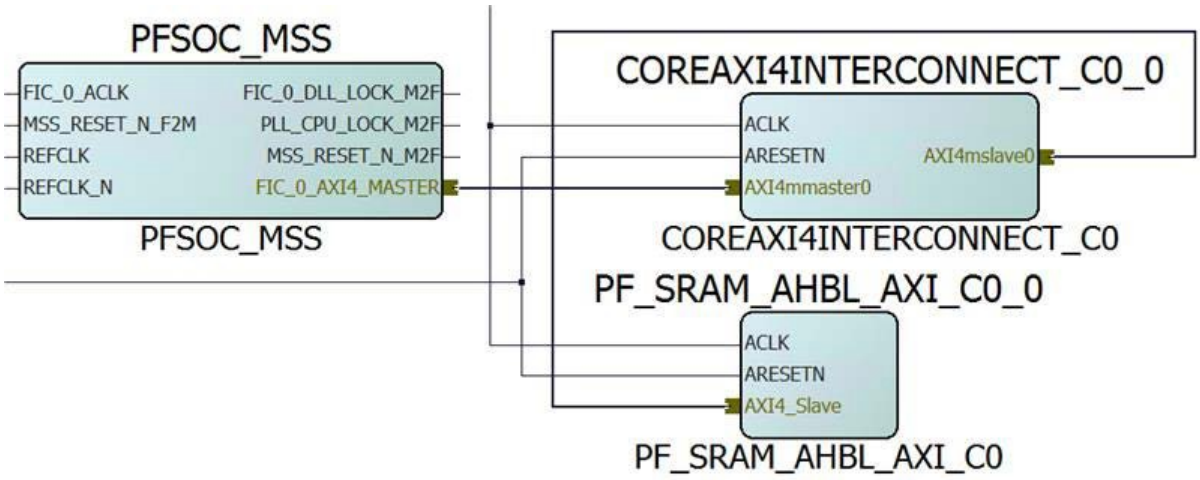
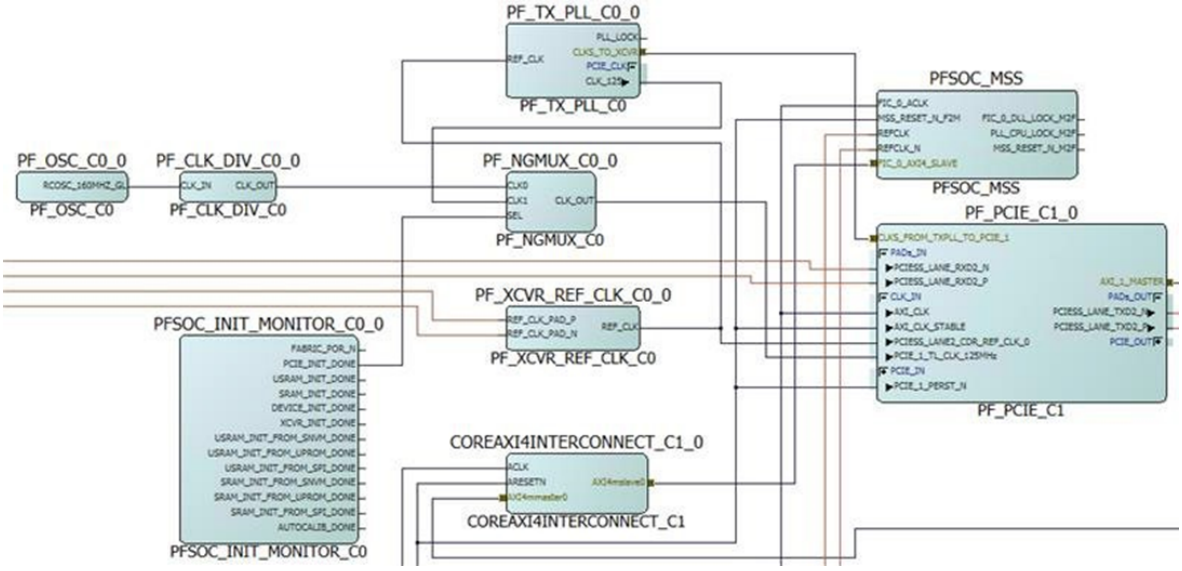
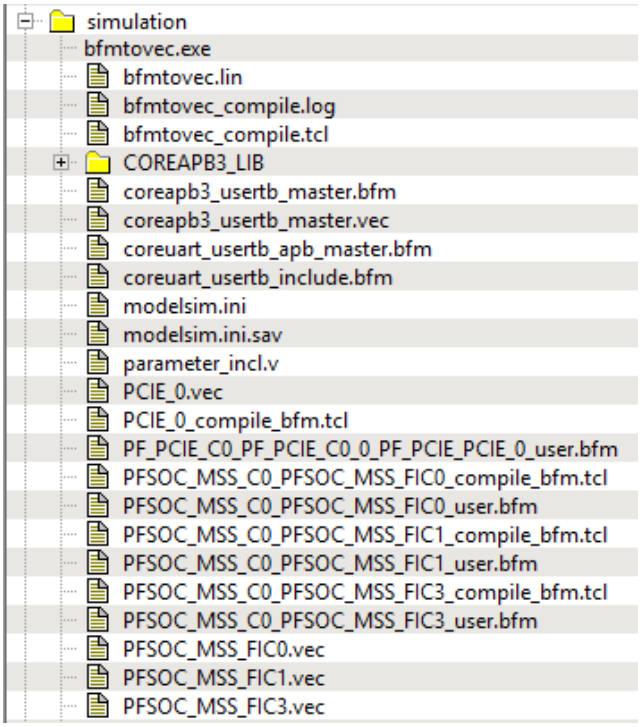


Figure 1-2. Example 2: Typical Smart Design Block



6. After designing the entire system, check the DRC and generate the system.
Libero generates three BFM files for three master FIC interfaces in a simulation folder, as shown in the following figure.

Figure 1-3. BFM Files in the Simulation Folder



7. Add the supported BFM instructions in these BFM files to perform the simulation.

2. Simulation Flow

This section describes the simulation flow for FIC interface, interrupts, the User Crypto Processor, DDR controller, and quality of service (QoS) parameters.

2.1 FIC Interface

The PolarFire SoC FPGA provides multiple FICs to enable connectivity between user logic in the FPGA fabric and the MSS. FIC is part of the MSS and acts as a bridge between the MSS and fabric.

The master FIC interface provides access to the address range listed in the following table.

Table 2-1. FIC Interface Address Ranges

FIC Interface	Number of Regions	Start Address	End Address	Size
FIC0	2	0x6000_0000	0x7FFF_FFFF	512 MB
		0x20_0000_0000	0x2F_FFFF_FFFF	64 GB
FIC1	2	0xE000_0000	0xFFFF_FFFF	512 MB
		0x30_0000_0000	0x3F_FFFF_FFFF	64 GB
FIC3	1	0x4000_0000	0x5FFF_FFFF	512 MB

The master FIC allows and initiates the AXI transaction only when addresses entered in the BFM file are within the dedicated address range. Otherwise, it shows a DRC in simulation log.

The slave FIC responds to AXI master in fabric in the following way:

- Uses AXI transaction details to clear interrupts and provides a valid AXI response.
- Provides a transparent connection between the AXI switch and FIC interface to access the DDR controller and DDR memory.
- Prints a message in simulation log on incorrect addressing for other addresses.

2.1.1 BFM Commands

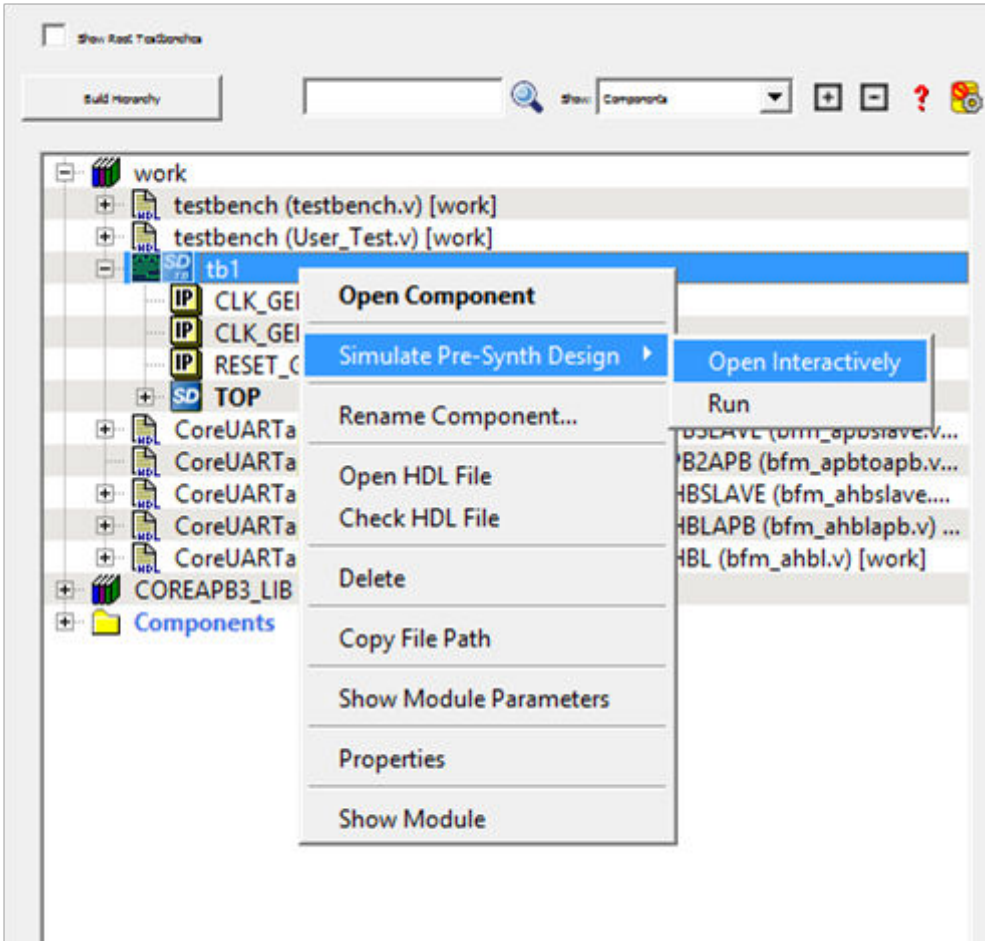
All BFM commands in the *Microchip DirectCore AMBA BFM User's Guide*, *PolarFire PCI BFM* and *SmartFusion2 FPGA High Speed Serial Interface Simulation* can be used to simulate the MSS.

The following code block shows typical BFM instructions.

```
procedure main;
memmap FPR_BASE_ADDR 0x2060000000;
int u; int l;
write64 w FPR_BASE_ADDR 0x0 0x10102020 0xaaaaaaaa read64 w FPR_BASE_ADDR 0x0
readcheck64 w FPR_BASE_ADDR 0x0 0x10102020 0xaaaaaaaa readstore64 x FPR_BASE_ADDR 0x0 u l
print "Lower 32bits = %h", l print "Upper 32bits = %h", u
readmask64 x FPR_BASE_ADDR 0x0 0x10102020 0xaaaaaaaa 0xFFFFFFFF 0x0000FFFF readstore64 x
FPR_BASE_ADDR 0x0 u l
print "Lower 32bits = %h", l print "Upper 32bits = %h", u
writemult64 w FPR_BASE_ADDR 0x0 0xFFFFFFFF 0xEEEEEEEE 0xAAAAAAAA 0xBBBBBBBB 0xCCCCCCCC
0xDDDDDDDD 0x01010101 0x02020202 0x03030303 0xBADCAD00
readmult64 w FPR_BASE_ADDR 0x0 5
readmultchk64 w FPR_BASE_ADDR 0x0 0xFFFFFFFF 0xEEEEEEEE 0xAAAAAAAA 0xBBBBBBBB 0xCCCCCCCC
0xDDDDDDDD 0x01010101 0x02020202 0x03030303 0xBADCAD00
return
```

After adding a test bench to the design, the user can use these BFM files to perform an MSS simulation by launching the Per-Synth simulation.

Figure 2-1. Simulation Launching



The simulation log shows the BFM transactions, as shown in the following figure.

Figure 2-2. MSS FIC Simulation Log – FIC_0 as Master

```
# PFSOC_FIC_0_BFM: Data Write 20600f0010 ccccccccdddddddd
# PFSOC_FIC_0_BFM:25:readmult64 x 00000020 600f0000 10 at 568 ns
# PFSOC_FIC_0_BFM: Data Write 20600f0018 0101010102020202
# PFSOC_FIC_0_BFM: Data Write 20600f0020 03030303badcad00
# PFSOC_FIC_0_BFM: Data Read 20600f0000 ffffffffeeeeeeee at 895.179000ns
# PFSOC_FIC_0_BFM: Data Read 20600f0008 aaaaaaaabbbbbbbb at 905.181000ns
# PFSOC_FIC_0_BFM: Data Read 20600f0010 ccccccccdddddddd at 915.183000ns
# PFSOC_FIC_0_BFM:26:readmultchk64 x 00000020  600f0000 ffffffff ... at 919 ns
# PFSOC_FIC_0_BFM: Data Read 20600f0018 0101010102020202 at 925.185000ns
# PFSOC_FIC_0_BFM: Data Read 20600f0020 03030303badcad00 at 935.187000ns
VSIM 2> run
# PFSOC_FIC_0_BFM: Data Read 20600f0000 ffffffffeeeeeeee MASK:ffffffffffffffff at 1085.217000ns
# PFSOC_FIC_0_BFM: Data Read 20600f0008 aaaaaaaabbbbbbbb MASK:ffffffffffffffff at 1095.219000ns
# PFSOC_FIC_0_BFM: Data Read 20600f0010 ccccccccdddddddd MASK:ffffffffffffffff at 1105.221000ns
# PFSOC_FIC_0_BFM:31:return
# PFSOC_FIC_0_BFM: Data Read 20600f0018 0101010102020202 MASK:ffffffffffffffff at 1115.223000ns
# PFSOC_FIC_0_BFM: Data Read 20600f0020 03030303badcad00 MASK:ffffffffffffffff at 1125.225000ns
################################################################################
#
# FIC_0 BFM Simulation Complete - 7 Instructions - NO ERRORS
#
################################################################################
```

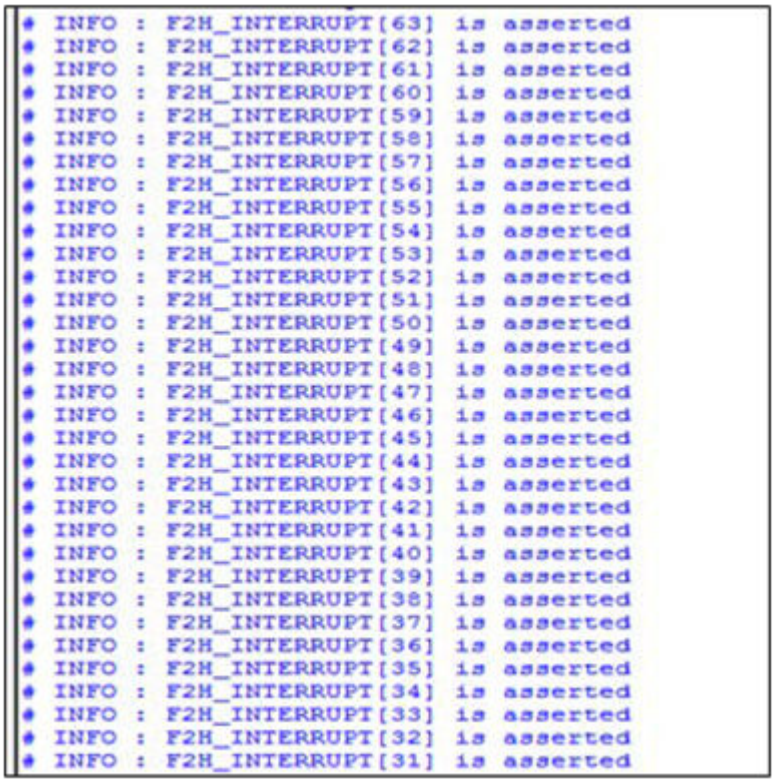
2.2 Interrupts

F2H Interrupts

The MSS simulation model acknowledges the assertion of F2H interrupts.

There are 64 F2H interrupt ports. MSS acknowledges them by printing a message when it receives a valid active high interrupt.

Figure 2-3. F2H Interrupt Simulation Log - Valid Interrupts



The interrupt inputs should be high for one clock of MSS clock; otherwise, the MSS model rejects the interrupt and prints a message about the interrupt level being too low.

Figure 2-4. F2H Interrupt Simulation Log - Invalid Interrupt

```
# ERROR : F2H_INTERRUPT[63] must stay high for at least one MSS clock cycle
```

H2F Interrupts

The MSS simulation model allows the user to use text files to set and clear H2F interrupts. To do this, add the following command in the `run.do` file:

```
vsim -L polarfire -L presynth -t 1ps -g H2F_MEMFILE=(path)/*.txt presynth.tb
```

Example: `vsim -L polarfire -L presynth -t 1ps -g H2F_MEMFILE=E:/mss_sim/h2f_sim.txt presynth.tb`

There are 16 H2F interrupts. The following table lists their allocation in MSS.

Table 2-2. Allocating MSS Interrupts

H2F Line	Group
0	GPIO

.....continued

H2F Line	Group
1	MMUART, SPI, CAN
2	I^2C
3	MAC0
4	MAC1
5	WATCHDOGS
6	Maintenance
7	SCB
8	G5C-Message
9	DDRC
10	G5C-DEVRST
11	RTC/USOC
12	TIMER
13	ENVM, QSPI
14	USB
15	MMC/SDIO

Use text file based entries to set and clear an interrupt, see the following example.

```
Wait time          (Time to wait in number MSS PLL clock cycles, Hex)
Interrupt Value    (16-bit value, Hex)
Wait time          (Time to wait in number MSS PLL clock cycles, Hex)
Interrupt Value    (16-bit value, Hex)
...
```

Example:

```
100          (Wait for 100 (256 in DEC) MSS PLL clock cycles)
FFFF         (Set all 16 interrupts)
1000         (Wait for 1000 (4096 in DEC) MSS clock cycles)
0000         (Clear all 16 interrupts)
...
```

The H2F interrupts can be cleared by clearing an interrupt register bit in the corresponding peripheral. These AXI transactions can be generated by a Master in fabric.

Table 2-3. Clearing Interrupts

H2F Line	Group	AXI Address and Data Bits to Clear an Interrupt	
0	GPIO	Reg	**g5soc_mss_regmap:GPIO:INTR**
		Physical Address	0x2012 0080 0x2012 1080 0x2012 2080 0x2812 0080 0x2812 1080 0x2812 2080
		Data	Bit-0: To clear an interrupt, write the bit with 1.
1	MMUART	Reg	**g5soc_mss_regmap:MMUART:IIM**
		Physical Address	0x2000 0028 0x2010 0028 0x2010 2028 0x2010 4028 0x2010 6028 0x2800 0028 0x2810 0028 0x2810 2028 0x2810 4028 0x2810 6028
		Data	Reading the IIM register clears this interrupt.
1	MMUART	Reg	**g5soc_mss_regmap:MMUART:MM2**
		Physical Address	0x2000 0038 0x2010 0038 0x2010 2038 0x2010 4038 0x2010 6038 0x2800 0038 0x2810 0038 0x2810 2038 0x2810 4038 0x2810 6038
		Data	Reading the MM2 clears the interrupt.

.....continued

H2F Line	Group	AXI Address and Data Bits to Clear an Interrupt	
1	MMUART	Reg	**g5soc_mss_regmap:MMUART:RTO**
		Physical Address	0x2000 004C 0x2010 004C 0x2010 204C 0x2010 404C 0x2010 604C 0x2800 004C 0x2810 004C 0x2810 204C 0x2810 404C 0x2810 604C
		Data	Writing the RTO register clears this interrupt.
1	SPI	Reg	**g5soc_mss_regmap:SPI:INT_CLEAR**
		Physical Address	0x2010 800C 0x2010 900C 0x2810 800C 0x2810 900C
		Data	Bit-5: Write 1 to clear the interrupt. Bit-4: Write 1 to clear the interrupt.
1	CAN	—	Support will be added in a future Libero release
2	I^2C	—	Support will be added in a future Libero release.
3	MAC0	—	Support will be added in a future Libero release.
4	MAC1	—	Support will be added in a future Libero release.
5	WATCHDOGS	—	Support will be added in a future Libero release.
6	Maintenance	—	Support will be added in a future Libero release.
7	SCB	—	Support will be added in a future Libero release.
8	G5C-Message	—	Support will be added in a future Libero release.

.....continued			
H2F Line	**Group**	**AXI Address and Data Bits to Clear an Interrupt**	
9	DDRC	—	Support will be added in a future Libero release.
10	G5C-DEVRST	—	Support will be added in a future Libero release.
11	RTC/USOC	—	Support will be added in a future Libero release.
12	TIMER	—	Support will be added in a future Libero release.
13	ENVM,QSPI	—	Support will be added in a future Libero release.
14	USB	—	Support will be added in a future Libero release.
15	MMC/SDIO	—	Support will be added in a future Libero release.

2.3 User Crypto Processor

The FIC-4 is a dedicated interface for the User Crypto Processor. FIC-4 provides two 32-bit AHB-Lite bus interfaces between the Crypto Processor and the fabric.

- One interface is mastered by the fabric and the Crypto Processor acts as slave.
- The other interface is mastered by the DMA controller of the User Crypto Processor and has a slave in the fabric.

Crypto simulation is similar to the PolarFire model, where only the AHB interface to fabric is exposed. Streaming/ Direct Transfer DXI interface support is not modeled for this release, so these ports are not exposed to the fabric.

The following table describes the simulation support for each crypto mode.

Table 2-4. Matching Cryto Modes with Simulation Support

Crypto Mode	Description	Simulation Support
MSS	The Crypto block is available to the MSS only.	No support.
Fabric	The Crypto block is available to the fabric only.	The AHB interface is exposed and simulation can be performed with Crypto.
Shared-MSS	Initially, the Crypto block is connected to the MSS and can be requested by the fabric.	The AHB interface is exposed and simulation can be performed with Crypto; however, there is no support when changing between MSS and fabric modes.
Shared-Fabric	Initially, the Crypto block is connected to the fabric and can be requested by the MSS.	The AHB interface is exposed and simulation can be performed with Crypto; however, there is no support when changing between MSS and fabric modes.

For more information about using crypto block and performing simulation, see the AC464 Application Note: PolarFire FPGA: Implementing Data Security Using User Cryptoprocessor.

2.4 DDR

To enable fast simulation, the DDR controller follows a BFM behavioral model: It is a single model for “DDR controller + PHY + DDR Memory”, with no activity seen on the DDR pins connected to external DDR memory. DDR memory is modeled as a sparse array, and performs address decoding and prints row, column, bank, and rank address information in a simulation log.

The MSS standalone configurator configures the MSS DDR and generates configuration parameters. The simulation model considers only the parameters in the following table.

Table 2-5. MSS DDR Configuration Parameter Support

MSS Configurator	Considered Parameters
DDR_DDRC_CFG_CHIPADDR_MAP_CFG_CHIPADDR_MAP	All possible values
DDR_DDRC_CFG_BANKADDR_MAP_0_CFG_BANKADDR_MAP_0	All possible values
DDR_DDRC_CFG_ROWADDR_MAP_0_CFG_ROWADDR_MAP_0	All possible values
DDR_DDRC_CFG_ROWADDR_MAP_1_CFG_ROWADDR_MAP_1	All possible values
DDR_DDRC_CFG_ROWADDR_MAP_2_CFG_ROWADDR_MAP_2	All possible values
DDR_DDRC_CFG_ROWADDR_MAP_3_CFG_ROWADDR_MAP_3	All possible values
DDR_DDRC_CFG_COLADDR_MAP_0_CFG_COLADDR_MAP_0	All possible values
DDR_DDRC_CFG_COLADDR_MAP_1_CFG_COLADDR_MAP_1	All possible values
DDR_DDRC_CFG_COLADDR_MAP_2_CFG_COLADDR_MAP_2	All possible values
DDR_DDRC_CFG_MEM_COLBITS_CFG_MEM_COLBITS	All possible values
DDR_DDRC_CFG_MEM_ROWBITS_CFG_MEM_ROWBITS	All possible values
DDR_DDRC_CFG_MEM_BANKBITS_CFG_MEM_BANKBITS	All possible values
DDR_DDRC_CFG_NUM_RANKS_CFG_NUM_RANKS	All possible values
DDR_DDRC_CFG_MANUAL_ADDRESS_MAP_CFG_MANUAL_ADDRESS_MAP	All possible values
DDR_DDRC_CFG_MEMORY_TYPE_CFG_MEMORY_TYPE	All possible values
DDR_DDRC_CFG_BG_INTERLEAVE_CFG_BG_INTERLEAVE	All possible values
DDR_DDRC_CFG_BL_MODE_CFG_BL_MODE	8
DDR_DDRC_CFG_DQ_WIDTH_CFG_DQ_WIDTH	16, 32

The simulation model has the following limitations.

Table 2-6. MSS DDR Model Limitations

Sr. No.	Limitations
1	AXI transactions with 64-bit data only are supported. There is no support for word (32-bit)-, halfword (16-bit)-, and byte (8-bit)-based AXI transactions.
2	Supports Burst Length of Fixed BL8 only.
3	DDR parameters related to latency and timing are not considered.

In the context of page hits and page misses in real time applications, this simulation model always considers page hits to avoid latencies caused by page misses.

The model expects the user to use the `vsim` command to set the parameters in the following table while launching the simulation.

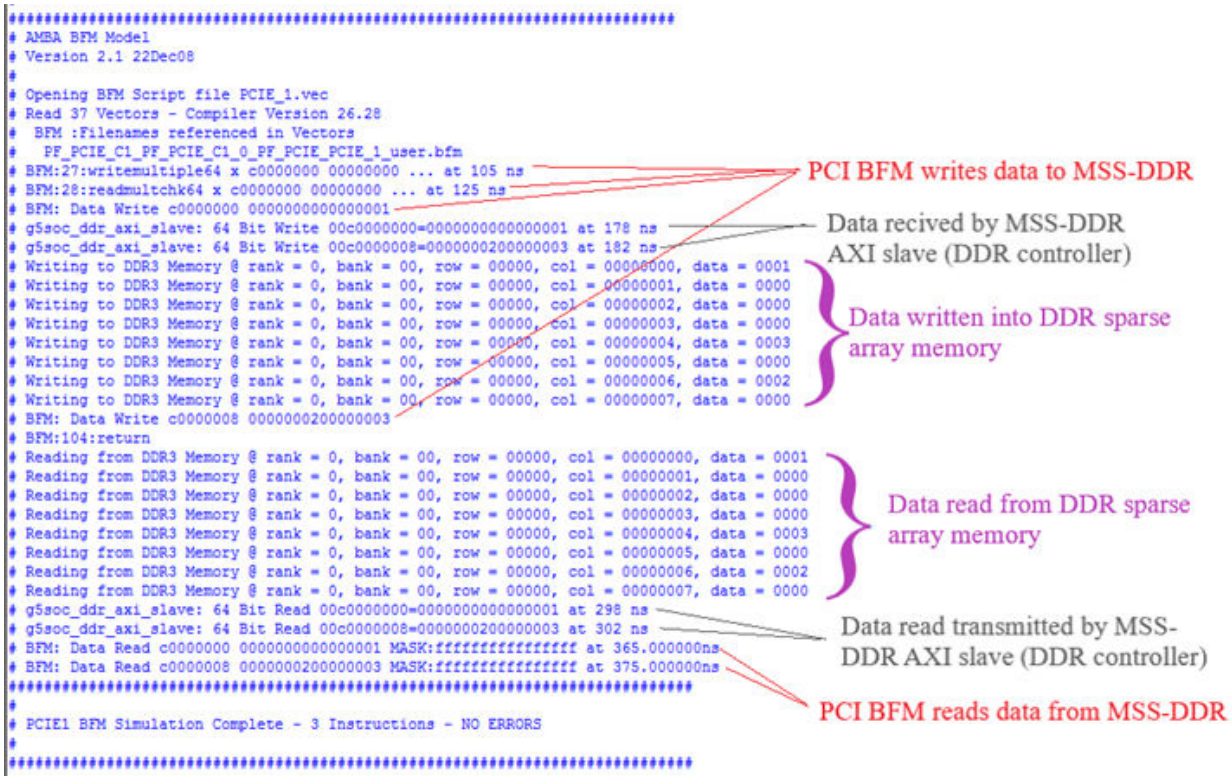
Table 2-7. MSS DDR Address Space Parameters

Parameter	Description	Value
DDR_ADDRESS_REGION	Selects 32-bit Vs 38-bit address region for DDR. You can change the value of this parameter using the `vsim` commands. For example, to set the 32-bit address region: `vsim -L polarfire -L presynth -t 1ps -gDDR_ADDRESS_REGION=0 presynth.tb`.	1: 38-bit address region, where the base address is 0x14_0000_000. (*default*) 0: 32-bit address region, where the base address is 0xC000_0000.

You can access MSS-DDR from any FIC interface and can choose to share (compromise) bandwidth to the QoS master.

The following figure shows an example of a simulation log where a fabric master such as PCIe-BFM is accessing MSS-DDR.

Figure 2-5. Simulation Log of PCIe-BFM Accessing MSS-DDR



2.5 QoS Parameter

The QoS feature allows bandwidth to be shared for the fabric masters when accessing DDR. To share bandwidth, an AXI master (referred as QoS master) is connected internally at the AXI switch that performs the DDR access. This

AXI master, which is hidden from you, performs DDR access controlled through QoS parameters. The QoS is enabled only when DDR is enabled.

You can change the QoS parameter values using `vsim` commands while launching the simulation, see the following table.

Table 2-8. MSS QoS Parameters

Parameter	Description	Default Value

QOS_AXI_CLKS	Number of AXI clocks at which QoS master performs read/write AXI transactions with DDR. To change the value of this parameter, use `vsim` command as shown below:
	`vsim -L polarfire -L presynth -t 1ps -g`
	`QOS_AXI_CLKS = 10000 presynth.tb`
		5000

QOS_START_ADDRESS	Base address for QoS operation. Change this address if the same address region is being used by another application through FIC. To avoid contention between QoS and FIC accessing the same DDR region, shift the QoS access region to an unused address region. To change the value of this parameter, use `vsim` command as shown below: For 38-bit: `vsim -L polarfire -L presynth -t 1ps -gQOS_START_ADDRESS=38'h1600000000 presynth.tb` For 32-bit: (also need to change DDR_ADDRESS_REGION for 32-bit) `vsim -L polarfire -L presynth -t 1ps -gQOS_START_ADDRESS=32'hcd000000 -gDDR_ADDRESS_REGION=0 presynth.tb`	This is as per the DDR_ADDRESS_REGION parameter. 1: 38-bit address region, where 0x14_0000_0000 is base address. (*default*) 0: 32-bit address region, where 0xC000_0000 is base address.
NO_OF_QOS_TRANSACTIONS	Number of burst read/write transactions performed by QoS at regular or cyclic interval of QOS_AXI_CLKS. If set to zero, QoS does not perform any AXI transactions to DDR and the entire bandwidth is allocated to FICs. **Note:** Make sure the QOS_AXI_CLKS value is much greater than the finish time of all QoS AXI transactions. The smallest burst size typically uses: • 10 AXI clocks for read or write burst transaction with DQ=16. • 20 AXI clocks for read or write burst transaction with DQ=16. To change the value of this parameter, use `vsim` command as shown below: `vsim -L polarfire -L presynth -t 1ps -gNO_OF_QOS_TRANSACTIONS=512 presynth.tb`	128 when DDR is used.

The following figure shows an example simulation log when QoS master accesses DDR.

Figure 2-6. Simulation Log when QoS Master Accesses DDR

```
# QoS Write Transactions          1 Completed
# g5soc_ddr_axi_slave: 64 Bit Write 00cd000000=aabbccdd12345678 at 16795 ns
# g5soc_ddr_axi_slave: 64 Bit Write 00cd000008=aabbccdd12345678 at 16798 ns
# Writing to DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000000, data = 5678
# Writing to DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000001, data = 1234
# Writing to DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000002, data = ccdd
# Writing to DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000003, data = aabb
# Writing to DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000004, data = 5678
# Writing to DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000005, data = 1234
# Writing to DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000006, data = ccdd
# Writing to DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000007, data = aabb
# QoS Read Transactions          1 Completed
# Reading from DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000000, data = 5678
# Reading from DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000001, data = 1234
# Reading from DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000002, data = ccdd
# Reading from DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000003, data = aabb
# Reading from DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000004, data = 5678
# Reading from DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000005, data = 1234
# Reading from DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000006, data = ccdd
# Reading from DDR3 Memory @ rank = 0, bank = 01, row = 0a000, col = 00000007, data = aabb
# g5soc_ddr_axi_slave: 64 Bit Read 00cd000000=aabbccdd12345678 at 16828 ns
# g5soc_ddr_axi_slave: 64 Bit Read 00cd000008=aabbccdd12345678 at 16832 ns
```

3. Revision History

Revision	Date	Description
A	11/2020	Document converted to Microchip template. Initial Revision.

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