

---

## MSS Configurator User Guide

---

### Introduction

---

The PolarFire SoC MSS Configurator provides a graphical user interface that allows embedded software engineers to quickly define the MSS startup state. It exports an XML file that is consumed by the embedded software flow that converts the XML into initialization constructs. Additionally, the tool outputs a CXZ file for inclusion into your Libero design flow. The CXZ file contains information about metadata and port needed by the FPGA designer to complete the connectivity between the MSS and the FPGA fabric.

MSS configurator is available as a standalone application and as part of the Libero® SoC design tool suite. The information in this user guide applies to both.

### References

---

- Configuration of the MSS clocks.
  - For detailed information about the MSS clocking features, see [UG0913: PolarFire SoC FPGA Clocking Resources User Guide](#).
- Configuration of the MSS interfaces to the FPGA fabric.
  - For detailed information about the MSS Fabric Interface Controller (FIC) features, see [UG0880: PolarFire SoC FPGA Microprocessor Subsystem \(MSS\) User Guide](#).
- Selection and assignment of the MSS peripherals to the MSS dedicated I/Os and/or the FPGA fabric dedicated peripheral interfaces.
  - For detailed information about the MSS Peripherals features, see [UG0886: PolarFire SoC FPGA Peripherals User Guide](#).
- Configuration of the MSS Bank voltages and I/O standards and attributes.
  - For detailed information about the MSS Banks and I/Os features, see [UG0916: PolarFire SoC FPGA I/O User Guide](#).
- Configuration of the MSS DDR memories (DDR3/L, DDR4, LPDDR3, and LPDDR4).
  - For detailed information about the MSS DDR4, DDR3, LPDDR3, and LPDDR4 features, see [UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide](#).
- Configuration of the MSS debug features.
  - For detailed information about the MSS debug features, see [UG0888: PolarFire SoC FPGA Trace and Debug User Guide](#).

## Table of Contents

Introduction.....	1
References.....	1
1. Installing the PolarFire SoC MSS Configurator.....	3
1.1. Input and Output Files.....	3
2. Running the PolarFire SoC MSS Configurator.....	4
2.1. Batch Mode.....	4
2.2. Interactive Mode.....	4
2.3. Using the PolarFire SoC MSS Configurator GUI.....	4
3. Creating a Project and Configuring MSS.....	21
4. Generating, Importing, and Exporting the MSS Component.....	23
4.1. Generating the MSS Component and Report.....	23
4.2. Importing the MSS CXZ File to Libero SoC.....	25
4.3. Importing the MSS XML File to SoftConsole.....	25
4.4. Exporting the FPGA Design Hardware Platform Information.....	25
5. Simulating an FPGA Design Interacting with MSS.....	26
6. Programming the Application Bitstream.....	27
7. Sample Project.....	28
8. Revision History.....	29
9. Microchip FPGA Technical Support.....	30
9.1. Customer Service.....	30
9.2. Customer Technical Support.....	30
9.3. Website.....	30
9.4. Outside the U.S.....	30
The Microchip Website.....	31
Product Change Notification Service.....	31
Customer Support.....	31
Microchip Devices Code Protection Feature.....	31
Legal Notice.....	32
Trademarks.....	32
Quality Management System.....	33
Worldwide Sales and Service.....	34

## 1. Installing the PolarFire SoC MSS Configurator

The PolarFire SoC MSS Configurator bundled with Libero is available at the following location in the Libero installation section:

- Windows: <\$Installation\_Directory>\Microsemi\Libero\_SoC\_vX.X\Designer\bin64\pfsoc\_mss.exe
- Linux: <\$Installation\_Directory>\Microsemi\Libero\_SoC\_vX.X\bin64\pfsoc\_mss

The PolarFire SoC MSS Configurator can also be installed as a standalone application.

For information about how to install Libero, see [www.microsemi.com/product-directory/design-resources/1750-libero-soc#documents](http://www.microsemi.com/product-directory/design-resources/1750-libero-soc#documents).

### 1.1 Input and Output Files

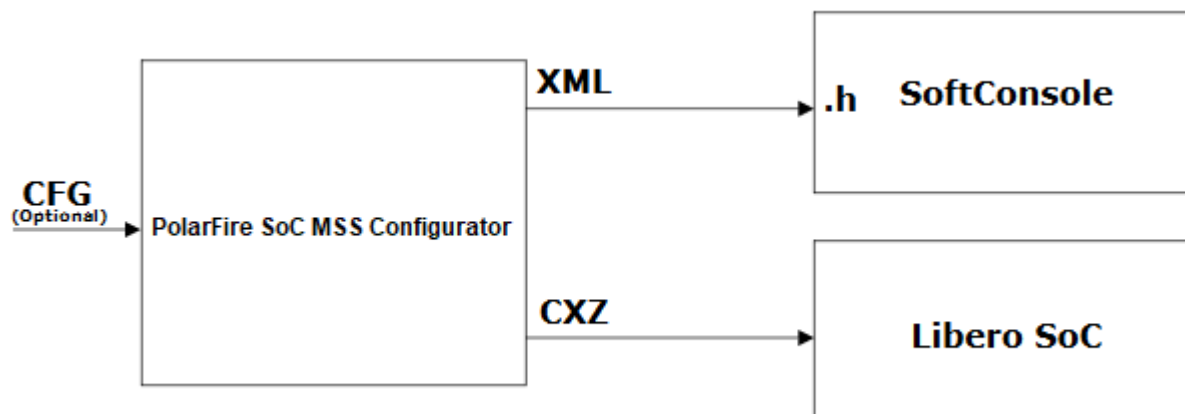
The following sections describe the PolarFire SoC MSS Configurator input and output files.

#### 1.1.1 Output Files

The PolarFire SoC MSS Configurator generates the output file formats shown in the following figure.

- **XML Configuration File** — Contains the MSS memory map, clock, DDR memory controller, and peripheral configuration. The XML file is used to generate hardware files required for building the firmware project.
- **CXZ File** — Encapsulates the hardware design of the MSS block and can be imported into Libero SoC project.

**Figure 1-1. PolarFire SoC MSS Configurator Block Diagram**



#### 1.1.2 Input files

The PolarFire SoC MSS Configurator can be invoked without any input files. A configuration file (.cfg) from an earlier MSS configurator session, can be optionally provided to the PolarFire SoC MSS Configurator.

**Note:** A .cfg file and a report file can also be generated from the PolarFire SoC MSS Configurator.

## 2. Running the PolarFire SoC MSS Configurator

You can run the PolarFire SoC MSS Configurator in Batch mode or Interactive mode.

### 2.1 Batch Mode

The PolarFire SoC MSS Configurator application can be executed in the Batch mode for scripted execution as follows:

- Windows:

```
<Liberio SoC or Standalone MSS Configurator installation area>\bin64\pfsoc_mss.exe -  
CONFIGURATION_FILE:<absolute path for configuration file name (.cfg)> -  
OUTPUT_DIR:<absolute path for output directory>
```

- Linux:

```
<Liberio SoC or Standalone MSS Configurator installation area>/bin64/pfsoc_mss -  
CONFIGURATION_FILE:<absolute path for configuration file name (.cfg)> -  
OUTPUT_DIR:<absolute path for output directory>
```

**Note:** Relative path is not supported for PolarFire SoC MSS Configurator. Specify the complete path to execute PolarFire SoC MSS Configurator in Batch mode.

### 2.2 Interactive Mode

In the Interactive (GUI) mode, the PolarFire SoC MSS Configurator provides the following high-level options.

**Table 2-1. Configurator-Project Menu Options**

Option	Description
<b>New</b>	Starts configuring a new MSS subsystem.
<b>Open</b>	Opens a configuration (.cfg) file.
<b>Save/Save As</b>	Saves the current configuration of the MSS subsystem to a configuration (.cfg) file.
<b>Generate</b>	Generates MSS configuration (.xml) and component (.cxz) files after configuring the MSS subsystem.
<b>Close</b>	Closes the current configuration (.cfg) file.

### 2.3 Using the PolarFire SoC MSS Configurator GUI

The PolarFire SoC MSS Configurator GUI has the following tabs.

- Peripherals
- DDR Memory
- L2 Cache
- Crypto
- Fabric Interface Controllers
- Clocks
- MSS REFCLK I/O
- Bank 4 I/Os
- Bank 2 I/Os
- SGMII I/Os
- Misc

### 2.3.1 Clocks

Use the **Clocks** tab to configure the MSS PLL clock frequency and clock sources. For more information, see the [UG0913: PolarFire SoC FPGA Clocking Resources User Guide](#).

There are three PLLs inside MSS, which generates the necessary clocks:

- MSS PLL
- DDR PLL
- SGMII PLL

Each PLL generates four output clocks from one input reference clock.

The actual output that can be achieved by the PLL Solver is shown in GUI next to the "Actual:" label. The color of the label is blue, if the requirement is met; it is red, if the requirement (from you) cannot be met.

In case of MSS PLL, you must specify the four output clock requirements.

- Output 0 (CPU Clock)
  - Output 1 (Crypto Clock)
  - Output 2 (eMMC Clock)
  - Output 3 (CAN Clock)
1. When eMMC is enabled, the output clock requirement is fixed at 200 MHz.
  2. When the CAN peripheral is enabled, the output clock requirement must be multiple of 8 (max 80 MHz).
  3. Crypto can be at most 200 MHz.
  4. CPU has the maximum frequency of 625 MHz.

The preceding conditions pose restrictions on PLL solver. Solver attempts to solve the fixed requirements first and then the ones without restriction.

In case of DDR PLL, the required output clock frequency is entered by you in DDR tab in Line Edit 'Memory clock frequency'. All four output clocks are generated by PLL that is the same frequency.

In case of SGMII PLL, output frequency requirement is fixed at 625 MHz for all four outputs. You do not have to enter this. Additionally, the output clocks are phase shifted by 90 deg (output 0 clock has 0 deg phase shift, output 1 clock has 90 deg, and so on).

The following table lists the option provided in MSS **Clocks** selection tab.

**Table 2-2. MSS Clock Selection Tab**

Option	Description
MSS Reference Clock Input Source	MSS can be clocked from dedicated I/O from Bank 5 (REFCLK) or North West PLL output.
MSS PLL clock frequency	You can set the frequency value of up to 625 MHz. All MSS clock frequencies are derived from this setting.
MSS CPU cores clock frequency Divider	The MSS CPU clock frequency is based on the MSS PLL clock frequency and is set using the divider values /1, /2, /4, or /8. The frequency must be greater or equal to the MSS AXI clock, and can have a maximum value of 625 MHz.
MSS AXI clock frequency Divider	The MSS AXI clock frequency is based on the MSS CPU clock frequency and is set using the divider values of /1, /2, /4, or /8. The frequency must be greater or equal to MSS AHB/APB clock, and can have a maximum value of 312.5 MHz.
MSS AHB/APB clock frequency Divider	The MSS AHB/APB clock frequency is based on the MSS CPU clock frequency and is set using the divider values /2, /4, or /8. The maximum supported frequency is 156.25 MHz.

# PolarFire® SoC

## Running the PolarFire SoC MSS Configurator

.....continued	
Option	Description
DDR Reference Clock Input Source	You can select the NW PLL ports or I/Os from Bank 5.
RTC/MAC SGMII Reference Clock Input Source	You can select the NW PLL ports or I/Os from Bank 5.
Dedicated I/O from Bank5 (REFCLK) frequency	This is a dedicated I/O from Bank 5 to the MSS PLL. It can be either be 100 MHz or 125 MHz.
NW PLL (REF_0_PLL_NW) frequency (MHz)/ NW PLL (REF_1_PLL_NW) frequency (MHz)	This option is available when any peripheral is clocked from North West PLL output. It can be any value between 50 MHz to 125 MHz.
Crypto clock frequency from MSS (MHz)	You can set the reference clock frequency for Crypto between 1 MHz to 200 MHz.
MSS CAN clock frequency (MHz)	The MSS CPU clock frequency is based on the MSS PLL clock frequency. The supported frequencies in MHz are 8, 16, 24, 32, 40, 48, 56, 64, 72, and 80.

**Note:** The **DDR Reference Clock Input Source** option appears only when the DDR Memory type is selected from the **DDR Memory** tab.

The following figure shows the **Clocks** tab in the PolarFire SoC MSS Configurator. In this example, the following configuration is used:

- Dedicated I/Os from Bank 5 (REFCLK) are selected as the reference clock input source for the MSS. The MSS PLL clock frequency is set to 600 MHz.
- Dedicated I/Os from Bank 5 (REFCLK) are used to source the reference clock input frequency for the DDR subsystem.
- The DDR clock source and MSS clock source are set to 125 MHz.

**Figure 2-1. Clocks Tab**

The screenshot displays the 'Clocks' tab in the PolarFire SoC MSS Configurator. The interface is organized into sections with expandable/collapsible headers. The 'MSS' section is expanded, showing the following configurations:

- MSS Reference Clock Input Source:** Set to 'Dedicated I/O from Bank5 (REFCLK)' via a dropdown menu.
- MSS PLL clock frequency (MHz):** Set to '600.000' in a text input field, with a blue label indicating 'Actual: 600.000 MHz'.
- MSS CPU cores clock frequency Divider:** Set to '/1' via a dropdown menu. To the right, 'MSS CPU cores clock frequency (MHz)' is set to '600.000'.
- MSS AXI clock frequency Divider:** Set to '/2' via a dropdown menu. To the right, 'MSS AXI clock frequency (MHz)' is set to '300.000'.
- MSS AHB/APB clock frequency Divider:** Set to '/4' via a dropdown menu. To the right, 'MSS AHB/APB clock frequency (MHz)' is set to '150.000'.

The 'Real Time Clock (RTC) / Gigabit Ethernet MAC' section is also expanded, showing:

- RTC / MAC SGMII Reference Clock Input Source:** Set to 'Dedicated I/O from Bank5 (REFCLK)' via a dropdown menu.

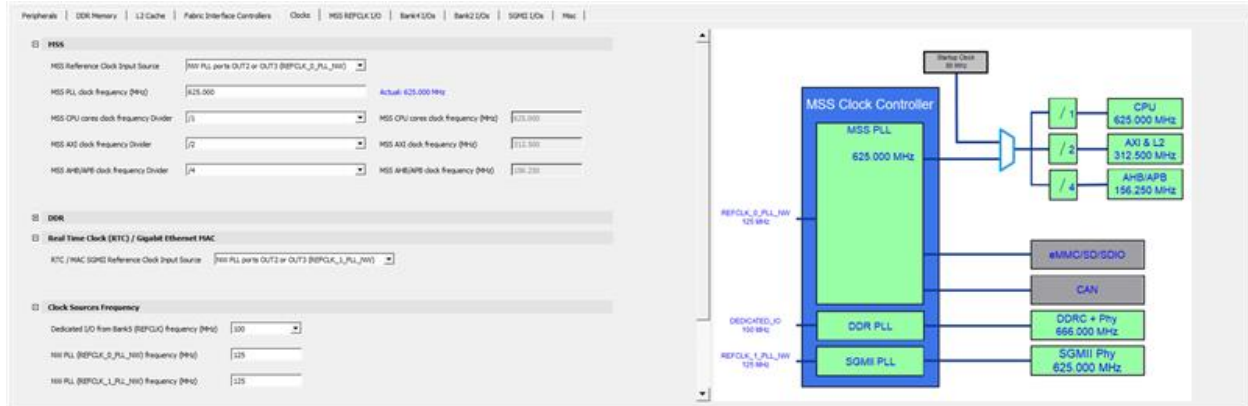
The 'Clock Sources Frequency' section is expanded, showing:

- Dedicated I/O from Bank5 (REFCLK) frequency (MHz):** Set to '100' in a text input field.

The following figure shows the **Clocks** tab with PLL in the PolarFire SoC MSS Configurator. In this example, the following configuration is used:

- NW PLL ports OUT2 or OUT3 (REFCLK\_0\_PLL\_NW) are selected as the reference clock input source for the MSS. The MSS PLL clock frequency is set to 600.000 MHz.
- NW PLL ports OUT2 or OUT3 (REFCLK\_1\_PLL\_NW) are used to source the reference clock input frequency for the DDR subsystem and Real Time Clock/Gigabit Ethernet MAC.
- The DDR Clock Source and MSS Clock Source are set to 100 MHz.

**Figure 2-2. Clocks Tab with PLL**



For more information about configuring the MSS DDR subsystem, see [DDR Memory](#).

### 2.3.2 Fabric Interface Controllers

Using the **Fabric Interface Controllers** tab, any combination of **FIC\_0**, **FIC\_1**, **FIC\_2**, **FIC\_3** can be enabled and configured to support master and slave interfaces. For more information, see the [UG0880: PolarFire SoC FPGA Microprocessor Subsystem \(MSS\) User Guide](#).

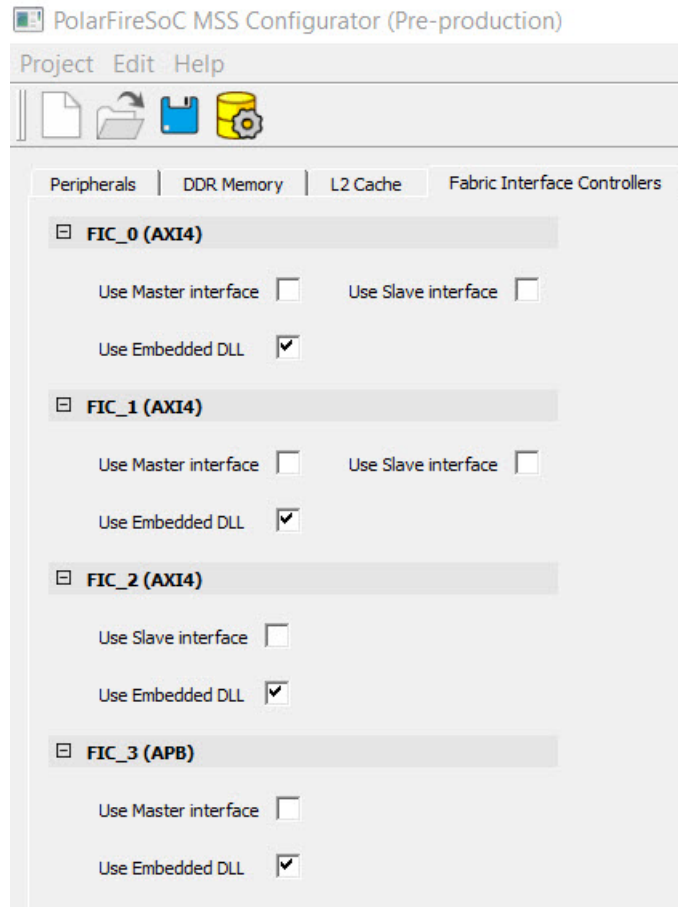
**FIC\_0**, **FIC\_1**, and **FIC\_2** support AXI4 interfaces, while **FIC\_3** supports APB.

For **FIC\_0** and **FIC\_1** interfaces, both master and slave interfaces can be enabled at the same time. **FIC\_2** interface can support only slave interface and **FIC\_3** interface can only support master interface. (MSS is master).

**FIC\_0** and **FIC\_1** have both master and slave interfaces to and from the FPGA fabric, while **FIC\_2** and **FIC\_3** support slave or master interfaces, respectively.

The following figure shows all FIC options available and enabled. By default, the DLLs of all the FICs are enabled.

**Figure 2-3. Fabric Interface Controllers Tab**



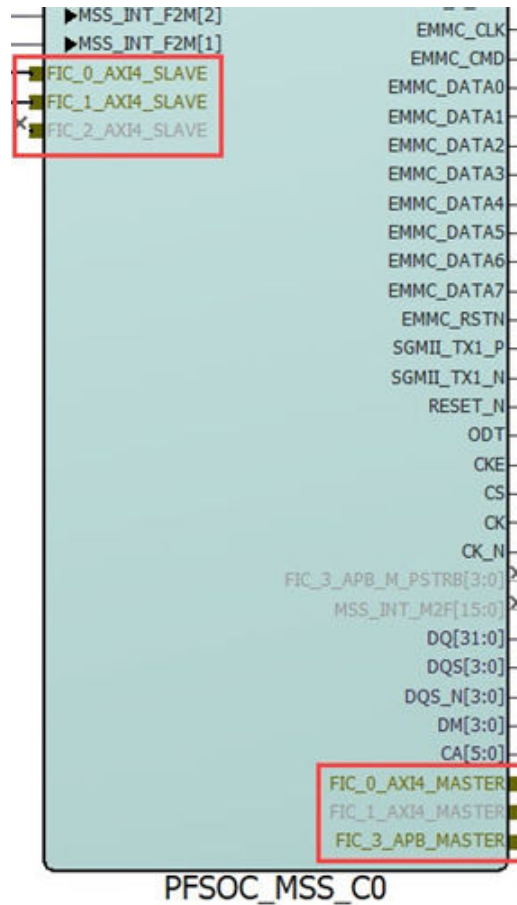
**Note:** The FIC interface can operate up to 250 MHz. The FIC clock is independent of the MSS clock. If the frequency of the FIC block is greater than or equal to 125 MHz, the embedded DLL must be enabled for removing clock insertion delay. If the frequency of the FIC block is less than 125 MHz, the embedded DLL must be bypassed.

When a master interface is enabled for a FIC, that master interface must be connected to a slave in the fabric. When a slave interface is enabled for a FIC, that slave interface must be connected to a master in the fabric.

There is clock domain crossing logic in the FIC block to address the asynchronous MSS and Fabric clocks and therefore user logic is not required to implement clock domain crossing synchronization for this interface.



Figure 2-4. FIC Interfaces Enabled



**Note:** The MSS SmartDesign component is visible only after importing the MSS CXZ file.

### 2.3.3 Peripherals

Select the following I/Os using the **Peripherals** tab:

- GPIOs from Bank 2 and Bank 4, which are dedicated to the MSS.
- Fabric I/Os, if the dedicated I/Os from Bank 2 and Bank 4 are not available.
- GPIOs from Bank 5 are dedicated to SGMII but can be routed to GMII or MII fabric I/Os. GPIO from Bank 5 are displayed only when Gigabit Ethernet MAC\_0 or Gigabit Ethernet MAC\_1 is selected.

**Note:** I/Os from the DDR bank are dedicated to the DDR Controller in the MSS.

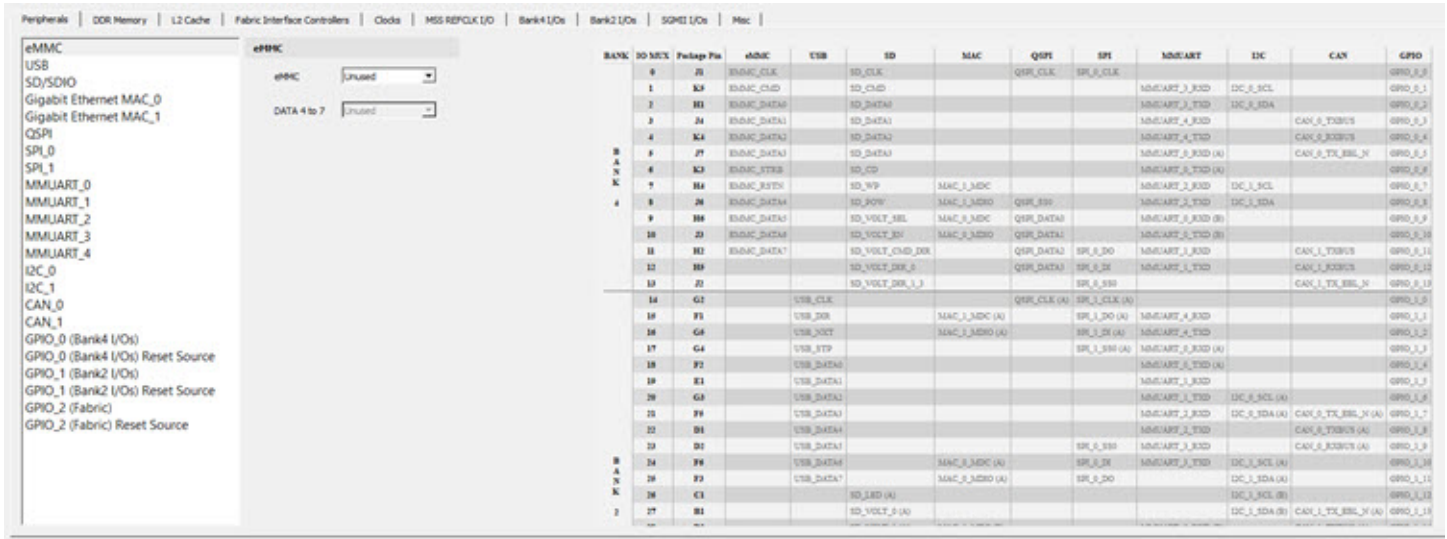
For more information, see [UG0880: PolarFire SoC FPGA Microprocessor Subsystem \(MSS\) User Guide](#)

The following figure shows the **Peripherals** tab on the PolarFire SoC MSS Configurator.

Figure 2-5. Peripherals Tab

# PolarFire® SoC

## Running the PolarFire SoC MSS Configurator



By default, all peripherals are marked as unused. To include peripherals that are required in the design, select the peripheral from the left-hand side of the window and use the corresponding drop-down to assign MSS I/Os or fabric I/Os.

The I/Os associated with the following peripherals are dedicated and cannot be assigned to fabric I/Os:

- USB peripherals are dedicated in Bank 2.
- eMMC peripherals are dedicated in Bank 4.
- SD/SDIO peripherals are dedicated in Bank 4.

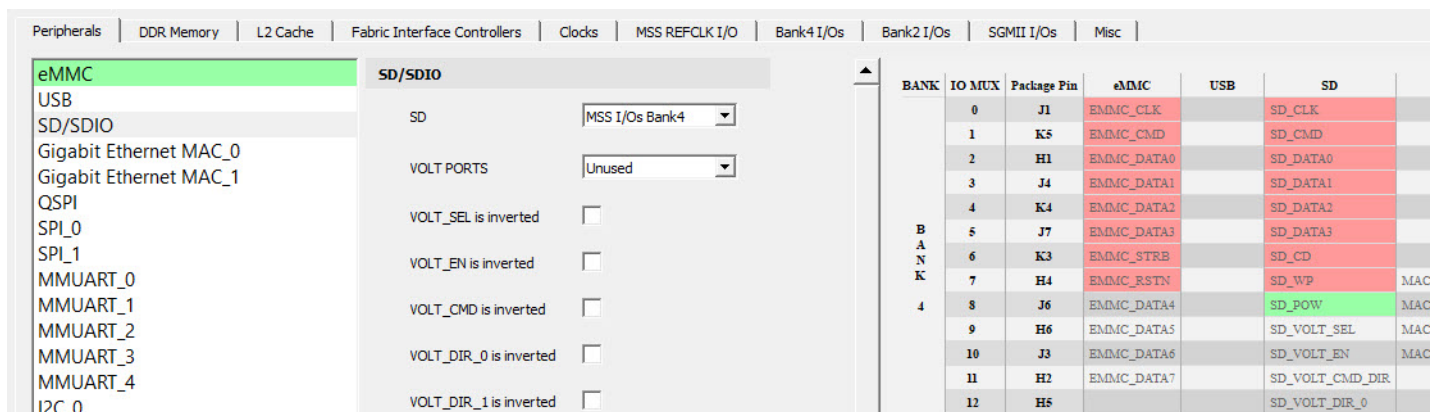
**Note:** If the I/Os for a peripheral are selected in a bank, you cannot select the same I/Os for another peripheral from the same bank. If you try, the tool generates the following warning message in the log window:

**Figure 2-6. Error Message**



For example, eMMC and SD cannot be used simultaneously as shown in the following figure.

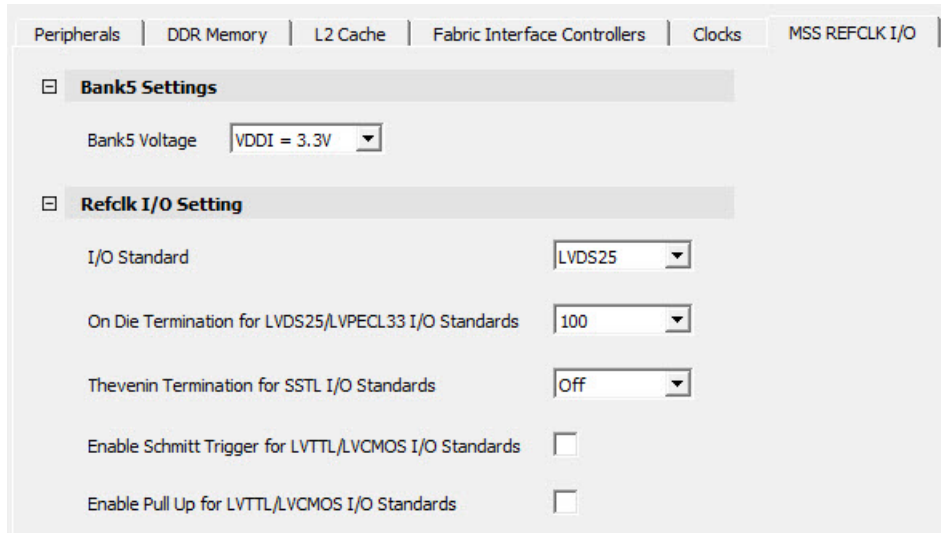
**Figure 2-7. Overlapping I/O Warning**



### 2.3.4 MSS REFCLK I/O

Using the **MSS REFCLK I/O** tab, you can select electrical characteristics of the Bank 5 I/Os, as shown in the following figure. The tool generates a warning in the log window for unsupported selections.

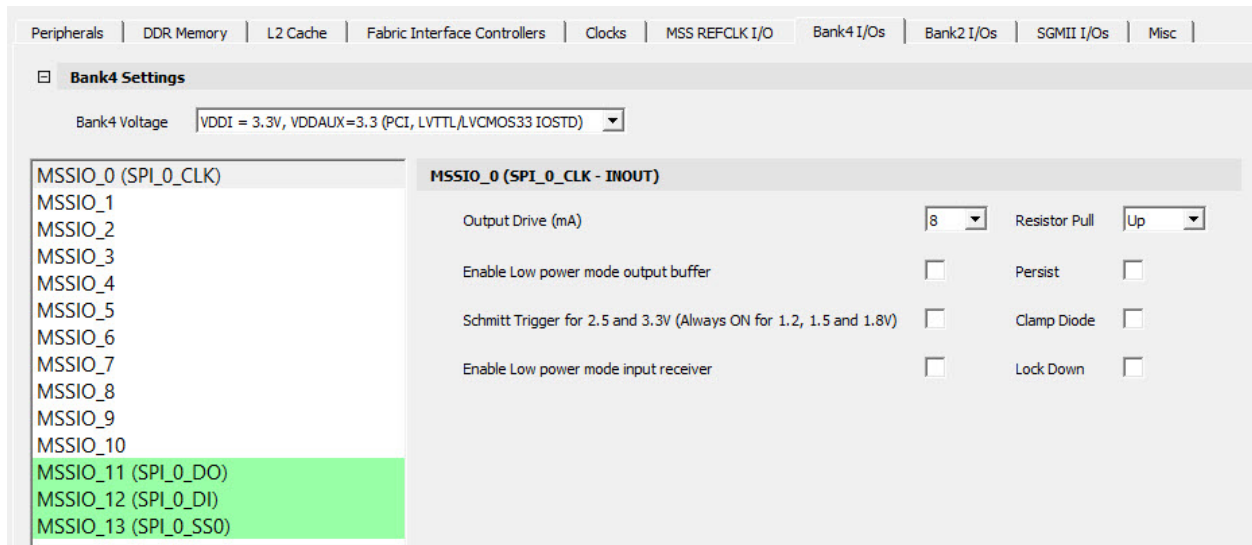
**Figure 2-8. MSS REFCLK I/O Tab**



### 2.3.5 Bank4 and Bank2 I/Os

The MSS I/Os are available across Bank 4 and Bank 2. The **Bank4 I/Os** and **Bank2 I/Os** tabs allow you to select the electrical characteristics of the MSS I/Os. Each MSS I/O along with the settings must be enabled one by one.

**Figure 2-9. Bank 4 I/Os Tab**



### 2.3.6 DDR Memory

Select the required DDR type from the **DDR Memory Type** pulldown. The DDR configuration options are available on the **DDR Topology**, **DDR Controller**, **DDR Memory Initialization**, and **DDR Memory Timing** tabs (see the following figure).

For more information, see the [UG0906: PolarFire SoC FPGA DDR Memory Controller User Guide](#).

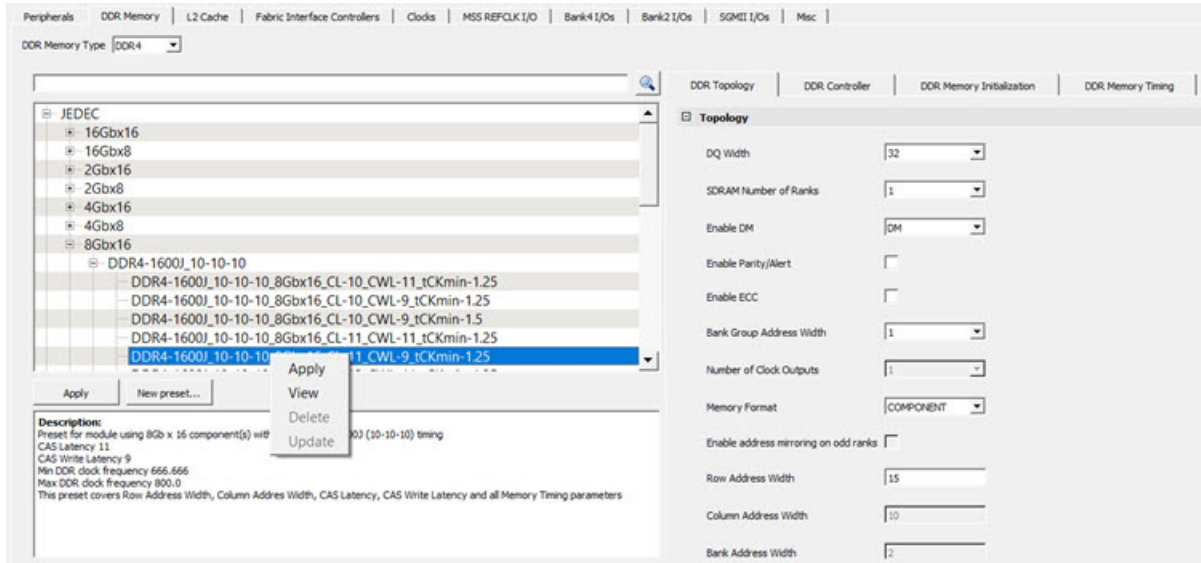
# PolarFire® SoC

## Running the PolarFire SoC MSS Configurator

The **DDR Topology** tab, in the following figure, controls the physical aspects of the memory, such as data and address widths, enabling of ECC and DM, and setting the clock frequency.

- For DDR3 and DDR4, the COMPONENT, UDIMM, RDIMM, LRDIMM, and SODIMM memory formats are supported.
- For LPDDR3/4, only the COMPONENT memory format is supported.

**Figure 2-10. DDR Memory Tab**



**Note:** Configure the DDR parameters according to the datasheet from the DDR vendor.

The **DDR Controller** tab controls the DQS Drive, ODT, Precharge look-ahead, and Address Ordering.

**Figure 2-11. DDR Controller Tab**

The screenshot shows the 'DDR Memory Initialization' tab of the MSS Configurator. It contains several expandable sections:

- Drive**: Contains four dropdown menus: 'DQ Drive' (48), 'DQS Drive' (48), 'ADD/CMD Drive' (34), and 'Clock Drive' (48).
- ODT**: Contains two dropdown menus: 'DQ ODT' (120) and 'DQS ODT' (120).
- Efficiency**: Contains a checkbox for 'Enable Activate/Precharge look-ahead' (unchecked) and a dropdown for 'Address Ordering' (Chip-Row-BG-Bank-Col).
- ODT Activation Settings on Write**: Contains four checkboxes: 'Enable Rank0 - ODT0' (unchecked), 'Enable Rank0 - ODT1' (unchecked), 'Enable Rank1 - ODT0' (unchecked), and 'Enable Rank1 - ODT1' (unchecked).
- ODT Activation Settings on Read**: This section is partially visible at the bottom.

The **DDR Memory Initialization** tab controls the DDR mode register configuration according to the JEDEC specification. In the PolarFire SoC FPGA DDR architecture, these parameters are passed to the start-up code running on the E51 monitor core, which then performs the DDR initialization sequence and configures the mode registers.

The following figure shows the memory initialization configuration.

**Figure 2-12. DDR Memory Initialization**

DDR Topology	DDR Controller	DDR Memory Initialization	DDR Memory Timing
<b>Mode Register 0</b>			
Burst Length		Fixed BL8	
Read Burst Type		Sequential	
Memory CAS Latency		12	
<b>Mode Register 1</b>			
ODT Rtt Nominal Value		RZQ/4	
Memory Additive CAS Latency		CL-1	
Output Drive Strength		RZQ/7	
<b>Mode Register 2</b>			
Low Power Auto Self Refresh		Automatic	
Memory Write CAS Latency		11	
Dynamic ODT (Rtt_WR)		RZQ/1	
<b>Mode Register 3</b>			

The **DDR Memory Timing** tab controls the timing parameters, which are translated to the appropriate configuration values for the DDR subsystem IP.

**Figure 2-13. DDR Memory Timing Tab**

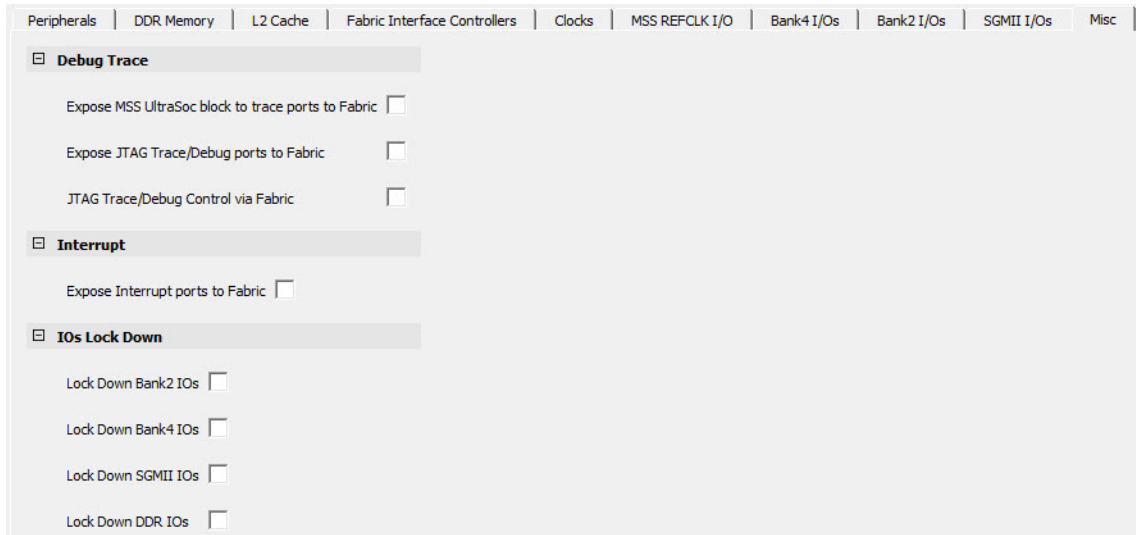
DDR Topology	DDR Controller	DDR Memory Initialization	DDR Memory Timing
<b>Timing parameters dependent on speed bin</b>			
tRAS (ns)		35	
tRCD (ns)		15	
tRP (ns)		15	
tRC (ns)		50	
tWR (ns)		15	
tCCD_L (cycles)		5	
tCCD_S (cycles)		4	
<b>Timing parameters dependent on operating condition</b>			
tREFI (us)		7.8	
<b>Timing parameters dependent on speed bin and page size</b>			
tRFC (ns)		160	
tF&W (ns)		75	

### 2.3.7 Misc

Use the **Misc** tab to enable the following options:

- Trace functionality
- JTAG (Debug) functionality
- Interrupts to/from MSS
- Lock down of Bank 2 and Bank 4 I/Os
- Lock down of DDR and SGMII I/Os

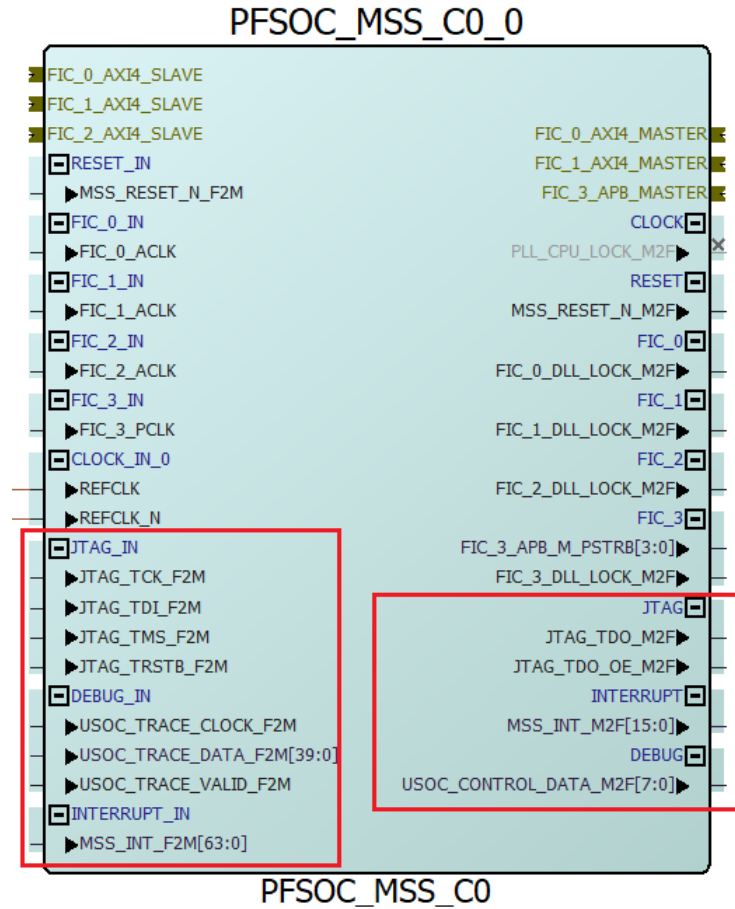
**Figure 2-14. Misc Tab**



For more information, see [UG0888: PolarFire SoC FPGA Trace and Debug User Guide](#).

By default, these options are marked as unused. When any of the options are enabled, the corresponding ports are exposed on the MSS block (see the following figure).

Figure 2-15. PFSOC\_MSS\_C0\_0 Jtag Trace Enabled



### 2.3.8 L2 Cache

Level2 memory subsystem has three operating modes – Cache, Loosely-Integrated-Memory (LIM), and Scratchpad. These modes can be configured in MSS configurator using the options in the L2 Cache tab based on user needs. The goal is to make the configuration options easier to use and understand for the users.

Users can allocate L2 memory for the processor or peripheral using the L2 Cache tab as shown in the following table:

Figure 2-16. L2 Cache



# PolarFire® SoC

## Running the PolarFire SoC MSS Configurator

Peripherals

DDR Memory

L2 Cache

Crypto

Fabric Interface Controllers

Clocks

MSS REFCLK I/O

Bank4 I/Os

Bank2 I/Os

SGMII I/Os

Misc

L2-LIM WAYs (128 KB for each WAY)

8

Scratch Pad WAYs (128 KB for each WAY)

2

Masters	L2 Cache Size	WAY0	WAY1	WAY2	WAY3	WAY4	WAY5	WAY6	WAY7	WAY8	WAY9	WAY10	WAY11	WAY12	WAY13	WAY14	WAY15
DMA	768 KB	1	1	1	1	1	1	Scratch Pad 256 KB									
FPGA Port0	768 KB	1	1	1	1	1	1										
FPGA Port1	768 KB	1	1	1	1	1	1										
FPGA Port2	768 KB	1	1	1	1	1	1										
FPGA Port3	768 KB	1	1	1	1	1	1										
E51 D5	768 KB	1	1	1	1	1	1										
E51 I5	768 KB	1	1	1	1	1	1										
US4_1 D5	768 KB	1	1	1	1	1	1										
US4_1 I5	768 KB	1	1	1	1	1	1										
US4_2 D5	768 KB	1	1	1	1	1	1										
US4_2 I5	768 KB	1	1	1	1	1	1										
US4_3 D5	768 KB	1	1	1	1	1	1										
L2-LIM 1024 KB																	

Note1: 'L2 Cache Size' in each row is the size accessible by that particular Master out of 'Total Shared L2 Cache Size' (768 KB)

Note2: Click on any Table box to toggle between 1 and 0

Note3: 0 in Table box means 'Master cannot evict from cache'

- There are 16 WAYs. WAY0 is always allocated for Cache.
- In the GUI, the default L2-LIM size will be set at 15 (WAY1 – WAY15). This means that 1 Way (128 Kbytes) is configured as L2 cache and 1920 Kbytes is configured as LIM. User can increase or decrease the L2-LIM size to configure the LIM as Cache memory for various processors and peripherals.
- In the GUI, all the WAYs are enabled for Cache by default. The user can disable the selection to allocate it for Scratchpad.
- Cache size shows the amount of memory available and is shared among all processors and peripherals.

### 2.3.9 SGMII

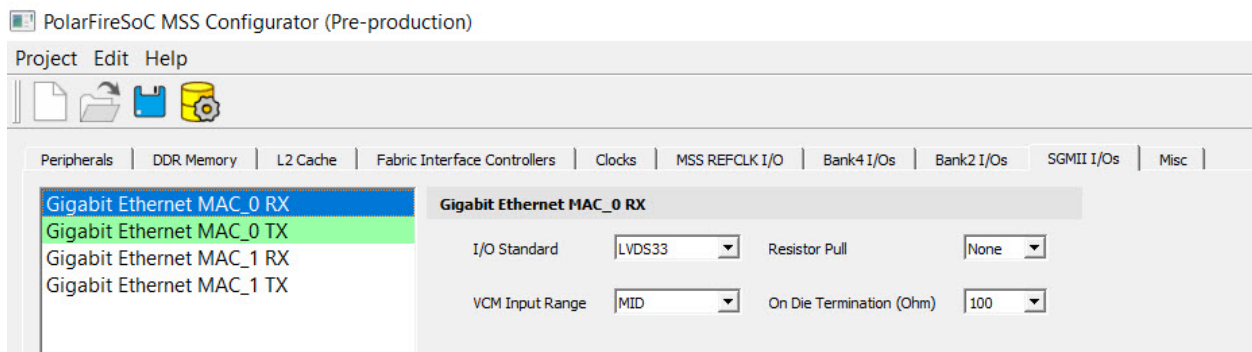
PolarFire SoC supports two full-duplex SGMII channels (Channel0 and Channel1). Each channel has one RX and one TX. There are two input and two output I/Os that need to be configured for SGMII, and all I/Os are differential.

#### SGMII Inputs

MAC\_0 (Channel0) RX and MAC\_1 (Channel1) RX are inputs and have the following options:

- I/O Standard  
**Note:** The IOSTD must match the bank voltage in the **MSS REFCLK I/O** tab. For example, if the bank 5 voltage VDDI is 3.3 V, you cannot set SGMII I/Os to any IOSTD, which is 2.5 V such as LVDS25, RSDS25, MINILVDS25, SUBLVDS25, PPDS25, and LCMD25.
- Resistor Pull
- VCM Range
- On Die Termination (Ohm)

Figure 2-17. SGMII RX



### SGMII RX Register Settings

The following table shows the Channel0/1 RX register settings.

**Table 2-3. Channel0/1 RX Register Settings**

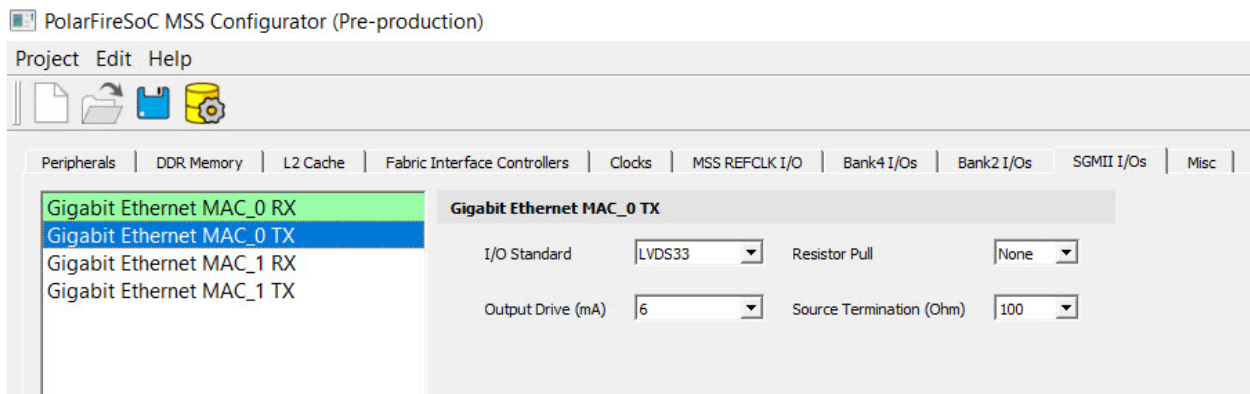
GUI Labels/Parameter Name	Options
I/O Standard	LVDS33, LVDS25, RSDS33, RSDS25, MINILVDS33, MINILVDS25, SUBLVDS33, SUBLVDS25, PPDS33, PPDS25, LCMD33, LCMD25
Resistor Pull	None, Up, Down
VCM Input Range	MID, LOW
On Die Termination (Ohm)	OFF, 100

### SGMII Outputs

MAC\_0 (Channel0) TX and MAC\_1 (Channel1) TX are outputs and have the following options:

- I/O Standard
- Resistor Pull
- Output Drive
- Source Termination (Ohm)

**Figure 2-18. SGMII TX**



### SGMII TX Register Settings

**Table 2-4. Channel0/1 TX Register Settings**

GUI Labels/Parameter Name	Options
I/O Standard	LVDS33, LVDS25, RSDS33, RSDS25, MINILVDS33, MINILVDS25, SUBLVDS33, SUBLVDS25, PPDS33, PPDS25, LCMD33, LCMD25
Resistor Pull	None, Up, Down
Output Drive (mA)	1.5, 2, 3, 3.5, 4, 6
Source Termination (Ohm)	OFF, 100

### SGMII Output I/O Standard Settings

Based on the selection of the I/O standard the user needs to enforce the following DRC checks:

**Table 2-5. SGMII Output DRC Check**

I/O_TYPE	Direction	Legal Output DRIVE Settings (mA)
LVDS33	Output	6, 4, 3.5, 3
LVDS25	Output	6, 4, 3.5, 3
RSDS33	Output	4, 3, 2, 1.5
RSDS25	Output	4, 3, 2, 1.5
MINILVDS33	Output	6, 4, 3.5, 3
MINILVDS25	Output	6, 4, 3.5, 3
SUBLVDS33	Output	3, 2, 1.5, 1
SUBLVDS25	Output	3, 2, 1.5, 1
PPDS33	Output	4, 3, 2, 1.5
PPDS25	Output	4, 3, 2, 1.5
LCMDS33	Output	6, 4, 3.5, 3
LCMDS25	Output	6, 4, 3.5, 3

**I/O Standard and Supported Output Drive**

Voltage selection for Bank5 should match the I/O Standard selected for TX and RX in both channels.

**Example 2-1.**

Bank5 Voltage selection -> VDDI = 3.3v -> LVDS33 is legal but not LVDS25

**Table 2-6. Legal Values/Settings for I/O\_TYPE/Output Drive Combination**

I/O_TYPE	Legal Output DRIVE Settings (mA)
LVDS33	6, 4, 3.5, 3
LVDS25	6, 4, 3.5, 3
RSDS33	4, 3, 2, 1.5
RSDS25	4, 3, 2, 1.5
MINILVDS33	6, 4, 3.5, 3
MINILVDS25	6, 4, 3.5, 3
SUBLVDS33	3, 2, 1.5, 1
SUBLVDS25	3, 2, 1.5, 1
PPDS33	4, 3, 2, 1.5
PPDS25	4, 3, 2, 1.5
LCMDS33	6, 4, 3.5, 3
LCMDS25	6, 4, 3.5, 3

### 2.3.10 Crypto

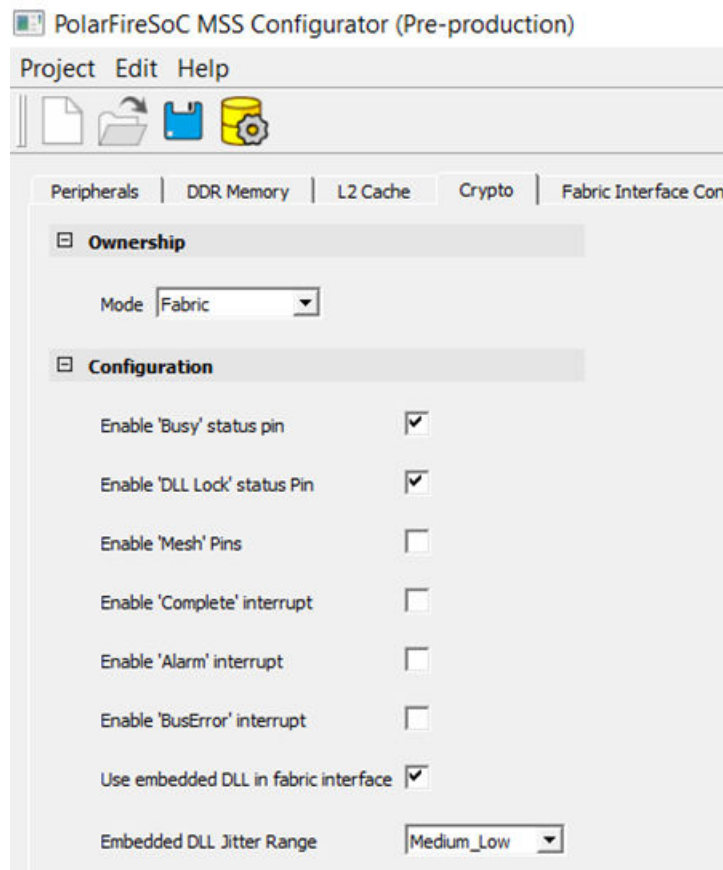
The following table lists the crypto mode ownership modes.

**Table 2-7. Crypto Ownership Modes**

Owner	Description
MSS	The MSS owns the crypto.
Fabric	The Fabric owns the crypto and ports are exposed to the fabric.
Shared MSS	This is shared between the MSS and the Fabric. The MSS is the first owner. There are regular ports and other ports for handshaking to switch the ownership.
Shared Fabric	This is shared between the MSS and the Fabric. The Fabric is the first owner. There are regular ports and other ports for handshaking and to switch ownership.

**Note:** Streaming Interface is not available for Fabric mode.

**Figure 2-19. Crypto Tab**



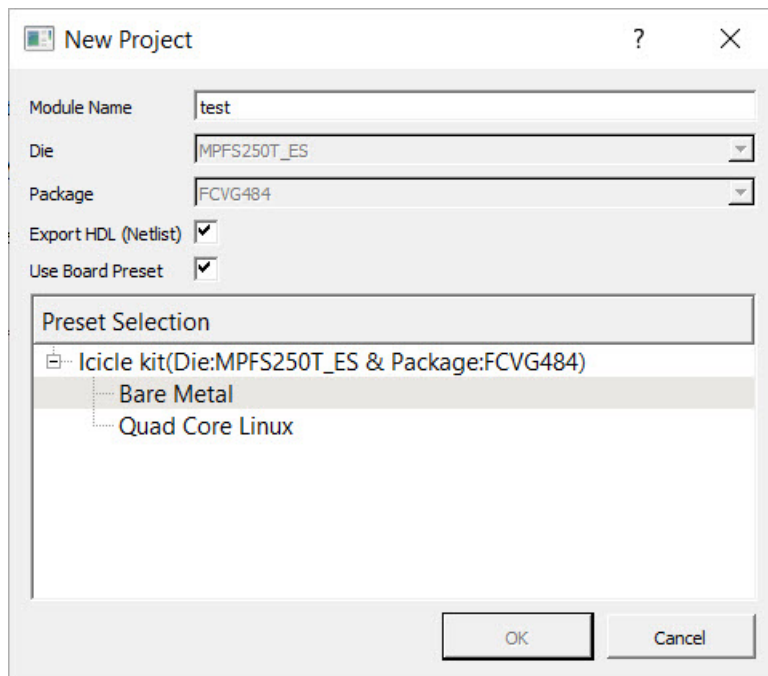
- The status pins and interrupt pins are available as configuration options in all the ownership modes except the MSS ownership mode.
- There are three options that expose the DLL lock, Busy, and Mesh ports. The Busy and DLL Lock are ON by default, while the Mesh input pin connects to 0 when not used.

### 3. Creating a Project and Configuring MSS

To create a project and configure MSS:

1. Launch the PolarFire SoC MSS Configurator (`pfsoc_mss`) using one of the following ways:
  - Libero SoC installation directory
  - Standalone MSS installation area
  - Windows Start menu
2. Create a new project using **Project > New**.
3. Enter a module name (for example `PFSOC_MSS_C0`), and then select the appropriate die and package. The module name you enter appears in the following places:
  - File names of the PolarFire SoC MSS Configurator generated outputs at the specified output/generation directory
  - MSS component file (`<module_name>.cxz`)
  - MSS XML configuration file (`<module_name>_mss_cfg.xml`)
  - MSS configuration file corresponding to the current MSS configuration that is generated (`<module_name>.cfg`)
  - MSS configuration report file (`<module_name>_Report.html`)
  - Component/module name of the MSS component (`cxz`) that can be imported to a Libero SoC project

**Figure 3-1. MSS - Module Name Dialog Box**



#### **Presets for Icicle Kit**

When users create a 'New Project,' they can import one of the available presets for Icicle kit. These presets will be staged in data folder and will be in 'CFG' format. All the parameter/values from the CFG file will loaded, except for the following three parameters:

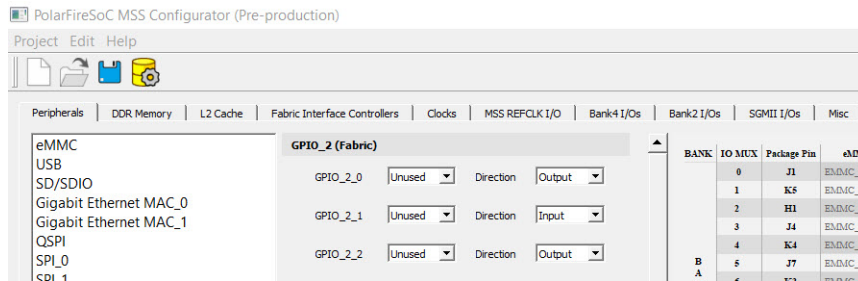
- Module name
- Die
- Package

User-selected values will be used for Module name, Die, and Package parameters in the GUI. This is done to facilitate changing Module Name/Die/Package (from the Icicle kit preset) to meet users need.

The list of presets will be shown using a tree widget. By default, 'Default Configuration' preset is selected in GUI and user must explicitly select one of the presets for Icicle kit to load them. Once a preset is selected, users will not be able to edit them using **Edit settings** option as the Preset tree widget will not be shown in 'Edit Settings' dialog.

The following figure shows the MSS configurator tabs.

**Figure 3-2. MSS Configurator Tabs**



4. Configure **Clocks**, **Fabric Interface Controllers**, **I/O Configuration**, **DDR Memory**, and **Misc settings**.
5. Click the **Save** option to save the MSS configuration to a `.cfg` file.
6. From the Save MSS Configuration dialog box:
  - Browse to a directory and create a folder. For example, create `C:\Microsemi\PFSOC_MSS_Configuration`.
  - Enter a file name (for example `PFSOC_MSS_C0`) and click **Save**.

**Note:** The file name you enter is for the standalone MSS project only and is not used as the component name.

The MSS Configuration is created and saved to the file specified and the Log window shows the following message:  
 INFO: Successfully saved MSS configuration in `C:/Microsemi/PFSOC_MSS_Configuration/PFSOC_MSS_C0.cfg` file

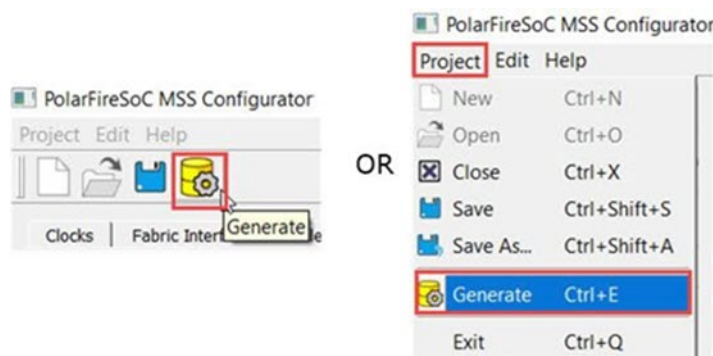
## 4. Generating, Importing, and Exporting the MSS Component

The following sections describe the steps for generating, importing, and exporting the MSS component.

### 4.1 Generating the MSS Component and Report

To generate the MSS component, use the **Generate** option (see the following figure).

**Figure 4-1. Generate Option**



The configuration file (`module_name.xml`) required for the firmware project and the configuration report file (`module_name.html`) are also generated at this time.

The Log window shows the following messages indicating the generated files:

```
INFO: Successfully generated MSS configuration report to 'C:/Microsemi/PFSOC_MSS_Configuration/
PFSOC_MSS_C0_Report.html'
```

```
INFO: Successfully generated MSS component file to 'C:/Microsemi/PFSOC_MSS_Configuration/
PFSOC_MSS_C0.cxz'
```

The report file `module_name.html` consists of following sections:

- Design Information – This section consists of design parameters like device family name, die, package, configurator version, and the date the report was generated.
- FPGA Fabric – This section mentions whether FPGA Fabric programming is required or not.
- Fabric Interface Controllers – Consists information about status of the interface controllers.
- Peripherals – Contains information about which peripherals are being used or unused.
- DDR Memory – Shows the memory type.
- List of Ports – Depicts information about all the ports with direction.
- I/O REFCLK Port Settings – Shows all the information about Reference clock ports.
- MSSIO Port Settings – Shows all the information about MSSIO ports.
- DDRIO Port Settings – Shows all the information about DDRIO ports.
- SGMII I/O Port Settings – Shows all the information about SGMII ports.

Figure 4-2. Configuration Report for PolarFire SoC MSS Configurator (Pre-production)

### Design Information

Design Parameter Name	Design Parameter Value
Family	PolarFireSoC
Die	MPFS460TS
Package	FCG1152_Eval
Version	2.0
Date	Wed Oct 28 15:39:08 2020

### FPGA Fabric

FPGA Fabric Programming	Required
-------------------------	----------

### Fabric Interface Controllers

Interface Controller Name	Enabled
FIC_0 AXI4 Master Interface	false
FIC_0 AXI4 Slave Interface	false
FIC_1 AXI4 Master Interface	false
FIC_1 AXI4 Slave Interface	false
FIC_2 AXI4 Slave Interface	false
FIC_3 APB Master Interface	false

### Peripherals

Peripheral Name	Enabled
eMMC	UNUSED
USB	UNUSED
SD/SDIO	UNUSED
Gigabit Ethernet MAC_0	SGMII_IO_B5
Gigabit Ethernet MAC_1	GMII_MII_FABRIC
QSPI	UNUSED
SPI_0	UNUSED
SPI_1	UNUSED
SD/SDIO	UNUSED
MMUART_0	MSSIO_B2_A
MMUART_1	UNUSED
MMUART_2	UNUSED
MMUART_3	UNUSED
MMUART_4	UNUSED
I2C_0	UNUSED
I2C_1	UNUSED
CAN_0	MSSIO_B2_A
CAN_1	UNUSED

### DDR Memory

DDR	Protocol
Memory Type	DDR4

### List of Ports

Port Name	Direction
MSS_RESET_N_F2M	INPUT

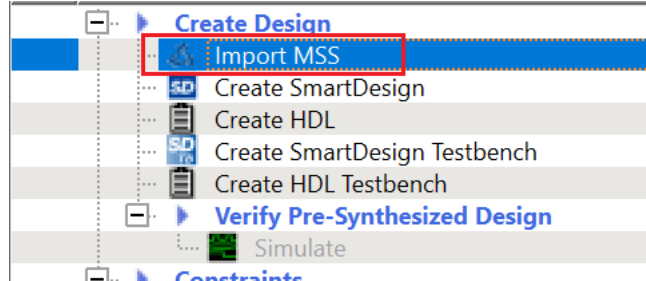


## 4.2 Importing the MSS CXZ File to Libero SoC

To import the PFSOC\_MSS\_C0.cxz file:

1. Use the **Import MSS** option shown in the following figure.

**Figure 4-3. Import MSS to Libero**



2. From Design Hierarchy, drag the MSS component to SmartDesign canvas.
3. Build the hierarchy.

**Note:** Any changes required in the MSS configuration must be performed in the PolarFire SoC MSS Configurator, and the updated MSS CXZ file must be re-imported and used in Libero SmartDesign.

## 4.3 Importing the MSS XML File to SoftConsole

Copy the XML file from:

```
<$Directory>:/Microsemi/PFSOC_MSS_Configuration/PFSOC_MSS_C0_mss_cfg.xml
```

to:

```
<$Installation Directory>:\Microchip\<$SoftConsole_Workspace>\Project_Name\src\platform\config\xml
```

**Note:** This step can also be performed using the **Import** option from SoftConsole.

## 4.4 Exporting the FPGA Design Hardware Platform Information

When using PolarFire SoC, the overall application runs an embedded software application on the RISC-V cores that may use the FPGA fabric to expand the number of I/O peripherals, accelerate software functions using FPGA logic, or control FPGA fabric functions. In these cases, the processor communicates with the FPGA fabric via the MSS Fabric Interface Controllers (FIC) and interrupt ports. The embedded software application must contain the following information to establish this communication properly:

- Fabric blocks like LSRAM, DMA Controller, and PCIe are connected to the AXI interconnect IP on the Fabric side. MSS communicates with these fabric blocks via Fabric Interface Controllers, which connects to the AXI Interconnect IP. The memory addresses of these fabric blocks are specified in the AXI Interconnect IP Configurator. These memory addresses must be specified in the software application.
- In the Libero SoC design, the user must drive the required MSS interrupt ports and other interrupts can be grounded. The corresponding Interrupt Request (IRQ) handler routines must be invoked in the software application for interrupt handling.

Libero SoC v12.5 does not export the FPGA fabric peripheral memory map, interrupt mapping, or peripheral clock frequencies. Therefore, add this information manually in your embedded software projects. For example, if fabric blocks such as LSRAM and DMA Controller are used in the design and interfaced with the MSS through a FIC, then the memory addresses of these fabric blocks must be specified in the user application code for accessing them from MSS.

## **5. Simulating an FPGA Design Interacting with MSS**

The MSS simulation model has been designed to verify the connectivity to the MSS has been properly established with the FPGA fabric logic.

The MSS Simulation model can be used to verify:

- The Fabric—MSS connectivity using the Fabric Interface Controllers (FICs).
- The Fabric—MSS interrupt (M2F and F2M ) interface.

For information about how to set up and run the simulation for the PolarFire SoC MSS, see [UG0926 User Guide PolarFire SoC FPGA MSS Simulation](#).

## 6. Programming the Application Bitstream

To program the application bitstream:

1. Use Libero SoC or FlashProExpress to program the FPGA fabric array, sNVM, eNVM and any security settings.
2. Use Libero SoC to program any eNVM client.

**Note:** SoftConsole must be used to program the Boot mode.

Alternatively, you can also perform the following steps:

1. Use SoftConsole to program the eNVM with the First Stage Boot image.
  - 1.1. Select the project you want programmed to eNVM in SoftConsole's **Project Explorer** pane.
  - 1.2. Click the **PolarFire SoC Boot Mode 1** external tool.

Programming progress messages appear in the Console.

For more information, see [PolarFire SoC Software Development and Tool Flow User Guide](#).

## **7. Sample Project**

To view a sample project, see [AC489: Building the PolarFire SoC MSS Design](#) .

## 8. Revision History

Revision	Date	Description
B	12/2020	Revision B is released in December 2020. Following is a list of changes made in this revision: <ul style="list-style-type: none"><li>• Updated the <a href="#">Using the PolarFire SoC MSS Configurator GUI</a> section.</li><li>• Updated the <a href="#">Creating a Project and Configuring MSS</a> section.</li><li>• Updated the <a href="#">Generating the MSS Component and Report</a> section.</li><li>• Updated the <a href="#">Clocks</a> section.</li><li>• Added a note in the <a href="#">SGMII</a> section.</li></ul>
A	9/2020	Initial Revision

## 9. Microchip FPGA Technical Support

Microchip FPGA Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. This section provides information about contacting Microchip FPGA Products Group and using these support services.

### 9.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

### 9.2 Customer Technical Support

Microchip FPGA Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microchip FPGA Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

You can communicate your technical questions through our Web portal and receive answers back by email, fax, or phone. Also, if you have design problems, you can upload your design files to receive assistance. We constantly monitor the cases created from the web portal throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

Technical support can be reached at [soc.microsemi.com/Portal/Default.aspx](https://soc.microsemi.com/Portal/Default.aspx).

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), log in at [soc.microsemi.com/Portal/Default.aspx](https://soc.microsemi.com/Portal/Default.aspx), go to the **My Cases** tab, and select **Yes** in the ITAR drop-down list when creating a new case. For a complete list of ITAR-regulated Microchip FPGAs, visit the ITAR web page.

You can track technical cases online by going to [My Cases](#).

### 9.3 Website

You can browse a variety of technical and non-technical information on the Microchip FPGA Products Group [home page](#), at [www.microsemi.com/soc](https://www.microsemi.com/soc).

### 9.4 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support at (<https://soc.microsemi.com/Portal/Default.aspx>) or contact a local sales office.

Visit [About Us](#) for [sales office listings](#) and [corporate contacts](#).

---

## The Microchip Website

---

Microchip provides online support via our website at [www.microchip.com/](http://www.microchip.com/). This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

---

## Product Change Notification Service

---

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to [www.microchip.com/pcn](http://www.microchip.com/pcn) and follow the registration instructions.

---

## Customer Support

---

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: [www.microchip.com/support](http://www.microchip.com/support)

---

## Microchip Devices Code Protection Feature

---

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

## Legal Notice

---

Information contained in this publication is provided for the sole purpose of designing with and using Microchip products. Information regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL OR CONSEQUENTIAL LOSS, DAMAGE, COST OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

---

## Trademarks

---

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Klear, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PackTime, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, FlashTec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, Inter-Chip Connectivity, JitterBlocker, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SMART-I.S., storClad, SQL, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2020, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-7289-6



## **Quality Management System**

---

For information regarding Microchip's Quality Management Systems, please visit [www.microchip.com/quality](http://www.microchip.com/quality).

## Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
<b>Corporate Office</b> 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: <a href="http://www.microchip.com/support">www.microchip.com/support</a> Web Address: <a href="http://www.microchip.com">www.microchip.com</a>	<b>Australia - Sydney</b> Tel: 61-2-9868-6733 <b>China - Beijing</b> Tel: 86-10-8569-7000 <b>China - Chengdu</b> Tel: 86-28-8665-5511 <b>China - Chongqing</b> Tel: 86-23-8980-9588 <b>China - Dongguan</b> Tel: 86-769-8702-9880 <b>China - Guangzhou</b> Tel: 86-20-8755-8029 <b>China - Hangzhou</b> Tel: 86-571-8792-8115 <b>China - Hong Kong SAR</b> Tel: 852-2943-5100 <b>China - Nanjing</b> Tel: 86-25-8473-2460 <b>China - Qingdao</b> Tel: 86-532-8502-7355 <b>China - Shanghai</b> Tel: 86-21-3326-8000 <b>China - Shenyang</b> Tel: 86-24-2334-2829 <b>China - Shenzhen</b> Tel: 86-755-8864-2200 <b>China - Suzhou</b> Tel: 86-186-6233-1526 <b>China - Wuhan</b> Tel: 86-27-5980-5300 <b>China - Xian</b> Tel: 86-29-8833-7252 <b>China - Xiamen</b> Tel: 86-592-2388138 <b>China - Zhuhai</b> Tel: 86-756-3210040	<b>India - Bangalore</b> Tel: 91-80-3090-4444 <b>India - New Delhi</b> Tel: 91-11-4160-8631 <b>India - Pune</b> Tel: 91-20-4121-0141 <b>Japan - Osaka</b> Tel: 81-6-6152-7160 <b>Japan - Tokyo</b> Tel: 81-3-6880-3770 <b>Korea - Daegu</b> Tel: 82-53-744-4301 <b>Korea - Seoul</b> Tel: 82-2-554-7200 <b>Malaysia - Kuala Lumpur</b> Tel: 60-3-7651-7906 <b>Malaysia - Penang</b> Tel: 60-4-227-8870 <b>Philippines - Manila</b> Tel: 63-2-634-9065 <b>Singapore</b> Tel: 65-6334-8870 <b>Taiwan - Hsin Chu</b> Tel: 886-3-577-8366 <b>Taiwan - Kaohsiung</b> Tel: 886-7-213-7830 <b>Taiwan - Taipei</b> Tel: 886-2-2508-8600 <b>Thailand - Bangkok</b> Tel: 66-2-694-1351 <b>Vietnam - Ho Chi Minh</b> Tel: 84-28-5448-2100	<b>Austria - Wels</b> Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 <b>Denmark - Copenhagen</b> Tel: 45-4485-5910 Fax: 45-4485-2829 <b>Finland - Espoo</b> Tel: 358-9-4520-820 <b>France - Paris</b> Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 <b>Germany - Garching</b> Tel: 49-8931-9700 <b>Germany - Haan</b> Tel: 49-2129-3766400 <b>Germany - Heilbronn</b> Tel: 49-7131-72400 <b>Germany - Karlsruhe</b> Tel: 49-721-625370 <b>Germany - Munich</b> Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 <b>Germany - Rosenheim</b> Tel: 49-8031-354-560 <b>Israel - Ra'anana</b> Tel: 972-9-744-7705 <b>Italy - Milan</b> Tel: 39-0331-742611 Fax: 39-0331-466781 <b>Italy - Padova</b> Tel: 39-049-7625286 <b>Netherlands - Drunen</b> Tel: 31-416-690399 Fax: 31-416-690340 <b>Norway - Trondheim</b> Tel: 47-72884388 <b>Poland - Warsaw</b> Tel: 48-22-3325737 <b>Romania - Bucharest</b> Tel: 40-21-407-87-50 <b>Spain - Madrid</b> Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 <b>Sweden - Gothenberg</b> Tel: 46-31-704-60-40 <b>Sweden - Stockholm</b> Tel: 46-8-5090-4654 <b>UK - Wokingham</b> Tel: 44-118-921-5800 Fax: 44-118-921-5820