Libero SoC v12.6 Release Notes

Introduction

The Libero® system on chip (SoC) v12.6 unified design suite is Microchip's flagship FPGA software for designing with Microchip's latest power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry-standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v12.6 for designing with Microchip's RTG4™ Rad-Tolerant FPGAs, SmartFusion®2 and IGLOO® 2 SoC FPGAs, PolarFire® FPGAs, and PolarFire SoC FPGAs.

To design with Microchip's older Flash FPGA families, use Libero SoC v11.9 and subsequent service packs.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Note: Libero SoC v12.6 does not support Classic Constraint Flow. IGLOO2, SmartFusion2, and RTG4 projects using the "Classic" flow cannot be opened in this release. For details about how to migrate Classic Constraint Flow projects to the Enhanced Constraint Flow, refer to Migrating an Existing Project Created with Classic Constraint Flow to Enhanced Constraint Flow.

Related Release Notes

In addition to these release notes, you may find the information in the following release notes helpful.

- PolarFire SoC MSS Configurator v2.0 Release Notes

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1. Libero SoC v12.6 Software Release Notes

These release notes contain important information about the Libero® system on chip (SoC) v12.6 unified design suite.

1.1 Customer Notification (CN) Support

Libero SoC v12.6 includes changes that address certain important issues.

1.1.1 PolarFire PCN20027 Maximum Read Frequency on Certain LSRAM Read Modes Have Been Reduced

The following PolarFire LSRAM configurations have derated Fmax specifications.

Users who use one of the following LSRAM configurations with a design that runs faster than the new limits listed in the following table should upgrade to Libero v12.6 and re-run static timing using SmartTime. For more information, see PCN200027 at www.microsemi.com/company/quality/product-notifications/pcn/asic-soc-fpga.

Table 1-1. LSRAM Configurations that have Derated Fmax Specifications

Condition	Datasheet Revision 1.7		Datasheet Revision 1.8		
	STD	–1	–STD	–1	Unit
Dual-port, all supported widths, non-pipelined, and read-before-write	274	285	**240**	285	MHz
Dual-port, all supported widths, pipelined, and read-before-write	274	285	**240**	285	MHz
Two-port, all supported widths, pipelined, and read-before-write	274	285	**240**	285	MHz
Two-port, all supported widths, non- pipelined, and read-before-write	274	285	**240**	285	MHz
Two-port pipelined ECC mode, pipelined, and read-before-write	274	285	**240**	285	MHz
Two-port non-pipelined ECC mode, pipelined, and read-before- write	274	285	**198**	**240**	MHz
Two-port pipelined ECC mode, non- pipelined, and read-before-write	274	285	**240**	285	MHz
Two-port non- pipelined ECC mode, non-pipelined, and read-before-write	193	285	193	**240**	MHz

1.2 New Device Support

1.2.1 PolarFire SoC

Libero SoC v12.6 introduces programming support, and Advance/Preliminary timing and power support for PolarFire SoC devices. The following tables summarize the preliminary and advanced timing and power information. For detailed information, see 9.1 PolarFire SoC New Device Support Matrices.

Table 1-2. PolarFire SoC Preliminary Timing and Power

Part Number	Speed Grade/Temperature	Device Range
MPFS250TS_ES	STD/-1 1.0/1.5V	EXT devices along with programming and SmartDebug

.....continued		
Part Number	**Speed Grade/Temperature**	**Device Range**
MPFS250TS	STD/-1 1.0/1.5V	IND devices
MPFS250TLS	STD 1.0/1.5	IND devices

Table 1-3. PolarFire SoC Advanced Timing and Power

Part Number	Speed Grade/Temperature	Device Range
MPFS025/095/160T	STD/-1 1.0/1.5V	EXT/IND devices
MPFS025/095/160TL	STD 1.0/1.5V	EXT/IND devices
MPFS025/095/160/460TS	STD/-1 1.0/1.5V	IND devices
MPFS025/095/160/460TLS	STD 1.0/1.5V	IND devices

1.2.2 PolarFire

Production timing support has been added for PolarFire devices for 1.0 V and 1.05 V. The following table summarizes the automotive Tgrade2 production timing and power information. For detailed information, see 9.2 PolarFire New Production Timing Support Matrix.

Table 1-5. PolarFire Automotive Tgrade2 Production Timing and Power

Part Number	Speed Grade/Temperature	Device Range
MPF100/200/300T	STD/-1 1.0/1.05V	Tgrade2 devices

1.2.3 RT PolarFire

Libero SoC v12.6 introduces programming support, and Advance timing and power support for RT PolarFire devices within the PolarFire device family selection. The following table summarizes the advance timing and power information. For detailed information, see 9.3 RT PolarFire Licensing and Device/Package Combination Matrix.

Table 1-6. RT PolarFire Advance Timing and Power

Part Number	Speed Grade/Temperature	Device Range
RTPF500T/TS	-1 1.0/1.05V	MIL devices
RTPF500TS/TL/TLS	STD 1.0/1.05V	MIL devices

1.3 Software Features and Enhancements

1.3.1 Timing Report Explorer

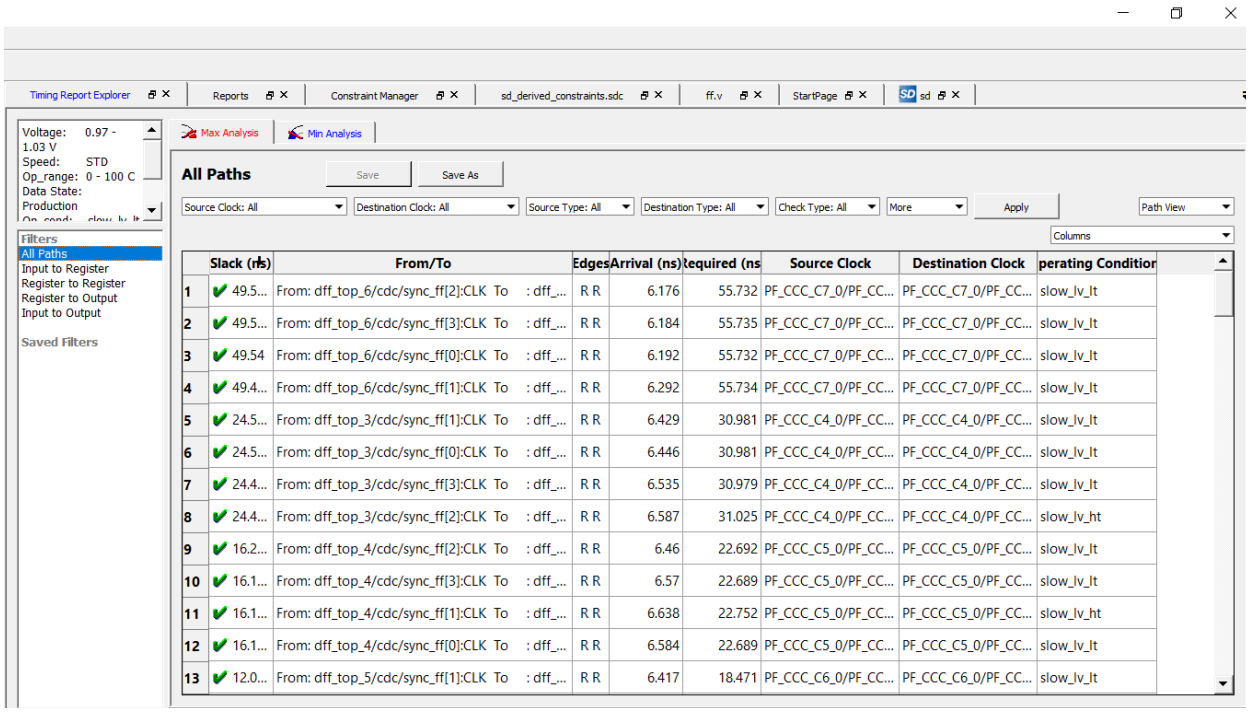
Libero SoC v12.6 introduces Timing Report Explorer to provide a consolidated view of the timing paths present in the Timing Report. The Timing Report Explorer contains filters to select:

- Launch clock and Capture clock
- Start point and End point
- Setup and hold violations

The Timing Report Explorer is invoked from the Libero menu by selecting **Tools > Timing Browser**.

For more information, see the *SmartTime User Guide*.

Figure 1-1. Timing Report Explorer

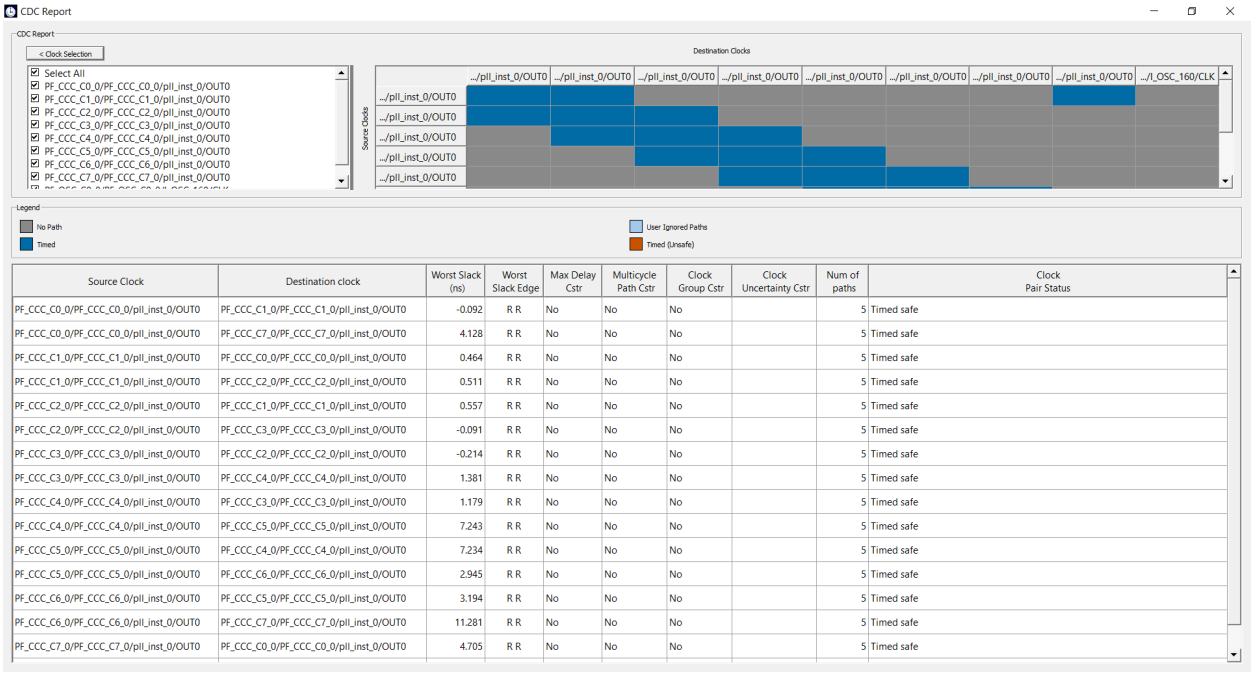


1.3.2 SmartTime CDC Report Enhancements

The CDC Report from SmartTime has been enhanced in Libero SoC v.12.6 to display the following additional information for each source and destination clock group:

- Source Clock
- Destination clock
- Worst Slack
- Max Delay Cstr
- Multicycle Path Cstr
- Worst Slack Edge
- Number of Paths
- Clock Pair Status

Figure 1-2. CDC Report



Source Clock	Destination clock	Worst Slack (ns)	Worst Slack Edge	Max Delay Cstr	Multicycle Path Cstr	Clock Group Cstr	Clock Uncertainty Cstr	Num of paths	Clock Pair Status
PF_CCC_C0_0/PF_CCC_C0_0/pll_inst_0/OUT0	PF_CCC_C1_0/PF_CCC_C1_0/pll_inst_0/OUT0	-0.092	R R	No	No	No		5	Timed safe
PF_CCC_C0_0/PF_CCC_C0_0/pll_inst_0/OUT0	PF_CCC_C7_0/PF_CCC_C7_0/pll_inst_0/OUT0	4.128	R R	No	No	No		5	Timed safe
PF_CCC_C1_0/PF_CCC_C1_0/pll_inst_0/OUT0	PF_CCC_C0_0/PF_CCC_C0_0/pll_inst_0/OUT0	0.464	R R	No	No	No		5	Timed safe
PF_CCC_C1_0/PF_CCC_C1_0/pll_inst_0/OUT0	PF_CCC_C2_0/PF_CCC_C2_0/pll_inst_0/OUT0	0.511	R R	No	No	No		5	Timed safe
PF_CCC_C2_0/PF_CCC_C2_0/pll_inst_0/OUT0	PF_CCC_C1_0/PF_CCC_C1_0/pll_inst_0/OUT0	0.557	R R	No	No	No		5	Timed safe
PF_CCC_C2_0/PF_CCC_C2_0/pll_inst_0/OUT0	PF_CCC_C3_0/PF_CCC_C3_0/pll_inst_0/OUT0	-0.091	R R	No	No	No		5	Timed safe
PF_CCC_C3_0/PF_CCC_C3_0/pll_inst_0/OUT0	PF_CCC_C2_0/PF_CCC_C2_0/pll_inst_0/OUT0	-0.214	R R	No	No	No		5	Timed safe
PF_CCC_C3_0/PF_CCC_C3_0/pll_inst_0/OUT0	PF_CCC_C4_0/PF_CCC_C4_0/pll_inst_0/OUT0	1.381	R R	No	No	No		5	Timed safe
PF_CCC_C4_0/PF_CCC_C4_0/pll_inst_0/OUT0	PF_CCC_C3_0/PF_CCC_C3_0/pll_inst_0/OUT0	1.179	R R	No	No	No		5	Timed safe
PF_CCC_C4_0/PF_CCC_C4_0/pll_inst_0/OUT0	PF_CCC_C5_0/PF_CCC_C5_0/pll_inst_0/OUT0	7.243	R R	No	No	No		5	Timed safe
PF_CCC_C5_0/PF_CCC_C5_0/pll_inst_0/OUT0	PF_CCC_C4_0/PF_CCC_C4_0/pll_inst_0/OUT0	7.234	R R	No	No	No		5	Timed safe
PF_CCC_C5_0/PF_CCC_C5_0/pll_inst_0/OUT0	PF_CCC_C6_0/PF_CCC_C6_0/pll_inst_0/OUT0	2.945	R R	No	No	No		5	Timed safe
PF_CCC_C6_0/PF_CCC_C6_0/pll_inst_0/OUT0	PF_CCC_C5_0/PF_CCC_C5_0/pll_inst_0/OUT0	3.194	R R	No	No	No		5	Timed safe
PF_CCC_C6_0/PF_CCC_C6_0/pll_inst_0/OUT0	PF_CCC_C7_0/PF_CCC_C7_0/pll_inst_0/OUT0	11.281	R R	No	No	No		5	Timed safe
PF_CCC_C7_0/PF_CCC_C7_0/pll_inst_0/OUT0	PF_CCC_C0_0/PF_CCC_C0_0/pll_inst_0/OUT0	4.705	R R	No	No	No		5	Timed safe

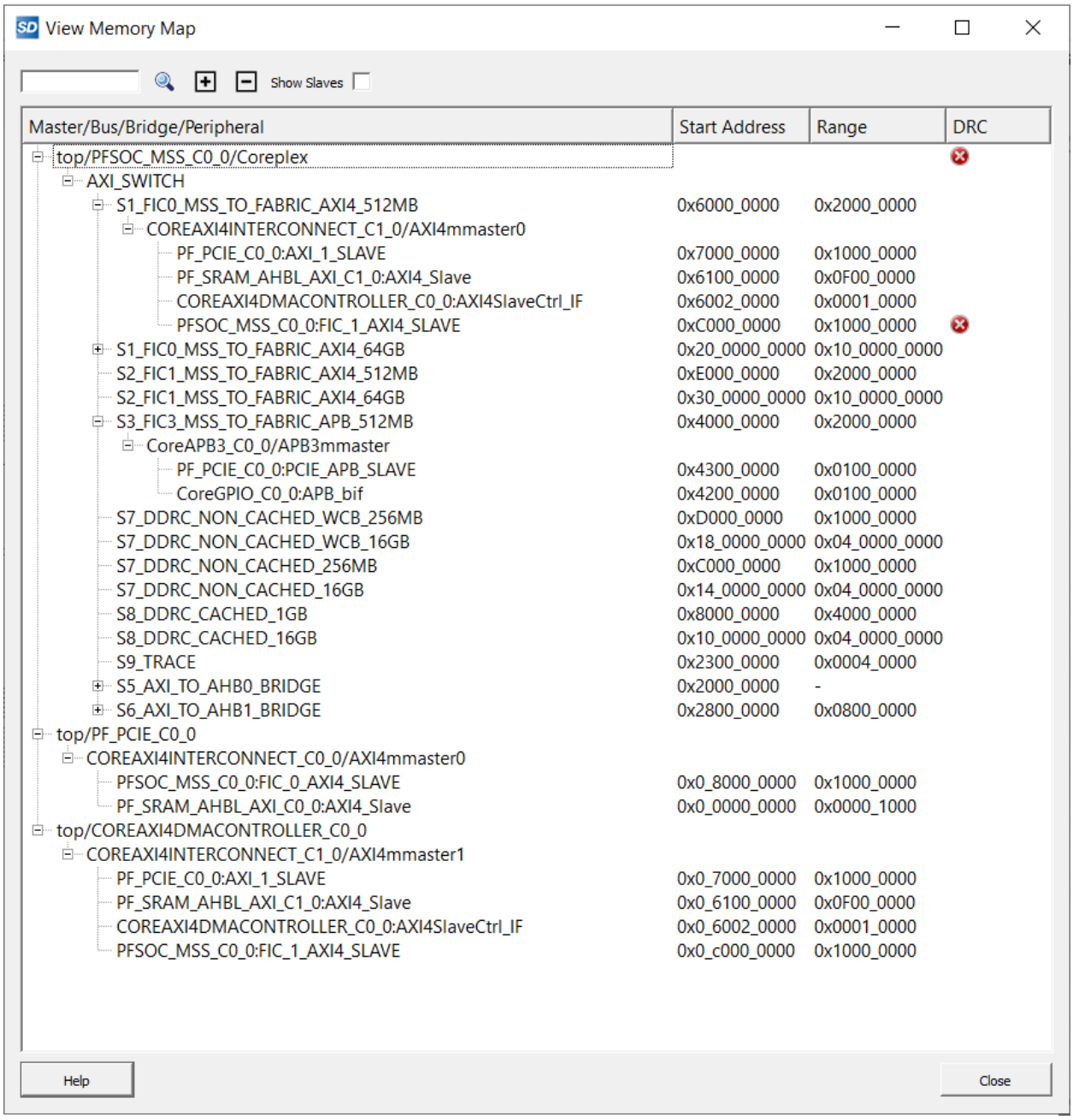
1.3.3 Memory Map Generator

Libero SoC v12.6 enables memory map generation for all AXI, AHB, and APB peripherals connected to a bus host within all SmartDesign components in the active design hierarchy.

The memory map generates Start Address, Range, and DRC, which can be viewed in the SmartDesign Memory Map View widget and can be exported to a JSON file using a menu or a Tcl command.

For more information, see the *SmartDesign User Guide*.

Figure 1-3. View Memory Map



1.3.4 Embedded IP Configuration Report in HDL

Starting with Libero SoC v12.6, the Tcl commands for IP core generation are embedded in the generated RTL created by SmartDesign. This simplifies regenerating the IP with the same configuration when the design is transferred to another user or when the Libero Project is archived.

For more information, see the *Libero SoC Design Flow User Guide* or the *PolarFire Design Flow User Guide*.

1.3.5 Bitstream Option to Sanitize All sNVM/eNVM Pages in Erase Action

Libero v12.6 supports **sanitize sNVM** and **sanitize eNVM** options for the ERASE action. This option programs all 0's into all eNVM/sNVM pages.

- The sNVM sanitize option is supported for PolarFire, RT PolarFire, and PolarFire SoC.
- The eNVM sanitize option is supported for SmartFusion2, IGLOO2, and PolarFire SoC.

The tools that have these options are:

- Generate bitstream.
- Export bitstream.
- Export job.

The tools have the new Tcl parameters **sanitize_snvm** (PolarFire, RT PolarFire, and PolarFire SoC) and **sanitize_envm** (SmartFusion2, IGLOO2, and PolarFire SoC).

The sNVM sanitization option is enabled in the Generate Bitstream and Export Job tools if Fabric/sNVM component is selected. In the Export Bitstream, the option is enabled if Fabric/sNVM component is selected for at least one programming file type (master or update).

The eNVM sanitization option is enabled in the Generate Bitstream and Export Job tools if eNVM is configured and eNVM component is selected. In the Export Bitstream tool, the option is available if eNVM is configured and selected for at least one file type (master or update).

Default for both options when they are enabled is “off”.

Note: The sanitization options do not depend on the OTP security setting. ERASE actions fail if there is OTP security.

1.3.6 SmartDebug LSRAM ECC Support

SmartDebug LSRAM ECC provides the ability to inject single-bit or multi-bit errors and validate design response. This feature applies to RTG4, PolarFire, RT PolarFire, and PolarFire SoC.

Libero SoC v12.6 enhances the SmartDebug GUI for Two-Port LSRAM configured in ECC mode. In this mode, SmartDebug:

- Allows error injection.
- Displays the Data and ECC bits separately.
- Reports Single-bit and Double-bit errors.

For more information, see the *SmartDebug User Guide*.

1.3.7 SynplifyPro and Identify

The SynplifyPro and Identify tools bundled in Libero SoC v12.6 have been upgraded to version Q-2020.03M-SP1.

SynplifyPro Q-2020.03M-SP1 flags warning messages for unconnected Input ports of instantiated macros. For non-hierarchical modules having unconnected input ports for the instantiated macros, the tool issues an error message. For hierarchical or black-box modules having unconnected input ports for instantiated macros, the tool issues a warning message, such as `<signal> is Unconnected. Assign a valid signal to this pin.`

1.3.8 Modelsim ME and Modelsim ME Pro

The Modelsim ME and Modelsim ME Pro bundled in Libero SoC v12.6 have been upgraded to version 2020.3 OEM.

For installations that use a floating license, the floating license daemons must be updated to the latest version listed in the following table.

Important: To work with Libero SoC v12.6, users must update their Daemons version. Otherwise, Mentor tool displays an error message and will not open.

Table 1-7. Updating Floating License Daemons

Download	lmgrd/lmutil/ lmhostid	actlmgrd	snpslmd	mgcld
Windows Daemons	v11.16.6.0	v11.16.1.0	v11.16.6.0	v11.16.4.0

.....continued

Download	lmgrd/lmutil/ lmhostid	actlmgrd	snpslmd	mgcld
Linux Daemons	v11.16.6.0	v11.16.1.0	v11.16.6.0	v11.16.4.0

1.4 New Silicon Features and Enhancements

1.4.1 PolarFire SoC

1.4.1.1 MPFS250 FCVG484 – Bank1 and Bank9 Common Voltage DRC

In the MPFS250-FCVG484 package, there is no VDDI for Bank9. Instead, this package supports VDDI on Bank1 as in the case of the FCVG484 package for the PolarFire SoC Icicle kit.

A Design Rule Check (DRC) has been implemented in Libero SoC v12.6 to check for this restriction.

For more information check the PPAT file for each package.

1.4.1.2 Fast MSS DDR Memory Simulation

Libero SoC v12.6 introduces a Fast Mode simulation model for the MSS DDR. The fast mode model bypasses the DDR initialization sequence to speed up simulation.

The model also includes a QoS feature to tune the bandwidth for the fabric hosts when accessing DDR.

For more information, see the *PolarFire SoC MSS simulation User Guide*.

1.4.1.3 Simulation of User Cryptoprocessor for “S” Devices

Libero SoC v12.6 introduces simulation support for User Cryptoprocessor for PolarFire SoC “S” devices.

For more information, see the *PolarFire SoC MSS simulation User Guide*.

1.4.1.4 MSS I/Os and Bank Configuration

Libero SoC v12.6 introduces MSS I/Os so that bank voltage, placement, and IOSTD are displayed in new columns in the I/O Editor and are read-only.

The I/O and bank information are also reported in the pin report. The board layout pin report has been updated to show how to connect all the bank VDDIs, depending on what is used in the design.

For more information, see the *PolarFire IO Editor User Guide*.

1.4.1.5 PolarFire SoC Security Policy Manager Option to Disable eNVM Field Updates

Using this option, eNVM can be pass key protected for field updates. By default, field updates are allowed for eNVM without requiring FlashLock Passcode (UPK1). To protect eNVM, select the option to disable erase/write operations, which requires FlashLock Passcode (UPK1) to be able to update eNVM.

1.4.1.6 PolarFire SoC Zeroization Support

Libero SoC v12.6 enables Zeroization support in “Export Bitstream”. The generated file will have ZEROIZE_LIKE_NEW and ZEROIZE_UNRECOVERABLE programming actions.

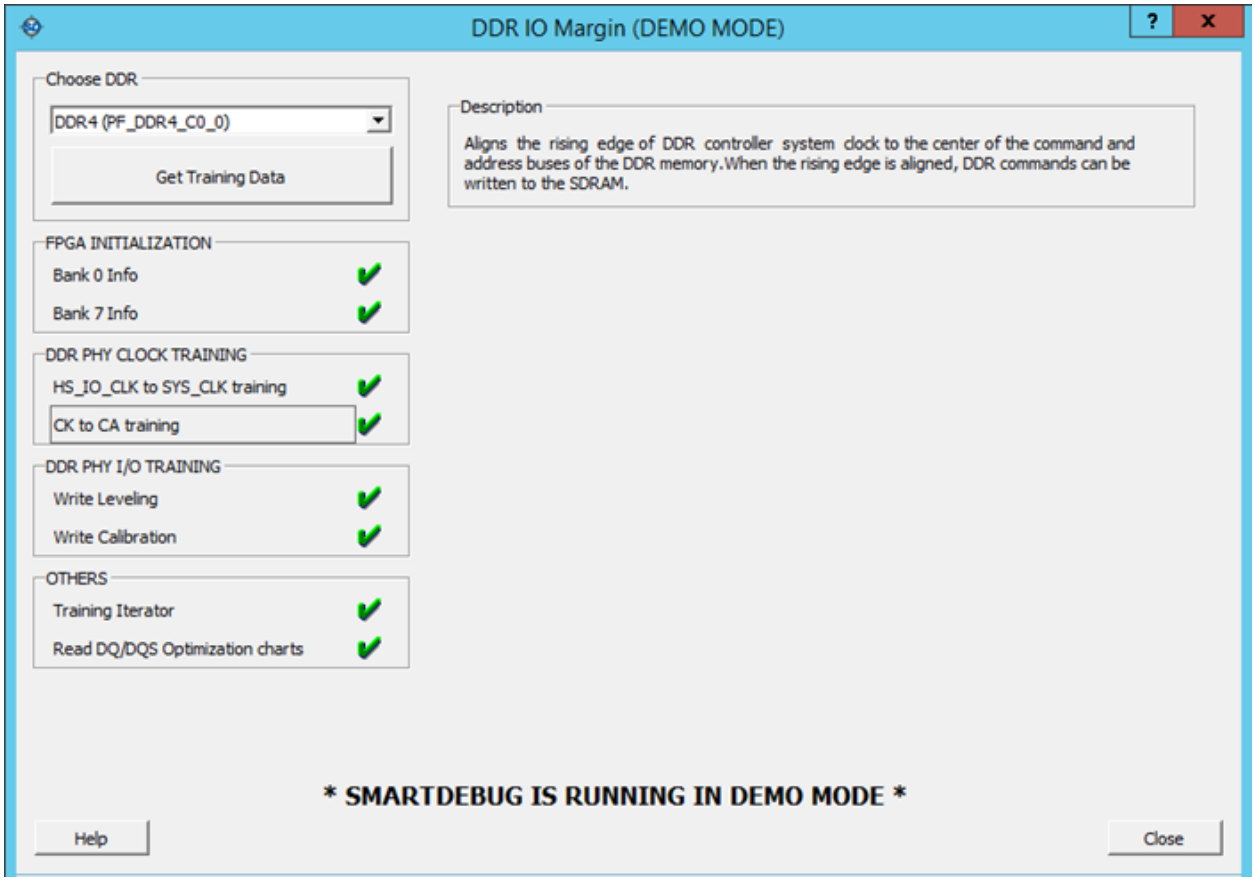
For more information, see the *PolarFire Design Flow User Guide*.

1.4.1.7 SmartDebug - I/O Margining Analysis for DDR Memory Controllers

With Libero SoC 12.6, SmartDebug extends the Debug DDR Memory tool for DDR3/DDR4/LPDDR3 for PolarFire SoC devices. This tool helps users visualize the margin on the DDR I/Os after the DDR Memory I/O interface is trained.

For more information, see the *PolarFire SmartDebug User Guide*.

Figure 1-4. DDR IO Margin



1.4.2 PolarFire, RT PolarFire, and PolarFire SoC

1.4.2.1 Synthesis Clock Gating

Synplify Pro bundled with Libero SoC v12.6 has been enhanced to support clock gating inference for PolarFire and PolarFire SoC in synthesis. Synplify Pro will infer clock enable logic coded in HDL as GCLKINT or RCLKINT PolarFire macros. This feature can be enabled in Tcl or from the GUI under the **Synthesis > Configure Options**.

For more information, see the *Synplify Pro User Guide*.

1.4.2.2 Bank-Based I/O Recalibration

Libero SoC v12.6 introduces the capability for users to recalibrate I/Os manually/on-demand for each bank. I/O recalibration is sometimes required to account for delays or to compensate Vt performance impact.

For more information, see the *PolarFire IO User Guide*.

1.4.2.3 FlashPro 6 Expanded SPI Flash Memory Device Support

Libero SoC v12.6 introduces support for additional SPI Flash devices for programming from FlashPro 6. The support includes devices from Microchip, Macronix, Spansion, ISSI, Winbond, and Micron. For more information, see the Programming User Guide for the specific device family.

Table 1-8. Expanded SPI Flash Memory Device Support

Manufacturer	Device
Micron	MT25QL01GBBB8ES

.....continued	
Manufacturer	**Device**
Micron	MT25QPL128AB
Macronix	MX25V4035
Macronix	MX66L51235SF
Macronix	MX66U1G45GMI00
Macronix	MX25L8006EM2I-12G
Spansion/Cypress	S25FL128S
Spansion/Cypress	S25FL256S
Spansion/Cypress	S25FL512S
Winbond	W25Q256FV
Winbond	W25Q80DVSSIG
Microchip	SST25PF040CT
Microchip	SST26VF064b
Cypress	CYRS16B256

1.4.2.4 FlashPro Express Developer Mode

In developer mode, users can create a new job project by automatically constructing chain by scanning the physical devices connected to the selected programmer. This feature is available only in JTAG mode. In FPExpress - developer mode, the programmer connectivity and interface feature is available, which can be used to add, edit, delete devices in a chain, load/unload programming files, and load/unload SPI flash files. This feature is similar to the programming connectivity and interface feature in Libero SoC.

1.4.2.5 SmartDebug XCVR Read/Write Access

Libero SoC v12.6 enables read/write access to the XCVR registers from the SmartDebug GUI. Register access was available from Tcl commands in previous Libero versions.

For more information, see the *SmartDebug User Guide*.

1.4.2.6 PolarFire XCVR Sourced Fabric Clocks and Jitter Compensation

The PolarFire XCVR can source three different clocks into the fabric:

- TX_CLK
- RX_CLK
- REFCLK (FAB_REF_CLK)

These clocks contain high frequency jitter that is not automatically taken into account by Libero in the timing report and SmartTime. It is recommended that users add clock-uncertainty constraints to these clocks in their design.

The following table shows recommended values for clock uncertainty per clock, resource, and speed-grade.

Table 1-9. Recommended Values for Clock Uncertainty

Clock Type	STD	-1
FAB_REF_CLK on Global	275 ps	200 ps
FAB_REF_CLK on Regional	N/A	N/A
TX_CLK_G on Global	300 ps	225 ps
TX_CLK_R on Regional	225 ps	150 ps

.....continued		
Clock Type	**STD**	**-1**
RX_CLK_G on Global	325 ps	250 ps
RX_CLK_R on Regional	250 ps	175 ps

The following example shows a clock-uncertainty constraint that can be added to the user's timing SDC file.

```
set_clock_uncertainty -setup 0.150 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/
TX_CLK_R } ]
set_clock_uncertainty -setup 0.175 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/
RX_CLK_R } ]

# TX_CLK and RX_CLK on Globals
set_clock_uncertainty -setup 0.300 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/
TX_CLK_G } ]
set_clock_uncertainty -setup 0.325 [ get_pins { PF_XCVR_ERM_LANE2/I_XCVR/LANE0/
RX_CLK_G } ]

# FAB_REF_CLK on Global
set_clock_uncertainty -setup 0.275 [get_clocks PF_DDR4_C0_0/CCC_0/pll_inst_0/OUT1]
```

The automatic management of these constraints will be added in a future release of Libero SoC.

Note: It is also important to add the other required jitter sources as clock uncertainty into your design constraints. See the datasheet for the jitter to be added for components such as PLL, DLL and RC Oscillator. For input pins that are direct or are inputs to the DLL (but not for a PLL), the input jitter on the clock input pin must also be added to your timing constraints.

2. Migrating Designs to Libero SoC v12.6

2.1 Design and Core Invalidation

2.1.1 MPFS250 FCVG484 Designs Layout Invalidation Designs Layout Invalidation

Place and route performed with earlier Libero SoC version will be invalidated when Libero SoC v12.6 is invoked for designs using any of the MPFS250-FCVG484 devices if Bank1 and Bank9 have a different VCCI setting. The two banks are physically connected in the package and have a common VCCI pin. For more information, see the Public Pin Assignment Table (PPAT).

2.2 Core Enhancements and Upgrades

Table 2-1. Core Enhancements and Upgrades

Core	12.6 Version	Status	Comments
PF_DRI	1.1.100	Production	Enhancements: Added APB Slave interface option to allow for connectivity via CoreAPB3.
PF_INIT_MONITOR	2.0.203	Production	Enhancements: Added options to enable I/O banks recalibration.
PF_IOD_OCTAL_DDR	2.0.101	Production	No functional change: Moved core from pre-production to production status.
PF_TX_PLL	2.0.300	Production	New advanced Jitter Attenuation options.
PFSOC_INIT_MONITOR	1.0.204	Pre-production	Enhancements: Added options to enable I/O banks recalibration.
RTG4_SRAM_AHBL_AXI	1.0.115	Production	Enhancement: Added Tcl support to specify memory files for simulation.

For more information about updating a core version, see 2.3 Updating a Core Version.

2.3 Updating a Core Version

Perform the following procedure to update a core version:

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version by right-clicking on the core component in the design hierarchy and selecting **Replace Component Version**.
3. Regenerate the core.
4. Derive the Timing Constraints again from the Constraint Manager tool to use the latest generated core timing constraints.
5. Rerun the design flow.

3. Resolved Issues

The following table lists the customer-reported defects and enhancement requests resolved in Libero SoC v12.6 that have case numbers. Resolution of previously reported “Known Issues and Limitations” are also noted in this table.

Table 3-1. Customer-reported Defects and Enhancement Requests with Case Numbers

Case Number	Description	Resolution
493642-2736476316	"Instruction not yet implemented" error in PolarFire PCIe BFM simulation.	Increased Max instruction size to 32768 in serdes_bfm.v file to support more instructions.
493642-2760929388	Net search/navigation problem not fixed.	Fixed the Libero code to allow for proper search and navigation between the design tree and the schematic view in the Netlist Viewer.
493642-2761848512, 493642-2789984624	Libero 12.4 Unlinking HDL files.	Fixed the issue to allow for proper search and navigation between the design tree and the schematic view in the Netlist Viewer.
493642-2739601296	First stage init client occupies 18 pages and user guide mentions only one page.	Updated the *PolarFire FPGA Design Flow User Guide* with the correct information.
493642-2717100262	TEMPR with custom-specific temperatures.	Updated the *PolarFire FPGA Tcl Command Reference Guide* and the *Libero SoC Tcl Command Reference Guide* to include the missing information.
493642-2174852554	Enable eNVM/sNVM Sanitization Action/command - ERASE action.	Added eNVM/sNVM sanitization to this release. See 1.3.5 Bitstream Option to Sanitize All sNVM/eNVM Pages in Erase Action.
493642-2787088315	Place and Route failure with MPF100T-FCG484I.	Fixed the assertion failure in this release. P&R passes when XCVR is placed using the IO Editor or PDC.
493642-2773005455	RTPF- Report that tells the user which registers Layout has placed with cluster separation.	Libero now prints a TMR summary after Place and Route is complete.
493642-2778179128	PF_SOC: xport MPE : SmartPower crashes for MSS-based designs.	Fixed the crash in this release.
493642-2736787772, 493642-2760732693	The I/O standard for the LPDDR4 is not present.	Corrected the I/O standard for DDR banks based on the selected DDR standard.
493642-2752765844	FP6 - Support for Spansion / Cypress S25FL512S SPI Flash memory.	Expanded support for SPI flash devices. See 1.4.2.3 FlashPro 6 Expanded SPI Flash Memory Device Support.
493642-2748414757	FP6 - Support for Macronix MX25V4035F SPI Flash memory.	Expanded support for SPI flash devices. See 1.4.2.3 FlashPro 6 Expanded SPI Flash Memory Device Support.

.....continued

Case Number	Description	Resolution
493642-2684754568, 493642-2490103952, 493642-2568791212, 493642-2606807822, 493642-2635375032, 493642-2661732256	FP6: PolarFire: SPI-Flash Programming devices supported.	Expanded support for SPI flash devices. See 1.4.2.3 FlashPro 6 Expanded SPI Flash Memory Device Support.
493642-2707013487	FP6 - Support for Cypress S70FS01GSAGMFI010 SPI Flash memory.	Expanded support for SPI flash devices. See 1.4.2.3 FlashPro 6 Expanded SPI Flash Memory Device Support.
493642-2706626995	FP6 - Support for Macronix MX66U1G45G SPI Flash memory.	Expanded support for SPI flash devices. See 1.4.2.3 FlashPro 6 Expanded SPI Flash Memory Device Support.
493642-2761396209	Provide SPI Flash memory custom size less than 1 MB.	Expanded support for SPI flash devices. See 1.4.2.3 FlashPro 6 Expanded SPI Flash Memory Device Support.
493642-2782147144	Import HDL Source Folders does not detect files with capital .VHD extension.	Extended Libero support to recognize files with .VHD extension as VHDL files.
493642-2754199742	Firmware catalog fails to run in Linux.	Fixed the crash in this release.
493642-2672550556	MEMORYMAP: PF: RISC-V system memory map.	Libero now generates a memory map report. For details, see 1.3.3 Memory Map Generator.
493642-2782712105	I/O editor crashes when io_std is assigned to JTAG banks in PDC.	Fixed the crash in this release. Libero reports an error when IO standard is assigned to dedicated I/Os.
493642-2782399975	Enhancement Request on ChipPlanner.	Mousing-over the I/O now displays package pin and I/O bank type.
493642-2758998134	HDL_LANGUAGE: Creating testbench instantiates package, but not top module.	Instantiated the top module as unit under test.
493642-2041544240, 493642-2289485500, 493642-2633077946, 493642-2725172462	Batch mode command for Libero to display the STD out on screen.	Added the new option `console_mode:show` to the Libero command line to display STDOUT on the console.
493642-2783805520	System Builder and MDDR Configurator seem to block 4 Burst.	Added checks for the Burst Length option based on the DDR memory type.
493642-2772574227	Issue programming PolarFire device through SmartDebug via Tcl script.	Corrected the exported Tcl file in this release and programming through the Tcl script passes.

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Case Number	Description	Resolution
493642-2507765827, 493642-2638828358	RTG4: Use SmartDebug to Inject Errors on ECC RAM blocks.	Enhanced Libero SmartDebug to inject errors in RAM blocks. See 1.3.6 SmartDebug LSRAM ECC Support.
493642-2205214756	MEMORY_MAP: Libero crashes (assertion failure) when Modify Memory Map is invoked.	Fixed the reported crash in this release.
493642-2798761326	Libero 12.5: B_WEN is wrongly configured for SF2 LSRAM.	Enabled SmartFusion2 LSRAM WEN bit for widths of 10-12.
493642-2766233920, 493642-2763576582	Libero crashes when trying to open Top level Smartdesign.	Fixed the crash in this release.
493642-2751906843	PF_XCVR: TXPLL: Switching between CDR ref clock and TxPLL.	Removed support for the clocks switching feature and removed the corresponding options from the Transceiver configurator.
493642-2747946263	RTG4FCCC: Frequency entry < 400 MHz	Fixed the issue in Libero CCC configurator by preventing users from entering a frequency greater than 400 MHz.
493642-2639320907	PF_SRAM_AHBL_AXI: Support of '.ihx' for PF_SRAM_AHBL_AXI.	Added '.ihx' file support to Libero.
493642-2790717260	Synplfiy Pro crashes: Error Code [nvhdlgen.cpp:6245 : Error occurred while inferring asymmetric ram.	Fixed this issue in the Synplify Pro version Q-2020.03M-SP1 bundled with Libero SoC.
493642-2774341913	m_generic.exe Synplify error.	Fixed this issue in the Synplify Pro version Q-2020.03M-SP1 bundled with Libero SoC.
493642-2757444781	Remove TMR fault injection feature in GUI.	Removed the fault injection feature from Synplify Pro options.
493642-2766323753	Synplify crash (on P2019, Q2020 releases).	Fixed this issue in the Synplify Pro version Q-2020.03M-SP1 bundled with Libero SoC.
493642-2746622253	Synthesis timing report question - Large delay associated with OUTBUF.	Corrected the output pad delay values.
493642-2759945306	Synplify inferring uSRAM instead of LSRAM.	Fixed this issue in SynplifyPro to infer LSRAM instead of uSRAM.
493642-2726041637	Synthesize error: VHDL slice array assignation not working correctly.	Fixed in the SynplifyPro version Q-2020.03M-SP1 bundled with Libero SoC.
493642-2725654320	Synthesize error: VHDL when else in the 'loop' not interpreted correctly.	Fixed in the SynplifyPro version Q-2020.03M-SP1 bundled with Libero SoC.
493642-2725616347	Synthesize error: VHDL concatenation (&) with array typed range does not work.	Fixed in the SynplifyPro version Q-2020.03M-SP1 bundled with Libero SoC.

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Case Number	**Description**	**Resolution**
493642-2775228780	Project state is not preserved while opening project via tcl command.	Fixed this issue in this release. Project state is preserved when the Libero project is reopened.
493642-2707807672	Absolute/Relative path: Enhancement Request: Synthesis script setting in the "configure_tool -name {SYNTHESIZE}" is stored with hard path.	Added this enhancement to this release. Relative paths can now be set in **Synthesis -> Configure Options**.
493642-2771635140	SpaceWire Data Timing path used in V12.3 no longer exists.	Fixed this issue in this release. SmartTime now allows path ending at a register clock pin to be reported in user sets.
493642-2820892077	When DRI mode is enabled, ECALIB configurator will not open in Libero SoC 12.5 and Libero SoC 12.5 SP1. When DRI mode is disabled and GL0 is not used in the design, ECALIB configurator will not open in Libero SoC 12.5 and Libero SoC 12.5 SP1.	Use Libero SoC v12.6 or Libero SoC v 12.4. While computing internal delays, Libero takes GL0 as the slowest clock that is not used. As a result, configurator does not open in Windows and causes an assertion failure in Linux. To avoid this, use Libero 12.6 or Libero 12.4.
493642-2829401262	In Libero v12.5 and v12.5 SP1, Chip Planner crashed after the regions were renamed in the **Regions** tab.	This issue has been resolved in Libero v12.6.

The following table lists the customer-reported defects and enhancement requests resolved in Libero SoC v12.6 that do not have case numbers. Resolution of previously reported “Known Issues and Limitations” are also noted in this table.

Table 3-2. Customer-reported Defects and Enhancement Requests (No Case Numbers)

Description	Resolution
I/O: Remove I/O placement table from compile and move it to the layout report.	For SmartFusion2/IGLOO2/RTG4, moved the I/O placement section from the compile report to the layout log after the resource report.
RTG4 exported full placement pdc constraint fails constraint manager check.	Excluded duplicated RGRESET created by layout from the PDC export that was causing the error.
Reading X.509 certificate from JTAG using FlashPro.	Displayed the X.509 certificate in FlashPro Express log window under "READ_DEVICE_CERTIFICATE" action.
Incorrect FPGA state printed relative to the selected run Action.	Fixed the issue with Flash Pro and the correct state of device is now displayed.
PF_IOD_CDR: hs io clk bridging in io cdr causes issues.	Prevents low skew bridging with PF_IOD_CDR.
IOFF Combining for DIFF IO PADN Flow and Reporting Issues.	Addressed reporting issues so that compile report now displays the correct differential IO usage.
Add Usage Details for PolarFire/IGLOO2/RTG4 routing conflicts report.	Added the routing conflicts report to the Libero online help to which users can.

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Description	Resolution
Tcl command download_core does not work in command line execution.	Fixed a Libero issue with loading web repositories in command line mode. Users can now download cores from the command line.
Utilization report doesn't match compile report.	Fixed a Power Estimator issue with exporting Math Blocks with zero activity. The utilization between Power Estimator and Libero compile report now matches.
Support for ISSI SPI Flash memory.	Expanded support for SPI flash devices. See 1.4.2.3 FlashPro 6 Expanded SPI Flash Memory Device Support.
MEMORY_MAP: REPORT: Incomplete Design Summary produced.	Enhanced Libero to generate a Memory map. For details, see 1.3.3 Memory Map Generator.
Don't limit NUM_MULTI_PASSES to 25.	Removed the limit on the number of multipass seeds. Users can set a number higher than 25 in Tcl mode only.
HDL_LANGUAGE: HDL check displays incorrect errors.	Fixed the error in "Check HDL" function. Check HDL no longer displays incorrect errors in this scenario.
PF_PCIE: AXI-Slave (from the fabric side) limit increase.	Fixed the Libero limitation of 2 GB addressing. PolarFire PCIe can now address the full 4 GB address range.
PF_DRI: APBS port on PF_DRI should be configured as a slave interface.	Enhanced PF_DRI IP to support a new APB slave interface.
Crash with msg::Internal Error in m_generic.exe.	Fixed the crash in this release.
SynplifyPro O-2018.09M-SP1-1: Enable signal disables input/output pipeline register packing for wide multipliers.	Fixed this issue in the SynplifyPro bundled with this release. Synplify now packs registers in the Math Block for wide multipliers.
Libero 12.2, Customer VHDL Issue with unconstrained array type error.	Fixed this issue in the SynplifyPro bundled with his release.
Synthesis VHDL Compiler gives error message “choice 0 is out of range” for the slice array assignment statement.	Corrected Synthesis VHDL Compiler to interpret the slice array assignment statement properly without any error.
Synthesis VHDL Compiler gives error message “index out of range” for when-else statement used in the for loop in the RTL.	Corrected Synthesis VHDL Compiler to interpret the when-else statement used in the for loop correctly without any error.
Synthesis VHDL Compiler fails in the concatenation of array if the Array range is defined as subtype natural_downto range <> instead of natural_range<>.	Corrected Synthesis VHDL Compiler to interpret the concatenation of array correctly if the Array range is defined as natural_downto range <>.

4. Known Issues and Limitations

The following table lists known issues and limitations associated with Libero SoC v12.6.

Table 4-1. Known Issues and Limitations Associated with Libero SoC v12.6

Family	Description
Libero	
All families	For designs using CoreAHBLite combined region slot, the SmartDesign Memory Map does not show the correct Range of the combined region slot. The expected range of the combined region slot is n times the size of each slot, where n is the number of slots assigned to the combined region slot. However, in the View Memory Map dialog, the range for the combined region slot is shown as 0x0000_0000 resulting in a DRC.

IGLOO2	For a System Builder design that uses only FDDR out of the DDR/SERDES peripherals, the exported Tcl description file shows the FABRIC_DDR_SETTLING_TIME is not set (the EXTMEM page is not configured).
	Note: There is no issues if only MDDR is used or if FDDR is used in combination with MDDR in a design.
	Workaround: If there's a requirement of a FABRIC_DDR_SETTLING_TIME other than its default value 200, manually update the exported Tcl description file to add the below lines after the Device Features page configuration.
	`# Configuring the Memories page of System Builder component`
	`sb_configure_page -component_name ${sysbld_name} -page_name {EXTMEM} \ -params {FABRIC_DDR_SETTLING_TIME:<non_default_value>}`

PolarFire	Opening two or more views (for example, Hierarchical RTL View and Flattened Post-Compile View) in Netlist Viewer may cause a crash due to memory usage. Avoid opening multiple views for large designs. The DRC check in the I/O Editor does not validate all the constraints set in the tool. You must run Place and Route to validate these constraints.
PolarFire	Using the protocol setting APMemory PSRAM of PF_IOD_OCTAL_DDR causes Place and Route to fail. Workaround: Change to configuration to HyperBus with I0R0_RSTO_N enabled and I0R0_INT_N disabled. The generated core will work properly with APMemory PSRAM.
PolarFire, PolarFire SoC	In Libero, selecting **Disable SNVM** through **Debug Policy** on the **Configure Security Wizard** dialog box does not disable sNVM SmartDebug access. This affects PolarFire family in Libero v12.0 and later, and PolarFire SoC family in Libero v12.5 and later.
N/A	If a module is present in an include file that is coming from a global include path but is not imported into the project, the file is shown as linked file in the Design Hierarchy. If the Global Include Path is broken (path is missing when opening a project), the include file also is shown with a broken link. If the user tries to fix the broken global include path with a new path, the broken file link with the old path still appears. This does not affect functionality, but an extra broken link is shown in the project. Users must remove this link manually when changing the Global Include Path in Project Settings.
Synthesis	

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Family	Description
PolarFire	With Automatic Compile Point ON in Synthesis, some designs with the CoreAXI4Interconnect IP might fail in derived constraints check in Place & Route. Workaround 1: In the **Synthesis -> Configure Options**, turn OFF the Automatic Compile Point and then run Synthesis. Workaround 2: Use get_pins instead of get_nets for the following constraint in <top_level>_derived_constraints.sdc file. `set_false_path -through [ get_pins { AXI4_Interconnect_0/ ARESETN* } ]`
RTG4 and PolarFire	The ECC inference has been deprecated from SynplifyPro for RTG4 and PolarFire families. All references to RAM Inference in ECC mode are removed from SynplifyPro documentation from Libero 12.5 onwards. Replace any inferred ECC memory in your design for all IP cores with modules generated by the respective LSRAM Configurators.
Timing/Power	
PolarFire	The datasheet has slight variations of Max Frequency that software does not represent. In particular, the following two modes have a slightly lower Max Frequency: • 18 × 19 multiplier pre-adder ROM mode • Complex 18 × 19 multiplication The variations are small and on the high-end of the chip frequencies (between 455 and 470MHz at dash-one).
PolarFire	Starting with Libero SoC v12.4, SmartTime stopped propagating clocks when a generated clock is reached. For example, in a design, the clocks are clk1 --> gen1 --> gen2. If gen2 is specified using gen1 as master, there is no issue. If gen2 is specified using clk1 as master, however, the generation fails as clk1 never reaches gen2 (it is stopped by gen1). Workaround: Specify the second generated clock using the first generated clock as master.
PolarFire	In the SmartTime tool, the search option using **Apply filter** is not working.
SmartDebug	
PolarFire, PolarFire SoC	In the SmartDebug when Dual mode PCIe design is considered, the following issues are observed in the PCIe debug feature: • Not showing the PCIe0, only PCIe1 is shown in the UI in the case of dual PCIe designs that have PCI0 and PCIe1 controllers. • LTSSM state is shown only for the PCIe1 design but not for the PCIe0, when PCIe0 Lane is selected, LTSSM state is shown for the PCIe1. • Data Rate, Link Width, and all are shown only for PCIe1, but not for PCI0.
Programming	
PolarFire SoC	For PolarFire SoC Libero designs that contain eNVM, running VERIFY_DIGEST after programming device will fail with "eNVM digest verification: FAIL". Workaround: Deselect procedure 'DO_ENABLE_ENVM' in VERIFY_DIGEST action.
PolarFire SoC	For PolarFire SoC Libero designs that generate/export eNVM only bitstream, the generated bitstream file/job will include ERASE action which is not applicable and does nothing. Affected releases are Libero SoC v12.4 and later. **Note:** For Libero SoC v12.6, this issue applies for the eNVM only case + no eNVM sanitization option.

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Family	**Description**
PolarFire SoC	For Libero designs with sNVM clients configured, no custom user security options selected, and have the program designed on device, modifying sNVM client content and sNVM client Fabric/MSS read/write permissions and run VERIFY action fails with the message "Failed to verify Security" instead of "Failed to verify SNVM".
PolarFire SoC	This release supports only the following Micron SPI Flash memory devices: • Using FlashPro5: MT25QL01G only • Using FlashPro6: all members of N25Q and MT25Q device families **Note:** Contact Microchip Technical Support about support for Flash memory devices from other vendors and device families using FlashPro6.
PolarFire, PolarFire SoC	Although sNVM / eNVM are being sanitized when enabled since the action is part of the bitstream, FP6 does not report a "Sanitizing sNVM..." or "Sanitizing eNVM..." message during erase operations in the ppd flow.
SmartFusion2, IGLOO2	Device Info log displays wrong CheckSum and Design name during SPI Slave programming.
Installation and System Limitations	
N/A	FlashPro6 Driver Re-installation Reports Error Message Customers with FlashPro6 drivers previously installed on their system may see the following message at the end of the installation: `The installation of Program Debug Tool v12.6 is finished, but some errors occurred during the install. Please see the installation log for details.` Resolution: Uninstall existing FlashPro6 drivers and restart the system before installing Libero SoC v12.6. If the software is already installed, ignore the above message if installation logs do not report any errors.
N/A	Linux Package Required If the installer does not boot in graphical mode, additional X window system libraries might be required. For RHEL/CentOS, the following system package is recommended: `$ sudo yum install -y libXau libX11 libXi libxcb libXext libXtst libXrender`
N/A	Antivirus Software Interaction Many antivirus and Host-based Intrusion Prevention System (HIPS) tools flag executables and prevent them from running. To avoid this problem, modify your security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance. Many users run Libero SoC PolarFire successfully with no modification to their antivirus software. Microchip is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC, ModelSim ME and/or Synplify Pro ME may or may not be affected. All public releases of Libero software are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, the Microchip software development and testing environment is also protected by antivirus tools and other security measures.

5. System Requirements

The Libero SoC v12.6 release has the following system requirements.

5.1 Supported 64-bit Operating Systems

- Windows 7 or Windows 10 OS
- RHEL 6.6-6.11 and RHEL 7.2-7.6
- CentOS 6.6-6.11 and CentOS 7.2-7.6
- OpenSUSE Leap 42.3 (SLES 12.3 equivalent)
- Ubuntu 18.04 (Synopsys and Mentor do not directly support the Ubuntu platform. FlashPro5 programmer is not supported with Ubuntu.)

Note: Setup instructions for using Libero SoC v12.6 on Red Hat Enterprise Linux OS, CentOS, or Ubuntu are available in the *UG0710 Libero SoC Linux Environment Setup User Guide*. As noted in that document, installation now includes running a shell script (`bin/check_linux_req.sh`) to confirm the presence of all required runtime packages.

5.2 Random-Access Memory (RAM) Requirements

Minimum of 16 GB RAM

6. Download Libero SoC v12.6 Software

The following are available for download:

- Libero SoC v12.6 for Linux
- Libero SoC v12.6 for Windows
- MegaVault (Linux)
- MegaVault (Windows)
- Program & Debug (Linux)
- Program & Debug (Windows)

Note: Windows installations require administrative privileges.
After a successful installation, clicking **Help** > **About Libero** shows release number v12.6.

7. Documents Updated in this Release

The following documents have been updated for the 12.6 release.

- Libero SoC Linux Environment Setup User Guide
- Libero SoC v12.6 Design Flow User Guide for PolarFire
- Libero SoC v12.6 Design Flow User Guide for RTG4, SmartFusion2, and IGLOO2
- FCCC with Enhanced PLL Calibration Configuration User Guide for RTG4
- Libero SoC v12.6 Tcl Commands Reference Guide for SmartFusion2, IGLOO2, and RTG4
- Libero SoC v12.6 Tcl Commands Reference Guide for PolarFire
- I/O Editor User Guide for Libero SoC v12.6 for all the families
- SmartPower v12.6 User Guide for all the families
- FlashPro Express v12.6 User Guide for all the families
- SmartDebug v12.6 User Guide for SmartFusion2, IGLOO2, and RTG4 04/2020
- SmartDebug v12.6 User Guide for PolarFire

8. Appendix A. RTG4 SPLL and FPLL Calibration and Workaround

Previously, SPLL (SERDES PCIe and XAUI) and FPLL (FDDR) lost lock during temperature ramp as described in CN19009 and CN19009A. To resolve this issue, a new CoreABC sequence has been developed in Libero SoC v12.4 that includes an SPLL/FPLL workaround and is available in all later Libero releases. The new sequence requires design changes to the initialization logic (CoreABC configuration and connections) in some cases described in the following sections.

9. Appendix B: New Device Support Matrices

The following sections provide matrices for new PolarFire SoC, PolarFire, and RT PolarFire devices.

9.1 PolarFire SoC New Device Support Matrices

The following tables list the licensing and device/package combinations for PolarFire SoC devices.

Table 9-1. Licensing, Timing/Power, and Programming Combinations for MPFS250TS_ES

Device	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
MPFS250TS_ES	MPFS250TS_ES-FCVG484E	Yes	—	—	Yes	Preliminary	Yes
	MPFS250TS_ES-FCG1152E	Yes	—	—	Yes	Preliminary	Yes
	MPFS250TS_ES-1FCVG484E	Yes	—	—	Yes	Preliminary	Yes
	MPFS250TS_ES-1FCG1152E	Yes	—	—	Yes	Preliminary	Yes
	MPFS250TS_ES-FCVG784_EvalE	Yes	—	—	Yes	Preliminary	Yes
	MPFS250TS_ES-1FCVG784_EvalE	Yes	—	—	Yes	Preliminary	Yes
	MPFS250TS_ES-FCSG536_EvalE	Yes	—	—	Yes	Preliminary	Yes
	MPFS250TS_ES-1FCSG536_EvalE	Yes	—	—	Yes	Preliminary	Yes

Table 9-2. PolarFire SoC Licensing, Timing/Power, and Programming Combinations Based on Speed Grade and Temperature

(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
T, STD, EXT	MPFS025T-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCSG536_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCSG536_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No
TL, STD, EXT	MPFS025TL-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCSG536_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCSG536E	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No

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(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
T, -1, EXT	MPFS025T-1FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCSG536_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCSG536_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No
T, STD, IND	MPFS025T-FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCSG536_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCVG784_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCSG536_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCVG784_EvalI	Yes	Yes	Yes	Yes	Advance	No

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(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
TL, STD, IND	MPFS025TL-FCVG484_Evall	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCSG536_Evall	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCVG484_Evall	Yes	Yes	Yes	Yes	Advance	No
		Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCVG784_Evall	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCSG536_Evall	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCVG484_Evall	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCVG784_Evall	Yes	Yes	Yes	Yes	Advance	No
T, -1, IND	MPFS025T-1FCVG484_Evall	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCSG536_Evall	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCVG484_Evall	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCVG784_Evall	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCSG536_Evall	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCVG484_Evall	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCVG784_Evall	Yes	Yes	Yes	Yes	Advance	No

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(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
TLS, STD, IND	MPFS025TLS-FCVG484_EvalI	Yes	—	—	Yes	Advance	No
	MPFS095TLS-FCSG536_EvalI	Yes	—	—	Yes	Advance	No
	MPFS095TLS-FCVG484_EvalI	Yes	—	—	Yes	Advance	No
	MPFS095TLS-FCVG784_EvalI	Yes	—	—	Yes	Advance	No
	MPFS160TLS-FCSG536_EvalI	Yes	—	—	Yes	Advance	No
	MPFS160TLS-FCVG484_EvalI	Yes	—	—	Yes	Advance	No
	MPFS160TLS-FCVG784_EvalI	Yes	—	—	Yes	Advance	No
	MPFS250TLS-FCSG536_EvalI	Yes	—	—	Yes	Preliminary	No
	MPFS250TLS-FCVG484I	Yes	—	—	Yes	Preliminary	No
	MPFS250TLS-FCVG784_EvalI	Yes	—	—	Yes	Preliminary	No
	MPFS250TLS-FCG1152I	Yes	—	—	Yes	Preliminary	No
	MPFS460TLS-FCG1152_EvalI	Yes	—	—	Yes	Advance	No

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(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
TS, STD, IND	MPFS025TS-FCVG484_EvalI	Yes	—	—	Yes	Advance	No
	MPFS095TS-FCSG536_EvalI	Yes	—	—	Yes	Advance	No
	MPFS095TS-FCVG484_EvalI	Yes	—	—	Yes	Advance	No
	MPFS095TS-FCVG784_EvalI	Yes	—	—	Yes	Advance	No
	MPFS160TS-FCSG536_EvalI	Yes	—	—	Yes	Advance	No
	MPFS160TS-FCVG484_EvalI	Yes	—	—	Yes	Advance	No
	MPFS160TS-FCVG784_EvalI	Yes	—	—	Yes	Advance	No
	MPFS250TS-FCSG536_EvalI	Yes	—	—	Yes	Preliminary	No
	MPFS250TS-FCVG484I	Yes	—	—	Yes	Preliminary	No
	MPFS250TS-FCVG784_EvalI	Yes	—	—	Yes	Preliminary	No
	MPFS250TS-FCG1152I	Yes	—	—	Yes	Preliminary	No
	MPFS460TS-FCG1152_EvalI	Yes	—	—	Yes	Advance	No

.....continued

(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
TS, -1, IND	MPFS025TS-1FCVG484_EvalI	Yes	—	—	Yes	Advance	No
	MPFS095TS-1FCSG536_EvalI	Yes	—	—	Yes	Advance	No
	MPFS095TS-1FCVG484_EvalI	Yes	—	—	Yes	Advance	No
	MPFS095TS-1FCVG784_EvalI	Yes	—	—	Yes	Advance	No
	MPFS160TS-1FCSG536_EvalI	Yes	—	—	Yes	Advance	No
	MPFS160TS-1FCVG484_EvalI	Yes	—	—	Yes	Advance	No
	MPFS160TS-1FCVG784_EvalI	Yes	—	—	Yes	Advance	No
	MPFS250TS-1FCSG536_EvalI	Yes	—	—	Yes	Preliminary	No
	MPFS250TS-1FCVG484I	Yes	—	—	Yes	Preliminary	No
	MPFS250TS-1FCVG784_EvalI	Yes	—	—	Yes	Preliminary	No
	MPFS250TS-1FCG1152I	Yes	—	—	Yes	Preliminary	No
	MPFS460TS-1FCG1152_EvalI	Yes	—	—	Yes	Advance	No

Libero SoC v12.6 introduces programming support, and Advance/Preliminary timing and power support for PolarFire SoC devices.

Licensing and device/package combinations are detailed in the following table.

Table 9-3. Licensing and Device Combination Details

Device	Part Number	Libero Licensing				Libero Timing/ Power	Programming
		Eval	Silver	Gold	Platinum		
MPFS250TS_ES	MPFS250TS_ES-FCVG484E	Yes			Yes	Preliminary	Yes
	MPFS250TS_ES-FCG1152E	Yes			Yes	Preliminary	Yes
	MPFS250TS_ES-1FCVG484E	Yes			Yes	Preliminary	Yes
	MPFS250TS_ES-1FCG1152E	Yes			Yes	Preliminary	Yes
	MPFS250TS_ES-FCVG784_EvalE	Yes			Yes	Preliminary	Yes
	MPFS250TS_ES-1FCVG784_EvalE	Yes			Yes	Preliminary	Yes
	MPFS250TS_ES-FCSG536_EvalE	Yes			Yes	Preliminary	Yes
	MPFS250TS_ES-1FCSG536_EvalE	Yes			Yes	Preliminary	Yes

Table 9-4. Licensing and Package Combination Details

(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/ Power	Programming
		Eval	Silver	Gold	Platinum		
T, STD, EXT	MPFS025T-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCSG536_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCSG536_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No
TL, STD, EXT	MPFS025TL-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCSG536_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCSG536E	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No

.....continued

(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/ Power	Programming
		Eval	Silver	Gold	Platinum		
T, -1, EXT	MPFS025T-1FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCSG536_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCSG536_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCVG484_EvalE	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCVG784_EvalE	Yes	Yes	Yes	Yes	Advance	No
T, STD, IND	MPFS025T-FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCSG536_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-FCVG784_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCSG536_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-FCVG784_EvalI	Yes	Yes	Yes	Yes	Advance	No
TL, STD, IND	MPFS025TL-FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCSG536_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095TL-FCVG784_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCSG536_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160TL-FCVG784_EvalI	Yes	Yes	Yes	Yes	Advance	No
T, -1, IND	MPFS025T-1FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCSG536_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS095T-1FCVG784_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCSG536_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCVG484_EvalI	Yes	Yes	Yes	Yes	Advance	No
	MPFS160T-1FCVG784_EvalI	Yes	Yes	Yes	Yes	Advance	No

.....continued

(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/ Power	Programming
		Eval	Silver	Gold	Platinum		
TLS, STD, IND	MPFS025TLS-FCVG484_EvalI	Yes			Yes	Advance	No
	MPFS095TLS-FCSG536_EvalI	Yes			Yes	Advance	No
	MPFS095TLS-FCVG484_EvalI	Yes			Yes	Advance	No
	MPFS095TLS-FCVG784_EvalI	Yes			Yes	Advance	No
	MPFS160TLS-FCSG536_EvalI	Yes			Yes	Advance	No
	MPFS160TLS-FCVG484_EvalI	Yes			Yes	Advance	No
	MPFS160TLS-FCVG784_EvalI	Yes			Yes	Advance	No
	MPFS250TLS-FCSG536_EvalI	Yes			Yes	Preliminary	No
	MPFS250TLS-FCVG484I	Yes			Yes	Preliminary	No
	MPFS250TLS-FCVG784_EvalI	Yes			Yes	Preliminary	No
	MPFS250TLS-FCG1152I	Yes			Yes	Preliminary	No
	MPFS460TLS-FCG1152_EvalI	Yes			Yes	Advance	No
TS, STD, IND	MPFS025TS-FCVG484_EvalI	Yes			Yes	Preliminary	No
	MPFS095TS-FCSG536_EvalI	Yes			Yes	Advance	No
	MPFS095TS-FCVG484_EvalI	Yes			Yes	Advance	No
	MPFS095TS-FCVG784_EvalI	Yes			Yes	Advance	No
	MPFS160TS-FCSG536_EvalI	Yes			Yes	Advance	No
	MPFS160TS-FCVG484_EvalI	Yes			Yes	Advance	No
	MPFS160TS-FCVG784_EvalI	Yes			Yes	Advance	No
	MPFS250TS-FCSG536_EvalI	Yes			Yes	Preliminary	No
	MPFS250TS-FCVG484I	Yes			Yes	Preliminary	No
	MPFS250TS-FCVG784_EvalI	Yes			Yes	Preliminary	No
	MPFS250TS-FCG1152I	Yes			Yes	Preliminary	No
	MPFS460TS-FCG1152_EvalI	Yes			Yes	Advance	No

.....continued

(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/ Power	Programming
		Eval	Silver	Gold	Platinum		
TS, -1, IND	MPFS025TS-1FCVG484_EvalI	Yes			Yes	Advance	No
	MPFS095TS-1FCSG536_EvalI	Yes			Yes	Advance	No
	MPFS095TS-1FCVG484_EvalI	Yes			Yes	Advance	No
	MPFS095TS-1FCVG784_EvalI	Yes			Yes	Advance	No
	MPFS160TS-1FCSG536_EvalI	Yes			Yes	Advance	No
	MPFS160TS-1FCVG484_EvalI	Yes			Yes	Advance	No
	MPFS160TS-1FCVG784_EvalI	Yes			Yes	Advance	No
	MPFS250TS-1FCSG536_EvalI	Yes			Yes	Preliminary	No
	MPFS250TS-1FCVG484I	Yes			Yes	Preliminary	No
	MPFS250TS-1FCVG784_EvalI	Yes			Yes	Preliminary	No
	MPFS250TS-1FCG1152I	Yes			Yes	Preliminary	No
	MPFS460TS-1FCG1152_EvalI	Yes			Yes	Advance	No

9.2 PolarFire New Production Timing Support Matrix

Production timing support has been added for the PolarFire devices for 1.0 V and 1.05 V in the following table.

Table 9-5. PolarFire Devices That Have Production Timing Support

(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
T, STD, Tgrade2	MPF100T-FCG484T2 MPF100T-FCSG325T2 MPF100T-FCVG484T2 MPF200T-FCG484T2 MPF200T-FCSG325T2 MPF200T-FCSG325T2 MPF200T-FCVG484T2 MPF300T-FCSG536T2 MPF300T-FCVG484T2	Yes			Yes	Production	Yes

.....continued

(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
T, -1, Tgrade2	MPF100T-1FCG484T2 MPF100T-1FCSG325T2 MPF100T-1FCVG484T2 MPF200T-1FCG484T2 MPF200T-1FCSG325T2 MPF200T-1FCSG536T2 MPF200T-1FCVG484T2 MPF300T-1FCSG536T2 MPF300T-1FCVG484T2	Yes			Yes	Production	Yes

9.3 RT PolarFire Licensing and Device/Package Combination Matrix

The following table lists the licensing and device/package combinations for RT PolarFire.

Table 9-6. RT PolarFire Licensing and Device/Package Combinations

(T/TL/TS/TLS), Speed Grade, Temperature	Part Number	Libero Licensing				Libero Timing/Power	Programming
		Eval	Silver	Gold	Platinum		
T, STD, MIL	RTPF500T-CG1509M	Yes	—	—	Yes	Advance	Yes
T, -1, MIL	RTPF500T-1CG1509M	Yes	—	—	Yes	Advance	Yes
TS, STD, MIL	RTPF500TS-CG1509M	Yes	—	—	Yes	Advance	Yes
TS, -1, MIL	RTPF500TS-1CG1509M	Yes	—	—	Yes	Advance	Yes
TL, STD, MIL	RTPF500TL-CG1509M	Yes	—	—	Yes	Advance	Yes
TLS, STD, MIL	RTPF500TLS-CG1509M	Yes	—	—	Yes	Advance	Yes

10. Revision History

Revision	Date	Description
G	4/21/2021	Made the following edits: • Updated the 5.1 Supported 64-bit Operating Systems to show CentOS 6.6-6.11 and CentOS 7.2-7.6. • In 4. Known Issues and Limitations, added the issue about ECC inference being deprecated from SynplifyPro for RTG4 and PolarFire families.
F	4/14/2021	Editorial updates only. No technical content updates.
E	3/25/2021	In 3. Resolved Issues, added a customer-reported defect about Chip Planner crashing after regions were renamed.
D	2/25/2021	In 4. Known Issues and Limitations, added known issues that: • ECALIB configurator will not open in Libero SoC 12.5 and Libero SoC 12.5SP1 when DRI mode is enabled. • ECALIB configurator will not open in Libero SoC 12.5 and Libero SoC 12.5 SP1 when DRI mode is disabled and GL0 is not used in the design.
C	01/2021	In 4. Known Issues and Limitations, added a known issue that selecting **Disable SNVM** through **Debug Policy** on the **Configure Security Wizard** dialog box does not disable sNVM SmartDebug access.
B	12/2020	Made the following edits: • On front page, added a link to the V2.0 MSS Configurator (Pre production) Release Notes. • Moved new device support matrices to Appendix B.
A	11/2020	Initial Revision

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