RTG4 SERDES Testing Report

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SUMMARY

The report presents the testing results of Heavy Ion induced single event effects on the SERDES blocks in Microsemi's RTG4 FPGA.

SERDES Lane data errors were observed for both Lane 0 and Lane 1 for RX/TX and RX modes only. No data errors were observed for the TX mode for both lanes, since the TX circuit is smaller in area compared to RX circuit.

I. TEST OBJECTIVE

The single event effects (SEE) of SERDES blocks in RTG4 are investigated and measured by heavy-ion irradiation. The results are summarized as Weibull distributions and parameters that will be used for error-rate calculations in space environments.

II. DEVICE UNDER TEST

The test was performed at the Berkeley National Laboratory. Table 1 lists facility and Device Under Test (DUT) parameters.

Table 1: Heavy Ion Testing Parameters

Condition	Setting
Beam Energy	10 MeV/Nucleon
Temperature	Room Temperature
Bias	1.2V, 2.5V & 3.3V
Sample Preparation	Reworked RTG4 evaluation board with a back grinded REVC RTG4 unit (production version). DUT #8566 thickness is 39 µm.

III. TEST METHODS

The test generally follows the guidelines of two SEE testing standards: ASTM standard F1192M-95, "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation on Semiconductor Devices," and JEDEC standard JESD57, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation."

1. Irradiation

The test was performed at the Berkeley National Laboratory. Table 2 lists ions and their respective LETs.

Table 2: Ions and LETs

Species & Tilt	LET
O–(0)	2.19
Si–(0)	6.09
V–(0)	14.59
Cu–(0)	21.17
Kr–(0)	30.86

2. DUT Design

The SERDES test was performed in 3 different configurations:

1) SERDES configured as Receiver/Transmitter (RX/TX) with external loop back
2) SERDES configured as Receiver (RX) only
3) SERDES configured as Transmitter (TX) only

In all three configurations, the whole RTG4 die is exposed to the beam. In the RX/TX mode, only one board is used (the DUT board with RTG4 die exposed to the beam), and the SERDES is sending and receiving data in external loopback. In the RX configuration, we have two boards, a master board (not exposed to the beam) that acts as the transmitter and sends data to the DUT board exposed to the beam with the RTG4 SERDES acting as the receiver. The third configuration is similar to the second configuration but this time the DUT is sending the data (RTG4 SERDES acting as transmitter only) and the master board is receiving the data. Figure 1 shows the RTG4 SERDES FMC/interposer boards connected to the DUT and master boards, the DUT board is shown on the left and the master board is shown on the right. The green cables represent the loopback cables.

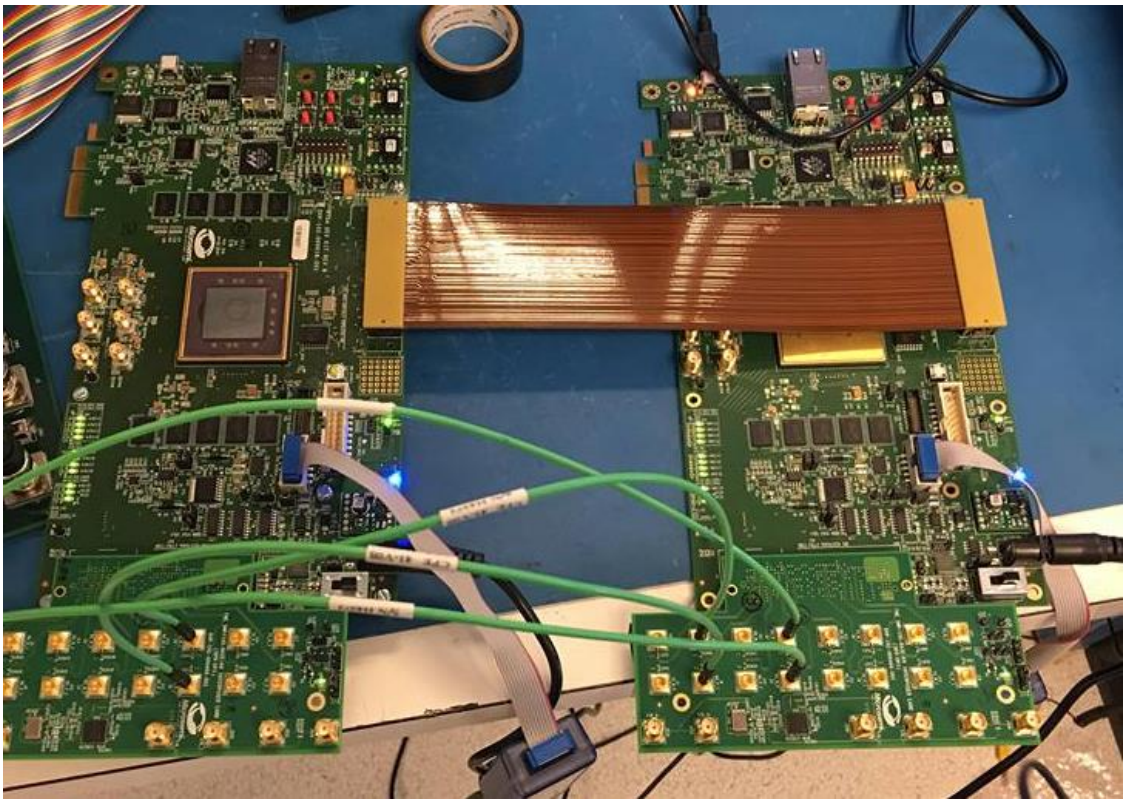

Figure 1: Board setup in TX configuration.

The Demo design was used as the test design (refer to Microchip Demo Guide DG0624). This test design uses an external 50MHz clock (instead of the RTG4 built-in 50-MHz RC Oscillator) and SERDES internal PRBS generator/checker. Previous tests using the built-in RC oscillator and fabric generator/checker did not result in meaningful data. Testing of the RTG4 built-in RC oscillator by itself will be planned.

IV. RESULTS AND DISCUSSIONS

SERDES Lane data errors were observed for both Lane 0 and Lane 1 for RX/TX and RX modes only. No data errors were observed for the TX mode for both lanes because the TX circuit is much smaller in area compared to RX circuit. A large portion of the RX and TX PLL area represents a loop filter capacitor to keep the jitter low, and generally we would not expect a hit to most of that area to cause more than a very slight frequency variation that will migrate the frequency slowly and not be picked up as a TX issue, and may not be seen as an error on the receiving side. For the RX side, it has much more digital logic, thus is more susceptible to errors. Figure 2 shows the cross section per SERDES Lane for all SERDES configurations stated above.

RX PLL and Lock-to-data errors were observed. RX PLL and TX PLL lock signals represent the tolerance of the PLL and only go low if the PLL goes too fast or too slow. Lock-to-data compares the two output clocks of RX PLL and TX PLL: if any of the two output clocks frequency is beyond the allowed frequency band, Lock-to-data would show an error, which is consistent with the results shown in Figure 3. SERDES RX/TX, RX and TX modes were tested and only RX/TX and RX modes showed errors.

When loss of RX PLL lock and Lock-to-data signals occurs, the CoreABC can be used to re-initialize the SERDES registers.

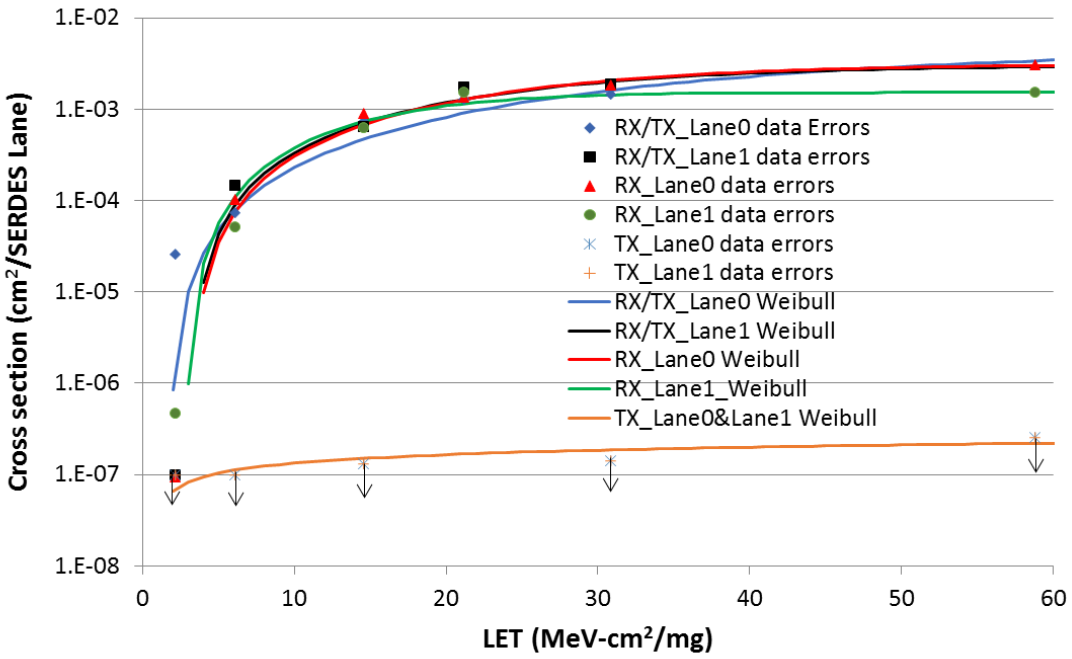

Figure 2: SERDES RX/TX, RX and TX Lane 0 and Lane 1 data cross sections and Weibull fit.

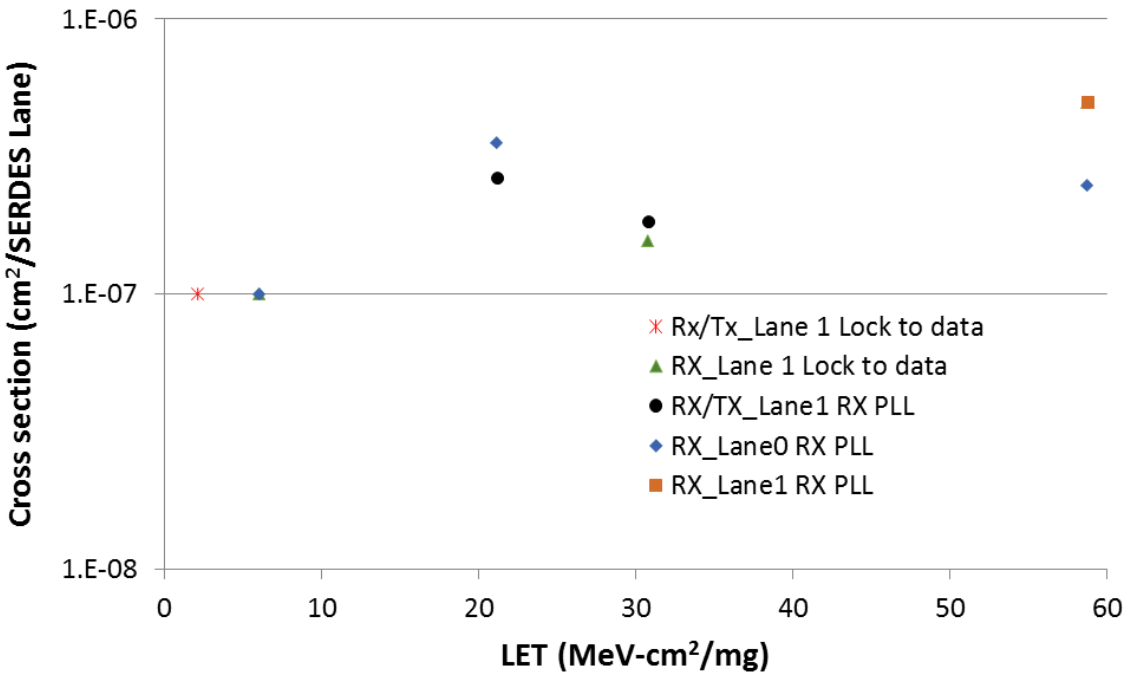

Figure 3: Lock-to-data and RX PLL errors for SERDES RX/TX and RX modes.

Table 3: RX/TX Lane 0 Weibull Parameters

L0	W	S	A0
0.7	47	1.7	4.50E-03

Table 4: RX/TX Lane 1 Weibull Parameters

L0	W	S	A0
2.15	26	1.6	3.00E-03

Table 5: RX Lane 0 Weibull Parameters

L0	W	S	A0
2.12	26	1.7	3.07E-03

Table 6: RX Lane 1 Weibull Parameters

L0	W	S	A0
1.8	15	1.7	1.52E-03

Table 7: TX Lane 0&1 Weibull Parameters

L0	W	S	A0
1.02	93	0.37	3.87E-07

V. ORBITAL UPSET RATE

The Weibull fit parameters in Tables 3 to 7 are used to calculate the orbital upset rates in GEO synchronous orbit at Solar min with 100 mil aluminum shielding.

Table 8: Orbital Upset Rates

Error Mode	GEO Solar Min Orbital Upset Rate
RX/TX Lane 0 data errors	7.75E-3 upset/SERDES Lane-day
RX/TX Lane 1 data errors	8.39E-3 upset/SERDES Lane-day
RX Lane 0 data errors	7.55E-3 upset/SERDES Lane-day
RX Lane 1 data errors	8.56E-3 upset/SERDES Lane-day
TX Lane 0 & Lane 1 data errors	< 9.01E-7 upset/SERDES Lane-day

REVISION HISTORY

Revision 1.0

Revision 1.0 was published in October 2020. It is the first publication of this document.