



a  MICROCHIP company

Total Ionizing Dose Test Report

No. 20T-RT4G150-LG1657-K96W1

November 5, 2020

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I. SUMMARY TABLE

Table. 1. Summary

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO ₂)
2. Power Supply Current	Passed 125 krad(SiO ₂)
3. Input Threshold (VIL/VIH)	Passed 125 krad(SiO ₂)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO ₂)
5. Propagation Delay	Passed 125 krad(SiO ₂) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO ₂)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at <http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports>

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the Automatic Test Equipment (ATE) program. The report summarizes sample pins.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 2 lists the DUT and irradiation parameters.

Table. 2. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	K96W1
Quantity Tested	6
Serial Number (Dose)	03972 (125 krad), 03998 (125 krad), 04002 (125 krad), 04009 (125 krad), 04017 (125 krad), 04037 (125 krad)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO ₂)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

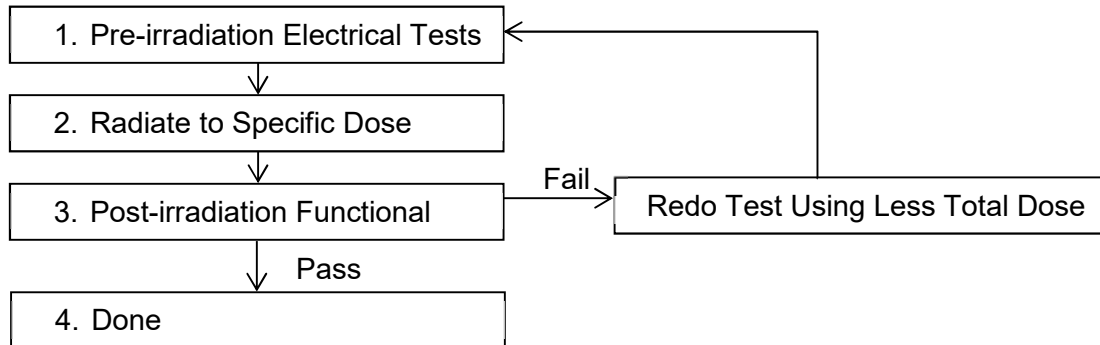


Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 3 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 3. Fabric Functional Coverage

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 μ RAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current I_{DD} , the I/Os power supply currents ($I_{DDI_2.5}/I_{DDI_3.3}$) and the charge pump and PLL power supply current (I_{PP_PLL}) are also monitored during irradiation in real time.

The input logic threshold (V_{IL}/V_{IH}) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (V_{OL}/V_{OH}) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design. LVTTTL and LVCMOS 2.5V standard at different sourcing and sinking currents are reported.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (I_{DD}) is 1.2 V, the I/O bank power supply currents (I_{DDI}) are 2.5 V ($I_{DDI_2.5}$) and 3.3 V ($I_{DDI_3.3}$). The charge pump and PLL power supply current (I_{PP_PLL}) is 3.3 V. Figures 2-25 illustrate the plot of in-flux standby I_{DD} , $I_{DDI_2.5}$, $I_{DDI_3.3}$ and I_{PP_PLL} versus total dose for every DUT. Tables 4-7 summarize the pre-irradiation and post-irradiation total current (static & dynamic) I_{DD} , $I_{DDI_2.5}$, $I_{DDI_3.3}$ and I_{PP_PLL} .

Table. 4. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
03972	125 krad	0.3853	0.4009	4.05
03998	125 krad	0.3844	0.3990	3.80
04002	125 krad	0.4444	0.4610	3.74
04009	125 krad	0.4428	0.4620	4.34
04017	125 krad	0.4100	0.4280	4.39
04037	125 krad	0.4368	0.4498	2.98

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
03972	125 krad	0.0089	0.0107	20.22
03998	125 krad	0.0089	0.0106	19.10
04002	125 krad	0.0096	0.0111	15.63
04009	125 krad	0.0101	0.0120	18.81
04017	125 krad	0.0091	0.0107	17.58
04037	125 krad	0.0091	0.0103	13.19

 Table. 6. Pre-irradiation and Post-irradiation $I_{DDI_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
03972	125 krad	0.0334	0.0362	8.38
03998	125 krad	0.0332	0.0361	8.73
04002	125 krad	0.0334	0.0363	8.68
04009	125 krad	0.0339	0.0367	8.26
04017	125 krad	0.0328	0.0355	8.23
04037	125 krad	0.0333	0.0359	7.81

 Table. 7. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
03972	125 krad	0.0154	0.0166	7.79
03998	125 krad	0.0154	0.0161	4.55
04002	125 krad	0.0153	0.0192	25.49
04009	125 krad	0.0152	0.0186	22.37
04017	125 krad	0.0152	0.0195	28.29
04037	125 krad	0.0152	0.0165	8.55

The following figures (2-25) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

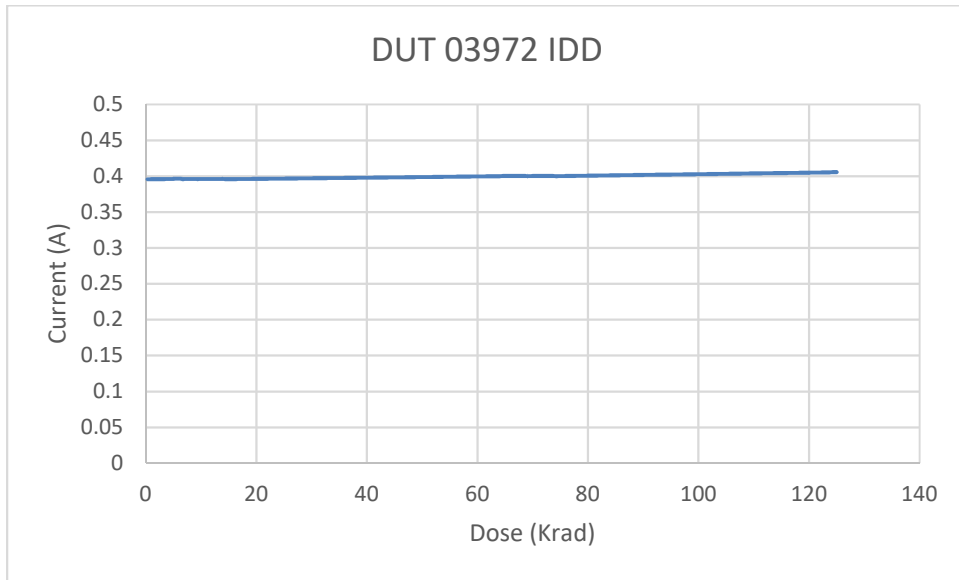


Fig. 2. DUT 3972 core power supply current (I_{DD}) versus TID

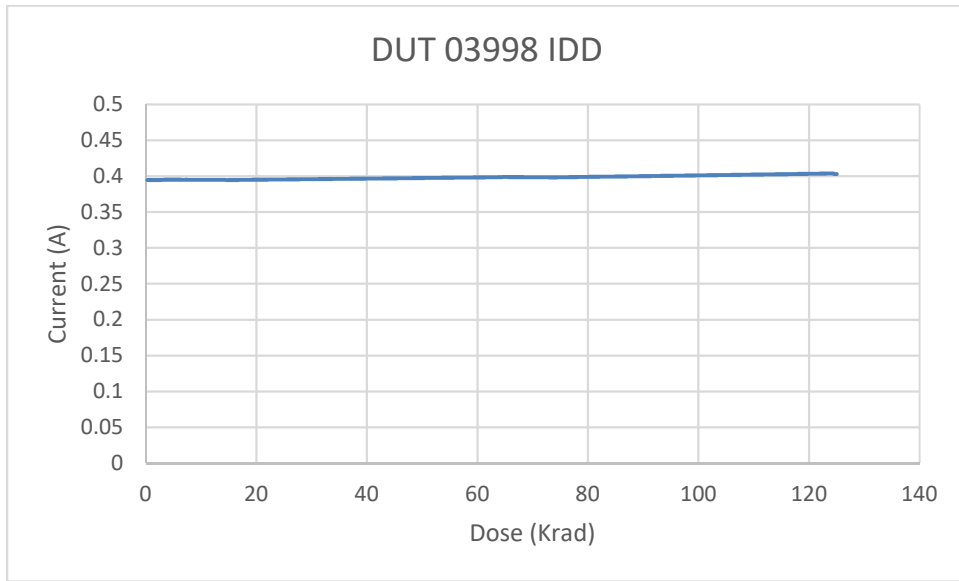


Fig. 3. DUT 3998 core power supply current (I_{DD}) versus TID

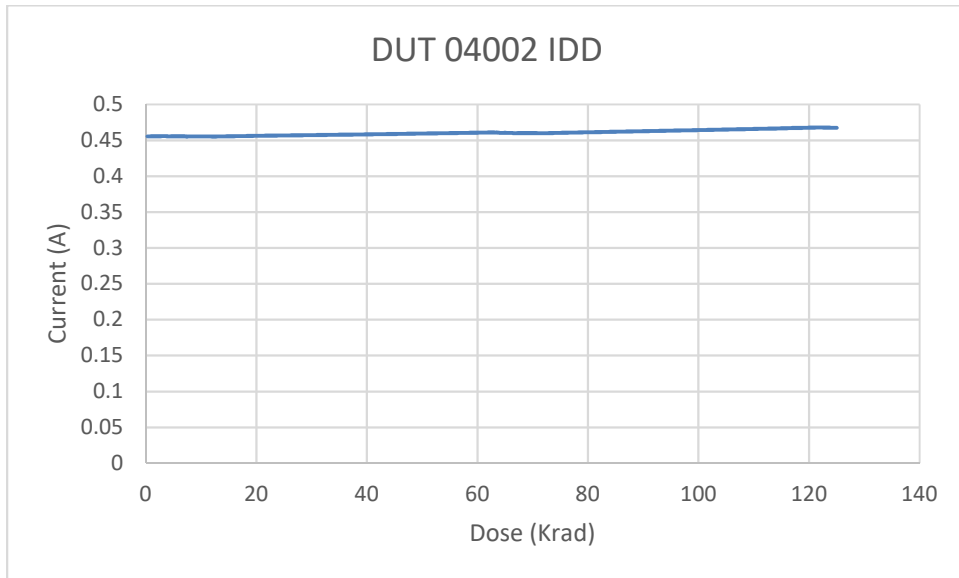


Fig. 4. DUT 4002 core power supply current (I_{DD}) versus TID

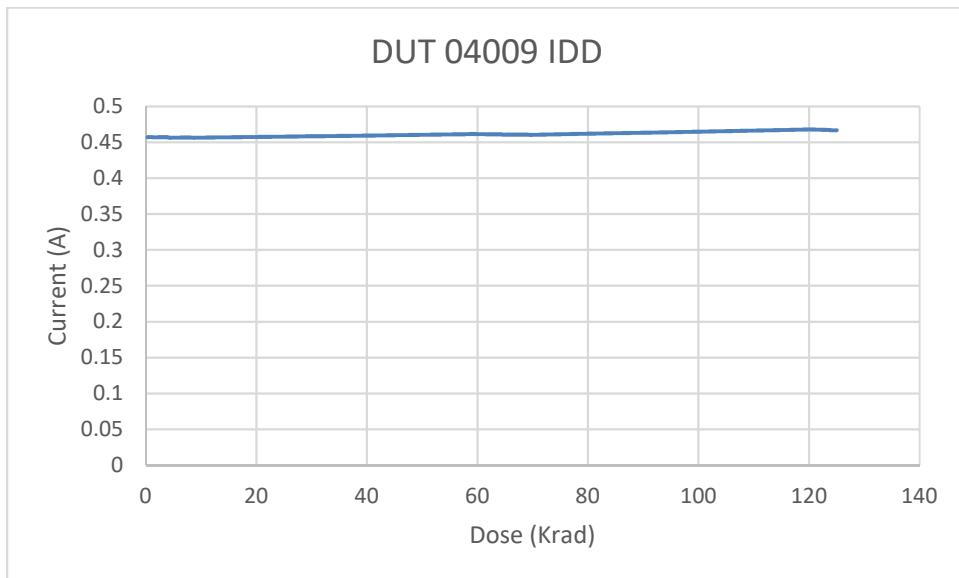


Fig. 5. DUT 4009 core power supply current (I_{DD}) versus TID

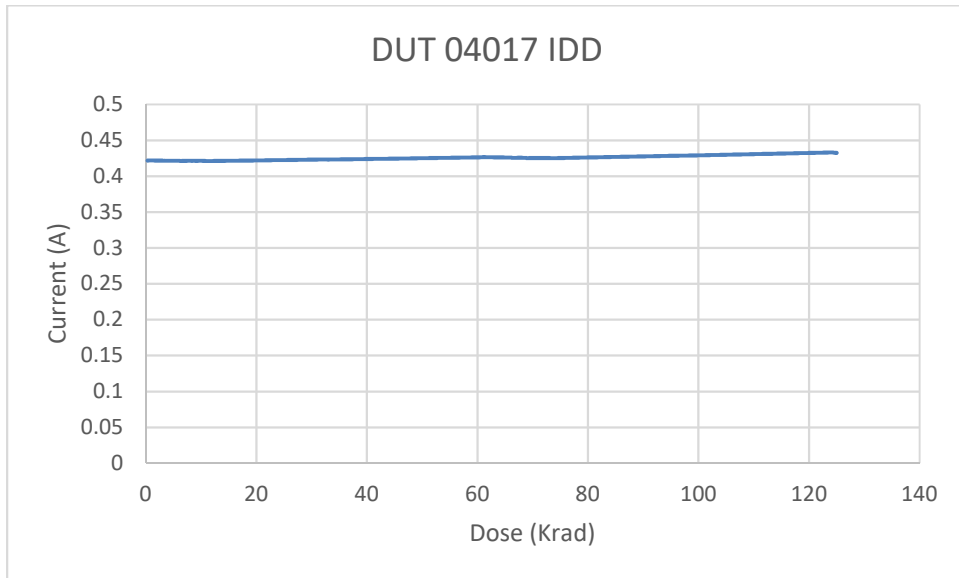


Fig. 6. DUT 4017 core power supply current (I_{DD}) versus TID

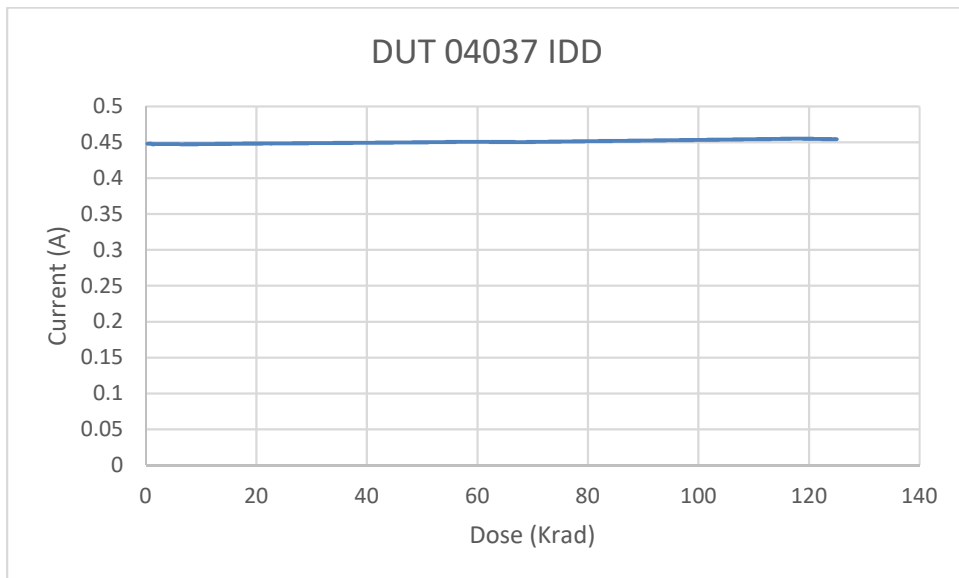


Fig. 7. DUT 4037 core power supply current (I_{DD}) versus TID

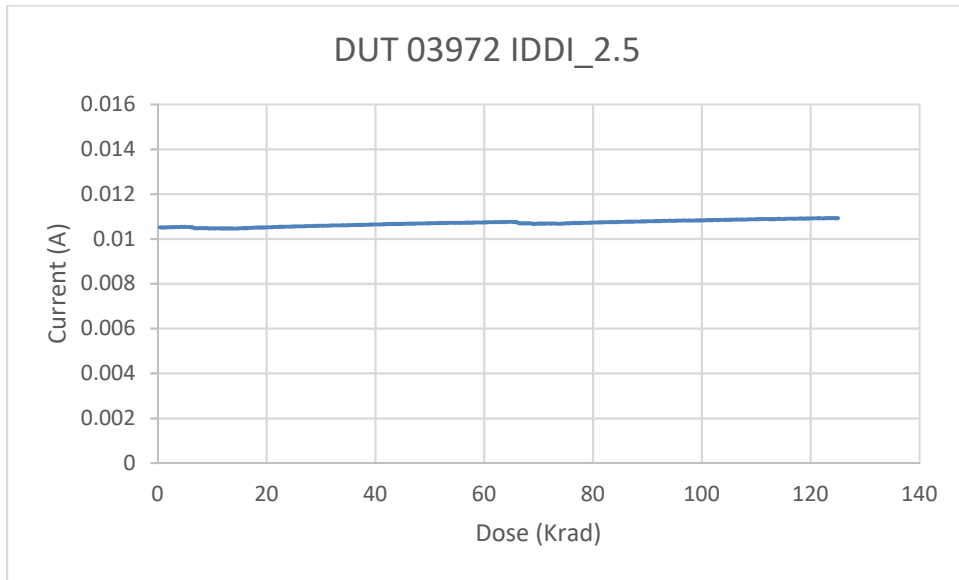


Fig. 8. DUT 3972 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

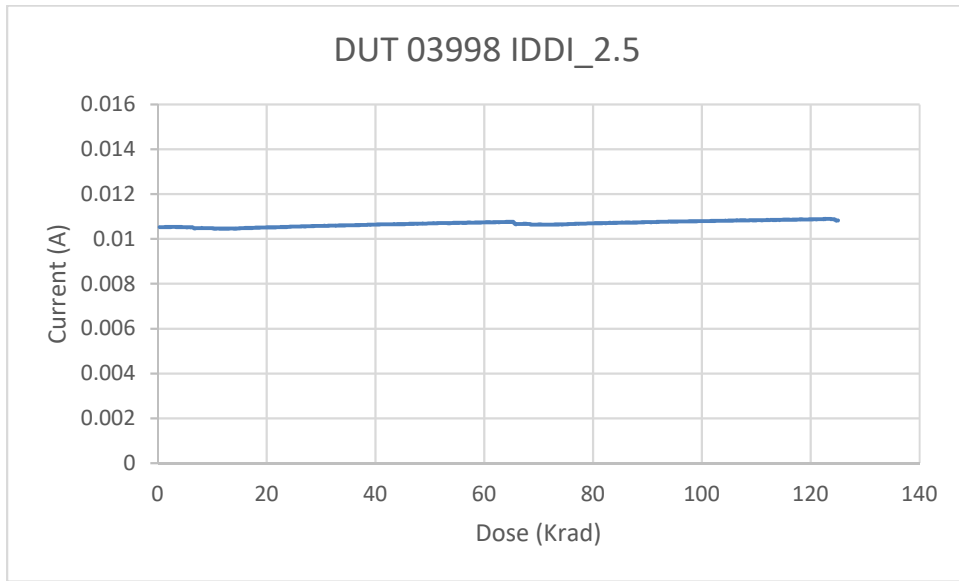


Fig. 9. DUT 3998 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

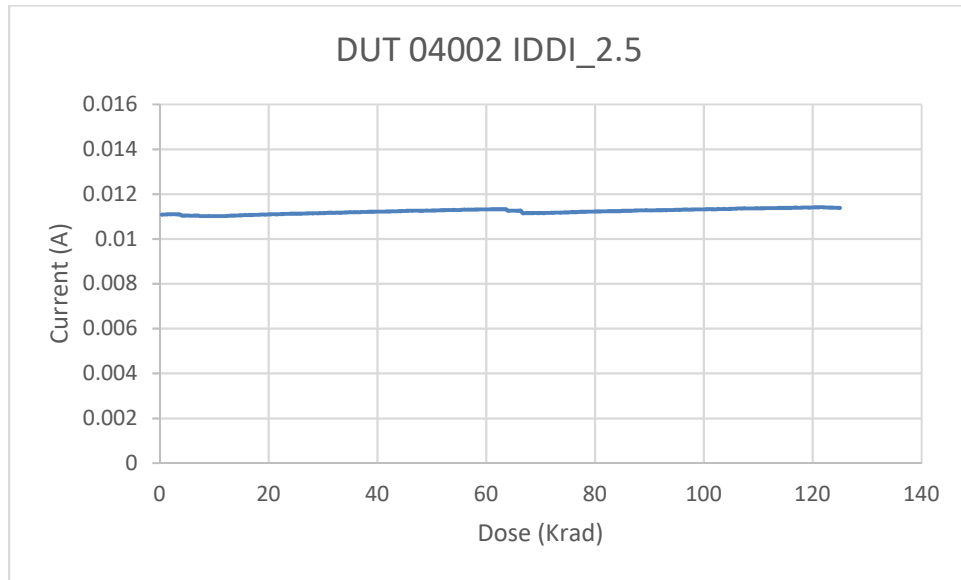


Fig. 10. DUT 4002 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

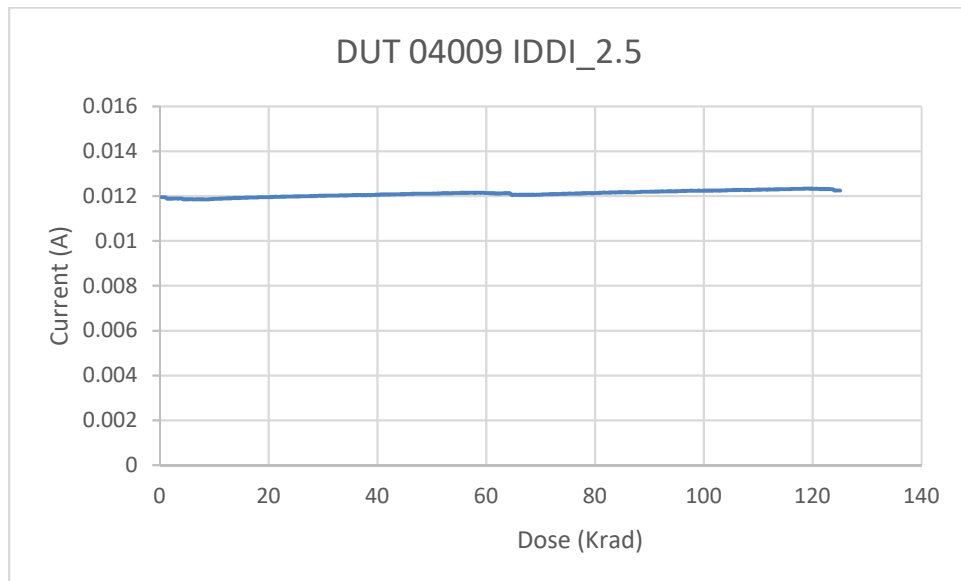


Fig. 11. DUT 4009 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

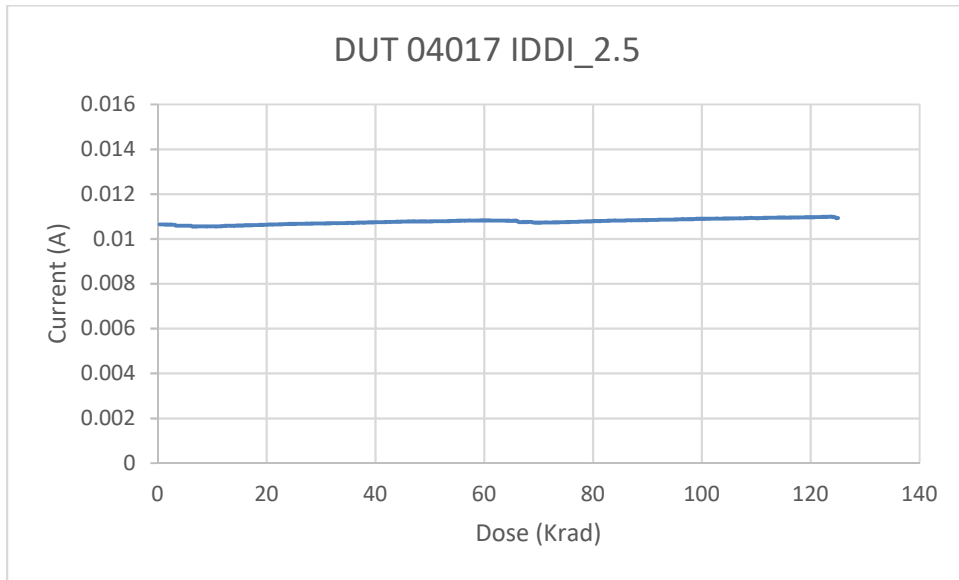


Fig. 12. DUT 4017 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

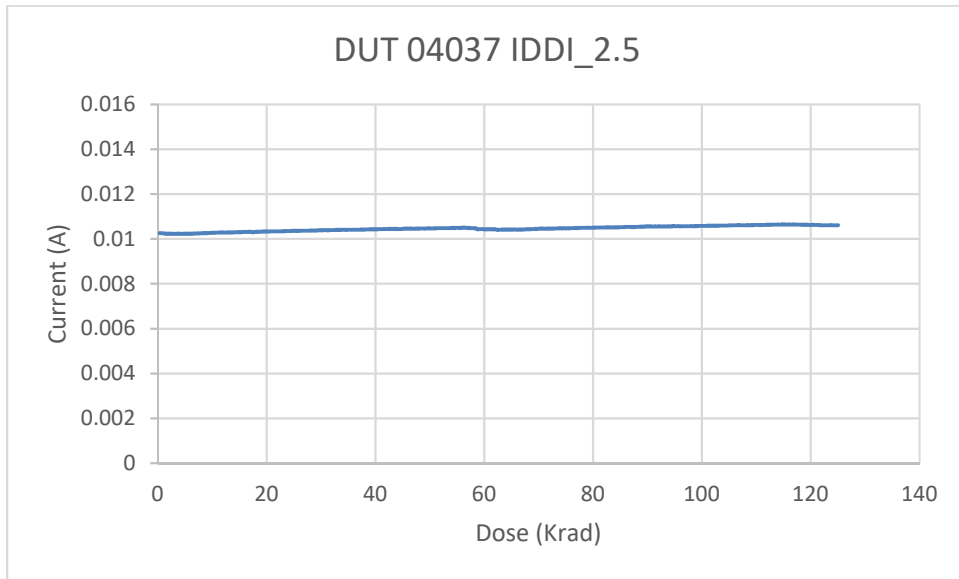


Fig. 13. DUT 4037 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

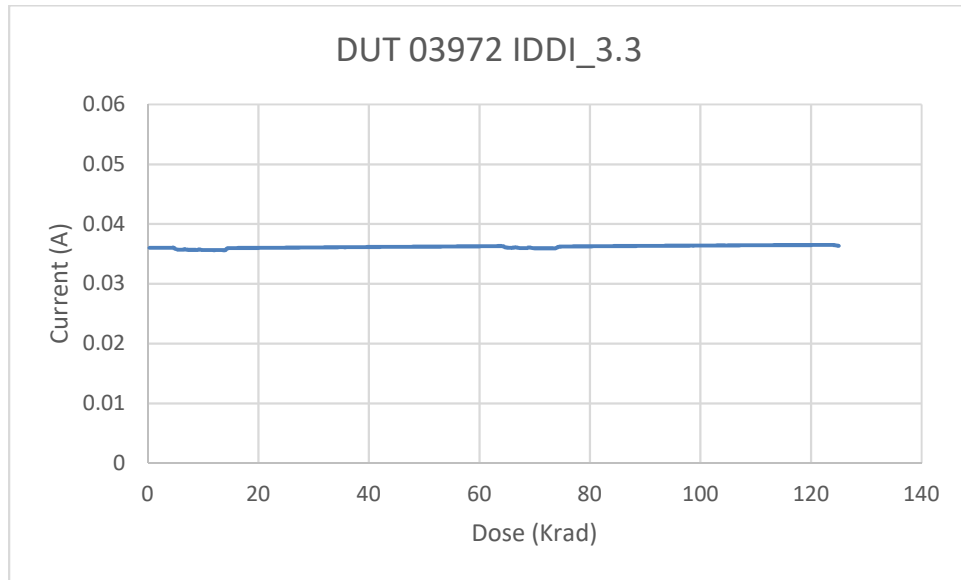


Fig. 14. DUT 3972 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

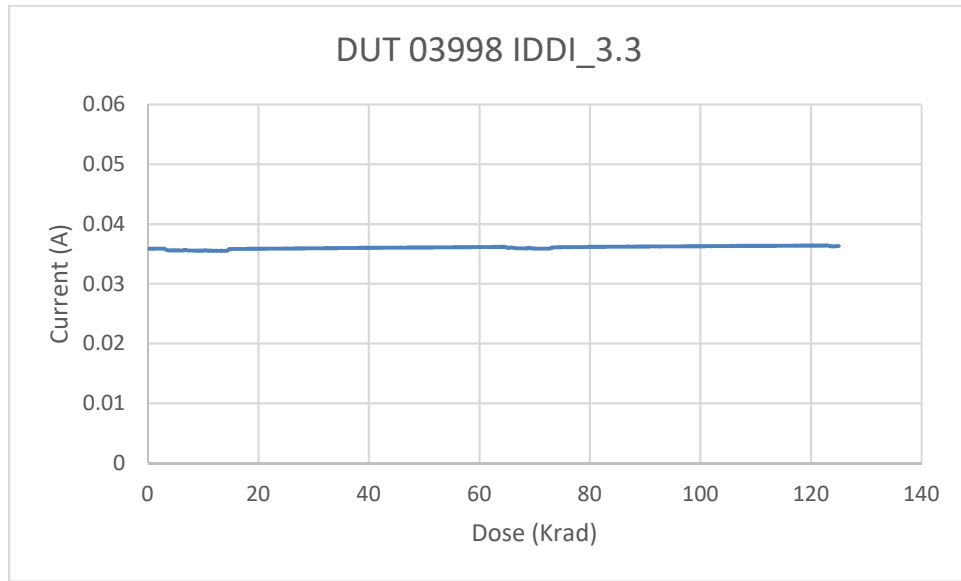


Fig. 15. DUT 3998 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

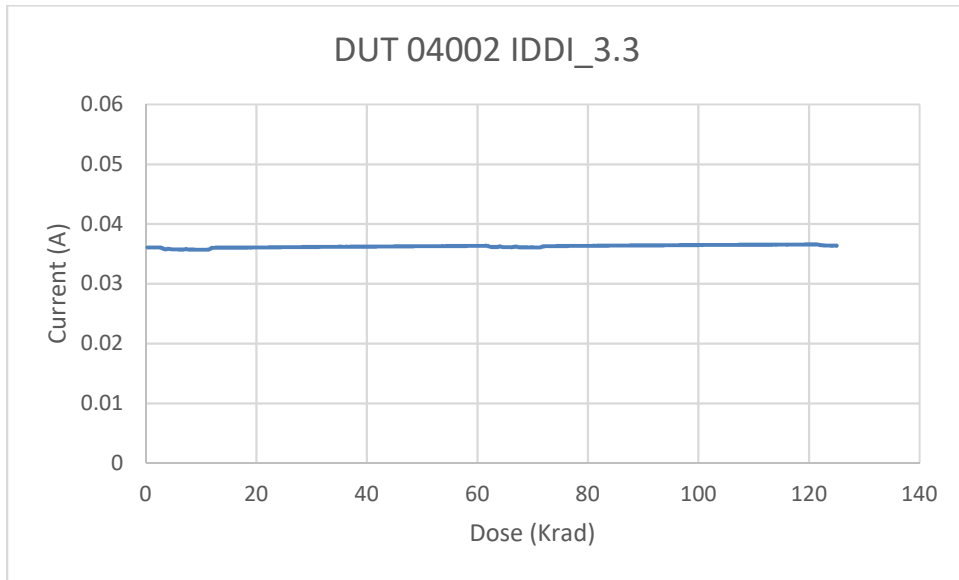


Fig. 16. DUT 4002 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

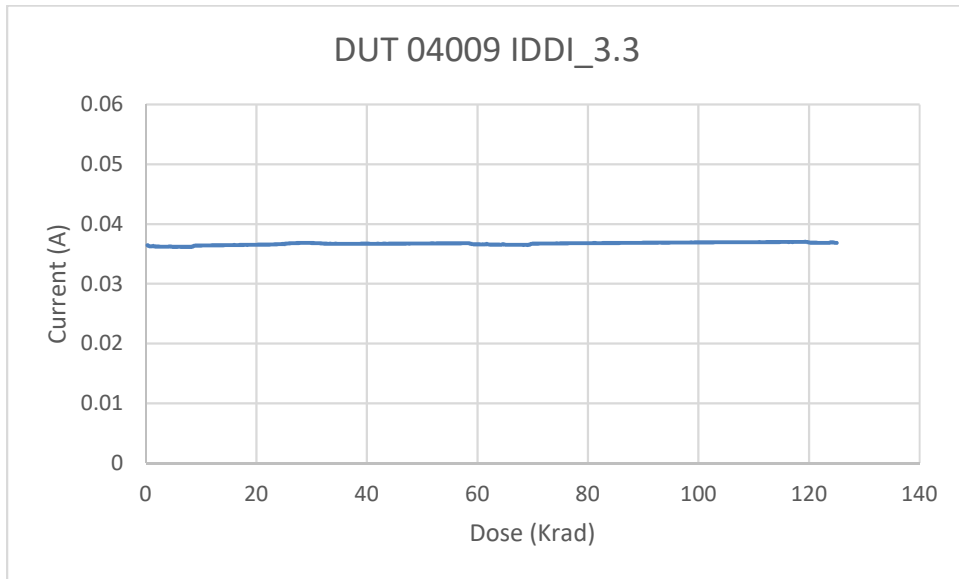


Fig. 17. DUT 4009 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

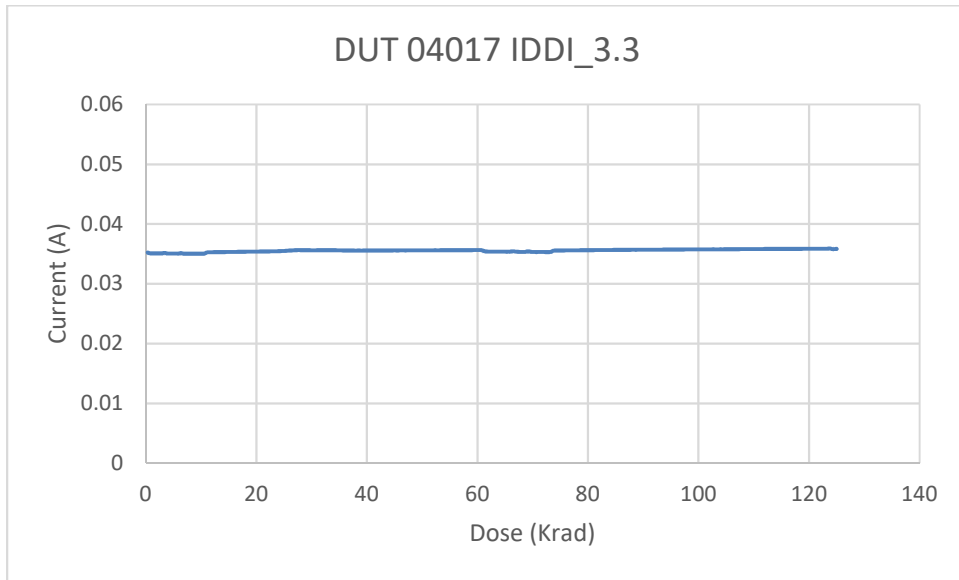


Fig. 18. DUT 4017 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

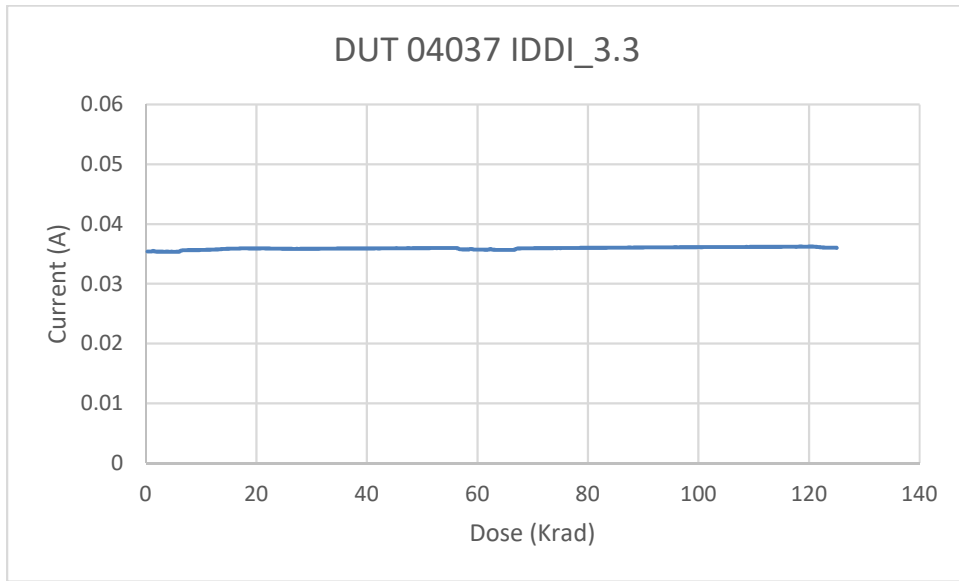


Fig. 19. DUT 4037 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

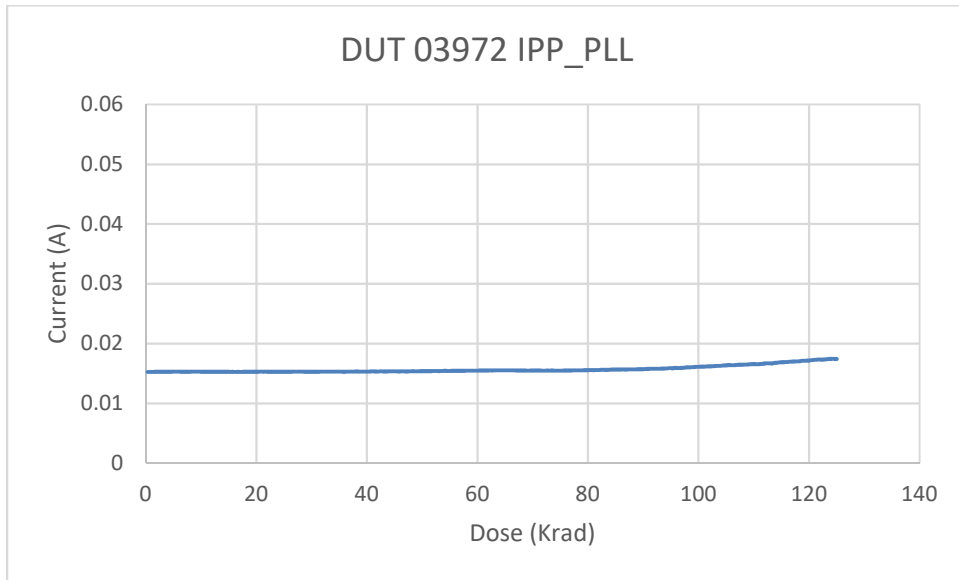


Fig. 20. DUT 3972 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

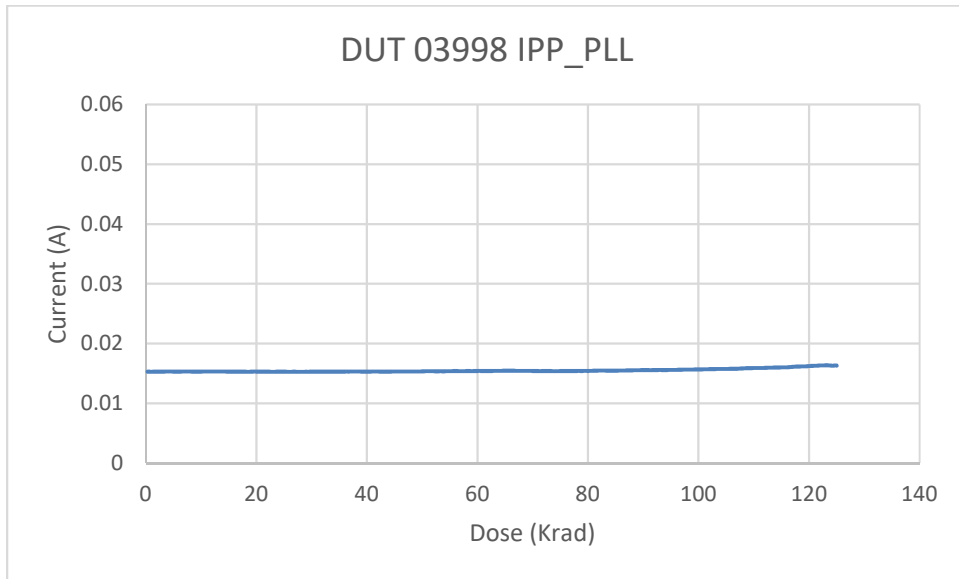


Fig. 21. DUT 3998 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

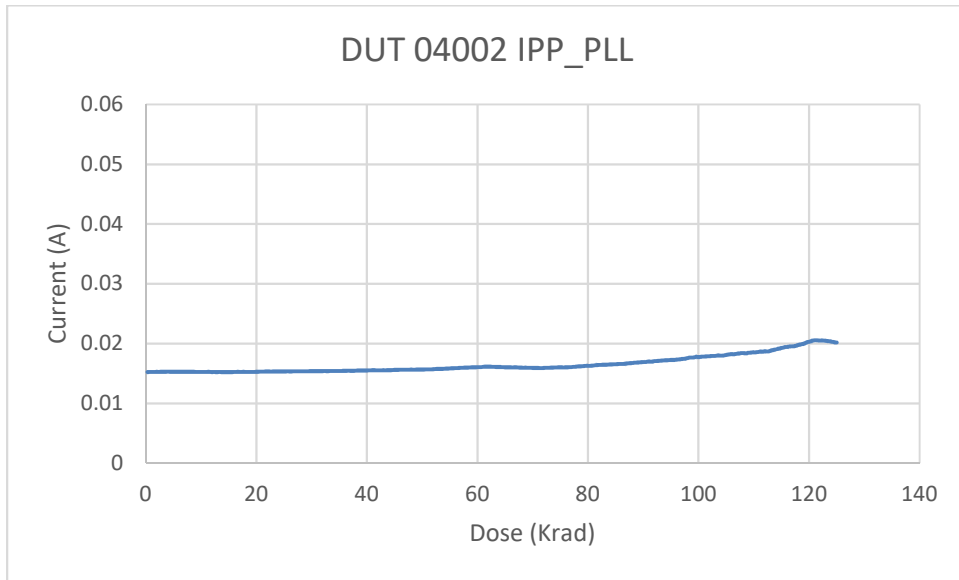


Fig. 22. DUT 4002 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

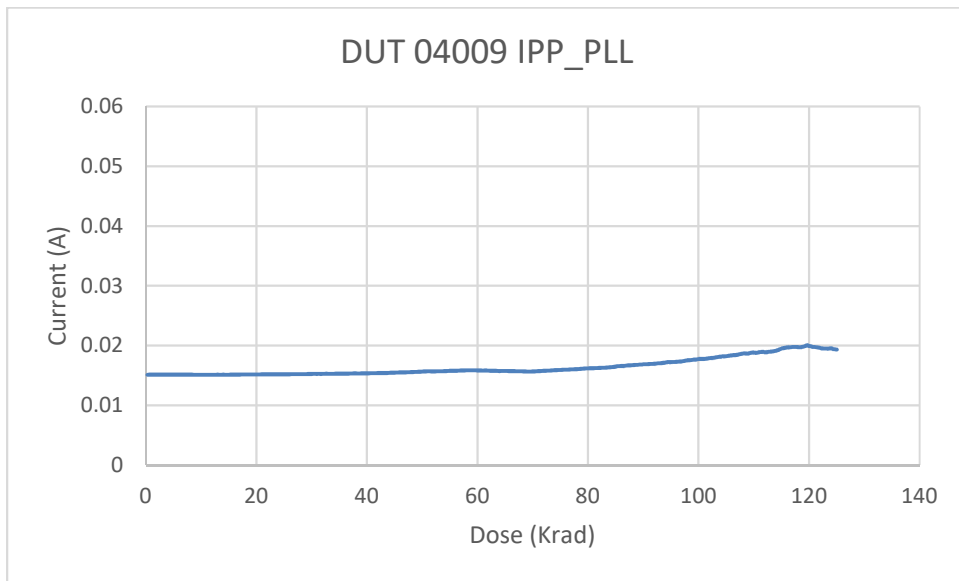


Fig. 23. DUT 4009 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

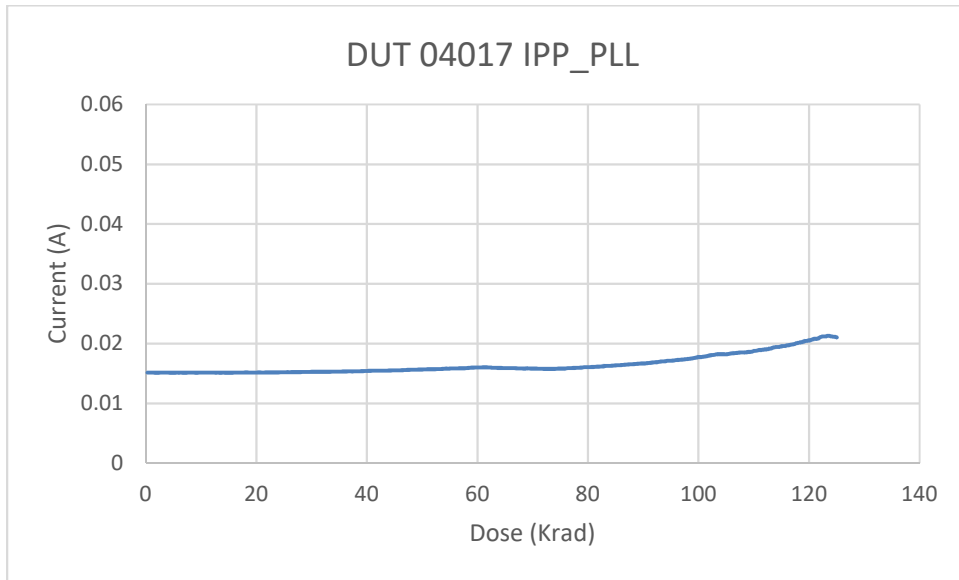


Fig. 24. DUT 4017 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

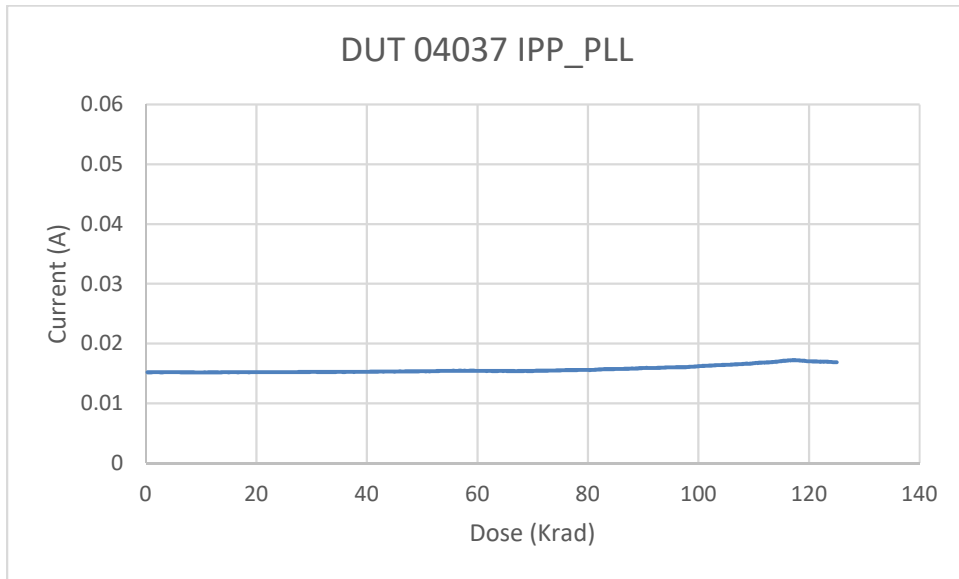


Fig. 25. DUT 4037 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 8. VIH Summary

DUT	Pre-irradiation	Post-irradiation
03972	Passed	Passed
03998	Passed	Passed
04002	Passed	Passed
04009	Passed	Passed
04017	Passed	Passed
04037	Passed	Passed

Table. 9. VIL Summary

DUT	Pre-irradiation	Post-irradiation
03972	Passed	Passed
03998	Passed	Passed
04002	Passed	Passed
04009	Passed	Passed
04017	Passed	Passed
04037	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 10 through 33 are sampled on several pins used in the burn in design.

Table. 10. LVC MOS 25 VOH – DUT 03972

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID BUF OUT	A33	2.134	2.135	2.203	2.203	2.175	2.175	2.152	2.155	2.124	2.125	2.105	2.113
EPCSRST N 0	B31	2.135	2.135	2.203	2.203	2.175	2.176	2.154	2.155	2.122	2.126	2.106	2.109
EPCSRST N 1	B32	2.136	2.136	2.205	2.205	2.177	2.177	2.157	2.156	2.127	2.125	2.114	2.112
EPCSRST N 2	B34	2.135	2.135	2.204	2.204	2.175	2.175	2.155	2.155	2.123	2.123	2.110	2.110
EPCSRST N 3	B35	2.136	2.136	2.205	2.205	2.178	2.178	2.158	2.158	2.128	2.128	2.116	2.116
EPCSRST N 4	B36	2.134	2.134	2.202	2.202	2.173	2.173	2.152	2.151	2.119	2.118	2.105	2.104
EPCSRST N 5	B37	2.135	2.135	2.204	2.204	2.176	2.176	2.155	2.155	2.123	2.124	2.111	2.111
MONITOR	K23	2.135	2.134	2.204	2.204	2.176	2.176	2.156	2.156	2.126	2.125	2.114	2.113
PLL MON	L20	2.136	2.136	2.207	2.206	2.180	2.180	2.162	2.161	2.134	2.133	2.122	2.122
TOGGLE MON	L22	2.135	2.134	2.206	2.205	2.179	2.178	2.160	2.158	2.131	2.129	2.120	2.118

Table. 11. LVC MOS 25 VOH – DUT 03998

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID BUF OUT	A33	2.135	2.132	2.203	2.203	2.175	2.175	2.155	2.148	2.121	2.155	2.109	2.107
EPCSRST N 0	B31	2.136	2.131	2.204	2.208	2.175	2.174	2.156	2.156	2.123	2.103	2.111	2.113
EPCSRST N 1	B32	2.137	2.136	2.205	2.205	2.178	2.177	2.158	2.157	2.127	2.126	2.115	2.113
EPCSRST N 2	B34	2.135	2.135	2.204	2.203	2.175	2.175	2.155	2.154	2.123	2.122	2.109	2.109
EPCSRST N 3	B35	2.136	2.136	2.206	2.206	2.179	2.178	2.159	2.159	2.129	2.129	2.117	2.117
EPCSRST N 4	B36	2.135	2.134	2.203	2.203	2.175	2.174	2.154	2.153	2.122	2.121	2.109	2.107
EPCSRST N 5	B37	2.136	2.136	2.204	2.204	2.176	2.176	2.156	2.156	2.124	2.124	2.111	2.111
MONITOR	K23	2.136	2.135	2.205	2.204	2.177	2.176	2.157	2.156	2.127	2.126	2.114	2.113
PLL MON	L20	2.136	2.135	2.207	2.206	2.180	2.179	2.162	2.161	2.134	2.133	2.123	2.122
TOGGLE MON	L22	2.136	2.136	2.207	2.206	2.180	2.179	2.161	2.159	2.133	2.131	2.121	2.119

Table. 12. LVC MOS 25 VOH – DUT 04002

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID BUF OUT	A33	2.134	2.134	2.203	2.202	2.174	2.174	2.154	2.154	2.121	2.125	2.106	2.115
EPCSRST N 0	B31	2.136	2.136	2.203	2.203	2.175	2.174	2.154	2.154	2.123	2.123	2.108	2.104
EPCSRST N 1	B32	2.136	2.136	2.205	2.205	2.177	2.176	2.157	2.156	2.127	2.125	2.114	2.112
EPCSRST N 2	B34	2.135	2.135	2.203	2.203	2.175	2.175	2.154	2.154	2.122	2.122	2.109	2.109
EPCSRST N 3	B35	2.136	2.135	2.205	2.205	2.178	2.178	2.158	2.158	2.128	2.128	2.116	2.116
EPCSRST N 4	B36	2.134	2.134	2.203	2.203	2.175	2.174	2.154	2.152	2.122	2.120	2.108	2.106
EPCSRST N 5	B37	2.135	2.135	2.204	2.204	2.176	2.175	2.155	2.155	2.124	2.124	2.111	2.111
MONITOR	K23	2.134	2.134	2.204	2.204	2.176	2.176	2.156	2.155	2.126	2.125	2.113	2.112
PLL MON	L20	2.136	2.136	2.207	2.206	2.180	2.180	2.162	2.162	2.134	2.134	2.122	2.122
TOGGLE MON	L22	2.136	2.135	2.206	2.205	2.179	2.179	2.160	2.159	2.132	2.131	2.121	2.119

Table. 13. LVCMOS 25 VOH – DUT 04009

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.133	2.133	2.202	2.202	2.173	2.173	2.151	2.153	2.120	2.120	2.105	2.108
EPCSRST_N_0	B31	2.134	2.133	2.203	2.203	2.174	2.174	2.153	2.153	2.119	2.120	2.108	2.108
EPCSRST_N_1	B32	2.135	2.134	2.204	2.204	2.177	2.176	2.156	2.155	2.126	2.124	2.113	2.111
EPCSRST_N_2	B34	2.133	2.133	2.202	2.202	2.174	2.173	2.152	2.152	2.121	2.120	2.107	2.107
EPCSRST_N_3	B35	2.135	2.134	2.204	2.204	2.177	2.176	2.157	2.157	2.127	2.127	2.115	2.114
EPCSRST_N_4	B36	2.133	2.132	2.202	2.201	2.173	2.172	2.152	2.150	2.120	2.118	2.107	2.104
EPCSRST_N_5	B37	2.133	2.133	2.203	2.203	2.175	2.174	2.154	2.154	2.123	2.122	2.110	2.109
MONITOR	K23	2.133	2.132	2.203	2.203	2.175	2.175	2.155	2.154	2.125	2.124	2.112	2.111
PLL_MON	L20	2.135	2.134	2.206	2.205	2.179	2.179	2.161	2.160	2.133	2.132	2.121	2.120
TOGGLE_MON	L22	2.135	2.133	2.205	2.204	2.178	2.177	2.159	2.158	2.131	2.129	2.119	2.117

Table. 14. LVCMOS 25 VOH – DUT 04017

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.133	2.132	2.202	2.202	2.173	2.174	2.153	2.153	2.121	2.121	2.105	2.108
EPCSRST_N_0	B31	2.135	2.134	2.203	2.203	2.175	2.174	2.154	2.153	2.122	2.121	2.106	2.108
EPCSRST_N_1	B32	2.135	2.134	2.204	2.204	2.177	2.176	2.157	2.156	2.127	2.125	2.114	2.113
EPCSRST_N_2	B34	2.134	2.134	2.203	2.203	2.175	2.175	2.154	2.154	2.122	2.122	2.110	2.109
EPCSRST_N_3	B35	2.135	2.135	2.204	2.204	2.177	2.177	2.157	2.157	2.127	2.127	2.114	2.114
EPCSRST_N_4	B36	2.133	2.133	2.202	2.201	2.173	2.172	2.151	2.150	2.118	2.117	2.104	2.103
EPCSRST_N_5	B37	2.134	2.134	2.204	2.203	2.175	2.175	2.155	2.154	2.123	2.123	2.110	2.110
MONITOR	K23	2.134	2.133	2.203	2.203	2.175	2.175	2.155	2.154	2.125	2.124	2.112	2.111
PLL_MON	L20	2.135	2.134	2.206	2.205	2.179	2.179	2.160	2.160	2.133	2.132	2.121	2.121
TOGGLE_MON	L22	2.135	2.134	2.205	2.204	2.178	2.177	2.159	2.158	2.130	2.129	2.119	2.117

Table. 15. LVCMOS 25 VOH – DUT 04037

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.135	2.135	2.203	2.204	2.175	2.175	2.154	2.155	2.119	2.123	2.108	2.110
EPCSRST_N_0	B31	2.136	2.135	2.204	2.204	2.176	2.175	2.154	2.155	2.123	2.124	2.108	2.109
EPCSRST_N_1	B32	2.137	2.136	2.206	2.205	2.178	2.178	2.158	2.157	2.128	2.126	2.115	2.113
EPCSRST_N_2	B34	2.136	2.135	2.204	2.204	2.175	2.175	2.155	2.155	2.123	2.123	2.110	2.110
EPCSRST_N_3	B35	2.137	2.137	2.206	2.206	2.179	2.179	2.159	2.159	2.130	2.129	2.117	2.117
EPCSRST_N_4	B36	2.136	2.135	2.204	2.203	2.175	2.175	2.155	2.153	2.123	2.121	2.109	2.107
EPCSRST_N_5	B37	2.136	2.135	2.204	2.204	2.176	2.176	2.156	2.156	2.125	2.125	2.112	2.112
MONITOR	K23	2.136	2.135	2.205	2.204	2.177	2.176	2.157	2.156	2.127	2.126	2.115	2.113
PLL_MON	L20	2.137	2.136	2.207	2.207	2.181	2.180	2.163	2.162	2.134	2.134	2.123	2.122
TOGGLE_MON	L22	2.137	2.136	2.207	2.206	2.180	2.179	2.161	2.160	2.133	2.131	2.122	2.119

Table. 16. LVCMOS 25 VOL – DUT 03972

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	235.2	233.1	167.6	164.4	195.5	193.5	217.2	212.3	250.2	243.3	259.1	254.9
EPCSRST_N_0	B31	234.4	233.6	167.5	166.5	195.6	191.8	216.9	211.2	248.2	243.6	263.2	267.3
EPCSRST_N_1	B32	233.2	232.6	165.5	165.4	192.7	192.6	212.4	212.5	242.7	242.8	255.3	255.8
EPCSRST_N_2	B34	234.9	234.1	167.4	166.8	195.2	194.4	215.5	214.4	246.5	245.5	259.8	258.6
EPCSRST_N_3	B35	234.8	233.8	166.1	165.5	193.1	192.2	212.6	211.5	241.8	240.7	254.2	253.0
EPCSRST_N_4	B36	236.3	235.6	169.1	168.8	197.4	197.2	218.3	218.1	250.5	250.8	264.4	264.7
EPCSRST_N_5	B37	235.4	234.5	167.4	166.6	195.1	194.2	215.3	214.1	246.1	244.6	259.1	257.7
MONITOR	K23	233.8	233.1	165.9	165.6	193.0	192.8	212.6	212.3	242.2	242.0	255.0	254.8
PLL_MON	L20	232.7	231.8	163.4	163.1	189.5	189.0	208.3	207.9	235.5	235.3	247.0	246.9
TOGGLE_MON	L22	233.2	232.7	164.0	164.1	190.2	190.5	208.6	209.2	236.5	237.5	248.3	249.4

Table. 17. LVCMOS 25 VOL – DUT 03998

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	235.2	235.3	168.1	166.9	196.2	195.0	216.1	222.0	246.9	250.8	262.2	258.9
EPCSRST_N_0	B31	234.4	236.0	167.0	172.3	194.8	196.8	214.4	238.9	247.9	253.2	260.8	256.1
EPCSRST_N_1	B32	233.3	232.9	165.4	165.4	192.5	192.8	212.1	212.5	242.2	242.8	254.9	255.7
EPCSRST_N_2	B34	235.2	234.6	167.7	167.3	195.6	195.0	216.0	215.2	247.1	246.3	260.4	259.7
EPCSRST_N_3	B35	234.6	233.8	165.7	165.2	192.6	191.9	212.0	211.1	241.2	240.5	253.4	252.7
EPCSRST_N_4	B36	236.0	235.5	168.1	168.0	196.2	196.3	216.6	216.6	248.0	248.4	261.5	262.0
EPCSRST_N_5	B37	235.0	234.1	167.3	166.6	195.0	194.3	215.1	214.1	246.0	244.9	258.9	257.8
MONITOR	K23	233.8	233.3	165.8	165.5	192.9	192.7	212.5	212.0	241.9	242.0	254.8	254.8
PLL_MON	L20	232.7	232.2	163.2	163.1	189.3	189.2	208.3	208.0	235.5	235.5	247.0	247.0
TOGGLE_MON	L22	232.6	232.1	163.5	163.6	189.6	189.9	208.0	208.3	235.4	236.4	247.1	248.2

Table. 18. LVCMOS 25 VOL – DUT 04002

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	235.8	235.2	167.8	167.2	196.2	195.1	217.6	205.6	246.9	240.0	263.1	254.2
EPCSRST_N_0	B31	233.7	236.8	166.7	171.2	195.3	200.3	215.1	217.0	247.2	267.6	260.1	262.4
EPCSRST_N_1	B32	233.5	233.2	165.5	165.5	192.6	192.8	212.3	212.6	242.3	243.0	255.1	256.0
EPCSRST_N_2	B34	235.1	234.7	167.4	167.1	195.4	195.0	215.7	214.9	246.8	246.2	260.1	259.3
EPCSRST_N_3	B35	234.7	234.1	165.7	165.3	192.7	192.3	212.2	211.4	241.1	240.4	253.5	252.8
EPCSRST_N_4	B36	236.0	235.7	168.1	168.1	196.1	196.2	216.7	216.8	248.2	248.6	261.6	262.1
EPCSRST_N_5	B37	235.5	234.9	167.2	166.8	194.9	194.4	215.0	214.1	245.8	244.9	258.7	257.8
MONITOR	K23	234.5	234.1	166.2	166.2	193.4	193.4	212.7	212.8	242.6	242.6	255.3	255.4
PLL_MON	L20	232.3	231.9	163.1	162.7	189.2	188.8	208.0	207.5	235.2	234.6	246.6	245.9
TOGGLE_MON	L22	232.7	232.4	163.5	163.7	189.7	190.2	208.1	208.4	235.8	236.5	247.4	248.4

Table. 19. LVCMOS 25 VOL – DUT 04009

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	237.7	236.9	169.6	168.7	197.7	196.6	219.1	217.7	252.4	248.4	265.3	261.0
EPCSRST_N_0	B31	236.8	236.3	169.0	168.3	197.1	196.7	217.2	218.4	248.6	247.3	261.9	262.4
EPCSRST_N_1	B32	235.5	235.3	166.9	167.0	194.2	194.5	214.0	214.4	244.1	244.7	256.8	257.8
EPCSRST_N_2	B34	237.4	237.2	169.2	168.9	197.2	197.1	217.7	217.2	249.2	248.6	262.7	261.9
EPCSRST_N_3	B35	236.5	236.0	167.2	166.9	194.4	194.0	213.9	213.2	243.4	242.7	255.8	255.0
EPCSRST_N_4	B36	238.4	238.2	169.6	170.1	198.0	198.6	218.6	219.3	250.2	251.7	263.7	265.5
EPCSRST_N_5	B37	237.7	237.3	168.7	168.3	196.7	196.2	217.1	216.3	248.0	246.9	261.0	259.9
MONITOR	K23	236.8	236.3	167.8	167.5	195.2	195.0	214.8	214.6	244.7	244.4	257.5	257.3
PLL_MON	L20	234.8	234.4	164.7	164.5	190.9	190.7	209.9	209.7	237.4	237.1	248.9	248.5
TOGGLE_MON	L22	234.8	234.7	165.2	165.3	191.6	191.8	210.0	210.3	237.9	238.7	249.9	250.7

Table. 20. LVCMOS 25 VOL – DUT 04017

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	237.2	236.4	168.8	167.8	196.6	195.7	218.9	216.1	250.4	247.2	263.3	260.6
EPCSRST_N_0	B31	235.5	235.2	167.8	167.7	196.6	195.7	217.2	217.3	250.1	247.0	262.8	261.3
EPCSRST_N_1	B32	234.7	234.4	166.2	166.2	193.4	193.4	212.9	213.0	242.8	243.1	255.5	256.0
EPCSRST_N_2	B34	236.5	235.9	168.1	167.7	195.9	195.4	216.0	215.4	246.9	246.2	260.1	259.3
EPCSRST_N_3	B35	236.1	235.3	167.0	166.5	194.2	193.6	213.6	212.9	243.3	242.6	255.8	255.0
EPCSRST_N_4	B36	237.4	236.9	169.7	169.6	198.2	198.3	219.3	219.2	251.7	252.1	265.6	266.2
EPCSRST_N_5	B37	236.9	236.2	168.2	167.5	195.9	195.2	215.9	215.0	246.6	245.6	259.5	258.4
MONITOR	K23	235.2	234.6	166.8	166.6	194.2	194.1	213.8	213.7	243.7	243.6	256.6	256.6
PLL_MON	L20	233.7	233.1	164.2	163.8	190.4	190.0	209.3	208.9	236.4	236.0	248.0	247.6
TOGGLE_MON	L22	233.8	233.2	164.6	164.7	191.0	191.2	209.6	209.9	237.6	238.2	249.5	250.3

Table. 21. LVCMOS 25 VOL – DUT 04037

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	234.4	233.0	166.9	166.1	195.4	193.9	215.5	214.3	246.2	245.1	262.0	258.1
EPCSRST_N_0	B31	233.2	232.5	166.5	166.1	193.8	193.6	214.1	214.0	246.3	245.3	258.8	259.3
EPCSRST_N_1	B32	232.0	231.7	164.4	164.6	191.5	191.8	211.1	211.4	241.0	241.7	253.7	254.6
EPCSRST_N_2	B34	234.0	233.5	166.7	166.3	194.6	194.0	214.7	213.9	245.9	245.1	259.1	258.3
EPCSRST_N_3	B35	233.0	232.2	164.8	164.5	191.6	191.3	210.9	210.4	240.1	239.8	252.3	252.0
EPCSRST_N_4	B36	234.1	233.5	167.2	167.1	195.1	195.2	215.4	215.4	246.7	247.2	260.1	260.8
EPCSRST_N_5	B37	234.4	233.5	166.4	165.9	194.0	193.4	214.0	213.2	244.5	243.6	257.4	256.4
MONITOR	K23	232.8	232.2	164.9	164.9	192.0	192.2	211.5	211.5	241.1	241.4	253.9	254.1
PLL_MON	L20	231.4	230.9	162.5	162.2	188.4	188.2	207.4	207.2	234.7	234.6	246.2	246.2
TOGGLE_MON	L22	230.9	230.6	162.8	163.0	188.9	189.2	207.1	207.5	234.7	235.6	246.4	247.5

Table. 22. LVTTTL VOH – DUT 03972

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.922	2.919	2.912	2.914	2.894	2.895	2.875	2.878	2.858	2.856
EPCSRST_N_0	B31	2.922	2.922	2.913	2.909	2.894	2.893	2.875	2.874	2.857	2.854
EPCSRST_N_1	B32	2.923	2.923	2.915	2.914	2.897	2.897	2.880	2.879	2.863	2.862
EPCSRST_N_2	B34	2.923	2.922	2.913	2.913	2.895	2.895	2.877	2.877	2.858	2.859
EPCSRST_N_3	B35	2.923	2.923	2.915	2.915	2.898	2.898	2.882	2.882	2.865	2.865
EPCSRST_N_4	B36	2.921	2.921	2.912	2.911	2.892	2.892	2.873	2.872	2.853	2.852
EPCSRST_N_5	B37	2.923	2.922	2.913	2.913	2.896	2.896	2.877	2.878	2.859	2.860
MONITOR	K23	2.921	2.921	2.913	2.913	2.896	2.896	2.880	2.878	2.863	2.861
PLL_MON	L20	2.922	2.922	2.916	2.915	2.901	2.901	2.887	2.886	2.873	2.872
TOGGLE_MON	L22	2.922	2.921	2.914	2.914	2.900	2.898	2.885	2.883	2.870	2.867

Table. 23. LVTTTL VOH – DUT 03998

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.922	2.922	2.913	2.913	2.894	2.895	2.875	2.876	2.857	2.858
EPCSRST_N_0	B31	2.923	2.923	2.913	2.913	2.895	2.895	2.877	2.877	2.858	2.859
EPCSRST_N_1	B32	2.924	2.923	2.915	2.914	2.898	2.897	2.881	2.880	2.864	2.862
EPCSRST_N_2	B34	2.922	2.922	2.913	2.913	2.894	2.894	2.876	2.876	2.858	2.858
EPCSRST_N_3	B35	2.924	2.923	2.915	2.915	2.899	2.899	2.883	2.883	2.866	2.866
EPCSRST_N_4	B36	2.922	2.922	2.913	2.912	2.894	2.893	2.876	2.874	2.857	2.855
EPCSRST_N_5	B37	2.923	2.923	2.914	2.914	2.896	2.896	2.878	2.878	2.860	2.860
MONITOR	K23	2.922	2.922	2.914	2.913	2.897	2.896	2.880	2.879	2.863	2.862
PLL_MON	L20	2.923	2.922	2.916	2.915	2.901	2.901	2.887	2.886	2.873	2.872
TOGGLE_MON	L22	2.923	2.922	2.916	2.915	2.901	2.900	2.886	2.884	2.871	2.869

Table. 24. LVTTTL VOH – DUT 04002

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.922	2.921	2.912	2.913	2.894	2.894	2.874	2.876	2.856	2.858
EPCSRST_N_0	B31	2.922	2.922	2.913	2.913	2.895	2.895	2.876	2.877	2.857	2.858
EPCSRST_N_1	B32	2.924	2.923	2.915	2.914	2.898	2.897	2.881	2.879	2.863	2.862
EPCSRST_N_2	B34	2.922	2.922	2.913	2.913	2.894	2.894	2.876	2.876	2.858	2.858
EPCSRST_N_3	B35	2.923	2.923	2.915	2.915	2.898	2.898	2.882	2.882	2.866	2.866
EPCSRST_N_4	B36	2.922	2.921	2.913	2.912	2.894	2.893	2.875	2.874	2.856	2.855
EPCSRST_N_5	B37	2.922	2.922	2.913	2.913	2.895	2.896	2.878	2.878	2.860	2.860
MONITOR	K23	2.921	2.921	2.913	2.912	2.896	2.895	2.879	2.878	2.862	2.861
PLL_MON	L20	2.923	2.923	2.916	2.915	2.901	2.901	2.887	2.887	2.873	2.873
TOGGLE_MON	L22	2.922	2.922	2.915	2.914	2.900	2.899	2.886	2.884	2.871	2.869

Table. 25. LVTTTL VOH – DUT 04009

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.920	2.920	2.911	2.911	2.893	2.892	2.873	2.874	2.854	2.856
EPCSRST_N_0	B31	2.921	2.921	2.911	2.911	2.893	2.893	2.875	2.875	2.855	2.856
EPCSRST_N_1	B32	2.922	2.922	2.913	2.913	2.897	2.895	2.879	2.878	2.862	2.860
EPCSRST_N_2	B34	2.921	2.920	2.911	2.911	2.893	2.892	2.874	2.874	2.856	2.856
EPCSRST_N_3	B35	2.922	2.921	2.914	2.913	2.897	2.897	2.881	2.881	2.864	2.864
EPCSRST_N_4	B36	2.920	2.919	2.911	2.910	2.892	2.891	2.873	2.871	2.855	2.852
EPCSRST_N_5	B37	2.921	2.920	2.912	2.912	2.894	2.894	2.876	2.876	2.858	2.858
MONITOR	K23	2.920	2.920	2.912	2.911	2.895	2.894	2.878	2.877	2.861	2.860
PLL_MON	L20	2.921	2.921	2.914	2.914	2.900	2.899	2.885	2.885	2.871	2.871
TOGGLE_MON	L22	2.921	2.920	2.914	2.913	2.899	2.897	2.884	2.882	2.869	2.867

Table. 26. LVTTTL VOH – DUT 04017

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.920	2.920	2.911	2.912	2.892	2.893	2.874	2.875	2.855	2.857
EPCSRST_N_0	B31	2.922	2.922	2.912	2.912	2.893	2.894	2.874	2.875	2.855	2.856
EPCSRST_N_1	B32	2.922	2.922	2.914	2.913	2.897	2.897	2.880	2.879	2.864	2.862
EPCSRST_N_2	B34	2.922	2.921	2.912	2.912	2.894	2.894	2.876	2.876	2.858	2.858
EPCSRST_N_3	B35	2.923	2.922	2.914	2.914	2.897	2.897	2.880	2.881	2.864	2.864
EPCSRST_N_4	B36	2.921	2.920	2.911	2.910	2.892	2.891	2.872	2.871	2.853	2.851
EPCSRST_N_5	B37	2.922	2.921	2.913	2.913	2.895	2.895	2.877	2.877	2.859	2.860
MONITOR	K23	2.921	2.920	2.912	2.912	2.895	2.894	2.878	2.877	2.861	2.860
PLL_MON	L20	2.922	2.922	2.915	2.914	2.900	2.900	2.886	2.885	2.872	2.871
TOGGLE_MON	L22	2.922	2.921	2.914	2.913	2.899	2.898	2.884	2.882	2.869	2.867

Table. 27. LVTTTL VOH – DUT 04037

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.923	2.923	2.914	2.914	2.895	2.895	2.876	2.877	2.857	2.859
EPCSRST_N_0	B31	2.924	2.923	2.914	2.915	2.896	2.896	2.878	2.877	2.859	2.859
EPCSRST_N_1	B32	2.925	2.924	2.916	2.916	2.899	2.898	2.882	2.881	2.865	2.863
EPCSRST_N_2	B34	2.923	2.923	2.914	2.914	2.896	2.896	2.877	2.877	2.859	2.859
EPCSRST_N_3	B35	2.925	2.925	2.916	2.916	2.900	2.900	2.884	2.883	2.867	2.867
EPCSRST_N_4	B36	2.924	2.923	2.914	2.913	2.895	2.894	2.877	2.875	2.858	2.856
EPCSRST_N_5	B37	2.924	2.923	2.915	2.915	2.897	2.897	2.879	2.879	2.861	2.861
MONITOR	K23	2.923	2.922	2.914	2.914	2.898	2.897	2.881	2.880	2.864	2.863
PLL_MON	L20	2.924	2.924	2.917	2.916	2.903	2.902	2.888	2.887	2.874	2.873
TOGGLE_MON	L22	2.924	2.924	2.916	2.916	2.901	2.901	2.887	2.885	2.872	2.870

Table. 28. LVTTTL VOL – DUT 03972

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	215.1	214.9	223.7	222.6	241.9	245.1	260.1	260.4	276.0	271.9
EPCSRST_N_0	B31	214.7	218.5	222.4	240.1	241.0	238.2	260.0	262.6	278.2	268.6
EPCSRST_N_1	B32	213.3	212.9	221.0	220.6	238.3	238.7	255.5	255.9	273.0	273.5
EPCSRST_N_2	B34	214.7	214.1	223.2	222.2	241.5	240.7	259.7	258.5	277.9	276.7
EPCSRST_N_3	B35	214.5	214.0	222.1	220.6	238.5	237.5	255.0	253.8	271.4	270.2
EPCSRST_N_4	B36	216.2	215.6	224.9	224.4	244.3	244.2	263.6	263.9	283.2	283.7
EPCSRST_N_5	B37	215.1	214.3	223.3	222.0	241.5	240.0	259.1	257.8	277.1	275.6
MONITOR	K23	213.6	212.9	221.5	220.9	238.2	238.0	255.1	255.0	272.2	272.1
PLL_MON	L20	212.3	211.9	219.8	219.3	233.3	233.3	247.9	247.5	263.0	262.7
TOGGLE_MON	L22	212.6	212.4	219.2	218.6	234.5	235.0	249.4	250.3	264.5	266.0

Table. 29. LVTTTL VOL – DUT 03998

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	214.8	214.0	223.7	221.7	242.7	240.6	261.2	258.5	281.1	277.6
EPCSRST_N_0	B31	214.3	213.5	223.5	221.2	241.1	239.6	258.5	258.1	279.5	277.2
EPCSRST_N_1	B32	213.5	213.1	221.2	220.6	238.0	238.4	255.2	255.7	272.2	273.2
EPCSRST_N_2	B34	215.0	214.4	223.5	222.6	242.0	241.6	260.1	259.5	278.6	277.7
EPCSRST_N_3	B35	214.4	213.7	221.6	220.3	237.9	237.3	254.2	253.5	270.9	269.9
EPCSRST_N_4	B36	215.8	215.2	224.4	223.7	242.7	242.8	260.9	261.5	279.8	280.5
EPCSRST_N_5	B37	214.6	213.9	223.3	222.1	241.1	240.0	258.9	257.8	277.0	275.6
MONITOR	K23	213.7	212.9	221.2	220.7	238.1	238.2	255.0	255.1	271.8	272.1
PLL_MON	L20	212.6	212.1	220.0	219.7	233.7	233.5	247.9	247.8	262.8	263.1
TOGGLE_MON	L22	212.0	211.8	218.2	217.9	233.7	234.3	248.2	249.3	263.3	264.6

Table. 30. LVTTTL VOL – DUT 04002

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	215.4	214.8	223.6	221.5	242.2	240.7	261.0	259.3	280.1	277.5
EPCSRST_N_0	B31	214.2	214.4	222.6	222.1	241.5	239.6	258.9	257.9	279.7	277.4
EPCSRST_N_1	B32	213.6	213.2	221.3	220.9	238.1	238.5	255.4	256.3	272.4	273.6
EPCSRST_N_2	B34	215.1	214.6	223.4	222.4	241.7	241.0	259.8	259.2	278.4	277.6
EPCSRST_N_3	B35	214.6	213.8	221.8	220.8	238.2	237.5	254.2	253.6	270.7	269.9
EPCSRST_N_4	B36	215.7	215.2	223.9	223.5	242.5	242.7	261.2	261.8	280.0	280.8
EPCSRST_N_5	B37	215.3	214.7	223.1	222.3	241.2	240.4	258.8	257.8	276.7	275.5
MONITOR	K23	213.9	213.9	222.1	221.5	238.8	238.8	255.5	255.8	272.5	272.7
PLL_MON	L20	212.1	211.7	219.7	219.1	233.4	232.9	247.6	247.0	262.6	261.9
TOGGLE_MON	L22	212.2	212.0	218.4	218.2	233.8	234.5	248.5	249.4	263.5	264.6

Table. 31. LVTTTL VOL – DUT 04009

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	217.3	216.1	224.9	224.9	244.6	243.1	263.4	261.2	281.5	279.9
EPCSRST_N_0	B31	216.6	215.7	225.4	224.2	243.4	242.8	262.1	260.9	282.2	279.6
EPCSRST_N_1	B32	215.5	215.4	223.0	223.0	240.1	240.5	257.0	257.9	274.3	275.5
EPCSRST_N_2	B34	217.0	216.7	225.8	225.0	244.2	243.7	262.2	261.9	280.7	280.2
EPCSRST_N_3	B35	216.1	215.7	223.8	222.7	239.9	239.4	256.5	255.7	272.9	272.1
EPCSRST_N_4	B36	217.8	217.8	226.4	226.4	244.7	245.7	263.2	264.7	282.0	284.2
EPCSRST_N_5	B37	217.5	216.8	225.4	224.5	243.3	242.5	260.9	260.0	278.9	277.9
MONITOR	K23	216.0	215.7	224.1	223.5	240.9	240.6	257.9	257.6	274.8	274.8
PLL_MON	L20	214.2	214.1	221.7	221.4	235.2	235.2	249.7	249.6	264.9	264.5
TOGGLE_MON	L22	214.3	214.2	220.8	220.3	236.3	236.7	250.8	251.6	266.0	267.0

Table. 32. LVTTTL VOL – DUT 04017

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	216.4	215.5	224.9	224.0	242.7	241.4	261.4	259.8	280.8	278.4
EPCSRST_N_0	B31	214.8	214.1	223.2	223.0	242.7	241.6	261.2	260.1	281.5	279.4
EPCSRST_N_1	B32	214.4	214.1	221.7	221.6	238.6	239.0	255.3	255.7	272.4	272.9
EPCSRST_N_2	B34	215.8	215.1	224.1	223.1	241.9	241.4	259.6	259.0	277.8	276.9
EPCSRST_N_3	B35	215.4	215.0	223.2	222.1	239.4	238.6	255.9	255.3	272.8	271.8
EPCSRST_N_4	B36	216.6	216.2	225.8	224.9	245.2	245.1	264.4	265.1	284.1	284.8
EPCSRST_N_5	B37	216.2	215.6	224.3	223.1	241.9	241.0	259.2	258.4	277.0	276.0
MONITOR	K23	214.3	213.9	222.4	221.7	239.4	239.4	256.4	256.4	273.5	273.6
PLL_MON	L20	213.1	212.5	220.6	220.1	234.4	233.8	248.6	248.3	263.7	263.3
TOGGLE_MON	L22	212.8	212.4	219.7	219.4	235.2	235.5	250.2	251.0	265.4	266.5

Table. 33. LVTTTL VOL – DUT 04037

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	213.6	212.9	222.6	221.5	241.3	239.4	259.5	257.8	279.2	276.2
EPCSRST_N_0	B31	213.2	212.2	220.7	220.9	238.9	239.4	257.3	257.6	276.4	275.9
EPCSRST_N_1	B32	212.0	211.6	219.5	219.5	236.5	236.9	253.5	254.2	270.7	271.9
EPCSRST_N_2	B34	213.6	213.0	221.9	221.1	240.1	239.7	258.3	257.6	276.8	276.0
EPCSRST_N_3	B35	212.5	211.9	220.1	219.3	236.5	235.8	252.5	252.2	269.2	268.7
EPCSRST_N_4	B36	213.5	213.1	222.3	222.0	240.9	241.0	259.3	260.0	278.1	279.0
EPCSRST_N_5	B37	213.7	213.2	222.0	220.9	239.6	238.6	257.1	256.1	274.9	273.9
MONITOR	K23	212.4	211.9	220.2	219.7	237.0	237.1	253.5	253.8	270.5	271.1
PLL_MON	L20	210.9	210.4	218.0	217.8	232.0	232.0	246.6	246.5	261.7	261.9
TOGGLE_MON	L22	210.4	210.0	217.1	216.9	232.5	232.9	247.3	248.1	262.2	263.6

E. Propagation Delay

Table 34 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 34. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (μs)	Post-irradiation (μs)	Change Degradation (%)
03972	125 krad	0.4448	0.4470	0.49
03998	125 krad	0.4496	0.4532	0.79
04002	125 krad	0.4545	0.4579	0.75
04009	125 krad	0.4549	0.4584	0.77
04017	125 krad	0.4519	0.4532	0.29
04037	125 krad	0.4502	0.4502	0.01

F. Transition Time

The figures below show the pre-irradiation and post-irradiation transitions edges. In each case the radiation induced transition degradation is not observable.

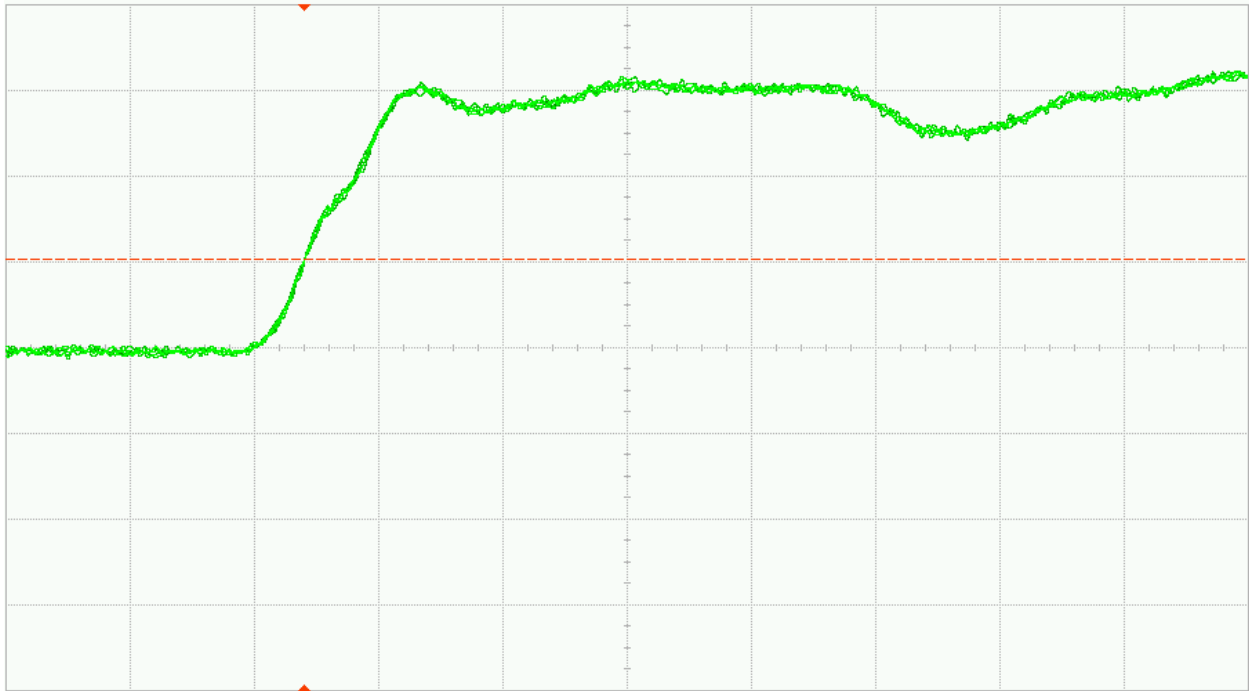


Fig. 26 (a). DUT 3972 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

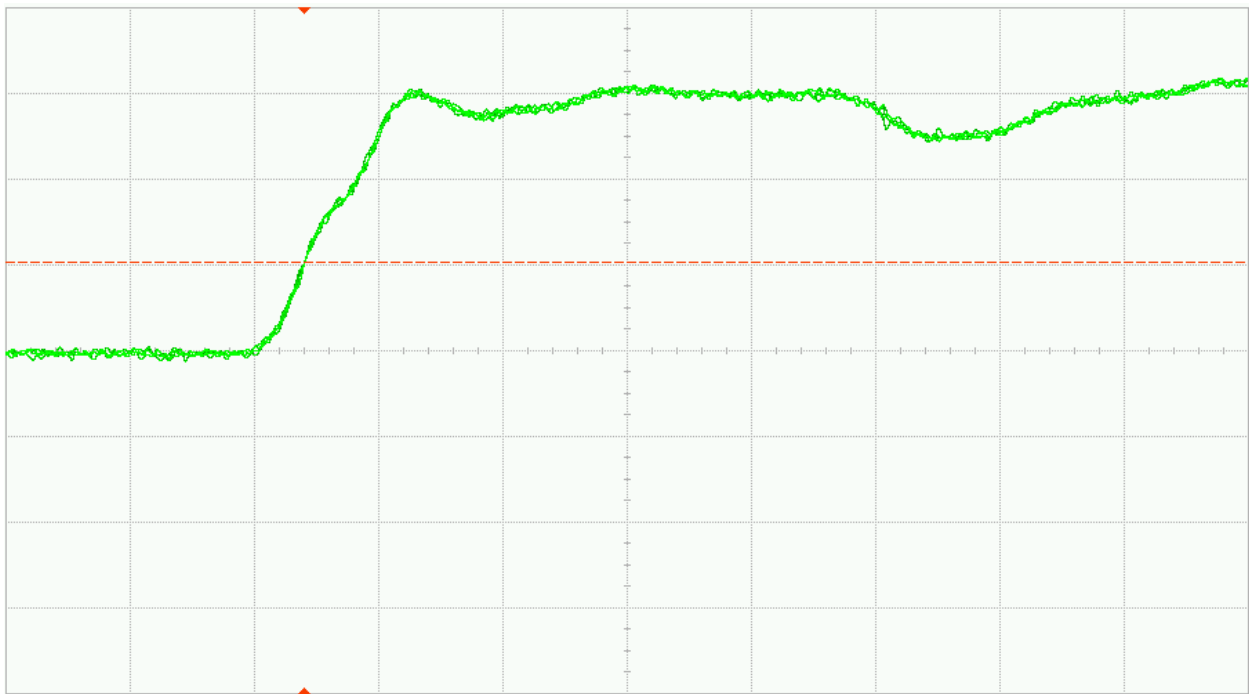


Fig. 26 (b). DUT 3972 post-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

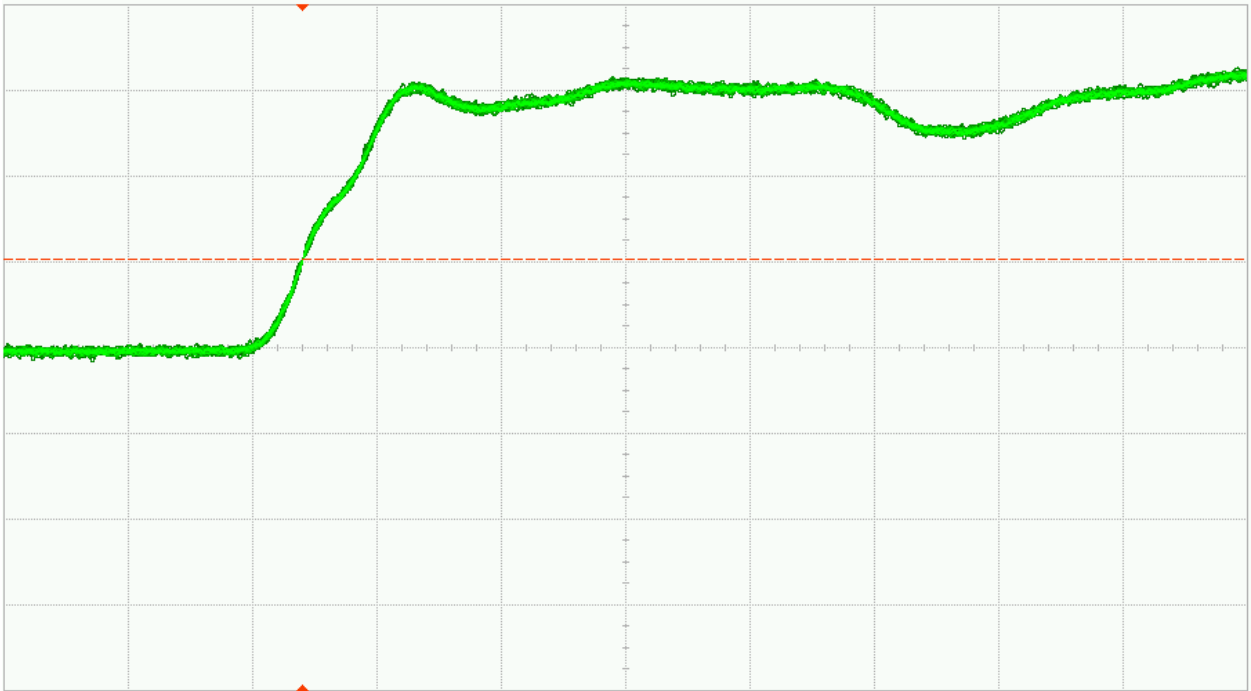


Fig. 27 (a). DUT 3998 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

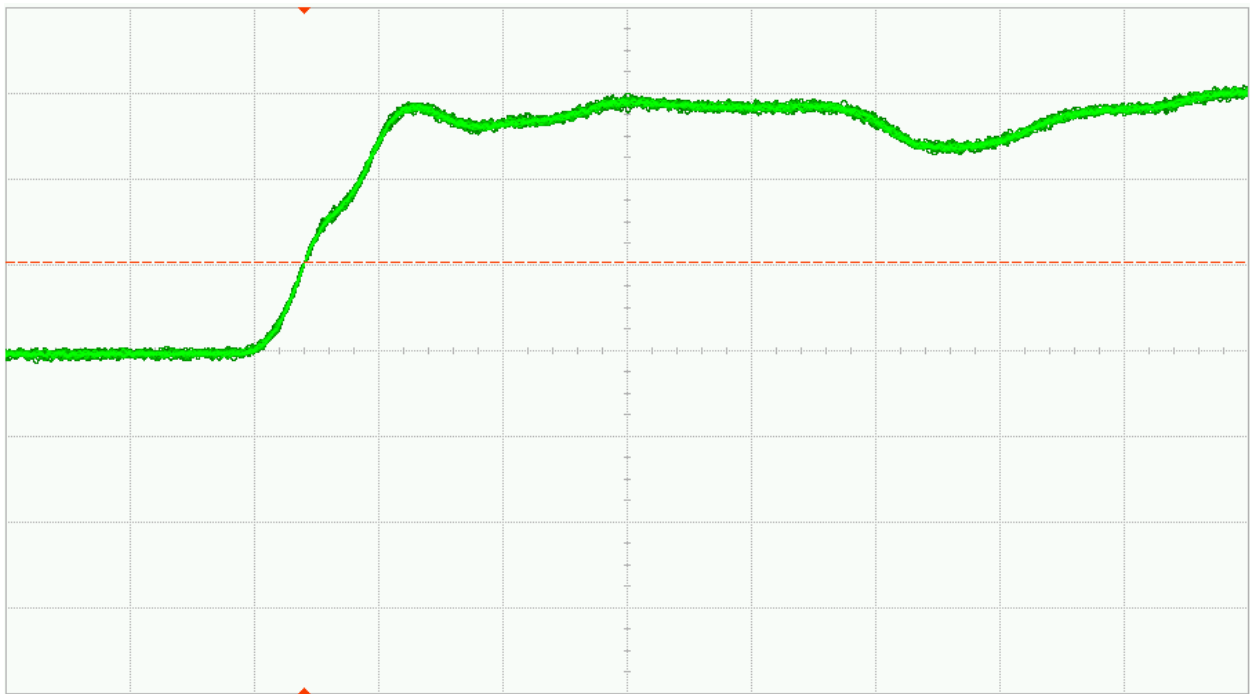


Fig. 27 (b). DUT 3998 post-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

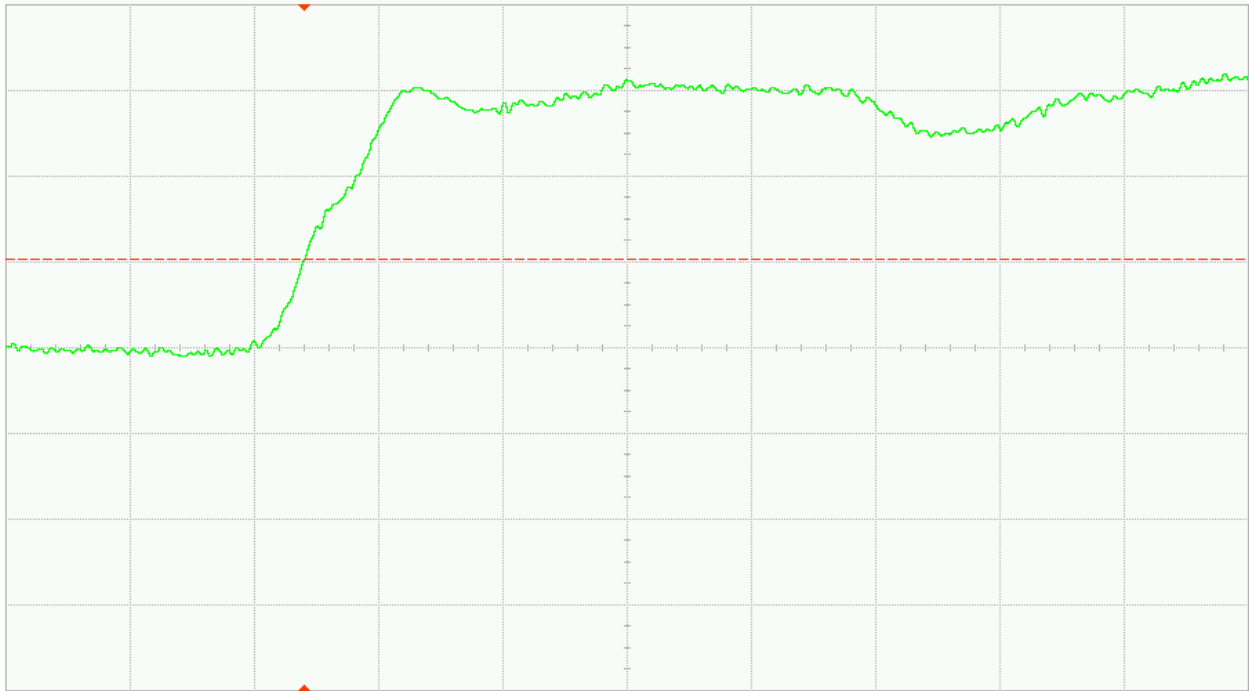


Fig. 28 (a). DUT 4002 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

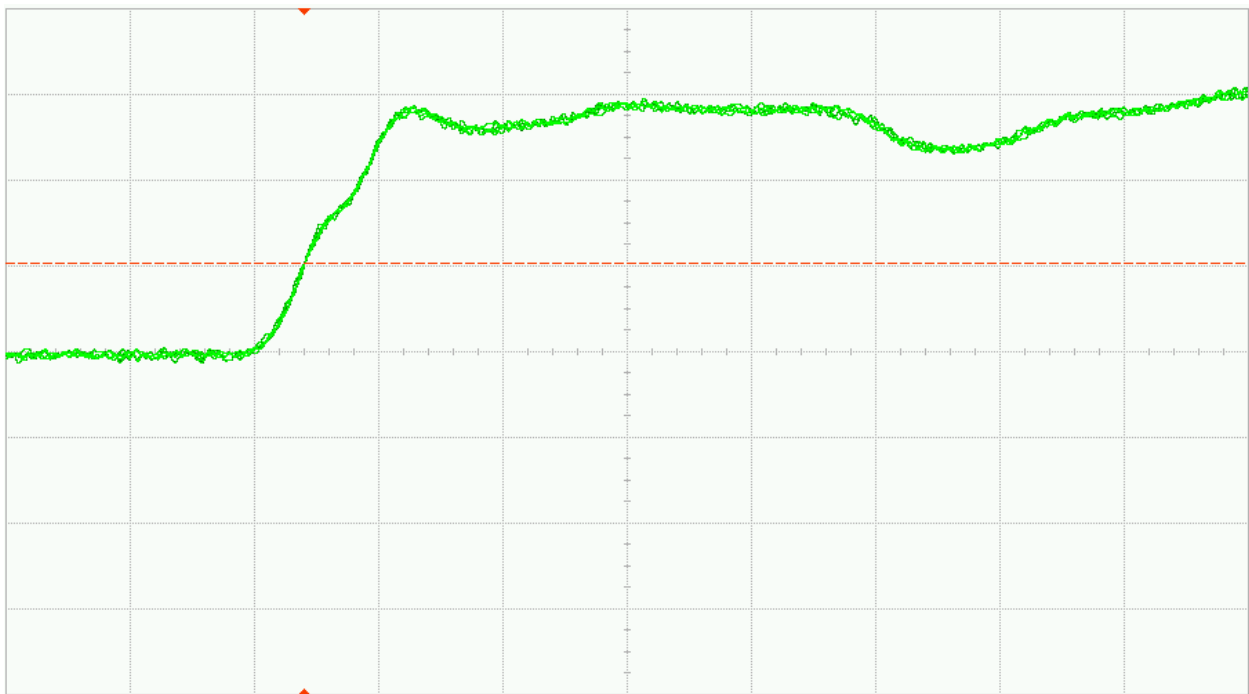


Fig. 28 (b). DUT 4002 post-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

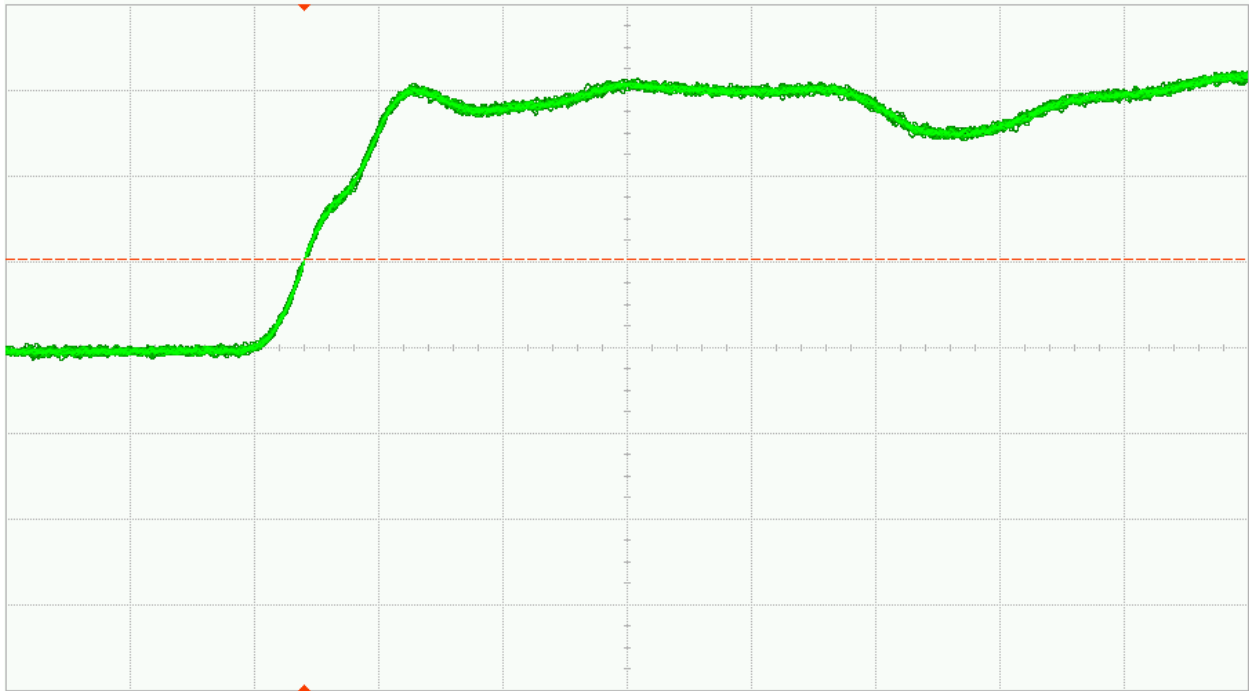


Fig. 29 (a). DUT 4009 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

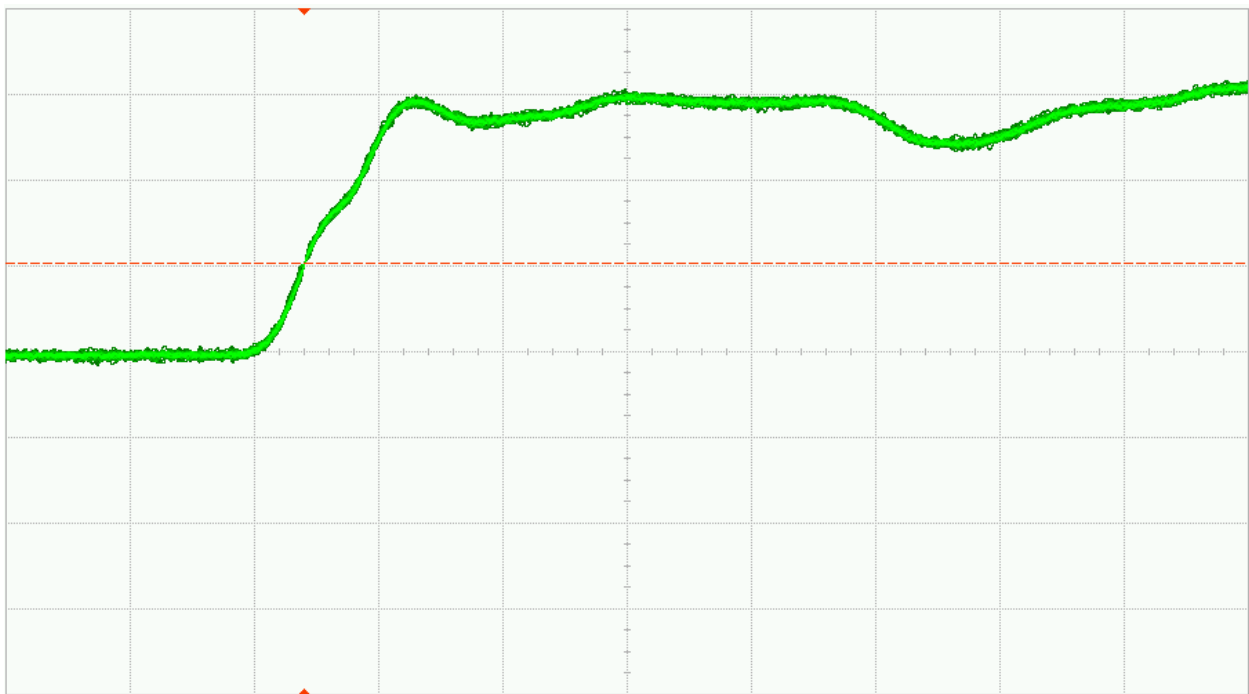


Fig. 29 (b). DUT 4009 post-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

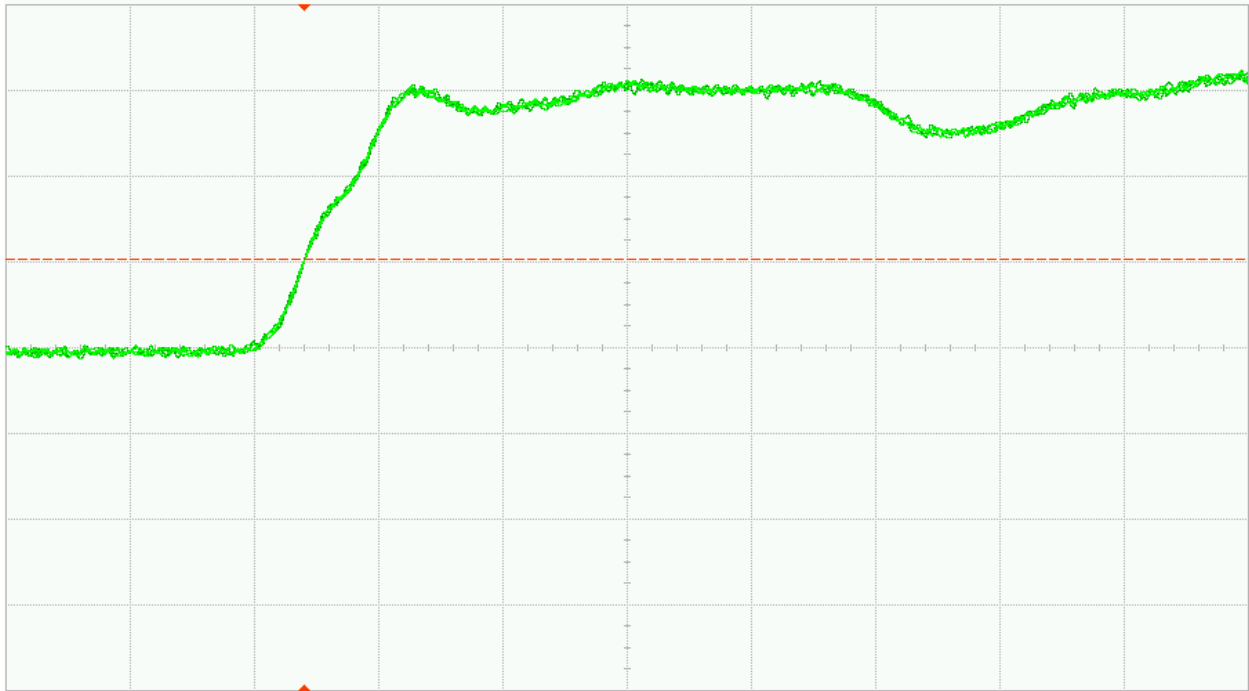


Fig. 30 (a). DUT 4017 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

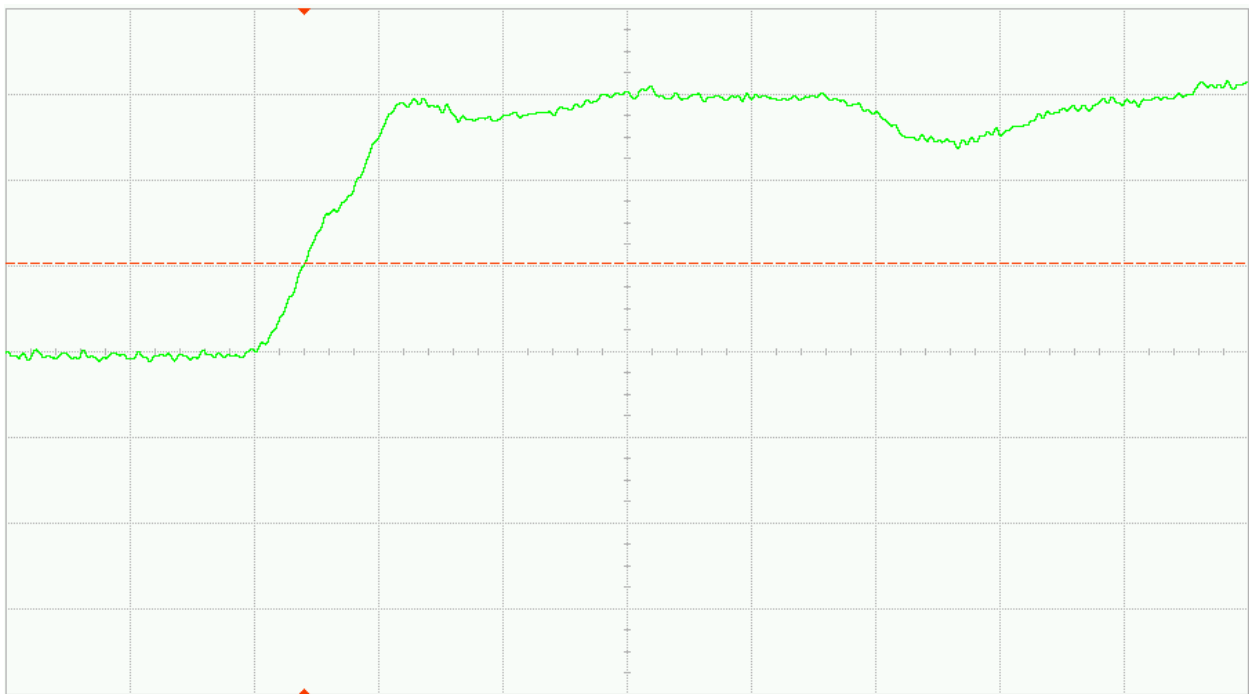


Fig. 30 (b). DUT 4017 post-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

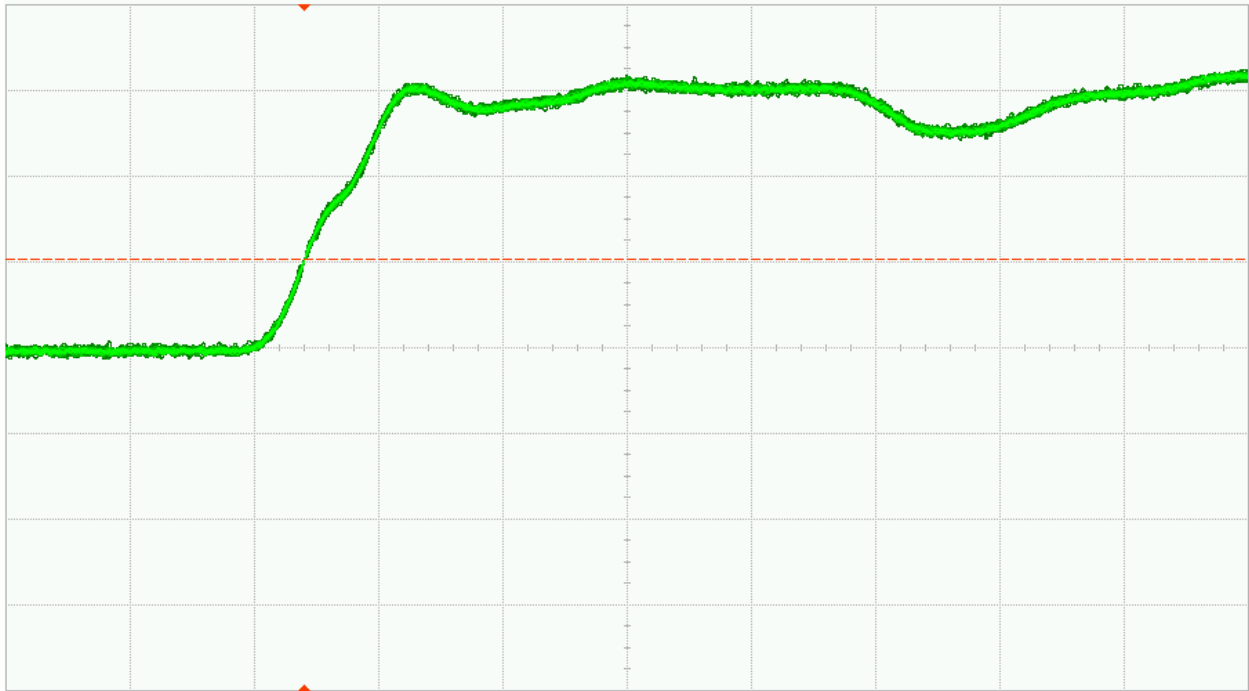


Fig. 31 (a). DUT 4037 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

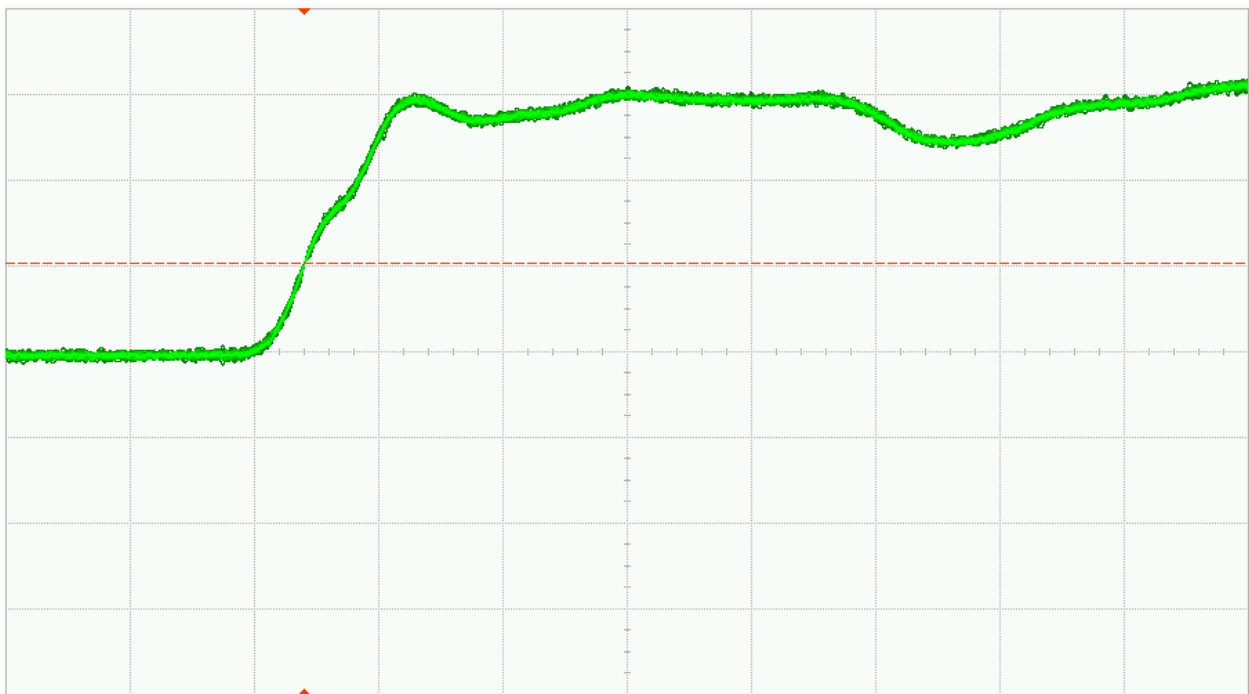


Fig. 31 (b). DUT 4037 post-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

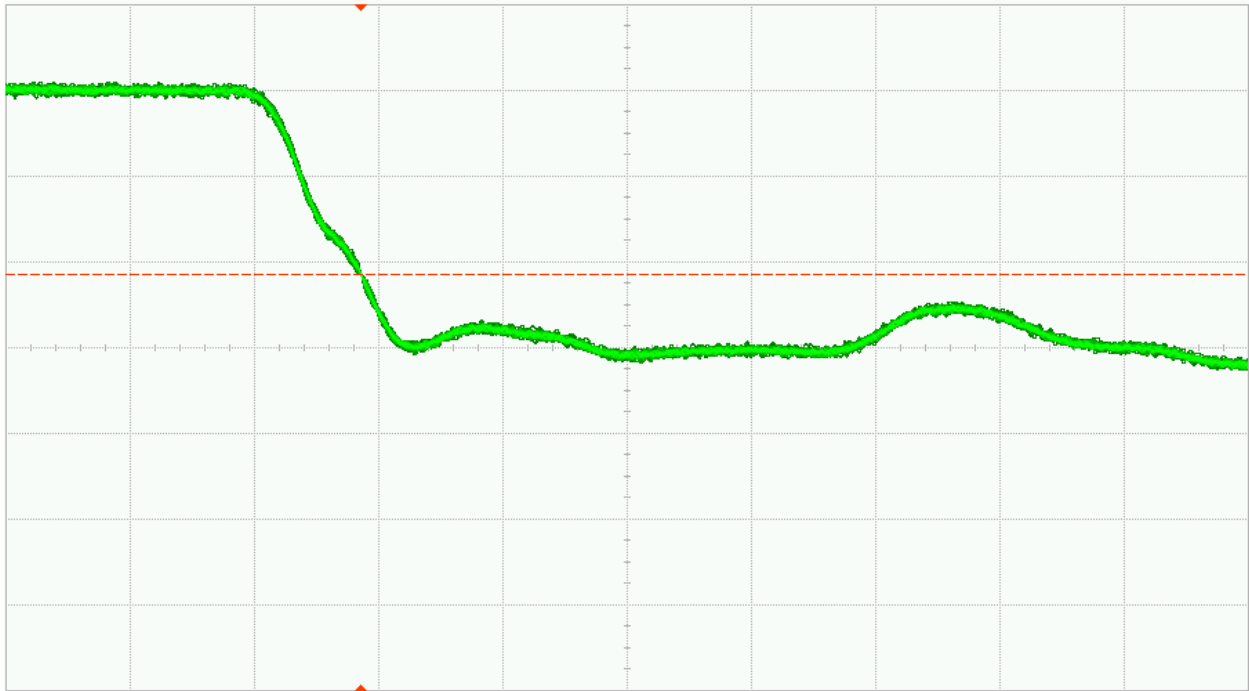


Fig. 32 (a). DUT 3972 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

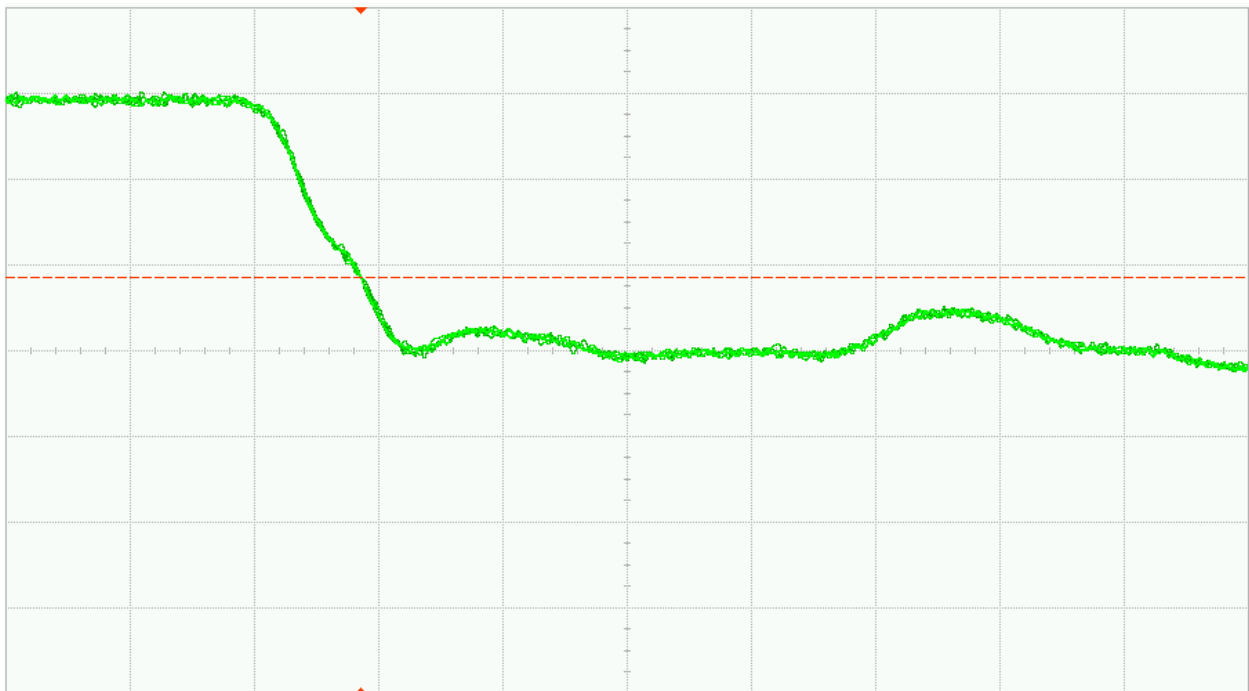


Fig. 32 (b). DUT 3972 post-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

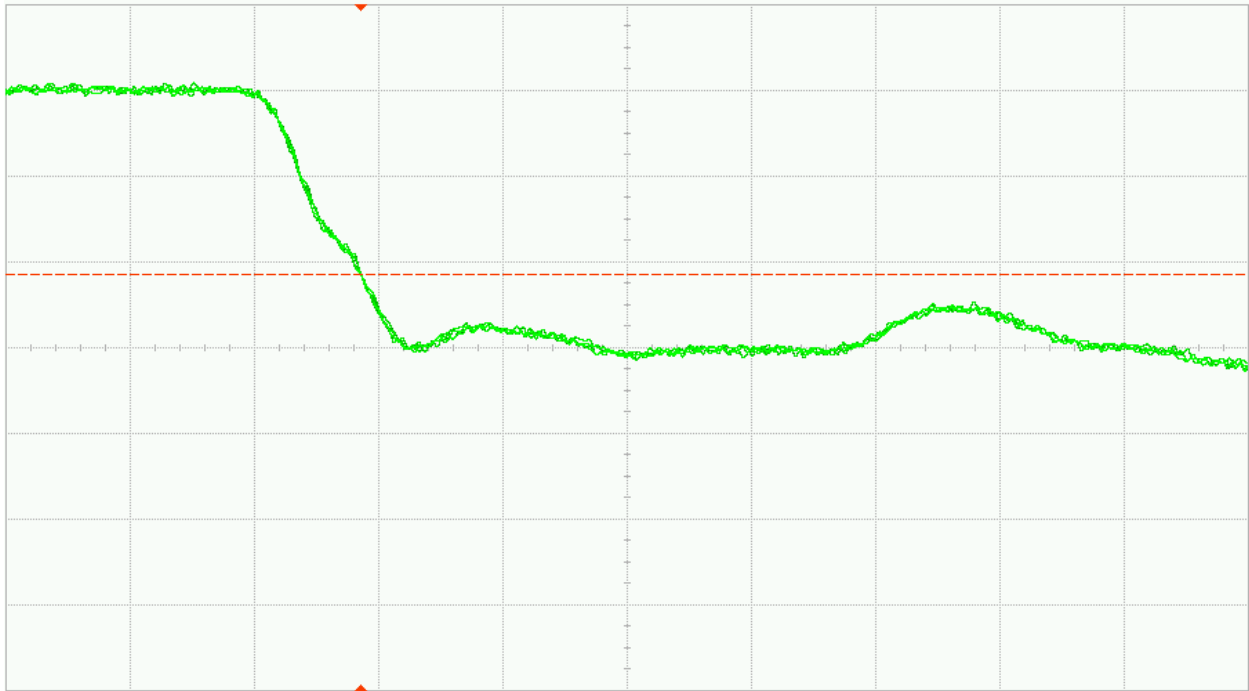


Fig. 33 (a). DUT 3998 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

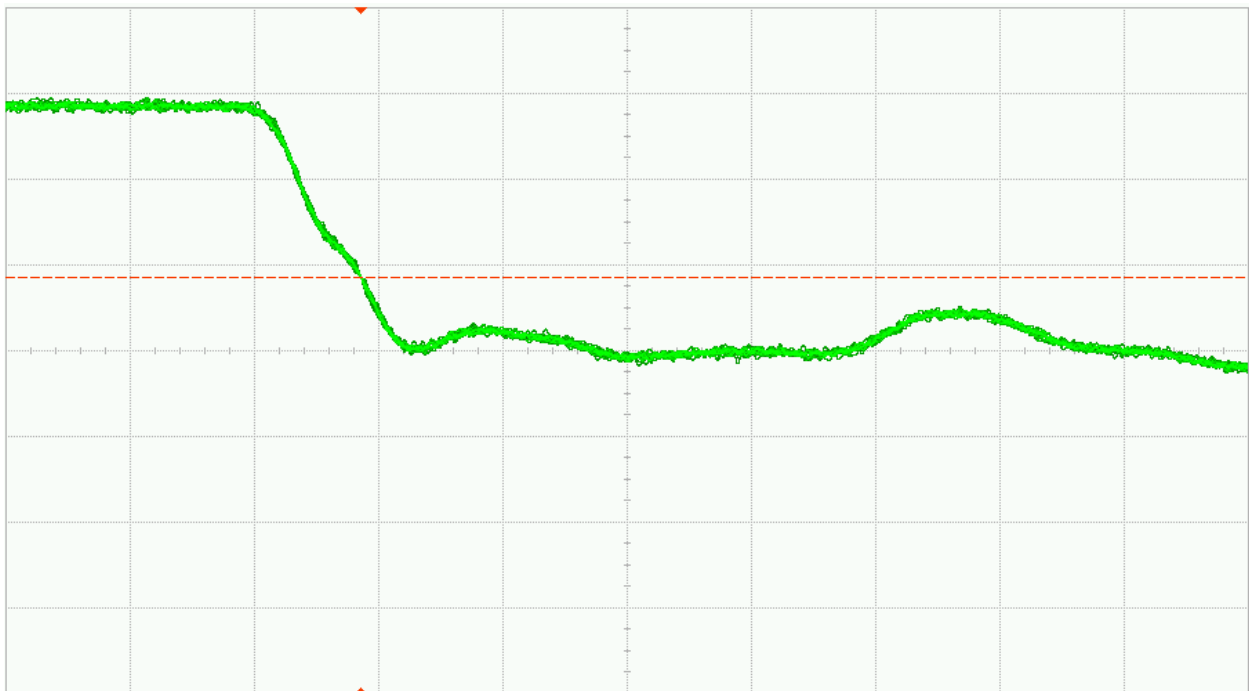


Fig. 33 (b). DUT 3998 post-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

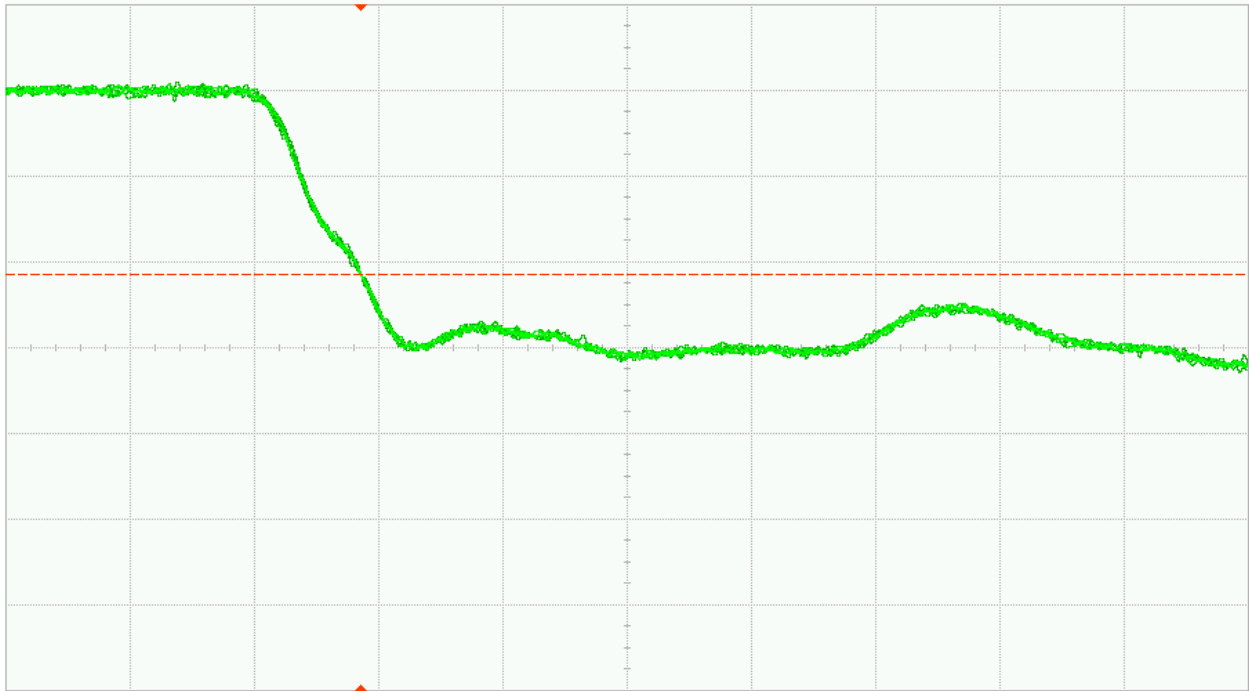


Fig. 34 (a). DUT 4002 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

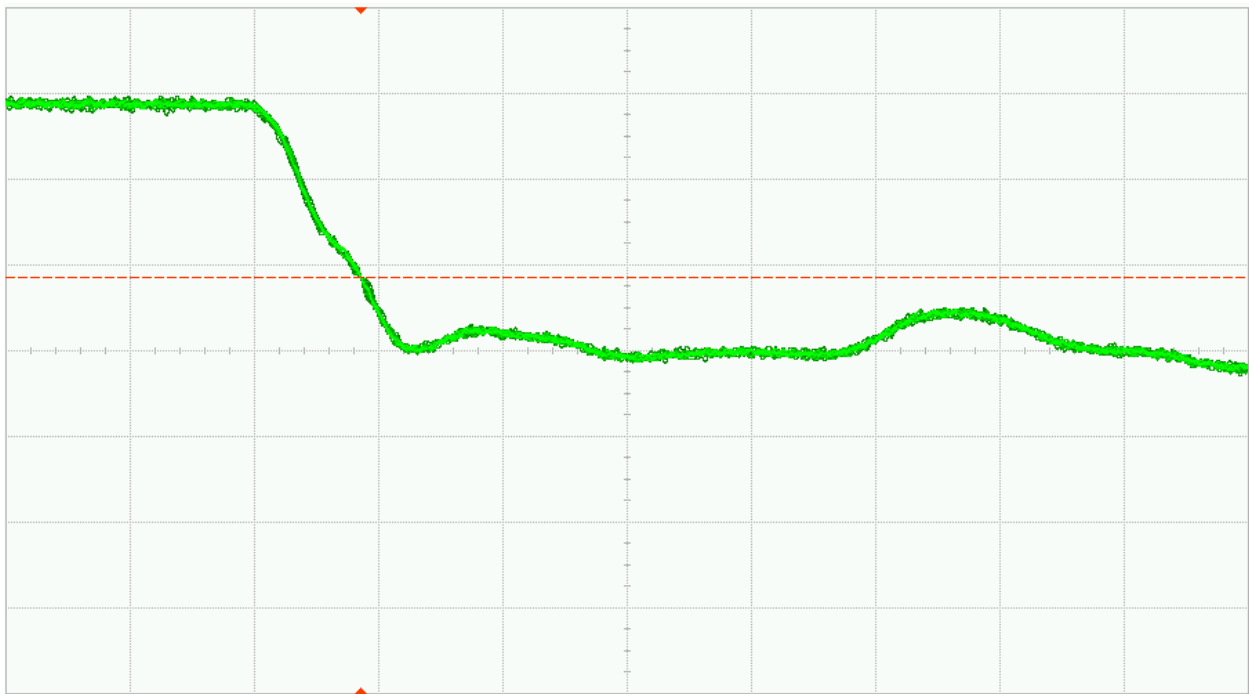


Fig. 34 (b). DUT 4002 post-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

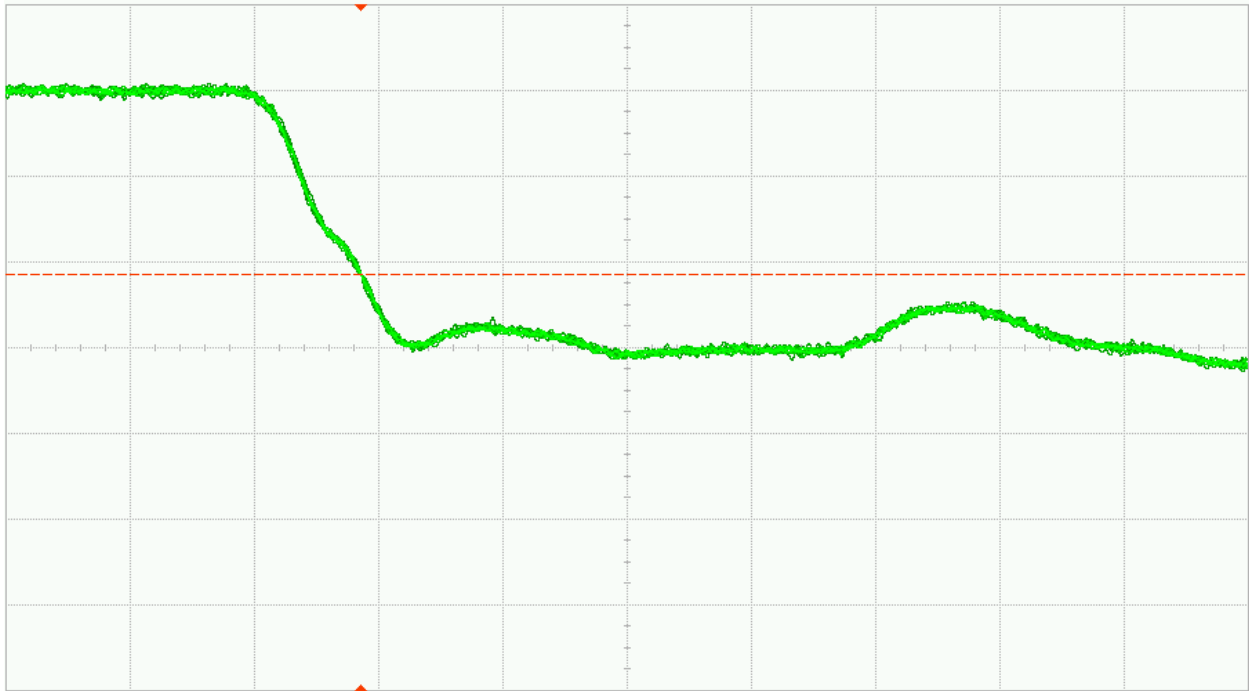


Fig. 35 (a). DUT 4009 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

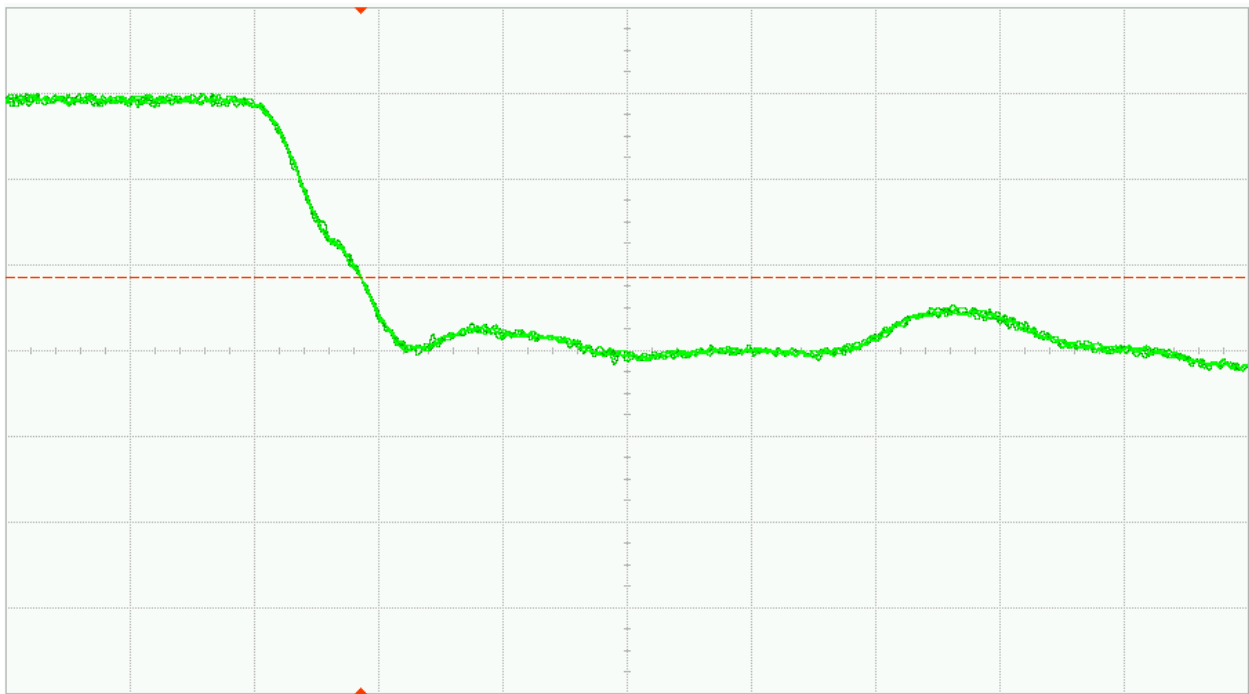


Fig. 35 (b). DUT 4009 post-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

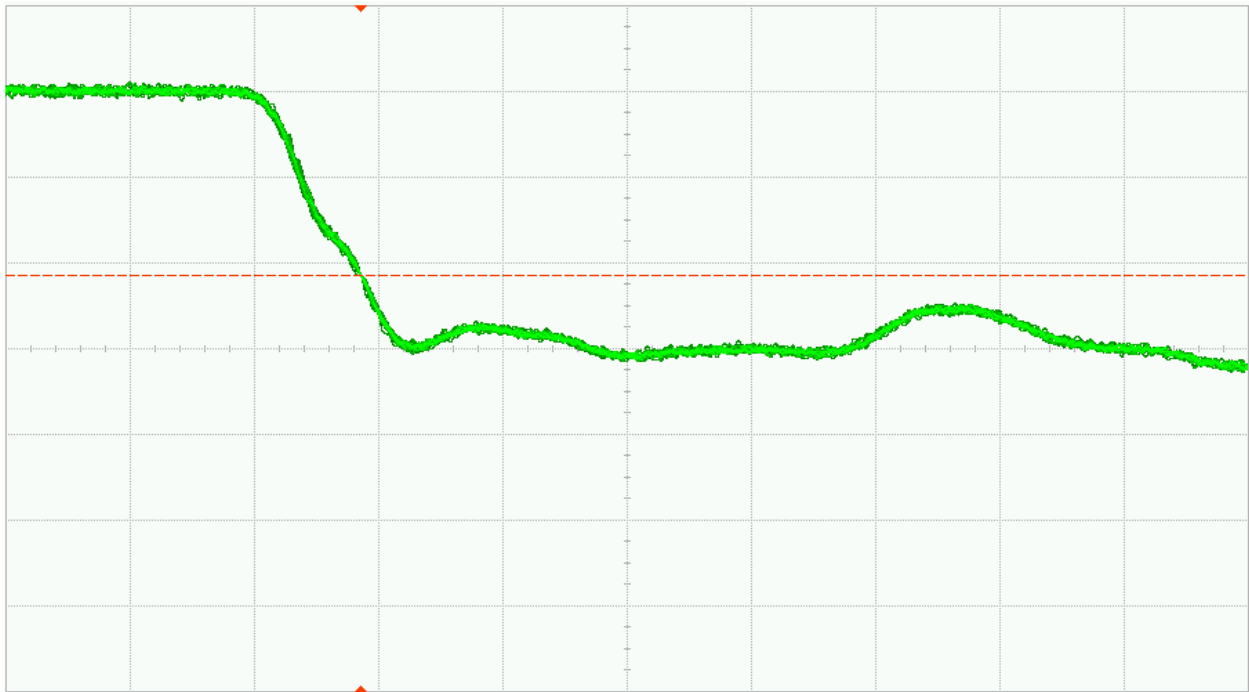


Fig. 36 (a). DUT 4017 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 36 (b). DUT 4017 post-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

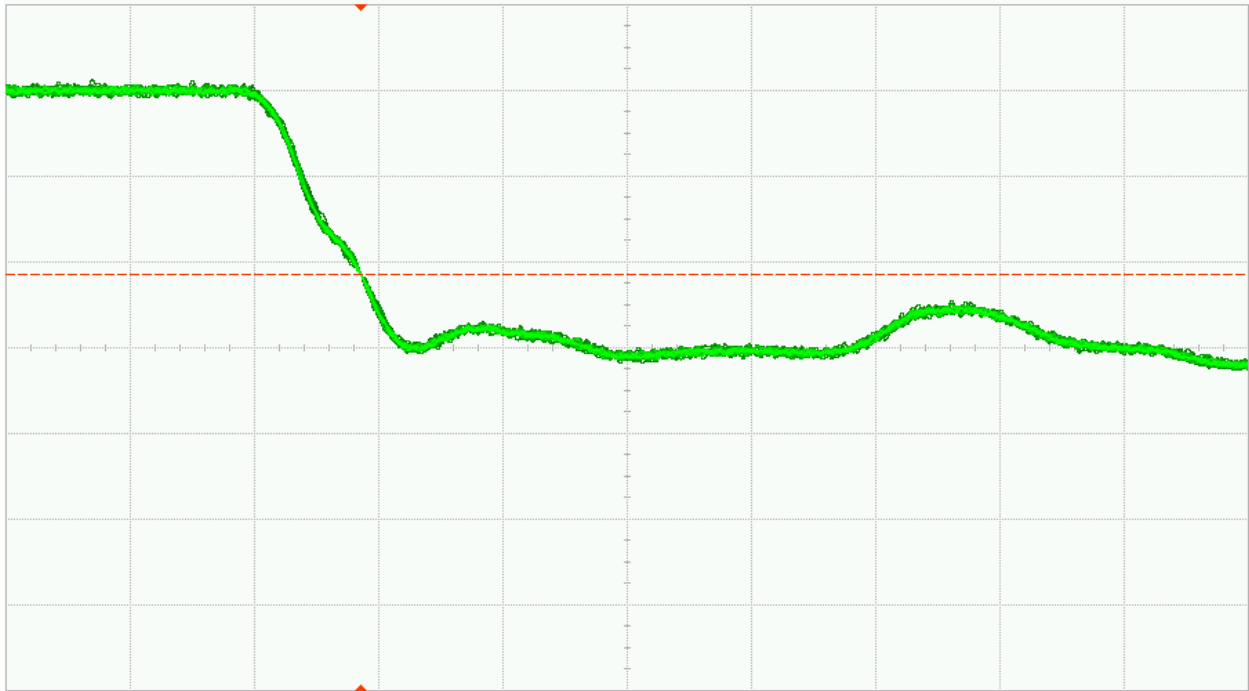


Fig. 37 (a). DUT 4037 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

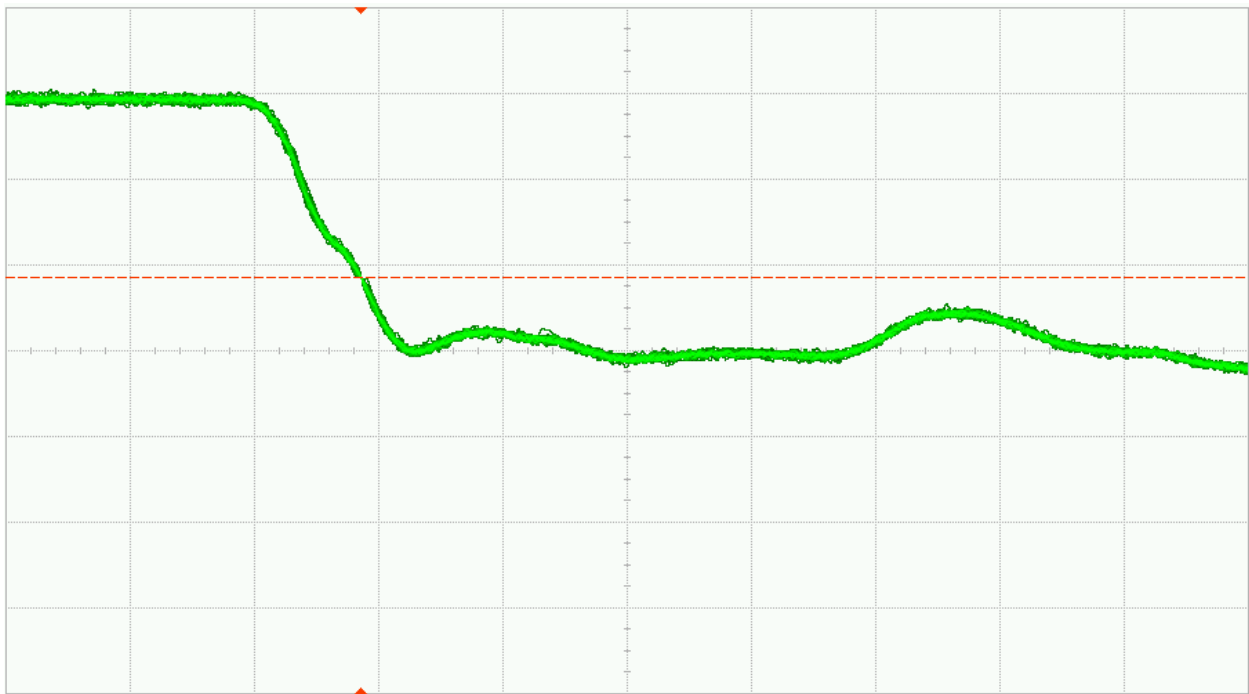


Fig. 37 (b). DUT 4037 post-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 35. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 μ RAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

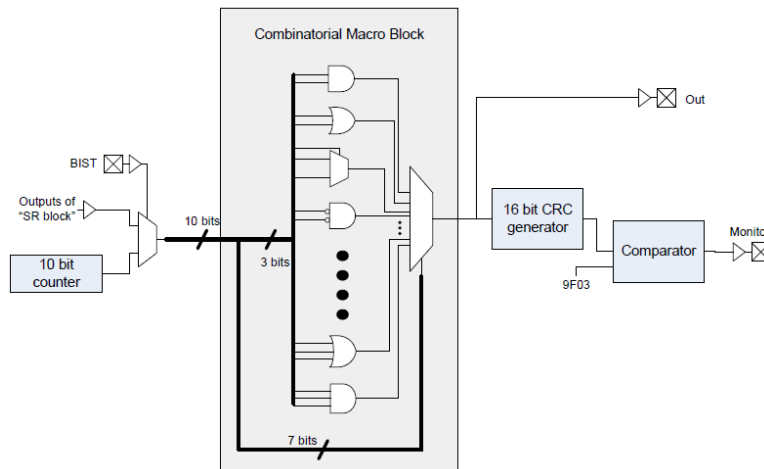


Fig. 38. Combo Block

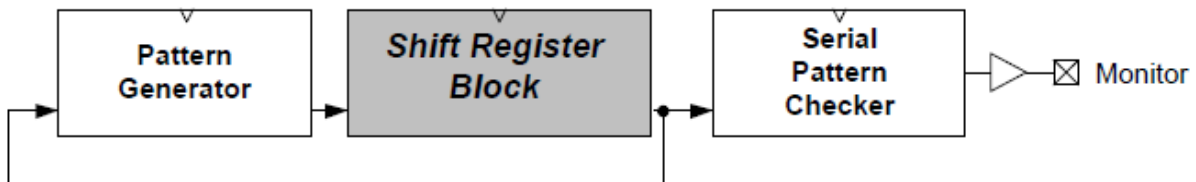


Fig. 39. Shift Register Block

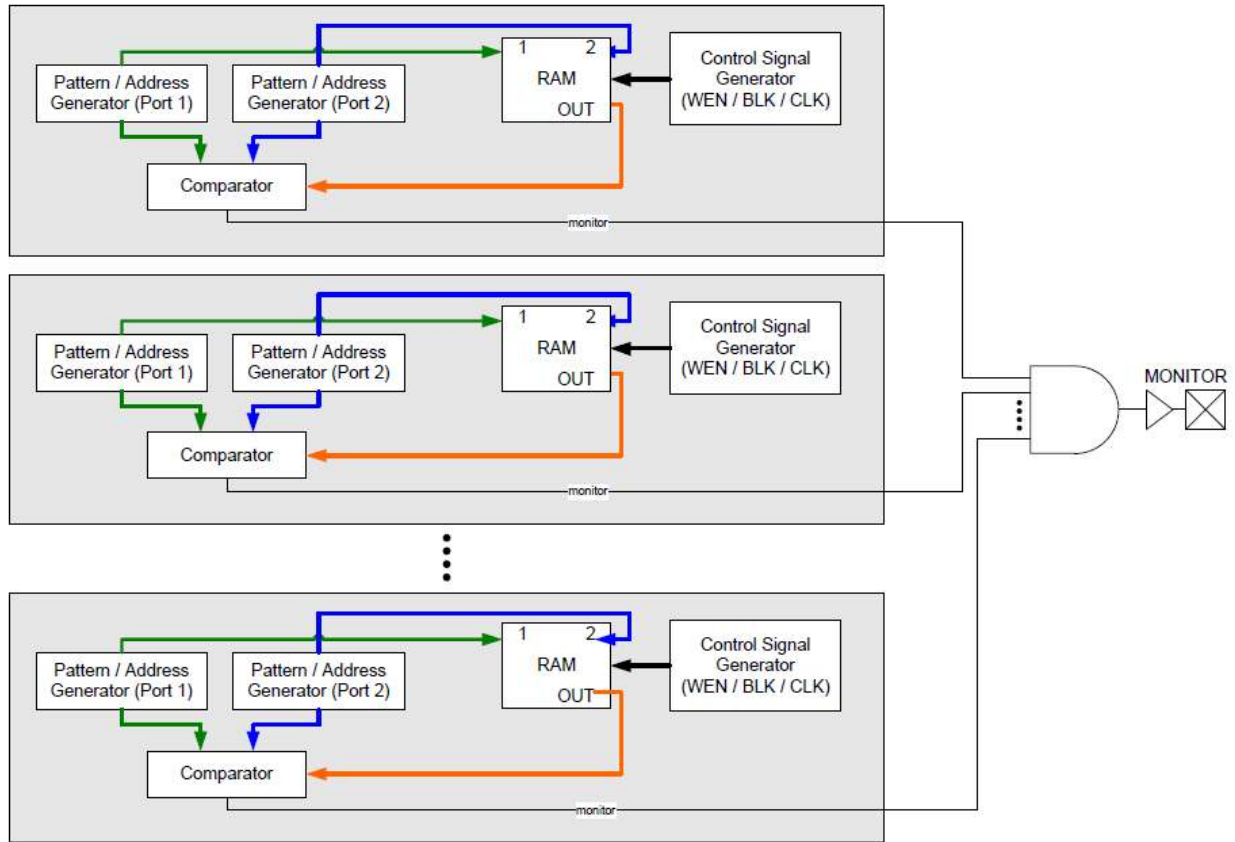


Fig. 40. Embedded Ram Blocks

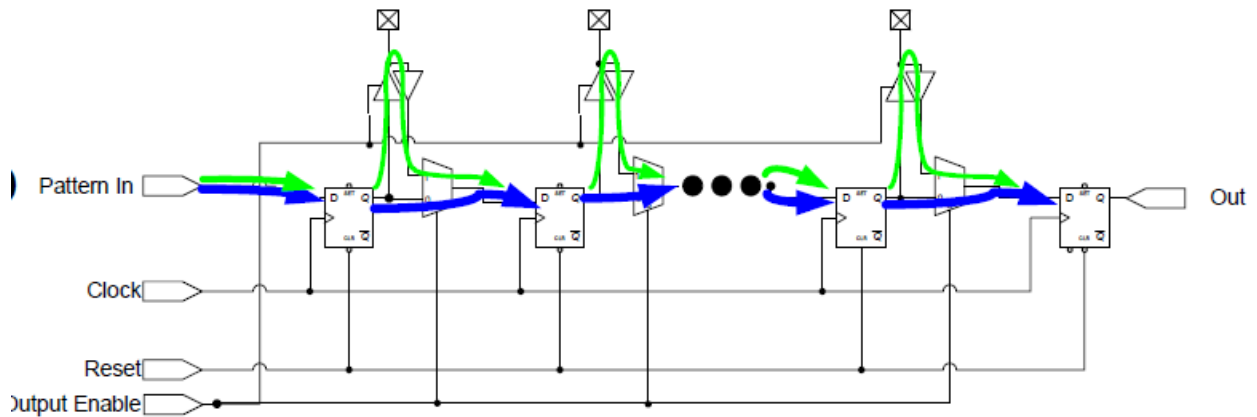


Fig. 41. IO Block

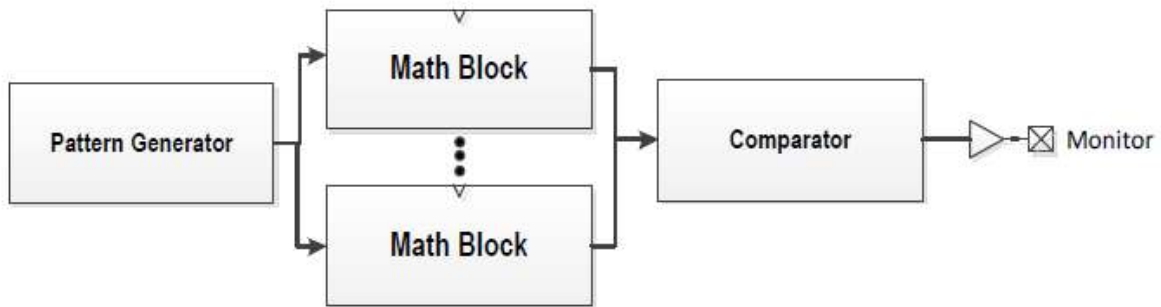


Fig. 42. Math Block



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