Total Ionizing Dose (TID) Radiation Testing of the Microsemi LX7720MFQ Power Driver (100krad(SiO_2) exposure)

Test information

Location: Defense Microelectronics Activity (DMEA) Science and Engineering Gamma Irradiation Test Facility in McClellan, California
Radiation Source: Co-60, Date: 10th September 2019
Lot #: Die1: U08301 - Die2: E49261
Quantity tested: 4; Serial Numbers: 18, 98, 99 and 102
Test Method: MIL-STD-883J, Test Method 1019.9, Condition A (Dose rate 50rad(SiO_2)/s)
Irradiation Temperature: Room
Irradiation Bias: VCC/VDD/VGS/DMOD_PS/VMPS/VEE: 5.5V/5.5V/18V/18V/60V/Internal VEE; CP Clock: 200kHz, Mod Clock: 24MHz
Annealing: Biased - Room temperature for 504 hours
Pre and Post Test facility: Microchip - San Jose

Summary

The LX7720 performance after 100krad(SiO_2) exposure is overall stable and comparable to pre-radiation.

A few shifts that could push some parameters outside the pre-radiation specifications were observed:

- ADC Converters
  - The THD can degrade by up to 4dB
- Floating Current Sense
  - The offset can vary by up to 2.0%FSR
  - The SNR can decrease by up to 6dB
  - The THD can degrade by up to 3dB
- MOSFET Drivers
  - Turn on delays typically increase from 250ns to 290ns or 460ns depending on the driver condition during irradiation
  - Turn off delays typically shift from 250ns to 235ns or 390ns depending on the driver condition during irradiation
  - Rise times typically increase from 70ns to 100ns or 140ns depending on the driver condition during irradiation
- Demodulator Driver
  - Turn on and off delays typically increase in high speed mode from 95ns to 112ns or 160ns depending on the driver condition during irradiation
  - Turn on and off delays typically increase in low speed mode from 112ns to 150ns or 200ns depending on the driver condition during irradiation
  - Rise and fall time also increase by different values depending on the driver condition during irradiation
- Internally generated negative supply VEE
  - At the minimum VGS voltage of 12V with internally generated VEE and using the maximum CP_CLK frequency of 300kHz, the VEE voltage drops below the minimum recommended voltage of -8V to about -7.6V.

Conclusions

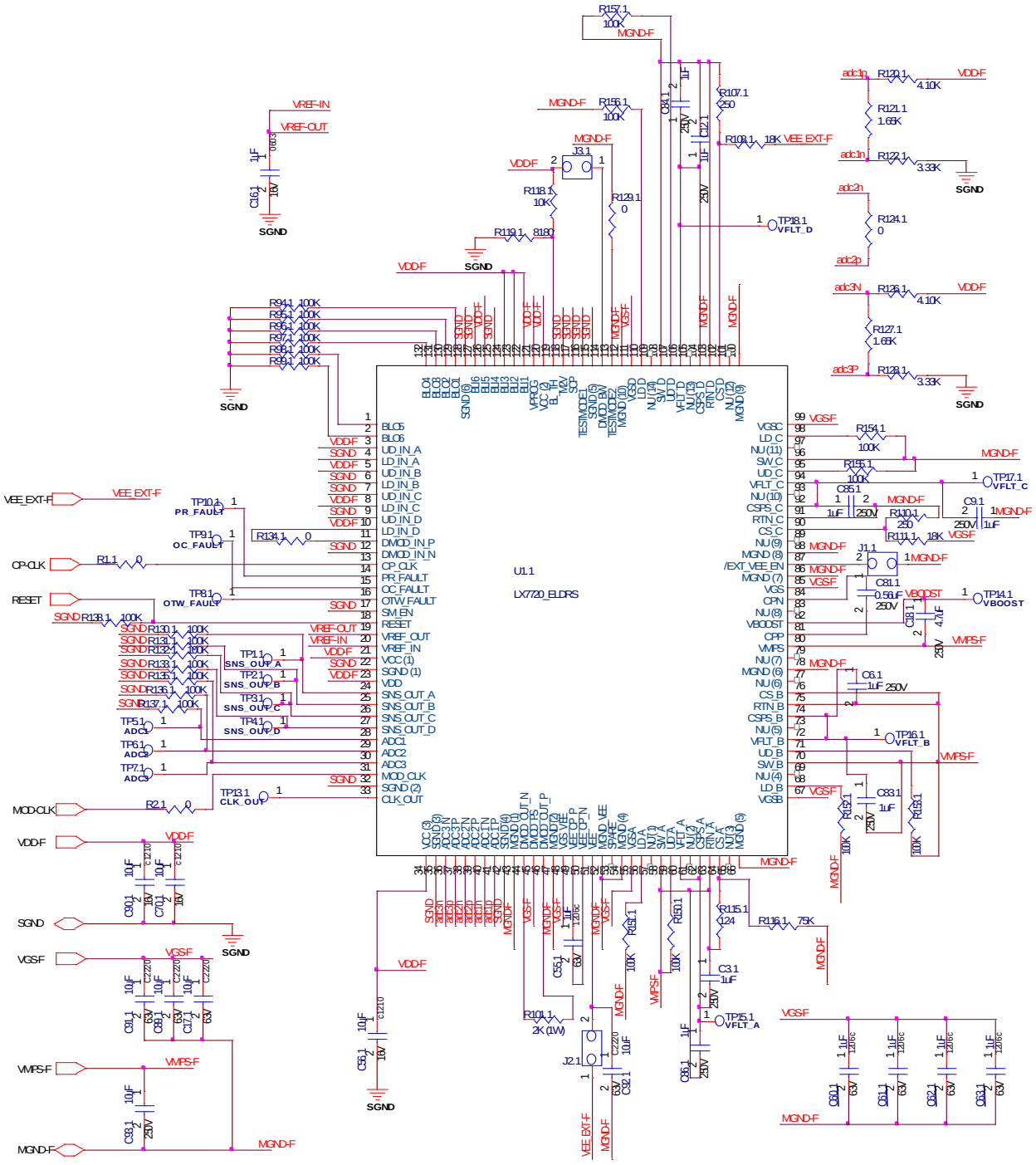
The test results indicate that after 100krad exposure, the performance of the LX7720 is consistent with the pre-radiation results.

The few observed performance variations can be mitigated at the system level as follows:

- Floating Current Sense
  - Offset can be measured and compensated at system level if necessary.
- MOSFET Drivers
  - The delays increase should not cause issues if adequate dead-time is used in the driving signals. Technical paper explaining optimization of driving timings is available on product's web page.

- Demodulator Driver
    - It is recommended to use the Demodulator driver in high speed mode if 100krad is expected
    - Delays asymmetry can be minimized by not driving static opposite signals for very long periods
- Internally generated negative supply VEE
    - It is not recommended to use the max CP_CLK frequency of 300kHz if minimum VGS voltage of 12V is used. The VEE voltage remains above the minimum recommended condition at CP_CLK of 100kHz and 200kHz.

Bias circuit



VCC/VDD/VGS/DMOD_PS/VMPS/VEE: 5.5V/5.5V/18V/18V/60V/Internal VEE; CP Clock: 200kHz, Mod Clock: 24MHz

Detailed Data

The pre-Radiation specifications apply over the operating ambient temperature of -55°C ≤ T_A ≤ 125°C except where otherwise noted with the following test conditions: VVCC= 5.0V, VVDD = 3.3V; VVREF_IN = 2.5V; VVGS=15.0V; VVEE =-15.0V (/EXT_VEE=GND); DMOD_PS=15.0V; VBL_TH=2.5V; MOD_CLK = 32MHz; CP_CLK = 200kHz, VMPS = 50V.Typical parameter refers to T_J = 25°C. Positive currents flow into the pin. THD is measured based on fundamental and harmonics up seventh order.

Pre and Post Irradiation measurements taken at 25C.

			Pre-Radiation Specification				SN018		SN098		SN099		SN102		
Symbol	**Parameters**	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Units**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Comment**
Operating Current															
I_{VCC}	VCC Current	All ADCs off, all current sense off	5	15	20	mA	15.79	15.73	15.82	15.74	15.66	15.59	15.84	15.79	Very Stable
		All ADCs on, all current sense off	25	46	55	mA	46.33	46.26	46.20	46.05	46.63	46.46	46.66	46.54	Very Stable
		All ADCs off, all current sense on	35	67	80	mA	67.28	67.09	67.19	66.91	67.45	67.22	67.70	67.50	Very Stable
		All ADCs on, all current sense off	60	98	120	mA	97.92	97.75	97.65	97.35	98.54	98.20	98.64	98.36	Very Stable
I_{VGS}	VGS Current	All UD_IN# and LD_IN# low	10	20	26	mA	19.80	19.63	19.69	19.62	19.18	18.98	18.69	18.72	Very Stable
		All LD_IN# and UD_IN# high	15	26	33	mA	27.09	26.06	26.61	25.88	26.07	25.25	26.17	25.48	Very Stable
I_{VEE}	VEE Current	All UD_IN# and LD_IN# low	-12	-8	-4	mA	-8.72	-8.62	-8.62	-8.58	-7.92	-7.77	-7.65	-7.65	Very Stable
		All UD_IN# and LD_IN# low; VEE = -15V; no load on DMOD_OUT_N/P; DMOD_IN_P high; DMOD_IN_N low; DMOD_BW low; DMOD_PS = 15V	-21	-14	-6	mA	-14.29	-13.97	-14.25	-13.92	-13.37	-13.01	-12.91	-12.62	Slight Decrease
I_{DMOD_PS}	DMOD_PS Current	No load on DMOD_OUT_N/P; DMOD_IN_P and DMOD_IN_N low; DMOD_BW low; DMOD_PS = 15V	0.2	1	1.5	mA	1.08	1.04	1.06	1.03	1.02	0.99	1.00	0.99	Very Stable
		No load on DMOD_OUT_N/P; DMOD_IN_P high; DMOD_IN_N low; DMOD_BW low; DMOD_PS = 15V	2	6	11	mA	6.05	5.83	6.12	5.83	5.91	5.70	5.73	5.48	Slight Decrease
		No load on DMOD_OUT_N/P; DMOD_IN_P high; DMOD_IN_N low; DMOD_BW high; DMOD_PS = 15V	4	10	17	mA	9.41	8.04	9.43	7.93	9.17	7.84	8.81	7.46	Slight Decrease
I_{VDD}	VDD Current	All LD_IN#=HI and UD_IN# =HI	0	25	42	mA	28.24	27.92	27.88	27.27	29.39	28.43	28.25	27.88	Very Stable
Under Voltage Detection															
V_{VCC}	VCC UVLO	Voltage rising; 200mV Hysteresis	4	4.25	4.5	V	4.24	4.24	4.16	4.16	4.23	4.23	4.27	4.27	Very Stable
V_{VDD}	VDD UVLO	Voltage rising; 200mV Hysteresis	1.6	1.8	2.0	V	1.77	1.77	1.78	1.78	1.78	1.78	1.77	1.79	Very Stable
$V_{VGS\ to\ MGND}$	VGS UVLO to MGND	Voltage falling; 200mV Hysteresis	9.1	9.4	9.8	V	9.51	9.64	9.44	9.63	9.44	9.63	9.46	9.61	Slight Increase
$V_{VGS\ to\ SGND}$	VGS UVLO to SGND	Voltage rising; 120mV Hysteresis	6.2	6.4	6.6	V	6.37	6.34	6.38	6.35	6.38	6.36	6.42	6.39	Very Stable
V_{VEE}	VEE_IN UVLO	Voltage falling; 350mV Hysteresis	-8	-7	-6	V	-6.81	-6.89	-6.94	-7.11	-6.99	-7.11	-7.06	-7.11	Stable
Internally Regulated Voltages and Currents															
V_{VREF_OUT}	VREF regulator		2.48	2.5	2.52	V	2.500	2.498	2.489	2.489	2.499	2.497	2.499	2.502	Very Stable
V_{VEE}	Inv Chg Pump	No external load; /EXT_VEE=open; V_{VGS} - |V_{VEE}|	1.0	1.9	2.4	V	1.93	2.07	1.99	2.07	1.88	1.98	1.85	1.96	Slight Increase
V_{VBOOST}	Charge Pump	Boot strap not connected;10mA load [V_{VGS} + V_{VMPS}] - V_{VBOOST}	0.5	1.6	2.1	V	1.71	1.72	1.70	1.71	1.69	1.72	1.70	1.71	Very Stable
V_{VBOOST} - $V_{VFLT\#}$	VBOOST switch	With UD_IN_# high, 4 mA load	0.05	0.3	0.6	V	0.252-0.268	0.31-0.358	0.257-0.259	0.321-0.358	0.247-0.254	0.31-0.349	0.251-0.257	0.313-0.359	Up to 0.12V increase
I_{VREF_OUT}	VREF regulator	Short Circuit Current	25	50		mA	42.5	42.6	42.8	42.9	44.2	44.5	42.9	43.1	Very Stable
$I_{VGS\ \#}$	Fault threshold	VGSA, VGSB, VGSC and VGSD fault current threshold	110		360	mA	130-265	125-265	210-290	220-295	205-240	205-285	145-314	125-308	Some variations
$I_{VGS\#}$	Fault blanking	VGS# spike duration to trigger fault with 400mA load	1.5	3.5		us	5.6-6.4	4.0-8.0	5.5-8.2	7.5-9.5	5.3-7.3	7.2-8.8	4.7-7.8	5.3-9.8	Some variations
I_{DMOD_PS}	Fault threshold	DMOD_PS fault current threshold	110		360	mA	225	195	155	125	250	235	230	235	Some variations

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I_{DMOD_PS}	Fault blanking	DMOD_PS spike duration to trigger fault with 400mA load	1.5	3.5		us	7.625	7.375	5.75	5.562	7.812	7.437	7	8.75	Some variations
Clocks															
F_{MOD_CLK}	MOD_CLK	Frequency range	24		32	MHz	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Very Stable
F_{MOD_CLK}	MOD_CLK missing	Minimum non-transition dead time		200		ns	102	90	92	83	94	86	107	95	Very Stable
P_{CLK_OUT}	CLK_OUT	Delay CLK_OUT to ADC# and SENS_OUT_#	0.5	7	12	ns	1.5-3.0	1.5-3.0	1.5-3.0	1.5-3.0	1.5-3.0	1.5-3.0	1.5-3.0	1.5-3.0	Very Stable
F_{CP_CLK}	CP_CLK	Frequency range	100	200	300	kHz	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Very Stable
MOSFET DRIVER (Cload = 1000pF)															
$R_{UD\_\#}$	Upper Driver Impedance	VFLT# to UD_#; UD_IN_# = high	0.85		10.0	Ω	3.43-4.57	3.69-5.03	3.43-4.56	3.69-4.95	3.38-4.57	3.67-5.00	3.37-4.52	3.72-4.92	Up to 13% increase
		UD_# to SW_#; UD_IN_# = low	0.85		10.0		3.72-4.34	4.03-4.63	3.71-4.31	4.03-4.61	3.71-4.34	4.02-4.63	3.68-4.29	4.01-4.61	Up to 11% increase
		UD_# to SW_#, VGS = 0 to UVLO			20k		13.04-13.08	13.06-13.11	13.02-13.05	13.04-13.08	12.89-13	12.92-13.03	13.06-13.12	13.09-13.14	Very Stable
$R_{LD\_\#}$	Lower Driver Impedance	VGS_OUT to LD_#; LD_IN_# = high	0.85		10.0	Ω	4.32-5.32	4.62-5.71	4.32-5.27	4.68-5.72	4.41-5.33	4.65-5.77	4.34-5.22	4.76-5.77	Up to 13% increase
		LD_# to MGND; LD_IN_# = low	0.85		10.0		4.64-4.96	4.97-5.35	4.63-4.93	4.94-5.3	4.64-4.97	4.97-5.36	4.61-4.92	4.99-5.37	Up to 10% increase
		LD_# to MGND; VGS = 0 to UVLO			20k		13.11-13.13	13.09-13.14	13.06-13.09	13.09-13.11	12.96-13.08	12.93-13.09	13.13-13.14	13.13-13.16	Very Stable
$t_{PHL,PLH}$	Propagation Delay	Upper Driver; UD_IN_# to UD_A	140	250	400	ns	209-262	230-474	224-270	215-460	229-280	225-481	238-284	217-498	See note 1
		Lower Driver; LD_IN_# to LD_A	140	250	400		231-268	230-453	241-265	220-445	243-275	223-507	244-282	228-508	See note 1
		Matching all drivers, all edges			150		58.5	244	46	245	51	284	46	291	See note 1
$t_{R,F}$	Rise time and Fall time	10% to 90%	20	60	120	ns	36-71	40-149	39-68	48-147	44-71	48-166	46-70	50-174	See note 1
$I_{UD\_\#}$	Leakage current with VGS and VCC = 0V	UD_#, SW_#, VFLT# wired together; VSW_# = 0V to 70V ref to MGND	-50		50	uA	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	Very Stable
$V_{UD\_\#}$	Upper drive voltage with 100% duty cycle	UD_IN# held High, UD_# loaded with 4 mA. Measured relative to VMPS	11.5		15	V	12.73-12.8	12.45-12.63	12.75-12.79	12.44-12.61	12.76-12.81	12.46-12.63	12.75-12.8	12.44-12.61	Up to 0.31V decrease
Internal bootstrap diodes															
V_{ON_B}	Forward voltage	IF = 100mA, Tj=25C	0.9		1.1	V	1.00-1.03	1.01-1.04	1.00-1.03	1.00-1.03	1.00-1.02	1.00-1.03	1.00-1.02	1.00-1.04	Very Stable
ADC Converters (with sinc3 filter and OSR = 256, input common mode = 2.1V unless otherwise noted)															
$FSR_{ADC\_\#}$	Max differential input	Clipping points of PDM output		+/-1400		mV	2.788-2.802	2.784-2.804	2.796-2.808	2.793-2.811	2.790-2.801	2.787-2.797	2.785-2.807	2.783-2.805	(as of full scale) Very stable
$SLR_{ADC\_\#}$	Specified linear range		+/-800			mV	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Very Stable
V_{CMR_ADC}	Input common mode	With Vdiff = +/-800mV and THD < $THD24/32_{ADC}$(Max) - 3dB	0.5		VCC-2.1V	V	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Very stable
V_{CMR_ADC}	Common mode rejection		43			dB	59.7-64.8	58.7-63.6	53.6-69.9	55.0-63.1	58.9-68.8	60.0-68.1	50.7-59.0	51.3-59.8	Slight variations
$BW_{ADC\_\#}$	Max frequency	With attenuation < 0.1dB	20			kHz	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Very stable
	Min frequency	By design			0	Hz	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Very stable
$AV_{ADC\_\#}$	Gain error	Tj=25C and 125C	-0.65		0.65	%	-0.06-0.43	-0.13-0.58	-0.27-0.15	-0.39-0.24	-0.03-0.37	0.11-0.47	-0.25-0.54	-0.18-0.60	Stable
V_{OS_ADC}	Offset error	Equivalent input for code measured to shorted inputs. Tj=25C	-0.05		0.05	%FSR	0.01-0.02	0.01-0.04	-0.02-0.03	-0.02-0.04	-0.02-0.01	-0.01-0.02	-0.02-0.02	-0.03-0.04	Up to 0.02%FSR variation
$INL24_{ADC}$	Integral Non-Linearity	Gain error from straight line at 24MHz	-0.03	+/-0.01	0.03	%FSR	-0.01-0.01	-0.01-0.01	-0.01-0.01	-0.02-0.01	-0.01-0.01	-0.02-0.01	-0.01-0.01	-0.01-0.01	Very stable
$INL32_{ADC}$	Integral Non-Linearity	Gain error from straight line at 32MHz	-0.06	+/-0.02	0.06	%FSR	-0.01-0.02	-0.01-0.02	-0.01-0.03	-0.01-0.01	-0.01-0.02	-0.02-0.02	-0.02-0.03	-0.01-0.02	Very stable
$RES24_{ADC}$	No missing codes	Histogram test using triangular wave	14	15		bits	15	15	14-15	15	15	15	15	15	Very stable

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	resolution at 24MHz														
$RES32_{ADC}$	No missing codes resolution at 32MHz	Histogram test using triangular wave	13	14		bits	15	15	14-15	15	14-15	15	15	15	Very stable
$SNR24_{ADC}$	Signal to Noise Ratio at 24MHz clock	Full scale sinewave RMS / noise RMS in 1kHz bandwidth	93	100		dB	98.9-99.1	97.4-100.0	98.6-100.3	98.3-99.8	98.9-99.8	96.1-99.2	97.9-99.9	97.5-99.7	Stable
$THD24_{ADC}$	Total Harmonic Distortion at 24MHz clock	Input frequency = 1kHz, amplitude = 800mV		-79	-73	dB	-79.5--78.6	-79.4--75.1	-78.7--78.1	-79.1--75.9	-79.6--78.3	-79.6--76.4	-79.6--79.3	-79.5--75.6	Up to 4dB degradation
$SNR32_{ADC}$	Signal to Noise Ratio at 32MHz clock	Full scale sinewave RMS / noise RMS in 1kHz bandwidth	92	98		dB	98.8-99.0	97.3-99.2	98.9-99.2	98.0-100.0	97.7-98.4	97.7-99.2	98.1-99.8	98.8-99.1	Stable
$THD32_{ADC}$	Total Harmonic Distortion at 32MHz clock	Input frequency = 1kHz, amplitude = 800mV		-78	-70	dB	-78.5--74.6	-78.6--74.2	-78.3--76.6	-76--74.4	-80.3--79.1	-79.3--76.0	-78.1--77.2	-77.1--74.4	Up to 4dB degradation
t_{SWTO}	ADC Timeout	ADC#_P= ADC#_N > **VSWTO** to cause ADC modulator sleep mode	225		325	us	282	282	282	282	282	282	282	282	Very stable
VSWTO	ADC timeout threshold		4.75	4.9	5	V	4.87-4.88	4.87-4.88	4.87-4.88	4.87-4.88	4.87-4.88	4.87-4.88	4.87-4.88	4.87-4.88	Very stable
$R_{ADC\#}$	Diff input resistance		50	250		kΩ	211-213	212-215	209-212	211-214	212-213	213-214	213-214	215-217	Very stable
Floating Current Sense (with sinc3 filter and OSR = 256, input common mode = 0V unless otherwise noted)															
$FSR_{CS\_\#}$	Max differential input	Clipping points of PDM output		+/-350		mV	699.7-701.0	699.7-701.1	700.2-701.3	700.2-701.5	699.2-700.2	699.5-700.4	698.9-701.1	698.6-701.0	(as of full scale) Very stable
$SLR_{CS\_\#}$	Specified linear range		+/-200			mV	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Very stable
E_{CMR_CS}	Input common mode induced gain error	Input common mode from 0 to 50V	-0.15		0.15	%	0.01-0.09	-0.13-0.02	0.01-0.07	-0.02-0.15	0.03-0.05	-0.08--0.03	-0.04-0.06	-0.12-0.11	Stable
V_{CMR_CS}	Input common mode rejection	CM = 50V	85			dB	96.3-105.4	98.8-102.9	98.7-127.7	98.1-110.3	99.5-116.1	97.7-113.3	96.4-118.5	96.2-110.3	Small variation
$BW_{CS\_\#}$	Max frequency	With attenuation < 3dB	75			kHz	-0.15--0.12	-0.13--0.12	-0.14--0.11	-0.14--0.10	-0.14--0.12	-0.13--0.11	-0.15--0.13	-0.14--0.13	Very stable (measured as attenuation at 75kHz
	Min frequency	With attenuation < 0.1dB			0	Hz	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Very stable
$AV_{CS\_\#}$	Gain error	Tj=25C	-0.5		0.5	%	-0.15-0.04	-0.16-0.04	-0.19--0.03	-0.21--0.03	-0.03-0.12	-0.06-0.08	-0.15-0.15	-0.15-0.21	Stable
V_{OS_CS}	Offset error	VCS_# = VRTN_#, Tj=25C	-0.4		0.4	%FSR	0.03-0.09	-2.0-2.0	-0.11-0.11	-1.15-0.58	-0.03-0.05	-1.77-1.14	-0.12-0.12	-1.25-0.38	Up to 2.0%FSR variation
$RES24_{CS}$	No missing codes resolution at 24MHz	Histogram test using triangular wave	14	14		bits	14-15	14-15	14-15	14-15	14-15	14-15	14-15	14-15	Very stable
$RES32_{CS}$	No missing codes resolution at 32MHz	Histogram test using triangular wave	13	14		bits	14-15	14-15	14-15	14-15	14-15	14-15	14-15	14-15	Very stable
$INL24_{CS}$	Integral Non-Linearity at 24MHz clock.	Gain error from straight line	-0.06	+/-0.03	0.06	%FSR	-0.02-0.02	-0.04-0.05	-0.02-0.02	-0.04-0.04	-0.02-0.02	-0.04-0.04	-0.02-0.02	-0.04-0.04	Slight Degradation
$INL32_{CS}$	Integral Non-Linearity at 32MHz clock.	Gain error from straight line	-0.06	+/-0.03	0.06	%FSR	-0.02-0.02	-0.04-0.04	-0.02-0.02	-0.04-0.05	-0.02-0.02	-0.04-0.04	-0.02-0.02	-0.04-0.05	Slight Degradation
$SNR24_{CS}$	Signal to Noise Ratio at 24MHz clock	Full scale sinewave RMS / noise RMS in 4kHz bandwidth, OSR=64	74	78		dB	80.2-81.6	75.0-76.1	80.1-81.5	75.4-77.0	80.4-81.3	76.4-78.1	80.7-81.5	75.2-77.1	Up to 6dB degradation
$THD24_{CS}$	Total Harmonic	Input frequency = 1kHz, amplitude = 200mV, OSR=64		-75	-65	dB	-76.9--73.5	-74.7--74.4	-78.5--76.7	-77.2--74.2	-77.7--75.2	-76.0--74.3	-76.9--73.8	-75.9--75.3	Up to 3dB degradation

			Pre-Radiation Specification				SN018		SN098		SN099		SN102		
Symbol	**Parameters**	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Units**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Comment**
	Distortion at 24MHz clock														
$SNR32_{CS}$	Signal to Noise Ratio at 32MHz clock	Full scale sinewave RMS / noise RMS in 4kHz bandwidth, OSR=64	73	77		dB	80-81.4	75.1-76.3	80.3-82.4	75.1-76.5	81.0-82.6	76.0-77.4	81.4-82.5	75.6-76.5	Up to 6dB degradation
$THD32_{CS}$	Total Harmonic Distortion at 32MHz clock	Input frequency = 1kHz, amplitude = 200mV, OSR=64		-75	-65	dB	-77--73.5	-74.6--74.2	-77.6--75.9	-74.4--73.0	-78.5--76.1	-76.8--74.7	-76.1--74.5	-76.6--73.5	Up to 3dB degradation
Z_{IN_CS}	Differential Input Imped.	CS_# to RTN_#	0.1	2		MΩ	>2	>2	>2	>2	>2	>2	>2	>2	Very stable
	Common mode	RTN# or CS# to MGND	50	150		kΩ	140-160	140-160	140-160	140-160	140-160	140-160	140-160	140-160	Very stable
IBIAS_CS#	CS# bias current		-0.2		0.2	mA	-0.09--0.08	-0.09--0.08	-0.09--0.08	-0.09--0.08	-0.09--0.08	-0.09--0.08	-0.09--0.08	-0.09--0.08	Very stable
IBIAS_RTN#	RTN# bias current		-1		1	mA	-0.73--0.71	-0.73--0.71	-0.73--0.71	-0.73--0.71	-0.73--0.71	-0.73--0.71	-0.73--0.71	-0.73--0.71	Very stable
$V_{CS\_\#}$	Over Current Sense Threshold	Current flow into SW_# pin	260	320	380	mV	325-349	310-352	304-316	298-319	313-343	313-349	322-337	316-346	Stable
		Current flow out of SW_# pin	-380	-320	-260		-328--292	-343--283	-334--316	-343--313	-328--307	-334--307	-319--304	-325--301	Stable
$V_{CS\_\#}$	Over Current Blanking	Spike filter pole	10		20	us	15.2-16.3	15.2-16.3	15.2-16.3	15.2-16.3	15.2-16.3	15.2-16.3	15.2-16.3	15.2-16.3	Very stable
ICS_#	Leakage current with VCPS_# and VCC = 0V	CPS_#, RTN_#, CS_# wired together; VCS= 0V to 70V referenced to MGND	-50		50	uA	-0.01-0.01	-0.01-0.01	-0.01-0.01	-0.01-0.01	-0.01-0.01	-0.01-0.01	-0.01-0.01	-0.01-0.01	Very stable
Fixed Threshold Bi-Level Inputs															
$V_{BLI\#}$	Threshold (Rising Voltage)		2.4	2.5	2.6	V	2.512-2.536	2.488-2.564	2.516-2.536	2.488-2.56	2.508-2.528	2.484-2.544	2.516-2.528	2.488-2.548	Up to 30mV variation
$V_{BLI\#}$	Hysteresis	Only falling edge has hysteresis	80	150	200	mV	146-150	142-150	142-154	138-154	142-146	142-146	142-150	138-146	Very stable
$V_{BLI\#}$	Voltage Clamp	Clamp Current = 1mA (into pin)	6.5	10	13	V	10.23-10.52	10.20-10.43	10.24-10.50	10.26-10.50	9.69-9.75	9.66-9.73	10.27-10.34	10.22-10.3	Very stable
		Clamp Current = 1mA (out of pin)	-1.9	-1.4	-0.9	V	-1.41--1.40	-1.41--1.40	-1.41--1.40	-1.41--1.40	-1.41--1.40	-1.41--1.40	-1.41--1.40	-1.41--1.40	Very stable
$I_{BLI\#}$	Bias Current	V_{BLI1}= 0V to 5V	-2	0	2	uA	0.72-0.73	0.72-0.73	0.72-0.73	0.72-0.72	0.69-0.70	0.70-0.71	0.71-0.72	0.71-0.72	Very stable
$I_{BLI\#}$	Leakage Current	V_{BLI1}= 0V to 5V; IC powered off	-1	0	1.2	uA	0.72-0.75	0.75-0.76	0.74-0.74	0.75-0.76	0.71-0.72	0.73-0.74	0.73-0.73	0.74-0.75	Very stable
$t_{BLI\#}$	Propagation Delay		10	40	80	ns	28.5-52.5	29.0-52.9	28.7-52.5	29.2-52.8	27.9-52.1	28.4-52.5	28.6-52.9	29.2-53.1	Very stable
V_{BL_TH}	Ext Threshold Pin Range		0.5		4.5	V	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Very stable
I_{BL_TH}	Threshold Pin Leakage	V_{BL_TH}= 0V to 5V	-1	0	1.5	uA	0.73	0.73	0.73	0.73	0.71	0.71	0.72	0.72	Very stable
Demodulator driver (differential load of 100Ω)															
$V_{DMOD\_OUT\_P,N}$	Voltage Range	Either output relative to MGND	10		18	V	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Very stable
$R_{DMOD\_OUT\_P,N}$	Source Impedance	WRT DMOD_PS; Sourcing current	0.8	2	4	Ω	1.99-2.00	2.15-2.18	1.97-1.98	2.15-2.17	1.98-2.00	2.15-2.17	1.97-1.97	2.15-2.19	Up to 0.20Ω increase
		WRT MGND; Sinking current	0.8	2	4		1.70-1.76	1.92-1.98	1.69-1.74	1.91-1.93	1.67-1.77	1.88-1.95	1.72-1.75	1.93-1.96	Up to 0.25Ω increase
$R_{DMOD\_OUT\_P,N}$	High-Z state Impedance	DMOD_IN_P/N inactive; WRT DMOD_PS or MGND	-50		50	uA	-0.1-0.1	-0.1-0.1	-0.1-0.1	-0.1-0.1	-0.1-0.1	-0.1-0.1	-0.1-0.1	-0.1-0.1	Very stable
t_{PHL}	Propagation Delay H to L	DMOD_IN_# to DMOD_OUT_#; DMOD_BW = HI	65		145	ns	95-101	119-156	95-101	119-154	94-102	120-154	96-103	123-162	See note 2
		DMOD_IN_# to DMOD_OUT_#; DMOD_BW = LOW	75		155		113-115	144-178	113-115	144-177	114-116	148-192	117-119	155-224	See note 2
t_{PLH}	Propagation Delay L to H	DMOD_IN_# to DMOD_OUT_#; DMOD_BW = HI	65		145	ns	95-99	112-159	95-100	110-156	93-99	110-156	95-100	114-164	See note 2
		DMOD_IN_# to DMOD_OUT_#; DMOD_BW = LO	75		155		112-114	148-191	112-113	146-180	112-113	149-192	116-116	156-246	See note 2
$t_{PHL,PLH}$	Propagation Delay	Matching between DMOD_OUT_P and DMOD_OUT_N; HL to HL and LH to LH, BW=HI		7	20	ns	6	37	6	35	8	35	7	40	See note 2

			Pre-Radiation Specification				SN018		SN098		SN099		SN102		
Symbol	**Parameters**	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Units**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Comment**
$t_{PHL,PLH}$	Propagation Delay	Matching between DMOD_OUT_P and DMOD_OUT_N; HL to HL and LH to LH, BW=LO		7	20	ns	4	47	5	46	5	47	5	50	See note 2
$t_{R,F}$	Rise time	10% to 90%, BW=HI	4	17	30	ns	14-15	19-32	13-13	19-29	13-15	18-30	13-15	19-33	See note 2
$t_{R,F}$	Rise time	10% to 90%, BW=LO	4	17	30	ns	14-16	18-33	14-15	18-30	14-15	30-31	15-15	26-36	See note 2
$t_{R,F}$	Fall time	10% to 90%, BW=HI	6	33	60	ns	32-33	62-65	31-32	59-63	32-34	60-66	34-35	62-71	See note 2
$t_{R,F}$	Fall time	10% to 90%, BW=LO	6	33	60	ns	39-40	61-63	38-39	60-65	39-40	62-63	41-41	61-71	See note 2
Logic Levels															
V_{LOG_IN} **VDD**	Input Logic Threshold for VDD related inputs Pins 3-13, 17-18, 31, 117	VIH	30		70	%VDD	51.1-51.6	49.8-52.3	51.1-51.6	49.8-52.3	50.9-51.4	49.4-51.6	51.1-51.6	50.0-52.3	Stable
		VIL	30		70	%VDD	46.6-47.4	45.7-47.9	46.5-47.4	45.7-47.9	46.1-46.8	45.0-47.2	46.5-47.2	45.7-47.7	Stable
		Hysteresis	100	160	220	mV	140-146	129-170	140-152	129-170	146-158	135-176	146-152	135-176	Stable
V_{LOG_IN} **other**	Input Logic Threshold for other input pins	VIH pin 87 (EXT_VEE)	0.25		1.2	V	0.68	0.73	0.68	0.73	0.68	0.73	0.68	0.73	Slight increase
		VIL pin 87 (EXT_VEE)	0.25		1.2		0.63	0.70	0.62	0.69	0.62	0.68	0.62	0.69	Slight increase
		VIH pin 114 (DMOD_BW)	0.4		1.8		1.06	1.06	1.06	1.08	1.08	1.06	1.06	1.08	Very Stable
		VIL pin 114 (DMOD_BW)	0.4		1.8		1.05	1.05	1.05	1.07	1.07	1.05	1.05	1.07	Very Stable
V_{LOG_OUT} **VDD**	Logic Output Levels for VDD related outputs Pins 1-2, 14-16, 24-30, 33, 129, 132	High Logic Level (100µA source)	3.0		VDD	V	3.27-3.30	3.27-3.30	3.27-3.30	3.27-3.30	3.27-3.30	3.27-3.30	3.27-3.30	3.27-3.30	Very Stable
		Low Logic Level (100µA sink)			0.3		0.01-0.04	0.01-0.04	0.01-0.04	0.01-0.04	0.01-0.04	0.01-0.04	0.01-0.04	0.01-0.04	Very Stable
I_{LOG_IN} **VDD**	Input currents for VDD related inputs	VLOG_IN = 3.3V (with pull down res)		4	7	µA	4.61-4.74	4.63-4.76	4.65-4.77	4.66-4.78	4.55-4.67	4.56-4.69	4.63-4.71	4.64-4.73	Very Stable
		VLOG_IN = 0V (with pull up res)	-7	-4			-4.73--4.56	-4.74--4.57	-4.73--4.59	-4.75--4.60	-4.64--4.58	-4.66--4.59	-4.69--4.63	-4.70--4.65	Very Stable
I_{LOG_IN} **other**	Input currents for other input pins	Pin 87 (EXT_VEE) V = 0V	-80	-38	-10	µA	-33.6	-33.3	-34.9	-34.6	-32.7	-32.4	-34.5	-34.2	Very Stable
		Pin 114, (DMOD_BW) V = 3.3V	10	37	80		32.0	30.7	32.8	31.3	31.7	30.4	32.7	31.1	Slight decrease
		Pin 114, (DMOD_BW) V = 0V	-1	0	1		-0.15	-0.08	-0.08	-0.08	-0.14	-0.08	-0.07	-0.09	Very Stable

Note 1: MOSFET Drivers timings

Upper Driver in the High condition during irradiation (UD_IN=High, SW is pulled to VMPS):

- The turn on delay increases typically from 250ns to 460ns.
- The rise time increases typically from 70ns to 140ns.
- The turn off delay decreases typically from 250ns to 235ns.
- Fall time are overall stable around 45ns.

Upper Driver in the Low condition during irradiation (UD_IN=Low, SW is pulled to MGND):

- The turn on delay increases from 250ns to 290ns.
- The rise time increases typically from 70ns to 100ns.
- The turn off delay increases typically from 250ns to 290ns.
- The fall time increases typically from 45ns to 60ns.

Lower Driver in the High condition during irradiation (LD_IN=High):

- The turn on delay increases typically from 260ns to 460ns.
- The rise time increase increases typically from 60ns to 135ns.
- The turn off delay decrease typically from 250ns to 240ns.
- The fall time is stable around 55ns with small variations

Lower Driver in the Low condition during irradiation (LD_IN=Low):

- The turn on delay increases typically from 260ns to 320ns.
- The rise time increase increases typically from 60ns to 100ns.
- The turn off delay increases typically from 250ns to 300ns.
- The fall time increases typically from 50ns to 60ns.

Note 2: DMOD Drivers timings

During irradiation, DMOD_P is high and DMOD_N is low.

DMOD_P in high speed mode:

- The turn on delay increases typically from 99ns to 160ns.
- The rise time increases typically from 15ns to 19ns.
- The turn off delay increases typically from 100ns to 120ns.
- The fall time increases typically from 35ns to 60ns.

DMOD_N in high speed mode:

- The turn on delay increases typically from 95ns to 112ns.
- The rise time increases typically from 13ns to 30ns.
- The turn off delay increases typically from 95ns to 155ns.
- The fall time increases typically from 33ns to 65ns.

DMOD_P in low speed mode:

- The turn on delay increases typically from 112ns to 200ns.
- The rise time increases typically from 14ns to 22ns.
- The turn off delay increases typically from 115ns to 145ns.
- The fall time increases typically from 40ns to 62ns.

DMOD_N in low speed mode:

- The turn on delay increases typically from 113ns to 148ns.
- The rise time increases typically from 16ns to 35ns.
- The turn off delay increases typically from 112ns to 190ns.
  The fall time increases typically from 40ns to 62ns.