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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0
Updated for Libero SoC v12.6.

1.2 Revision 1.0
The first publication of this document.
Microchip's PolarFire® SoC FPGAs include industry's first RISC-V based Microprocessor Subsystem (MSS) and a fabric that inherits all the features of the PolarFire family. The PolarFire SoC MSS includes 5x 64-bit RISC-V processor cores, AXI Switch, DDR Controller, fabric Interface Controllers (FIC), and a rich set of peripherals. For more information about the PolarFire SoC MSS and its components, see UG0880: PolarFire SoC FPGA MSS User Guide. PolarFire SoC FPGAs are ideal for running BareMetal applications.

PolarFire SoC standalone MSS Configurator (no separate license required) facilitates independent configuration of MSS for use in Libero® SoC and SoftConsole. The standalone MSS configurator provides a seamless interface and can be used by Embedded Software developers and FPGA designers. For more information, see PolarFire SoC Standalone MSS Configurator User Guide. FPGA designers can add fabric components by using Libero SoC SmartDesign and IP Library.

Microchip's MPFS-ICICLE-KIT features the MPFS250T_ES SoC FPGA, a rich set of peripherals, ROM, and RAM options. For ROM requirement, the kit includes an 8 GB eMMC Flash memory. For external RAM requirement, the kit includes a 2 GB LPDDR4 device. The kit also features an SD Card slot. For more information, see UG0882: PolarFire SoC FPGA ICICLE Kit User Guide.

This application note describes how to run BareMetal user applications on MPFS-ICICLE-KIT.

2.1 Prerequisites

Before running the BareMetal user applications, the ICICLE kit must be programmed with the ICICLE reference design. Ensure to follow the documentation provided on GitHub and program the ICICLE kit reference design with one of the FlashPro Express programming files.
Running the BareMetal User Applications

Before you start, ensure to program the ICICLE KIT as described in Prerequisites. After successful programming, the following user applications can be run:

- System Services
- Single-Bit Error Detection and Correction for L2 LIM
- MicroPython

This document describes the steps to run the System Services application.

**Note:** For information about running other BareMetal user applications, see the [baremetal_applications GitHub](https://github.com) web page.

### 3.1 System Services

System Services SoftConsole project includes the following source files for running System Services:

- BareMetal MSS System Services driver which is available at the following location: https://github.com/polarfire-soc/polarfire-soc-bare-metal-library/tree/master/src/platform/drivers/mss_sys_services
- PolarFire SoC hardware abstraction layer source code (`mpfs_hal`). Using the `mpfs_hal` code, the user can access all of the PolarFire SoC MSS registers like E51 and U54 local interrupt registers, L2 cache, MPU, segmentation blocks, and others registers. This folder also includes the MSS peripherals base address file.

**Note:** Hardware parameters like MSS clocks, memory, and peripheral source files are generated in SoftConsole using the MSS XML configuration file. The MSS XML configuration file is available at https://github.com/polarfire-soc/icicle-kit-reference-design/tree/master/XML.

#### 3.1.1 Running the System Service Application

This section describes how to launch the System Services application in debug mode using SoftConsole and run the PolarFire SoC System Services via serial interface.

**Note:** This SoftConsole project can also be built in release mode and run from eNVM. Select Run > External Tools > PolarFire SoC program non secure boot mode 1 option to program the eNVM with the application and execute it.

To run the System Services:

1. Launch SoftConsole with the provided System Services project.
2. Click Run->Debug Configurations.

![Figure 1 • Debug Configurations](image-url)
3. In the Debug Configurations window, select the debug project highlighted in Figure 2.
4. Select the **Debug** option in the dialog box for launching the application in debug mode.

**Figure 2** • Launching the Debugger

5. In the **Confirm Perspective Switch** window, click **Switch** to go to the debug view.

**Figure 3** • Confirm Perspective Switch Message

The debugger stops at the `void e51 (void)` startup function in the `e51.c` file. This function initializes the UART interface and sends a software interrupt to the U54_1 processor core and releases it from the wait for interrupt mode (WFI). The `u54_1` hart starts executing the System Services functions.
6. Click Resume to start running System Services application as shown in Figure 4.

**Figure 4 • Resume Debugging**

7. System Services options are displayed on the terminal, as shown in Figure 5. For information about each System Service and output bit fields, see UG0905: PolarFire SoC FPGA System Services User Guide.

**Figure 5 • System Services Options**

8. Enter 1 to select **Read Device Serial Number**.
   The 128-bit Read Device Serial Number (DSN) is displayed, as shown in Figure 6.

**Figure 6 • Read Device Serial Number**

Each PolarFire SoC FPGA device has a unique, publicly readable, 128-bit DSN. The DSN can be used in cryptographic protocols to uniquely identify the device. For more information, see UG0918: PolarFire SoC FPGA Security User Guide.

9. Enter 2 to select **Read Device User-code**.
   This can be configured in the Libero SoC project from Design flow->Program Design->Configure Programming Options.
   The 32-bit device USERCODE/Silicon signature is displayed, as shown in Figure 7.

**Figure 7 • Read Device User-code**

Note: In the Libero project, this USERCODE/silicon signature can be configured from Design flow->Program Design->Configure Programming Options. If the values are not entered, you can see zero.

10. Enter 3 to select **Read Device Design-info**.

**Figure 8 • Read Device Design-info**
The device design information consists of:

- 256-bit user-defined Design ID.
- 16-bit design version: This can be configured from Design flow->Program Design->Configure Programming Options. In auto update programming, the current design version is compared with the available images in external SPI flash to initiate the auto update on power up.
- 16-bit design back-level: This can be configured from Design flow->Program Design->Configure Security. When back level protection is enabled, the device can only be programmed if the target design version is more than the back-level value.

11. Enter 4 to select **Read Device certificate**.
   The device supply chain assurance certificate is displayed, as shown in Figure 9.

*Figure 9 • Read Device Certificate*

The Device Certificate is a 1024 bytes Microsemi-signed X-509 certificate programmed during manufacturing. The certificate is used to guarantee the authenticity of a device and its characteristics.
12. Enter 5 to select **Read Digest**.
   The 576 bytes Digest contains the fabric digest, sNVM digest, and user key digests. The digest protects data integrity. **Figure 10** shows the 576 bytes digest.

**Figure 10 • Read Digest**

13. Enter 6 to select **Query Security**.
   The non-volatile states of user security lock is displayed, as shown in **Figure 11**.
   The design does not include any user security settings for device security. Security locks can be configured from Design flow->Program and Debug Design->Configure Security.

**Figure 11 • Security Locks**

14. Enter 7 to select **Read Debug Information**.
   The debug information is displayed, as shown in **Figure 12**. In **Figure 12**, the highlighted 4 bytes E1000000 (LSB first) indicates the number of times the device was programmed (programming cycles).

**Figure 12 • Read Debug Information**

15. Enter 8 to select **Digital Signature**.
The digital signature in both Raw and DER formats is displayed, as shown in Figure 13.

**Figure 13 • Digital Signature**

The digital signature service takes a user supplied SHA384 hash and signs it with the devices private key. The application randomly generates the SHA384 hash value. The Digital Signature service sends the hash value to the System Controller. The System Controller Cryptoprocessor runs the Elliptic Curve Digital Signature Algorithm (ECDSA) using the hash and the device private key to generate the signature.

16. Enter 9 to select PUF Emulation service.

The PUF emulation service provides a mechanism for authenticating a device, or for generating a pseudo-random bit strings that can be used for different purposes. When this service is selected, the service by default accepts a 128-bit challenge and an 8-bit optype, and returns a 256-bit response unique to the challenge and the optype as shown in Figure 14.

**Figure 14 • PUF Emulation Service**

17. Enter “a” to select **Nonce service**.

The 32 bytes nonce value is generated by the device as shown in Figure 15.

**Figure 15 • Nonce Value**

This concludes the running System Services application and the SoftConsole debug session can be terminated.