Libero SoC v11.9 SP6 Release Notes

Introduction

The Libero® system on chip (SoC) v11.9 SP6 is a service pack release of the Libero SoC v11.9 software for designing with Microsemi's power efficient flash FPGAs, SoC FPGAs, and rad-tolerant FPGAs. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

To access datasheets, silicon user guides, tutorials, and application notes, visit www.microsemi.com, navigate to the relevant product family page, and click the **Documentation** tab. Development Kits & Boards are listed in the **Design Resources** tab.

Note: Enhancements and new features for SmartFusion2, IGLOO2, and RTG4 device families will no longer be added to the Libero SoC v11.9 software branch. Please create new projects in **Libero SoC v12.5** release or later using the **Enhanced Constraints Flow**.

Note: This release will be the final release in which the Classic Constraint Flow is supported for SmartFusion2, IGLOO2, and RTG4 device families. Subsequent releases will support only the Enhanced Constraint Flow. Consider migrating such designs to a new project using the **Enhanced Constraints Flow**. Refer to the Migration Guide.

Table of Contents

1. Customer Notification (CN) and Customer Advisory Notification (CAN) Support

Libero SoC v11.9 SP6 includes changes that address certain important issues. For more information about these issues, refer to www.microsemi.com/company/quality/product-notifications/cn/asic-soc-fpga.

1.1 RTG4 SET Filter Delay Calibration Update

RTG4 devices employ Single Event Transient (SET) filters for SET mitigation. These filters are optionally available for flip-flops in Fabric LEs, IOFF, Math blocks, and SRAM blocks via Libero SoC's global SET mitigation setting or the NDC set_mitigation constraint. SET mitigation is built into the SerDes and FDDR flip-flops. SpaceWire clock and data recovery circuits embedded in the CCCs include a similar, delay-based glitch filter. Libero SoC v11.9 SP6 includes an update to ensure SET filters use the intended, Process, Voltage, and Temperature (PVT)-compensated delay values (600ps typical) from the built-in Delay Calibration (DELCAL) circuits located at the SE and NE device corners.

Previous versions of Libero allowed SET filers to use an unintended filter delay value. This may result in incorrect ECC operation of LSRAMs in non- pipelined ECC mode with SET mitigation enabled.

Refer to 3. Migrating an Existing RTG4 Design to Libero SoC v11.9 SP6 for instructions about migrating a design to Libero SoC v11.9 SP6. For more information, refer to PCN20005.

1.2 RTG4 SERDES and FDDR PLL Enhanced Calibration

RTG4 PLLs can experience loss of lock at high temperature after being initialized, via device power-up or PLL reset, at cold temperature. Once loss of lock occurs, the PLL lock can be recovered by issuing a reset to the PLL. Libero SoC v11.9 SP6 enhances the calibration of the single-thread PLLs in the Fabric DDR controller PLL (FPLL) and for the SerDes PLL (SPLL) in the XAUI and PCI Express physical coding sublayer so that the VCO is provided with additional gain at reset, and is capable of maintaining lock throughout the entire military temperature operating range. FDDR and SerDes configuration cores will generate enhanced CoreABC initialization microcode that applies the PLL calibration sequence during the subsystem initialization.

There is no core invalidation. Refer to 3. Migrating an Existing RTG4 Design to Libero SoC v11.9 SP6 for instructions about migrating a design to Libero SoC v11.9 SP6.

For more information, refer to CN19009B.

1.3 RTG4 LSRAM Write Byte Enable Control Signals

RTG4 Two-port and Dual-port LSRAM configurators in Libero SoC v11.9 SP6 expose Write Byte Enable control signals (WBYTE_EN for Two-port LSRAM and A_WBYTE_EN, B_WBYTE_EN for Dual-port LSRAM). You can apply these signals to design a handshake circuit for accessing LSRAM data through SmartDebug. For more information, refer to CN19001 RTG4 LSRAM Data Errors When Accessing SmartDebug.

1.4 Timing Paths May be Missing from Static Timing Analysis (STA) for the SmartFusion2, IGLOO2, and RTG4 Families

Ongoing software quality testing on Libero SoC has found minor Static Timing Analysis (STA) coverage issues, preventing complete analysis of the path through combinational cells for specific scenarios for the SmartFusion2, IGLOO2, and RTG4 Product Families. Libero SoC v11.9 SP6 addresses these issues, allowing SmartTime to produce a complete static timing analysis.

For more information, refer to CN20022.

2. What's New in Libero SoC v11.9 SP6

Libero SoC v11.9 SP6 includes the following features and enhancements.

2.1 RT ProASIC3 Total Ionizing Dose Range

Libero SoC v11.9 SP6 extends the Total Ionizing Dose (TID) range of RT ProASIC3 designs from 25 to 30 Krad.

2.2 Export IBIS files for Fusion, IGLOO, ProASIC3, and RT ProASIC3 Devices

Libero SoC v11.9 SP6 enables IBIS file export for the following devices:

Family	Die	Package	Range
ProASIC3	A3PN250	100 VQFP	COM, IND
ProASIC3	A3PN020	68 QFN	COM, IND
ProASIC3	A3PN015	68 QFN	COM, IND
ProASIC3	A3PN010	48 QFN	COM, IND
ProASIC3	A3P1000	484 FBGA	MIL
IGLOO	AGLN250V2	100 VQFP , 81 CS	COM, IND
IGLOO	AGLN250V5	100 VQFP , 81 CS	COM, IND
IGLOO	AGLN125V2	100 VQFP , 81 CS	COM, IND
IGLOO	AGLN060V2	100 VQFP , 81 CS	COM, IND
IGLOO	AGLN060V5	100 VQFP , 81 CS	COM, IND
IGLOO	AGLN020V2	81 CS, 68 QFN, 81 UC	COM, IND
IGLOO	AGLN020V5	81 CS, 68 QFN, 81 UC	COM, IND
IGLOO	AGLN015V2	68 QFN	COM, IND
IGLOO	AGLN015V5	68 QFN	COM, IND
IGLOO	AGLN010V2	48 QFN, 36 UC	COM, IND
IGLOO	AGLN010V5	48 QFN, 36 UC	COM, IND
IGLOO	AGL400V2	144 FBGA, 256 FBGA, 484 FBGA	COM, IND
ProASIC3L	RT3PE600L	484 CCGA, 484 LGA	MIL
ProASIC3L	RT3PE3000L	484 LGA, 896 LGA	MIL
Fusion	AFS600	256 FBGA K, 484 FBGA K	EXT
Fusion	AFS1500	256 FBGA K, 484 FBGA K	EXT

2.3 RTG4 ODT Model to the Exported IBIS File

Libero SoC v11.9 SP6 adds the on-die-termination (ODT) model to the exported IBIS model for RTG4 designs.

3. Migrating an Existing RTG4 Design to Libero SoC v11.9 SP6

With Libero SoC v11.9 SP6, users opening existing designs have the choice to continue using the standard RTG4 FCCC core or manually migrating to the RTG4 FCCC with Enhanced PLL Calibration core.

Continuing with the PLL instantiated via the standard RTG4 FCCC core means that the PLL lock stability will be dependent on the operating junction temperature as discussed in CN19009. Users are encouraged to review the CN and confirm the supported temperature rise window for each PLL used in the design via the PLL Temp Rise Window calculator spreadsheet.

Migrating to the PLL instantiated in the RTG4 FCCC core with Enhanced PLL Calibration means that the non-triplicated fabric PLL lock stability is no longer dependent on the operating junction temperature.

Migration from the standard RTG4 FCCC core to the RTG4 FCCC with Enhanced PLL Calibration is recommended in the following scenario:

- The non-triplicated RTG4 Fabric PLL is used in the design and the application must support operation at a junction temperature rise window beyond that predicted by the PLL Temp Rise Window calculator described in CN19009.

Designs using the FCCC without the PLL or with triplicated PLL (internal feedback) do not need to migrate to the Enhanced PLL Calibration core unless the CCC shares the device corner with another fabric CCC that is using the non-triplicated PLL. Designs using the triplicated PLL (via PLL internal feedback) can only use the standard FCCC core because enhanced PLL calibration is not supported in this mode due to the reason described in CN19009B.

3.1 RTG4 Filter Calibration Design Invalidation and RTG4UPROM Core Update

As a result of PCN20005, all RTG4 designs with completed programming file are invalidated upon migrating a project created in a Libero release prior to v11.9 SP6 to Libero SoC v11.9 SP6. Completed designs that do not use the uPROM will not require re-running Place & Route, unless that step is invalidated due to other required updates, per the Libero SoC log window.

In the uPROM, total number of available 36-bit words has been reduced from 10,400 to 10,370. This allows space to be reserved for the instructions required to calibrate the filter delay.

New designs are not affected by this upgrade because they will use the updated RTG4UPROM core.

However, completed designs containing uPROM instance require a uPROM core version upgrade and revert to a pre-synthesis/pre-compile state.

Existing designs are impacted as described below:

- If the design does not contain a uPROM component, Libero SoC v11.9 SP6 will not invalidate Place and Route, but will invalidate “Generate FPGA Array Data”, “Generate Bitstream”, “Export Bitstream”, and “Export FlashPro Express Job”. The impacted flows must be rerun.
- If the design contains a uPROM component, Libero SoC v11.9 SP6 will invalidate “Synthesize” /“Compile”:
  - See 3.4 Core Update Procedure for information about how to update a core. Upgrade the uPROM component to v2.0.100 and rerun the entire flow. The run will fail if the clients exceed 10,370 words.
  - For a netlist-only project, regenerate the uPROM and rerun synthesis outsideLibero.

Rerun the tool flow, including “Generate FPGA Array Data” and “Generate Bitstream” steps. Reprogram device with updated bitstream.

3.2 RTG4 SERDES and Fabric DDR Core Update

As a result of CN19009B, the enhanced PLL calibration cores for FDDR PLLs and SerDes PLLs are included in the Libero SoC v11.9 SP6 software release and must be integrated into existing designs for the enhanced calibration to be applied to FDDR PLL and SerDes SPLL. With this update, all single-thread RTG4 PLLs will have lock stability independent of junction temperature rise during operation within datasheet limits.

See 9.1 RTG4 SPLL and FPLL Calibration and Workaround for details about the enhanced PLL solution for FDDR and SerDes PLL.

See 3.4 Core Update Procedure for information about how to update a core.

3.3 Summary of Migration Steps

1. Note the configuration of each CCC instantiated in the existing design. This can be done by either opening the configuration GUI for each CCC and saving screenshots of each tab, or by opening the CCC configuration report for each component instance.
   – Opening Existing CCC GUI: When opening an existing CCC in Libero SoC v11.9 SP6, the instance version must first be updated to RTG4 FCCC **v2.0.104** by right-clicking the component in the Design Hierarchy pane and selecting “Replace Component Version”

   Note: PLLs configured to Lock Window settings of 500 ppm or 1000 ppm will have their respective Lock Window setting reset to the 6000 ppm default

   – Using CCC configuration report: The configuration report is an XML file found in the example path shown below:
   `<libero_prj_folder>/component/work/<ccc_comp_name>/<inst_name>/<ccc_comp_name>_<inst_name>_configuration.xml`

   Note: The XML file can be viewed in a web browser if the rptstyle.xsl file is placed in the same folder as the XML file, before opening the file. The rtpstyle.xsl can be found in the Libero project folder path below:

   `<libero_prj_folder>/designer/<top_level_inst_name>/rptstyle.xsl`
2. Note the location and CCC number for each CCC instantiated in the existing design and group them by device corner (NW, NE, SW, or SE) and CCC number (0 or 1). This information is found in the Global Net Report available after running the Place and Route design flow step. Refer to the CCC Input Connections table for the CCC Location column to identify the die corner (NW, NE, SW, or SE) and CCC number (0, or 1). For example, a CCC Location can be listed as CCC-SE1 for CCC #1 in the Southeast corner.
   – The Global Net Report can be viewed in the Libero Reports tab under the Place and Route report list or by opening the file directly in a web browser from the default file location within the project folder. The file name format follows the convention: `<top_level_inst_name>_glb_net_report.xml` and it can be found in the project folder path `<libero_prj_folder>/designer/<top_level_inst_name>/`.
3. Delete all existing CCC instances that are being migrated to the CCC with Enhanced PLL Calibration, even those not using the PLL, if they share the device corner location with a PLL that *is* being migrated.
4. Configure a new instance of RTG4 FCCC with Enhanced PLL Calibration **v2.1.009** for each pair of CCCs being migrated.
   – Use the CCC configurations noted in step 1 above for each CCC location per device corner, ensuring that respective settings are mapped to the correct CCC tab in the configuration GUI for CCC_0 and CCC_1.
   – Refer to the RTG4 FCCC with Enhanced PLL Calibration Configurator User Guide for information about using the configurator GUI.
   – Refer to UG0586: RTG4 Clocking Resources User Guide *revision 8 or newer* for information about the CCC / PLL settings and use models, including Lock Window settings and Auto-Reset logic.
5. Open the Constraints Manager from the Design Flow tab, and click **Derive Constraints** in the Timing tab to generate the required clock and false-path constraints for the CCC/PLL instances.
6. Integrate the new CCC component into the design hierarchy by replacing the module instantiations and connections to the standard FCCC with an instantiation of the new FCCC with Enhanced PLL Calibration containing ports for CCC_0 and CCC_1 on the same component instance.

3.4 Core Update Procedure

Perform the following procedure to update a core version.

1. Download the latest version of the core into your vault.
2. Upgrade each configured core in your design to the latest version by right-clicking on the core component in the design hierarchy and selecting **Replace ComponentVersion**.

3. Regenerate the design.
4. Derive the Timing Constraints again from the Constraint Manager tool to use the latest generated core constraints.
5. Rerun the toolflow.

4. RTG4 New Cores

The following table lists new RTG4 cores for Libero SoC v11.9 SP6.

Core	Version	Description
RTG4 uPROM	2.0.100	Makes room for SET delay re-calibration. All RTG4 designs with RTG4UPROM are invalidated to pre-synthesis/compile state. Users MUST upgrade to 2.0.100. For more information, see 1.1 RTG4 SET Filter Delay Calibration Update.
RTG4 DDR Memory Controller (RTG4FDDRC added since 11.9 SP5)	2.0.100	This core version generates a new CoreABC initialization sequence that implements the FDDR FPLL temperature drift calibration solution. For more information, see 1.2 RTG4 SERDES and FDDR PLL Enhanced Calibration.
RTG4 DDR Memory Controller with Initialization (RTG4FDDRC_INIT)	2.0.010	This core version generates a new CoreABC initialization sequence that implements the FDDR FPLL temperature drift calibration solution. For more information, see 1.2 RTG4 SERDES and FDDR PLL Enhanced Calibration.
RTG4 High Speed Serial Interface (PCIe, EPCS, and XAUI) (PCIE_SERDES_IF added since 11.9 SP5)	2.0.100	This core version generates a new CoreABC initialization sequence that implements the Transceiver SPLL temperature drift calibration solution. For more information, see 1.2 RTG4 SERDES and FDDR PLL Enhanced Calibration.
RTG4 High Speed Serial Interface 1 – EPCS and XAUI – with Initialization (PCIE_SERDES_IF_INIT)	2.0.010	This core version generates a new CoreABC initialization sequence that implements the Transceiver SPLL temperature drift calibration solution. For more information, see 1.2 RTG4 SERDES and FDDR PLL Enhanced Calibration.
RTG4 High Speed Serial Interface 2 – EPCS and XAUI (NPSS_SERDES_IF added since 11.9 SP5)	2.0.100	This core version generates a new CoreABC initialization sequence that implements the Transceiver SPLL temperature drift calibration solution. For more information, see 1.2 RTG4 SERDES and FDDR PLL Enhanced Calibration.
RTG4 High Speed Serial Interface 2 – EPCS and XAUI – with Initialization (NPSS_SERDES_IF_INIT)	2.0.010	This core version generates a new CoreABC initialization sequence that implements the Transceiver SPLL temperature drift calibration solution. For more information, see 1.2 RTG4 SERDES and FDDR PLL Enhanced Calibration.
RTG4 Two-Port Large SRAM (RTG4TPSRAM)	1.1.109	Option to expose Write Byte Enables. The BUSY output from v1.1.107 is no longer available. For more information, see 1.3 RTG4 LSRAM Write Byte Enable Control Signals.
RTG4 Dual-Port Large SRAM (RTG4DPSRAM)	1.1.106	Option to expose Write Byte Enables. See CN19001 for more information. For more information, see 1.3 RTG4 LSRAM Write Byte Enable Control Signals.

5. Resolved Issues

The following table lists the customer-reported SARs resolved in Libero SoC v11.9 SP6. Resolution of previously reported “Known Issues and Limitations” is also noted in this table.

5.1 List of Resolved Issues

Case Number	Description
493642-2741966473	RTG4 TPSRAM generates unsupported configuration.
493642-2747946263	RTG4FCCC: Input frequency > 400 MHz.
493642-2545154827	ODT model missing from exported RTG4 IBIS file.
493642-2585301502	SmartFusion Analog I/Os when used the IBIS model export is having issues.
493642-2372004182	Unable to export IBIS model for AGLN125V5-VQ100.
493642-2223815205	Missing IBIS model error - RT3PE3000L-CG484.
493642-2523233678	SmartFusion2, IGLOO2, and RTG4:The delay value 8ns (late-early, 4-(-4)= 8 ns) is getting added to the clock net delay FCCC_0/GL0_net value in the required time calculations when we apply the latency clock constraints.
493642-2347204766, 493642-2377182134, 493642-2498053109	Invoking synthesis crashes in Libero version 11.8 SP1 ECF on a VHDL design.
493642-2529920812	ProASIC3 Macro Library Guide: FIFO4K18 aspect ratio.
493642-2730492553	RTG4 Simulation: FCCC output out of phase from Ref Clk.
493642-2718370360	Linked Files in SmartDesign.
493642-2756297422	RTG4 netlist with LSRAM using falling edge will retain INVerter cell and use unprotected net for clocks.
493642-2677619049	RTG4FCCC glitch filter with clock inversion not recognized in STA.
	RTG4FCCCECALIB configurator Display of Delay from Input to Output is not available in GUI.
	RTG4 Simulation FDDR with FPLL Calib Sim Failure with 300MHz Div 3 and FCCC eCalib Clock Base.

6. Known Limitations, Issues, and Workarounds

Known issues from Libero SoC v11.9 and its service packs may also apply to Libero SoC v11.9 SP6. Review the Libero SoC v11.9 Release Notes for Known Issues in Libero SoC v11.9.

6.1 Generating RTG4FCCC and RTG4FCCCECALIB Cores in the Same Design Shows a Warning Message in the Log Window

If you generate RTG4FCCC and RTG4FCCCECALIB cores in the same design, you will see the following warning message in the Log Window:

```
Warning: The BUFD_DELAY module is defined in multiple files. Duplicate modules are not supported.

Select the file you want to use from the Design Hierarchy.
```

This message will not cause any stoppage to the design flow and can be ignored.

6.2 Secure IP Flow Fails at Compile when Mentor Simulation Key is Removed

Compile fails in the Secure IP flow when the Mentor simulation key is removed. This issue is fixed in the Libero SoC v11.9 SP6 release.

6.3 FlashPro will Error Out if an Existing PDB is Modified to Disable the Fabric

If an existing PDB file is modified to disable the fabric and programmed only with eNVM, FlashPro will error out.

Workaround:

Create a new FlashPro project and create a new PDB. Enable eNVM and import the efc file required for programming eNVM. Save the PDB and use this PDB to program the device.

6.4 SmartTime Reports False Failure During max/best or min/worst Case Analysis

Timing reports may have incorrect slacks for the secondary corners “max/best” and “min/worst” if they were created with the constraint coverage option turned on. The reports for “max/worst” and “min/best” corners are not affected.

Workaround:

1. First, enable the constraint coverage option before running Verify Timing to generate and analyze the coverage report (but disregard the timing reports for “max/best” and “min/worst”). Then, disable the constraint coverage option before re-running Verify Timing to generate and analyze the timing reports at all corners, including “max/best” and “min/worst”.
2. Upgrade to Libero SoC v12.0 or later, where this issue has been fixed.

6.5 RTG4CCCECALIB Generation Fails When Only Local Clock Outputs (Y0, Y1, Y2, or Y3) are Used

Generation of the RTG4CCCECALIB core fails when only local clock outputs are used.

Workaround: To use local clocks, select the Global clock associated with the lowest local clock frequency among Y0, Y1, Y2, and Y3.

6.6 Post-Layout Simulation Goes to Infinite Loop

Infinite loops are caused by a disabled pathpulse construct in Mentor simulators. This construct is disabled in 10.7c and onwards.

If the Post-Layout Simulation is going to an infinite loop and some GLs are not toggling with the respective frequencies, +transport_path_delays option can be added in the vsim commands under project settings and disable pulse filtering. As a result, run.do will have +transport_path_delays +pulse_int_e/1 +pulse_int_r/1 +transport_int_delays options with the vsim command.

6.7 FlashPro Lite support on Windows10 with PCMCIA converters

Windows 10 support with FlashPro Lite was tested only on an integrated parallel port on a desktop. Customers using FlashPro Lite with Windows 10 via the PCMCIA converters given at the below link, are unable to detect the programmer in the tool:

www.microsemi.com/document-portal/doc_download/129781-ac351-pcmcia-adapter-for-parallel-port-programming-app-brief

FlashPro Lite support on Windows 10 machines with the PCMCIA converters will be fixed in the next release of Libero SoC v11.9.

7. System Requirements

7.1 Operating System Support

- Windows 7, Windows 10
- RHEL/CentOS 5 (see Note below), RHEL/CentOS 6.6-6.11, RHEL/CentOS 7.2-7.6
- SuSE 11 SP4 (Libero only. FlashPro Express, SmartDebug, and Job Manager are not supported.)

Note: RHEL 5 and CentOS 5 do not support programming using FlashPro5.

8. Download Instructions

Click the following links to download Libero SoC v11.9 SP6 on Windows and Linux operating systems:

- Windows Download
- Linux Download

Note: Windows installation requires administrator privileges to the system.

Libero SoC v11.9 SP6 is an incremental service pack and can be installed over Libero SoC v11.9 or Libero SoC v11.9 SP5.

After successful installation, clicking **Help-> About Libero** will show Release v11.9 SP6.

8.1 Instructions for Megavault Users

Download and install the Megavault for Libero SoC v11.9 SP6 if you have not already done so. Make sure you have write access to the Megavault.

Windows Operating Systems
S3: https://download-soc.microsemi.com/FPGA/v11.9/Libero_SoC_MegaVault_v11.9SP6_win.zip

md5sum: d3197442d432a29f6115d07ef170803a

sha256sum: f31fb7ad71e1c7cbcc817a740edf1ca066ea9a1028bbb8272c0866c23500db07

Installation Instructions

1. Make sure you have at least 5 GB of available hard drive space.
2. Copy the file `Libero_SoC_MegaVault_v11.9SP6_win.zip` from the path above to a temp directory.
3. Extract the zip file to a temp folder.
4. Execute the **Libero_SoC_MegaVault_v11.9_SP6.exe.lnk** shortcut and follow the installation instructions.

Linux Operating Systems
S3: https://download-soc.microsemi.com/FPGA/v11.9/Libero_SoC_MegaVault_v11.9_SP6_lin.bin

md5sum: 72dd5e0509b7425c2428ada25100ecdd

sha256sum: e5b09f1bc5cfdac795a49bbf2895d16b033d589bb4797f3fbd1be4bbe6a1d337

Installation Instructions:

1. Make sure you have at least 5 GB of available hard drive space for installation and 15 GB of space in your temp directory during installation.
2. Copy the file `Libero_SoC_MegaVault_v11.9_SP6_lin.bin` from the path above to a temp directory.
3. Change directory to the temp directory: `chmod +x Libero_SoC_MegaVault_v11.9_SP6_lin.bin`
4. Type: `./Libero_SoC_MegaVault_v11.9_SP6_lin.bin` to launch the Libero installer.
5. Follow the installation instructions.

8.2 Downloading SoftConsole 3.4/4.0/5.1

Libero SoC v11.9 SP6 is compatible with SoftConsole v3.4 SP1, SoftConsole v4.0 and SoftConsole v5.x

- SoftConsole Download

9. Appendix A. RTG4 SPLL and FPLL Calibration and Workaround

Previously, SPLL (SERDES PCIe and XAUI) and FPLL (FDDR) lost lock during temperature ramp as described in CN19009 and CN19009A. To resolve this issue, a new CoreABC sequence has been developed in Libero SoC v11.9 SP6 that includes an SPLL/FPLL workaround. The new sequence requires design changes to the initialization logic (CoreABC configuration and connections) in some cases described in the following sections.

9.1 RTG4 SPLL and FPLL Calibration and Workaround

Previously, SPLL (SERDES PCIe and XAUI) and FPLL (FDDR) lost lock during temperature ramp as described in CN19009 and CN19009A. To resolve this issue, a new CoreABC sequence has been developed in Libero SoC v11.9 SP6 that includes an SPLL/FPLL workaround. The new sequence requires design changes to the initialization logic (CoreABC configuration and connections) in some cases described in the following sections.

9.1.1 Affected Designs and Modes

This workaround applies to designs that use the following components and modes. These designs require upgrading to the latest core version. A few design changes may also be needed for designs that use components without built-in initialization. Refer to the following sections for details.

Table 9-1.

Libero Catalog Display Name	Component Name	Mode
RTG4 High Speed Serial Interface (PCIe, EPCS & XAUI)	PCIE_SERDES_IF	PCIE XAUI
High Speed Serial Interface 1 - EPCS and XAUI - with Initialization	PCIE_SERDES_IF_INIT	XAUI
RTG4 High Speed Serial Interface (EPCS & XAUI)	NPSS_SERDES_IF	XAUI
High Speed Serial Interface 2 - EPCS and XAUI - with Initialization	NPSS_SERDES_IF_INIT	XAUI
RTG4 DDR Memory Controller	RTG4FDDRC	DDR
RTG4 DDR Memory Controller with initialization	RTG4FDDRC_INIT	DDR

This workaround also applies to designs that use the following components that support built-in initialization. These designs require upgrading to the latest core version. Thereinafter, no user action is required because the *_INIT components handle the new CoreABC sequence and design updates automatically for SPLL/FPLL Lock polling.

Table 9-2.

Libero Catalog Display Name	Design	Mode
High Speed Serial Interface 1 - EPCS and XAUI - with Initialization	PCIE_SERDES_IF_INIT	XAUI
High Speed Serial Interface 2 - EPCS and XAUI - with Initialization	NPSS_SERDES_IF_INIT	XAUI
RTG4 DDR Memory Controller with initialization	RTG4FDDRC_INIT	DDR

9.1.2 New CoreABC Sequence

The following section describe where the new SPLL/FPLL workaround is added in the CoreABC program/sequence.

9.1.2.1 SPLL (for SERDES PCIe/XAUI PCS-to-Fabric Interface)

Refer to the *abc.txt file generated for each block for the actual CoreABC program/sequence under: project/component/work/<PCIE or NPSS SERDES component>/PCIE (or NPSS)_SERDES_IF_0.

- Configure PMA, system registers.
- De-assert PHY_RESET_N.
- Perform the SPLL workaround, which includes polling for SPLL_LOCK output fromSERDES.
- De-assert CORE_RESET_N.
- PCIE mode only: Configure PCIE registers.
- Assert INIT_DONE.

9.1.2.2 FPLL (for FDDR)

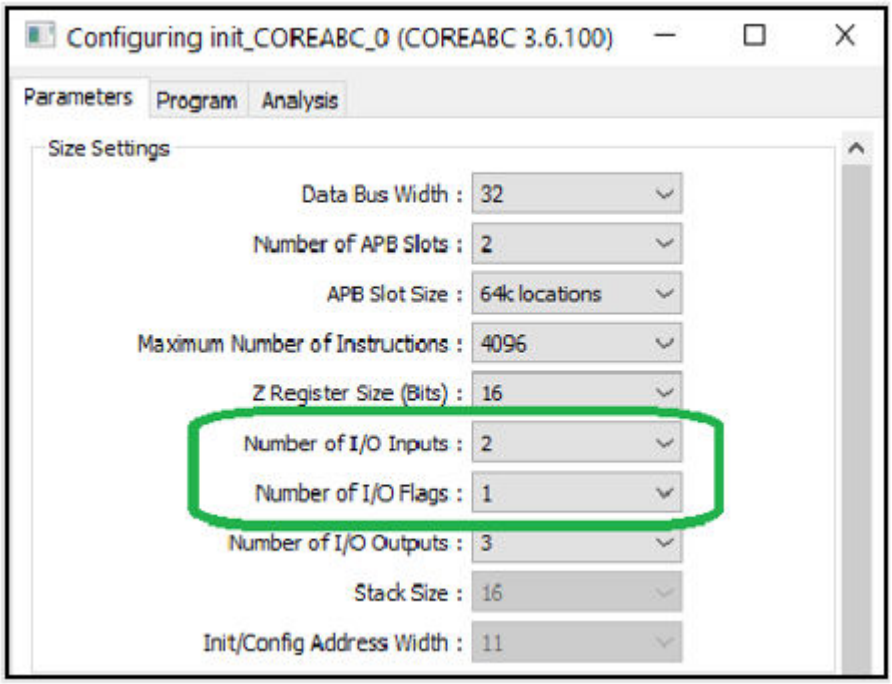
Refer to the *abc.txt file generated for each block for the actual CoreABC program/sequence under: project/component/work/<FDDR component>/FDDRC_0).

- Perform the FPLL workaround, which includes polling for the FPLL_LOCK output from FDDR.
- Configure the DDR registers.
- Wait for controller ready and memory settling time, and then assert INIT_DONE.

9.1.3 Design Updates for PCIE_SERDES_IF in PCIE Mode

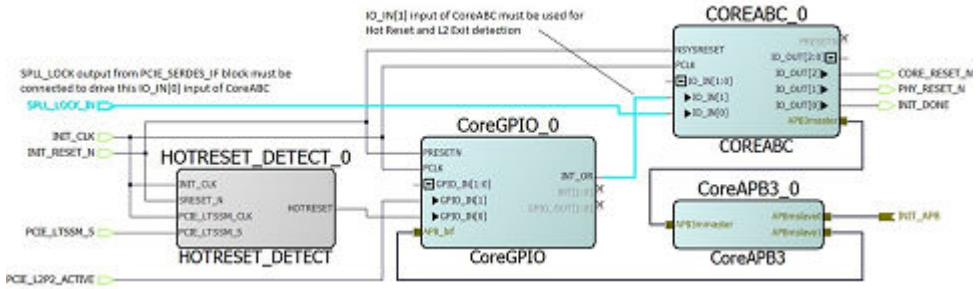
After upgrading to the latest PCIE_SERDES_IF core version, copy the latest CoreABC program/sequence from the generated *abc.txt file and paste it in the **Program** tab of CoreABC that is part of the assembled initialization logic

In addition, update the CoreABC configuration in the **Size Settings** section of the **Parameters** tab (refer to the following figures):



Parameter	Updated Setting	Comment
Number of I/O ports	2	IO_IN[0] = SPLL_LOCK IO_IN[1] = Hot Reset and L2 Exit detection logic. If your design does not use the Hot Reset and L2 Exit detection logic, tie IO_IN[1] to GND

.....continued		
Parameter	**Updated Setting**	**Comment**
Number of IO flags	1	

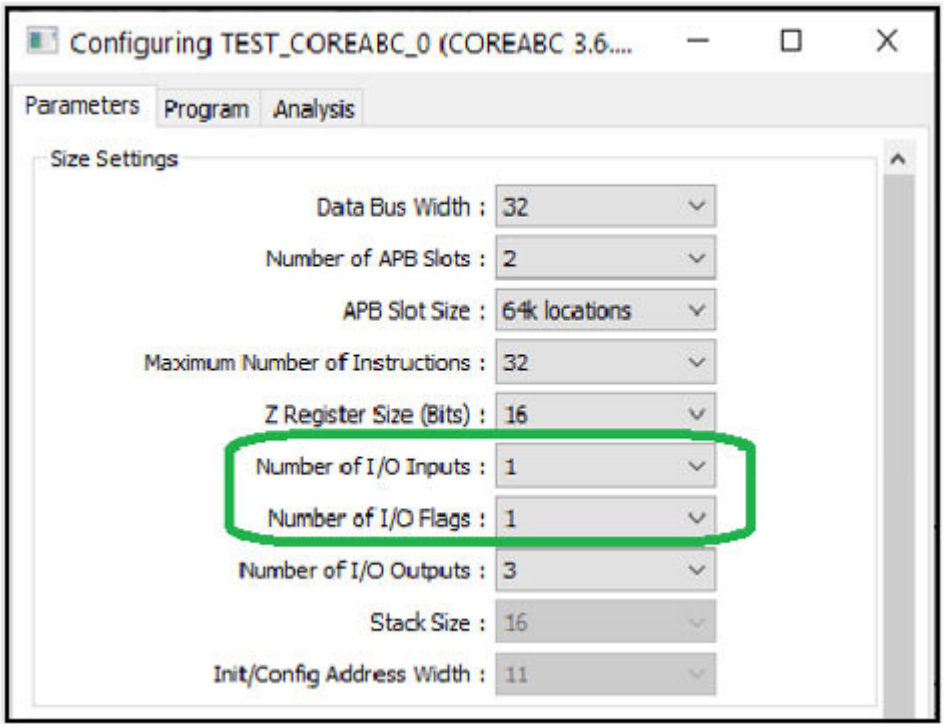


9.1.4 Design Updates for PCIE_SERDES_IF or NPSS_SERDES_IF in XAUI Mode

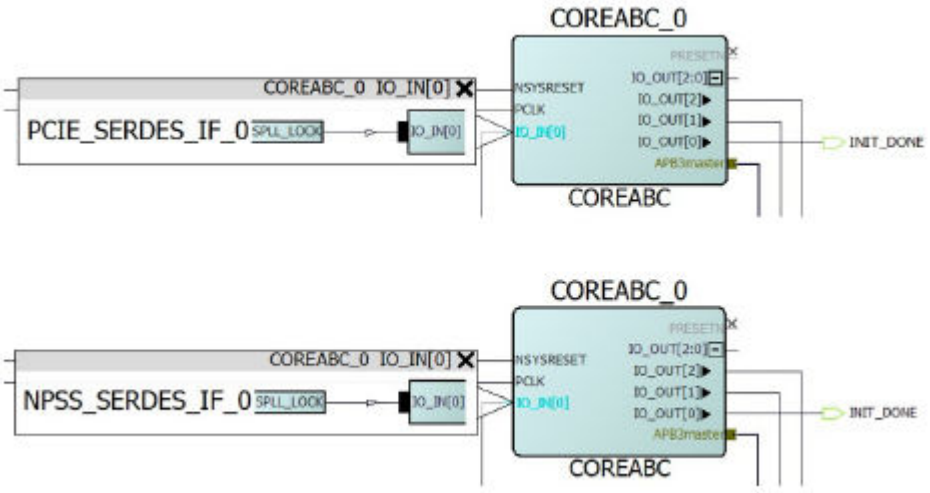
Perform the following changes only when using the SERDES blocks without built-in initialization (PCIE_SERDES_IF or NPSS_SERDES_IF). These changes are handled automatically when using the SERDES blocks with built-in initialization (PCIE_SERDES_IF_INIT or NPSS_SERDES_IF_INIT).

After upgrading to the latest PCIE_SERDES_IF or NPSS_SERDES_IF core version, copy the latest CoreABC program/sequence from the generated *abc.txt file and paste it in the **Program** tab of CoreABC that is part of the assembled initialization logic.

In addition, update the CoreABC configuration in the **Size Settings** section of the **Parameters** tab (refer to the following figures):



Parameter	Updated Setting	Comment
Number of I/O ports	1	IO_IN[0] = SPLL_LOCK
Number of IO flags	1	



9.1.5 Design Updates for RTG4FDDRC

Perform the following changes only when using the DDR memory Controller without built-in initialization (RTG4FDDRC). These changes are handled automatically when using the DDR memory Controller with built-in initialization (RTG4FDDRC_INIT).

After upgrading to the latest RTG4FDDRC core version, copy the latest CoreABC program/sequence from the generated *abc.txt file and paste it in the **Program** tab of CoreABC that is a part of the assembled initialization logic. Polling for FPLL_LOCK remains an existing requirement for FDDR, so there are no new design modifications required. The new sequence has moved the polling for FPLL_LOCK earlier in the sequence, before the DDR controller register initialization starts.

Refer to the following figures for CoreABC configuration requirements in the **Size Settings** section of the **Parameters** tab.

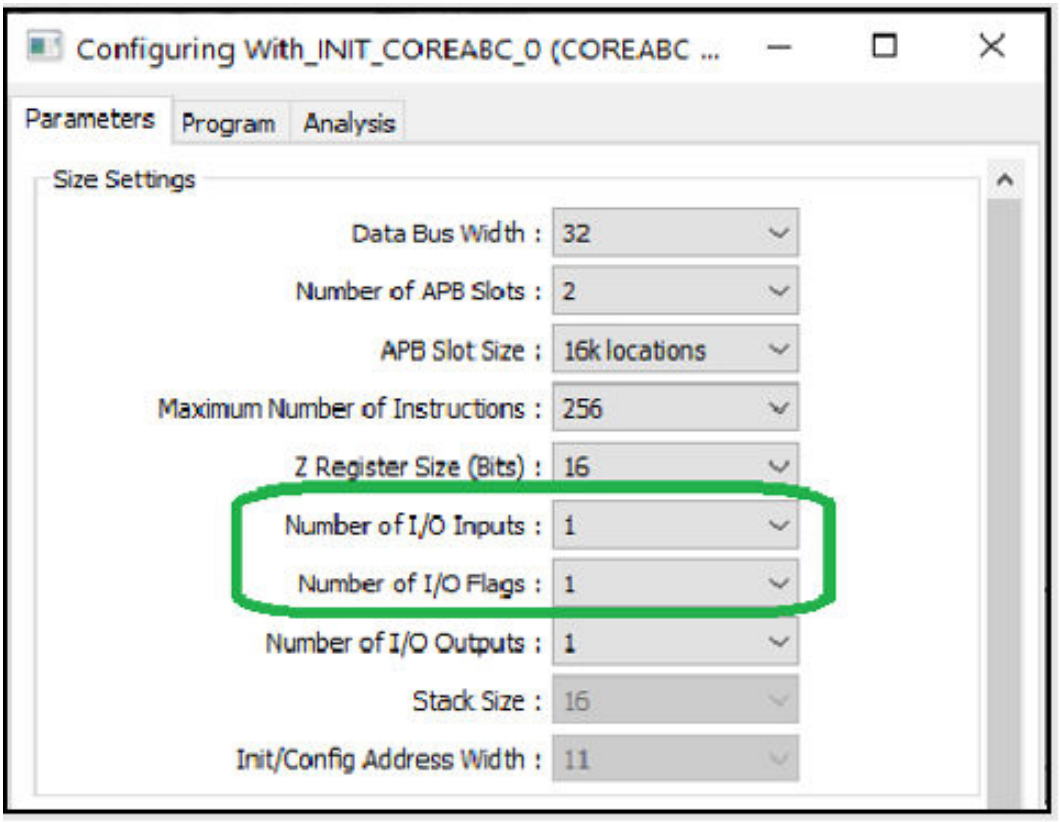
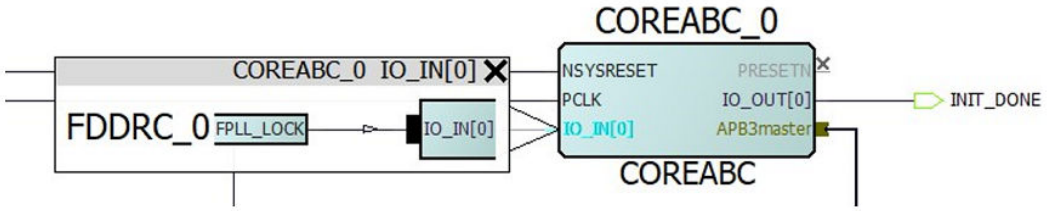


Table 9-3.

Parameter	Updated Setting	Comment
Number of I/O ports	1	IO_IN[0] for FPLL_LOCK
Number of IO flags	1	



9.1.6 Design Updates for RTG4FCCCECALIB

Clocks from RTG4FCCCECALIB that are used to drive the CLK_BASE of SPLL (SERDES blocks) or FPLL(FDDR) follow a cascaded PLL scenario. When building the design, it is the user's responsibility to make sure that CoreABC program execution does not start until CCC_0/1_LOCK of RTG4FCCCECALIB is asserted.

10. Revision History

Revision	Date	Description
F	08/2021	Updated section 10. Revision History.
E	08/2021	Updated section 7.1 Operating System Support.
D	07/2021	Added section 6.7 FlashPro Lite support on Windows10 with PCMCIA converters as a known issue.
C	01/2021	Updated section 8.1 Instructions for Megavault Users. Updated document footer to remove "Draft".
B	11/2020	Added section 1.4 Timing Paths May be Missing from Static Timing Analysis (STA) for the SmartFusion2, IGLOO2, and RTG4 Families. Updated section 8.1 Instructions for Megavault Users.
A	09/2020	Initial Revision

11. Microchip FPGA Technical Support

Microchip FPGA Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. This section provides information about contacting Microchip FPGA Products Group and using these support services.

11.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

11.2 Customer Technical Support

Microchip FPGA Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microchip FPGA Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

You can communicate your technical questions through our Web portal and receive answers back by email, fax, or phone. Also, if you have design problems, you can upload your design files to receive assistance. We constantly monitor the cases created from the web portal throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

Technical support can be reached at soc.microsemi.com/Portal/Default.aspx.

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), log in at soc.microsemi.com/Portal/Default.aspx, go to the **My Cases** tab, and select **Yes** in the ITAR drop-down list when creating a new case. For a complete list of ITAR-regulated Microchip FPGAs, visit the ITAR web page.

You can track technical cases online by going to My Cases.

11.3 Website

You can browse a variety of technical and non-technical information on the Microchip FPGA Products Group home page, at www.microsemi.com/soc.

11.4 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support at (https://soc.microsemi.com/Portal/Default.aspx) or contact a local sales office.

Visit About Us for sales office listings and corporate contacts.

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Trademarks

ISBN:

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-72400 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820