

RN0223

Release Notes CoreUHD_SDITX v2.0



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

This is the first publication of this document.

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2 CoreUHD_SDITX v2.0

2.1 Overview

These release notes accompany the production release of CoreUHD_SDITX v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CoreUHD_SDITX DirectCore IP is a Serial Digital Interface (SDI) Framer. The core accepts the raw video data and performs the framing of the SDI data stream.

CoreUHD_SDITX has the following features:

- Compliant with SMPTE ST 2081-1 (6G-SDI) standard.
- Compliant with SMPTE ST 2082-1 (12G-SDI) standard.
- Supports data rates 5.94 Gb/s and 5.94/1.001 Gb/s for 6G-SDI standard.
- Supports data rates 11.88 Gb/s and 11.88/1.001 Gb/s for 12G-SDI standard.
- Performs generation and insertion of Line Number (LN) packets.
- Performs generation and insertion of CRC packets.
- Performs generation and insertion of Video Payload Identification (VPID) packets.
- Performs insertion of sync-bits in timing reference words.
- Performs scrambling and NRZI encoding.

2.3 Delivery Types

CoreUHD_SDITX is available in two versions:

- **Evaluation:** Evaluation version is available for free and supports four hours of functionality on silicon.
- **Obfuscated:** Obfuscated version is license locked and is available only with Libero Platinum license.

2.4 Supported Families

PolarFire®

2.5 Supported Tool Flows

CoreUHD_SDITX requires Libero v12.0 or higher.

2.6 Installation Instructions

The core must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. When the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the [Libero SoC Online Help](#) for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the core Handbook. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also suggest implementation change. Refer to the [Liberio SoC Online Help](#) for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

<http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>.

2.8 Supported Test Environments

VHDL user testbench is provided with the core.

2.9 Release History

Table 1 describes the release history for CoreUHD_SDITX releases.

Table 1 • Release History

Version	Date	Change
2.0	August 2019	Initial release

2.10 Discontinued Features and Devices

There are no discontinued features and devices.

2.11 Known Limitations and Workarounds

There are no known limitations and workarounds.