UG0822
User Guide
CPRI

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Updated features list. For more information, see Features, page 3.
- Updated Table 34, page 23. For more information, see TestBench, page 22.

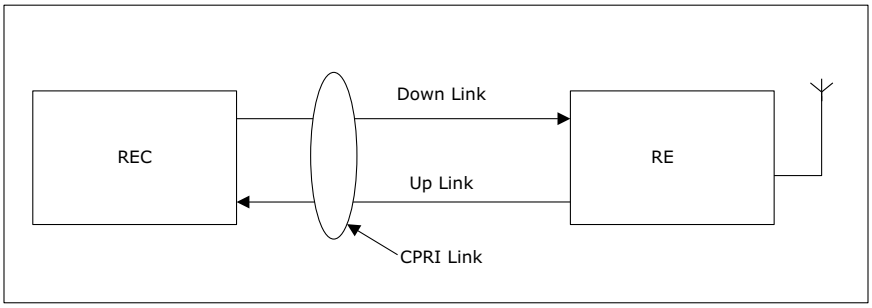
1.2 Revision 1.0

Revision 1.0 is the first publication of this document.

2 Common Public Radio Interface

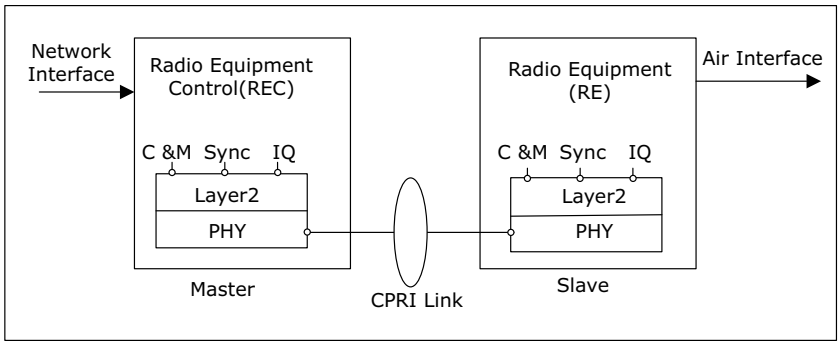
The Common Public Radio Interface (CPRI) is an industry standard aimed at defining a publicly available specification for the key internal interface of radio base stations between the Radio Equipment Control (REC) and Radio Equipment (RE). The following figure shows the single point-point link between one REC and one RE.

Figure 1 • **Single Point to Point Link Between Single REC and RE**



The following figure shows the Radio Base Station system, where REC is the master port and RE is the slave port. REC receives the IQ data from the network interface, packs the data in the CPRI frame format, along with the Layer2 protocols such as Ethernet, HDLC, vendor specific and antenna carrier control data. The CPRI frame is then transmitted from master to slave RE through the physical layer interface.

Figure 2 • **Radio Base Station System**



2.1 Features

Microsemi CPRI IP supports following features:

- Compliant with CPRI specification Version 6.1.
- Supports Protocol Version 1.
- Supports slave only mode on a CPRI link.
- Supports CPRI line rate options 1 to 7
  - Rate 1: 614.4 Mbps
  - Rate 2: 1228.8 Mbps
  - Rate 3: 2457.6 Mbps
  - Rate 4: 3072.0 Mbps
  - Rate 5: 4915.2 Mbps
  - Rate 6: 6144.0.Mbps
  - Rate 7: 9830.4 Mbps
- Supports upto 32 antenna carriers.
- Number of antenna carriers supported for line rate 7 is fixed to 8.
- 32-bit user interface for Fast Ethernet access.
- 32-bit user interface for vendor specific data.
- 32-bit user interface to antenna carrier control data.
- 32-bit user interface to antenna carrier IQ data.
- Ethernet pointer fixed to 20.
- Supports direct mapping of IQ samples as per EUTRA-FDD.
- Supports sample width of 15-bits for IQ data.
- Auto-Negotiation not supported.

2.2 Supported Device Families

PolarFire® FPGA families are supported by the CPRI IP.

Note: Ensure that the selected device in the family has transceivers.

2.3 License Requirement

The CPRI IP is available with all Libero licenses. The core can be instantiated, simulated, synthesized, and placed and routed using Libero SoC PolarFire. The RTL code for the core is encrypted.

2.4 References

For more information on CPRI protocol, see http://www.cpri.info/spec.html.

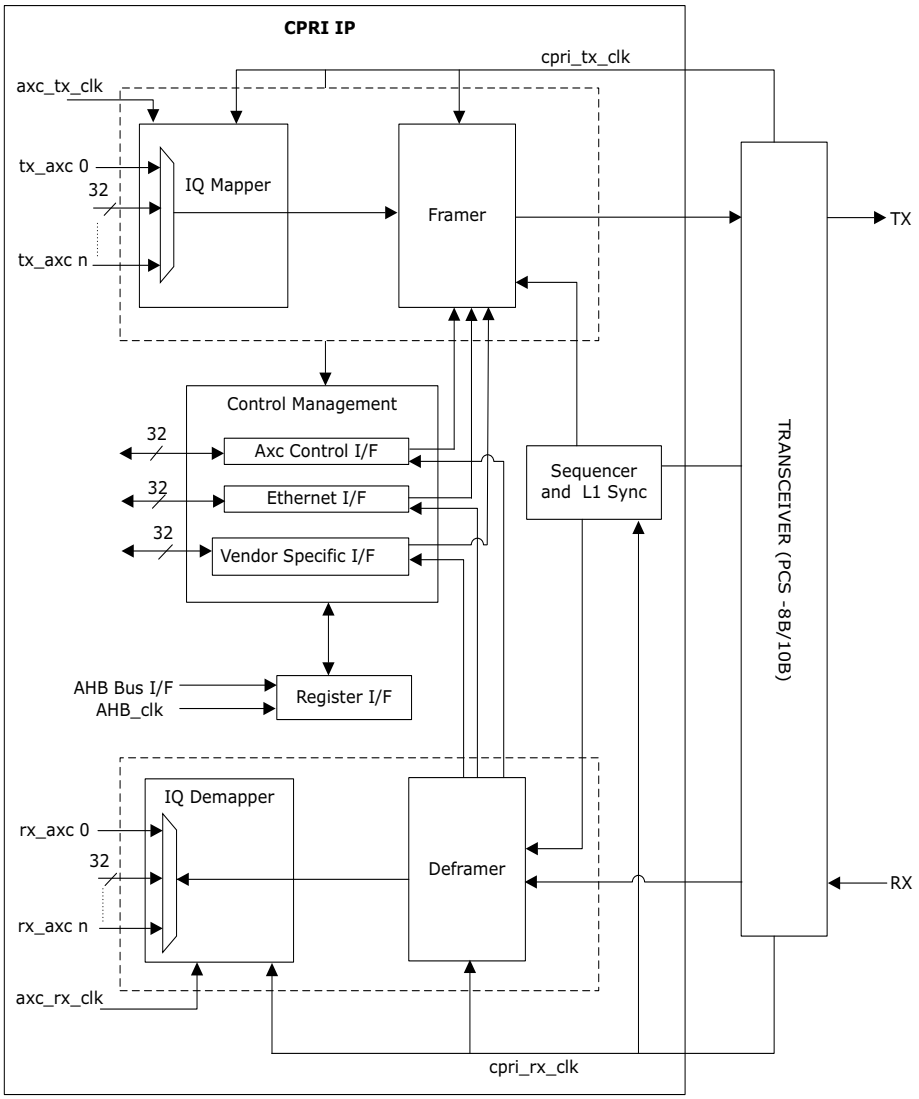
2.5 Core Architecture

2.5.1 Design Description

On the transmitter side, the CPRI IP receives mapped IQ data from the IQ Mapper block and control words from user interfaces such as Ethernet, vendor specific and antenna carrier control data. The framer block then receives the control and data words from the respective blocks and frames them into the 32-bit CPRI frame format before transmitting it to the CPRI link through transceiver.

On the receiver side, it receives the CPRI data from the CPRI link via transceiver. The 32-bit incoming frame from the XCVR is sent to the deframer block, which deframes the data. The deframer block then routes IQ data to the IQ demapper block and control words to the respective user interfaces such as Ethernet, vendor specific and antenna carrier control data. The IQ demapper block demaps the received IQ data and transmits them to the respective antenna carriers. Following figure shows the block diagram of CPRI IP.

Figure 3 • **CPRI IP Block Diagram**



Following sections describe the internal blocks of the CPRI IP.

- IQ Mapper Block
- IQ Demapper Block
- Framer Block
- Deframer Block
- Vendor Specific Data Block
- Ethernet Data Block
- Antenna Carrier Control Data Block
- AHB Slave Register Interface

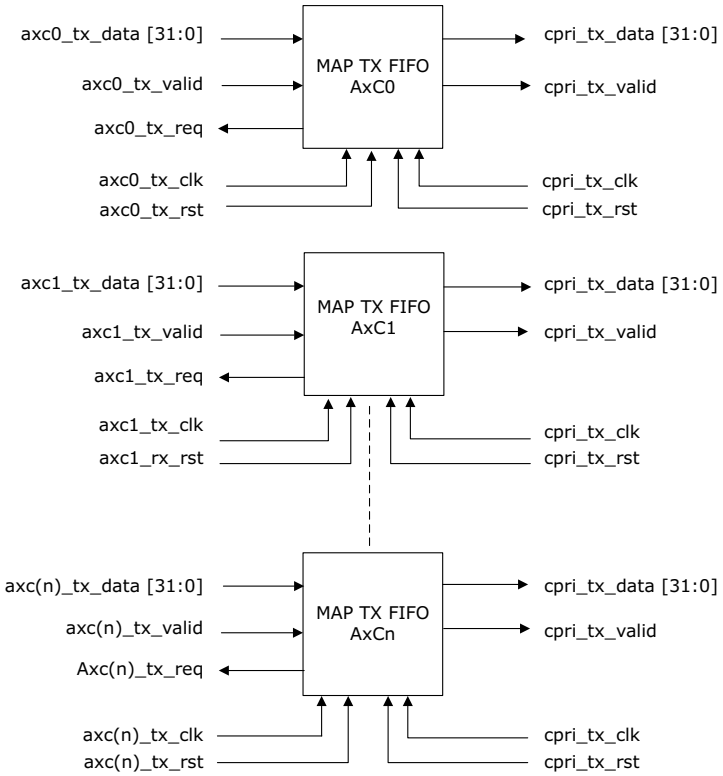
2.5.1.1 IQ Mapper Block

The IQ mapper block controls the transmission of IQ data samples received from the antenna carrier block. IQ mapper block interfaces to the antenna carrier through interface FIFOs. Received IQ samples are then mapped and transmitted to the CPRI framer block.

All the antenna carrier interfaces in the CPRI IP support the same sample rate and sample width. The uplink and downlink sample rates are also same.

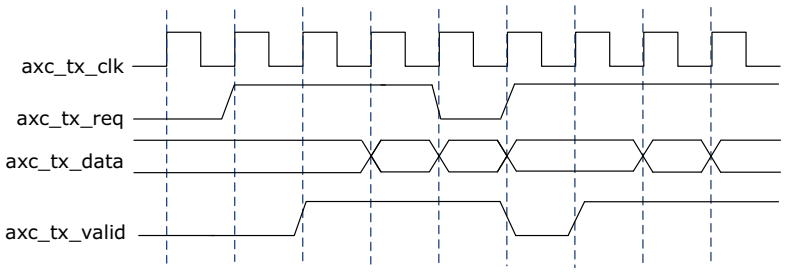
The following figure shows the interface diagram of antenna carrier and IQ mapper block. IQ mapper block interfaces to each antenna carrier block through a MAP TX FIFO. If the TX FIFO is not full, it indicates that IQ mapper block is ready to receive the data from the antenna carrier. It then sends request to the corresponding antenna carrier. The antenna carrier transmits the data to the TX FIFO.

Figure 4 • **IQ Mapper Block Diagram**



Following figure shows the timing diagram of antenna carrier TX interface to the CPRI IQ mapper block.

Figure 5 • **Antenna Carrier TX Block Timing Diagram**

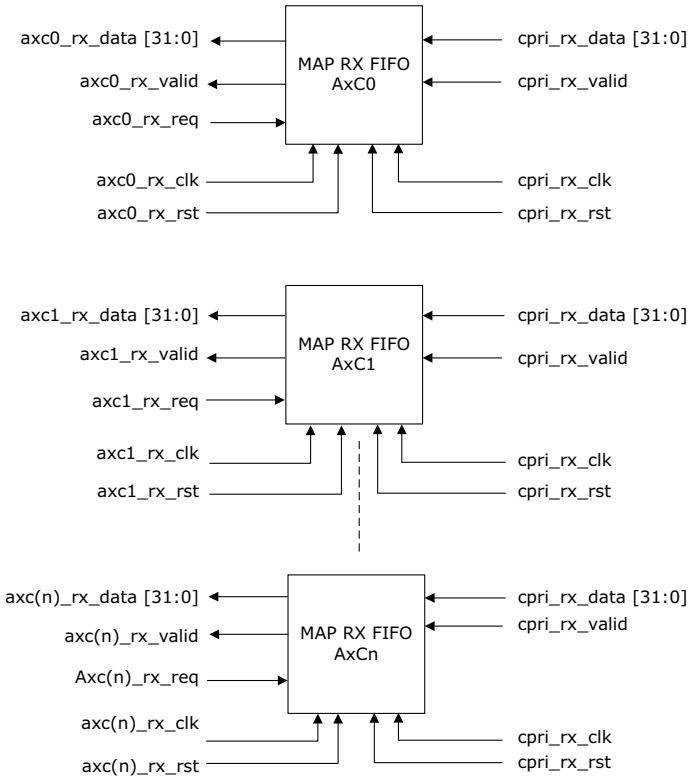


2.5.1.2 IQ Demapper Block

The IQ demapper block receives 32-bit CPRI data from the transceiver and transmits it to the corresponding antenna carrier interface. Each antenna carrier RX interface has a unique antenna carrier clock, which is driven by a user application.

The following figure shows the block diagram of the IQ demapper block. On one side IQ demapper block interfaces with the user application through antenna carrier data channel, on the other end it interfaces with the CPRI deframer.

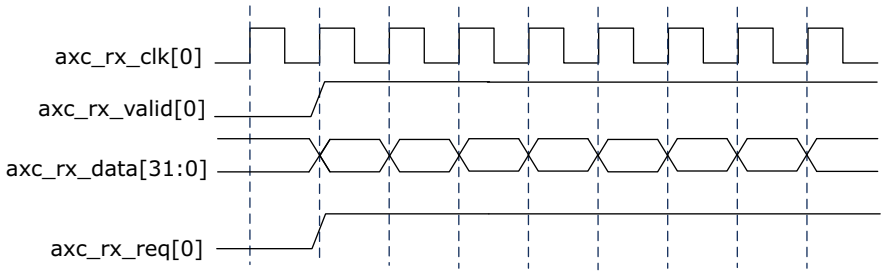
Figure 6 • **IQ Demapper Block**



The IQ demapper block interfaces with each antenna carrier block through a MAP RX FIFO. Each antenna carrier interface is sourced by corresponding `axc_rx_clk` from the application layer. When IQ demapper block receives the data from CPRI link, it writes the data to the corresponding MAP RX AxC FIFO at the `cpri_rx_clk`. When the data is available in the FIFO, then `axc_rx_valid` signal is asserted as shown in Figure 6, page 6. Once the user application is ready to accept the data, axc_rx_ready signal is asserted. If both `axc_rx_valid` and `axc_rx_ready` signals are asserted, then user application reads the data from the IQ demapper block. The data to MAP RX FIFO is written in the circular motion. If the data is not read from FIFO via user application, then data is overwritten in the circular motion.

The following figure shows the timing diagram of the antenna carrier interface to the IQ demapper block on the receive side.

Figure 7 • **Antenna Carrier RX Block Timing Diagram**



2.5.1.3 Framer Block

The framer block receives IQ data from the IQ mapper block and control information from Ethernet, vendor specific data and antenna carrier control user interfaces. It frames the incoming data in the CPRI frame format and transmits the 32-bit CPRI frame to the transceiver. This block operates at CPRI_TX_CLK.

2.5.1.4 Deframer Block

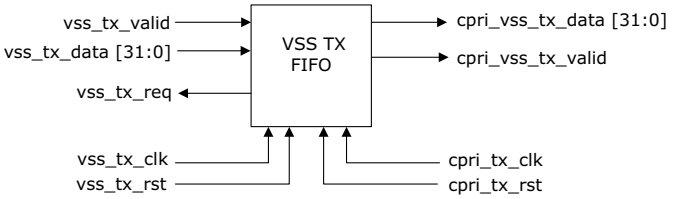
The deframer block receives 32-bit CPRI frame from the transceiver block. It deframes the incoming data and transmits the IQ data to the IQ demapper block and control information to Ethernet RX, vendor specific data RX and antenna carrier control RX user interfaces. This block operates at CPRI_RX_CLK.

2.5.1.5 Vendor Specific Data Block

The vendor specific data is available to the CPRI IP through a user interface. This data is embedded in the CPRI frame from the sub-channel 16 to pointer (p-1) of the hyperframe. The vendor specific data can be accessed through CPRI framer block on the transmitter side and the CPRI deframer block on the receiver side.

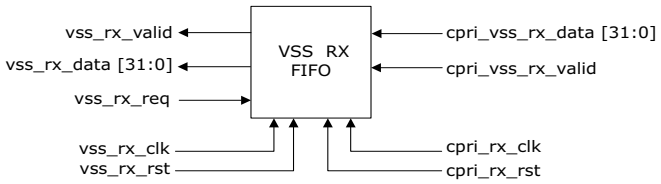
On the transmit side, vendor specific data block has a 32-bit interface to the user via FIFO through a request valid handshake mechanism as shown in the following figure.

Figure 8 • **Vendor Specific TX Data User Block**



On the receiver side, vendor specific data block has a 32-bit interface to the user via a FIFO through a request valid handshake mechanism, as shown in the following figure.

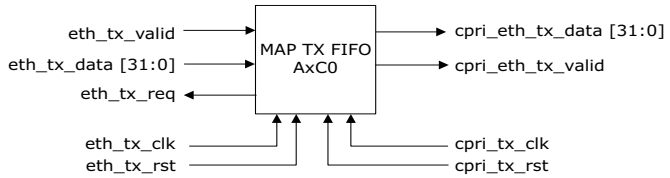
Figure 9 • **Vendor Specific RX Data User Block**



2.5.1.6 Ethernet Data Block

A 32-bit user interface is available for the Ethernet data on both transmit and receive paths. On the transmit side, Ethernet interface has a 32-bit interface to the user via a FIFO using a request valid handshake mechanism as shown in the following figure.

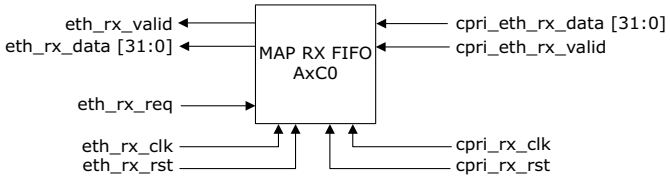
Figure 10 • **Ethernet TX Data User Block**



Ethernet data is available to the CPRI and is embedded in the CPRI frame from the sub-channel pointer (p) to 63 of the hyperframe. The Fast Ethernet data can be accessed through the CPRI Framer on the transmit side and the CPRI deframer block on the receive side.

On the receive side, Ethernet RX interface has a 32-bit interface to the user via a FIFO using request valid handshake mechanism as shown in the below figure.

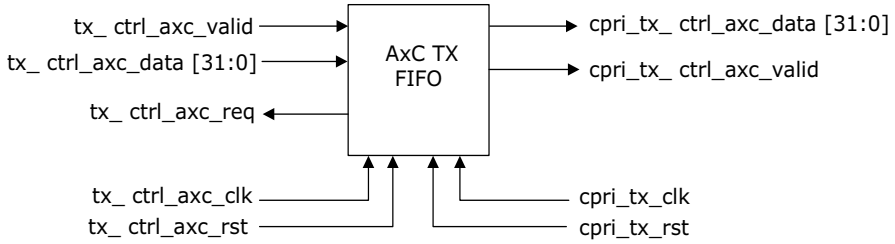
Figure 11 • **Ethernet RX Data User Block**



2.5.1.7 Antenna Carrier Control Data Block

A 32-bit user interface is available for the antenna carrier control data on both transmit and receive paths. On the transmit side, antenna carrier control data interface has a 32-bit interface to the user via a FIFO using a request valid handshake mechanism as shown in the following figure.

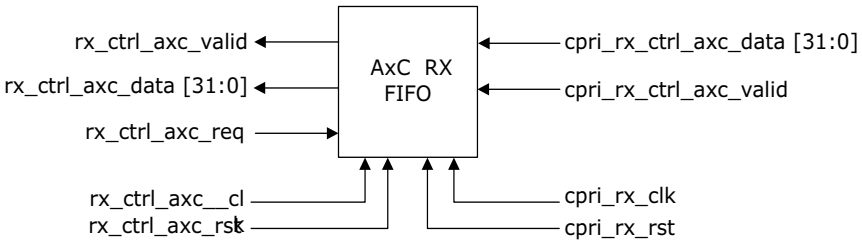
Figure 12 • **Antenna Carrier Control TX Data User Interface**



Antenna carrier control data is available to the CPRI and is embedded in the CPRI frame from the sub-channel 4 to 7 of the hyperframe. The antenna carrier control data can be accessed through the CPRI framer on the transmit side and the CPRI deframer block on the receive side.

On the receive side, antenna carrier control data RX interface has a 32-bit interface to the user via a FIFO using request valid handshake mechanism as shown in the below figure.

Figure 13 • **Antenna Carrier Control RX Data User Interface**



2.5.1.8 AHB Slave Register Interface

CPRI IP consists of an advanced high-performance bus (AHB) interface designed to connect to an AHB Master. All the CPRI registers are accessed through AHB Master. CPRI IP supports 32-bit AHB single read and write transfers. For more information on CPRI IP registers, see "Register Interface" on page 17.

2.5.2 CPRI IP Clocking Structure

The following table describes the CPRI IP clocking structure. It briefly describes about the CPRI IP clock and the various interface clocks used in the design.

Table 1 • **CPRI IP Clocking Structure**

Clock Name	Direction	Frequency	Interfaces	Description
CPRI_TX_CLK	In	Line Rate/40	Main CPRI IP clock on the TX path	Main clock for the CPRI IP on the CPRI transmission path. This clock is received from the transceiver.
CPRI_RX_CLK	In	Line Rate/40	Main CPRI IP clock on the RX path	Main clock for the CPRI IP on the CPRI receive path. This clock is recovered via clock data recovery from the transceiver.
HCLK	In	CPU Clock (50MHz)	Register Interface	Target frequency of the register interface.
tx_eth_clk	In	125 MHz	Ethernet-TX Block	Samples the incoming Ethernet data on the transmit path.
rx_eth_clk	In	125 MHz	Ethernet RX Interface	Samples the outgoing Ethernet data on the receive path.
axc_tx_clk	In	Antenna carrier Frequency on the transmit path	IQ Mapper	Samples the received data and clocks the transmissions of antenna carrier interface.
axc_rx_clk	In	Antenna carrier Frequency on the receive path	IQ Demapper	Samples the antenna carrier data and clocks the reception of antenna carrier interface.
vss_tx_clk	In	Vendor Specific data frequency on the transmit path	VSS_TX Interface	Sample the incoming vendor specific data on the transmission path.
vss_rx_clk	In	Vendor Specific data frequency on the receive path	VSS RX Interface	Samples the outgoing vendor specific data on the reception path.
Axc_ctrl_tx_clk	In	Antenna carrier control data frequency on the transmit path	AxC Ctrl TX Interface	Samples the incoming antenna carrier control data on the transmit path.
Axc_ctrl_rx_clk	In	AxC Control data frequency on the receive path	AxC Ctrl TX Interface	Samples the outgoing antenna carrier control data on the transmit path.

For all the line rates supported, TX_PLL derives the CPRI_TX_CLK based on the configured line rate.

Table 2 • **CPRI Line Rate and Corresponding Frequency**

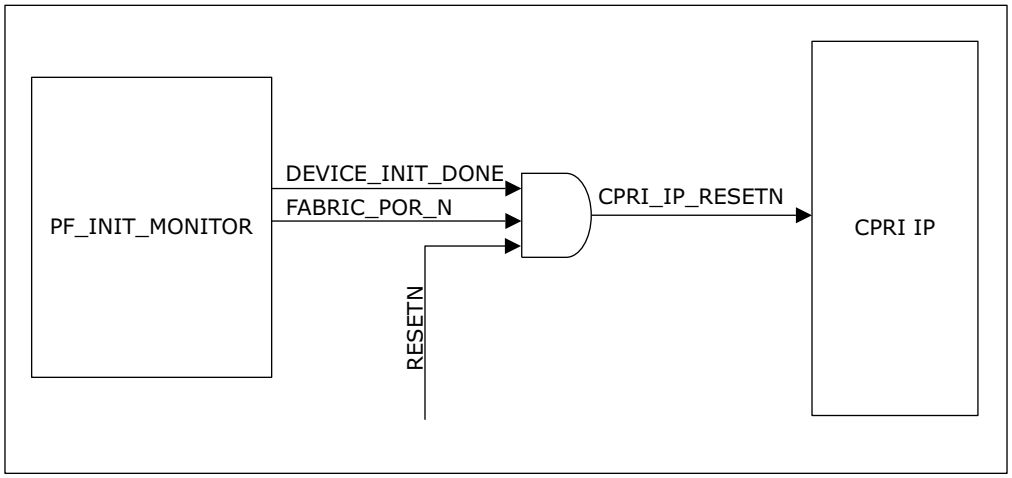
CPRI Line rate	CPRI Clock Frequency
614.4 Gbps	15.26 MHz
1228.8 Gbps	30.72 MHz
2457.6 Gbps	61.44 MHz
3072.0 Gbps	76.80 MHz
4915.2 Gbps	122.88 MHz
6144.0 Gbps	153.60 MHz
9830.4 Gbps	245.76 MHz

2.5.3 CPRI IP Reset Structure

All the reset signals coming as an input to the CPRI IP are active low.

Each incoming reset must be qualified with the FABRIC_POR_N and DEVICE_INIT_DONE signals from the PF_INIT_MONITOR block as shown in the following figure.

Figure 14 • **CPRI IP Reset Structure Block Diagram**



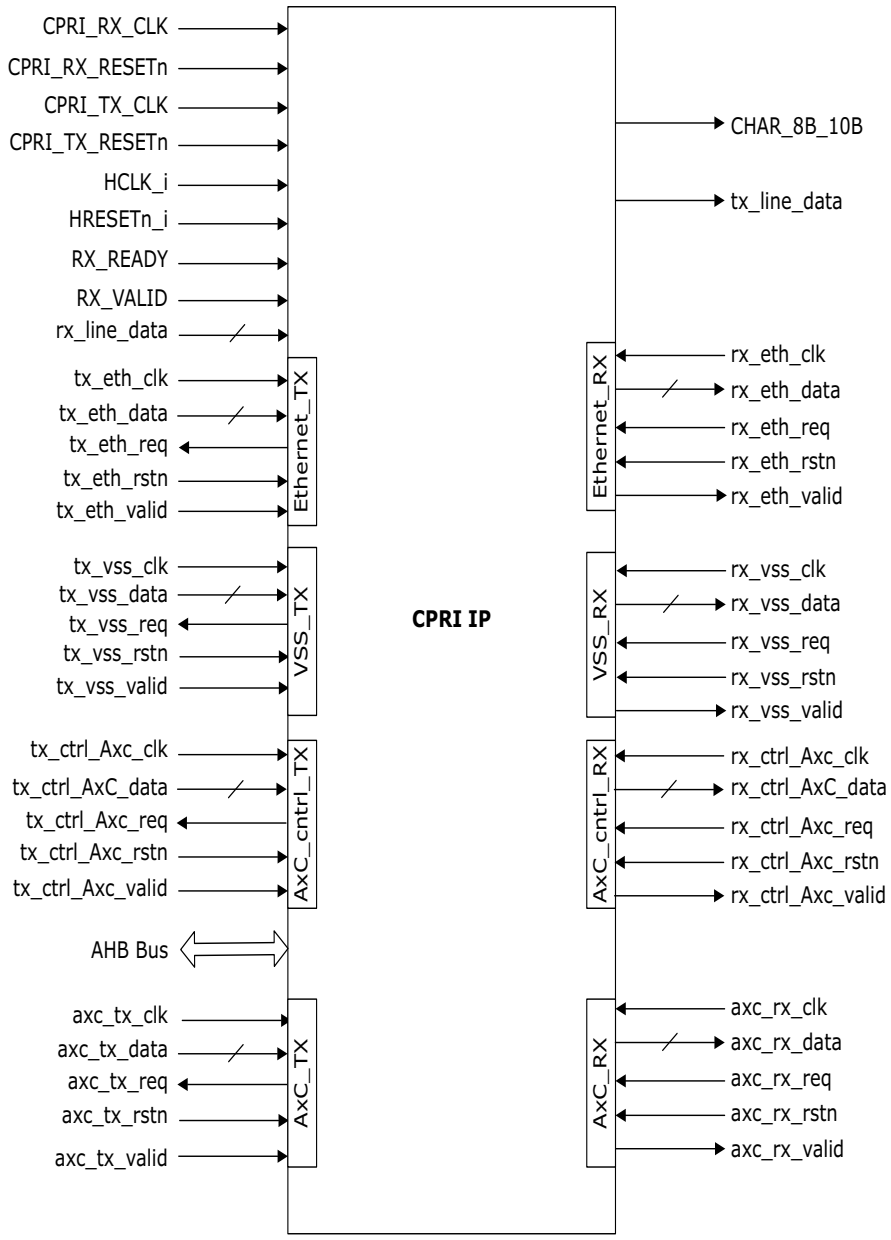
Note: The reset structure shown in above figure is applicable to all the reset signals coming as an input to CPRI IP.

2.6 Interface signals

2.6.1 Interface

The following figure shows the interface signals of the CPRI IP.

Figure 15 • **CPRI IP Interface Signal Description**



2.6.2 Configuration Parameters

The following table lists the configuration parameters used in the hardware implementation process of CPRI IP.

Table 3 • **Configuration Parameter**

Name	Default Setting	Range	Description
Line_Rate	5	1: Line Rate is 614.4 Mbps 2: Line Rate is 1228.8 Mbps 3: Line rate is 2457.6 Mbps 4: Line rate is 3072.0 Mbps 5: Line rate is 4915.2 Mbps 6: Line rate is 6144.0 Mbps 7: Line rate is 9830.4 Mbps	Select the CPRI Line Rate Default setting: 5
no_of_AxC	1	1 to n	Select the number of antenna carriers Default setting: 1 Where, n= number of antenna carriers.

Table 4, page 13 defines CPRI IP clock and reset signals. This table describes the clock and reset signals which are used by the CPRI IP.

Table 4 • **Line Side Interface**

Interface	Width	Input/output	Description
CPRI_TX_CLK	1	Input	Input line clock received from the transceiver (XCVR). This clock is used as the core clock in the CPRI IP transmitter path.
CPRI_RX_CLK	1	Input	Recovered line clock by the XCVR on the RX path.
CPRI_TX_RESETn	1	Input	Active low asynchronous reset, this reset is used to reset the CPRI IP transmit path.
CPRI_RX_RESETn	1	Input	Active low asynchronous reset, this reset is used to reset the CPRI IP receive path.
RX_READY	1	Input	Receive Ready Signal from the transceiver.
RX_VALID	1	Input	Receive Valid Signal from the transceiver.

Table 5, page 13 describes the antenna carrier RX internal signals.

Table 5 • **Antenna Carrier RX Interface Signals**

Interface	Width	Input/output	Description
AxC_rx_clk [n-1:0]	n	Input	Antenna carrier receive clock. Each antenna carrier has a unique clock, which is driven by the application.
AxC_rx_resetn [n-1:0]	n	Input	Antenna carrier receive active low asynchronous reset. Each antenna carrier has a unique reset input signal
AxC_rx_data [n-1:0]	32xn	Output	Antenna carrier RX data. Each antenna carrier has 32-bit data interface.
AxC_rx_valid[n-1:0]	n	Output	Antenna carrier RX valid. Each antenna carrier has a unique RX valid signal.
AxC_rx_req[n-1:0]	n	Input	This signal is sent by the application when it is ready to accept the data from the interface FIFO.

Note: n= number of Antenna carriers.

Table 6, page 14 describes the antenna carrier TX interface signals.

Table 6 • **Antenna Carrier TX Interface Signals**

Interface	Width	Input/output	Description
AxC_tx_clk [n-1:0]	n	Input	Antenna carrier transmit clock. Each antenna carrier has a unique clock, which is driven by the application
AxC_tx_resetn [n-1:0]	n	Input	Antenna carrier transmit active low asynchronous reset. Each Antenna carrier has a unique reset input signal
AxC_tx_data [n-1:0]	32xn	Input	Antenna carrier transmit data. Each antenna carrier has 32-bit data interface.
AxC_tx_valid[n-1:0]	n	Input	Antenna carrier transmit valid, each antenna carrier has a unique transmit valid signal.
AxC_tx_req [n-1:0]	n	Output	This signal is sent by the application when it is ready to accept the data from the interface FIFO.

Note: n= number of Antenna carriers.

Table 7, page 14 describes the CPRI IP Ethernet RX interface signals.

Table 7 • **Ethernet RX Interface**

Interface	Width	Input/output	Description
rx_eth_clk	1	Input	125MHz Ethernet Clock in the receive direction.
rx_eth_resetn	1	Input	Ethernet RX active low asynchronous reset signal.
rx_eth_data	32	Output	32-bit output data on the Ethernet RX user interface.
rx_eth_valid	1	Output	Data valid signal on the Ethernet RX user interface.
rx_eth_req	1	Input	Data Request to the CPRI IP from the Ethernet RX user interface.

Table 8, page 14describes the CPRI IP Ethernet TX interface signals

Table 8 • **Ethernet TX Interface Signals**

Interface	Width	Input/output	Description
tx_eth_clk	1	Input	125MHz Ethernet Clock on the transmit direction.
tx_eth_resetn	1	Input	Ethernet TX active low asynchronous reset.
tx_eth_data	32	Input	32-bit incoming data on the Ethernet TX user interface.
tx_eth_valid	1	Input	Data valid signal on the Ethernet TX user interface.
tx_eth_req	1	Output	Data Request sent by the CPRI IP on the Ethernet TX user interface.

Table 9, page 14 describes the CPRI IP vendor specific RX internal signals

Table 9 • **Vendor Specific RX Interface Signals**

Interface	Width	Input/output	Description
rx_vss_clk	1	Input	Vendor Specific RX Clock.

Table 9 • **Vendor Specific RX Interface Signals**

Interface	Width	Input/output	Description
rx_vss_resetn	1	Input	Vendor Specific RX active low asynchronous reset signal.
rx_vss_data	32	Output	32-bit output data on the vendor specific RX user interface.
rx_vss_valid	1	Output	Data valid signal on the vendor specific RX user interface.
rx_vss_req	1	Input	Data Request to the CPRI IP from the vendor specific RX user internal.

Table 10, page 15 describes the CPRI IP vendor specific TX internal.

Table 10 • **Vendor Specific TX Interface Signals**

Interface	Width	Input/output	Description
tx_vss_clk	1	Input	Vendor specific TX Clock.
tx_vss_resetn	1	Input	Vendor specific TX active low asynchronous reset.
tx_vss_data	32	Input	32-bit incoming data on the vendor specific TX user interface.
tx_vss_valid	1	Input	Data valid signal on the vendor specific TX user interface.
tx_vss_req	1	Output	Data Request sent by the CPRI IP on the vendor specific TX user internal.

Table 11, page 15 describes the CPRI IP antenna carrier control RX internal signals.

Table 11 • **Antenna Carrier Control RX Interface Signals**

Interface	Width	Input/output	Description
rx_ctrl_axc_clk	1	Input	Antenna carrier control RX Clock.
rx_ ctrl_axc _resetn	1	Input	Antenna carrier control RX active low asynchronous reset signal.
rx_ ctrl_axc _data	32	Output	32-bit output data on the antenna carrier control RX user interface.
rx_ ctrl_axc _valid	1	Output	Data valid signal on the antenna carrier control RX user interface.
rx_ ctrl_axc _req	1	Input	Data Request to the CPRI IP from the antenna carrier control RX user internal.

Table 12, page 16 describes the CPRI IP antenna carrier control TX internal signals.

Table 12 • **Antenna Carrier Control TX Interface Signals**

Interface	Width	Input/output	Description
tx_ ctrl_axc _clk	1	Input	Antenna carrier control TX Clock.
tx_ ctrl_axc _resetn	1	Input	Antenna carrier control TX active low asynchronous reset.
tx_ ctrl_axc _data	32	Input	32-bit incoming data on the antenna carrier control TX user interface.
tx_ ctrl_axc _valid	1	Input	Data valid signal on the antenna carrier control TX user interface.
tx_ ctrl_axc _req	1	Output	Data Request sent by the CPRI IP on the antenna carrier control TX user internal.

Table 13, page 16 describes the AHB Bus internal signals.

Table 13 • **AHB Slave Interface Signals**

Interface	Width	Input/output	Description
HWDATA	32	Input	AHB Interface WDATA
HADDR	32	Input	AHB address
HSEL	1	Input	AHB slave select
HTRANS	2	Input	AHB Transaction type
HWRITE	1	Input	AHB Transaction direction
HRDATA	32	Output	AHB slave read data
HRESP	2	Output	AHB slave response
HREADYOUT	1	Output	AHB slave ready
HBURST	3	Input	AHB burst transactions
HSIZE	3	Input	Size of AHB transaction

2.7 Register Interface

2.7.1 AHB Bus Memory Address Map

Following table lists the AHB Bus Memory Map.

Table 14 • **List of Registers**

Offset	Register
0x0	CPRI Control Register see Table 15, page 18
0x4	TX Interface Sequence Number Register see Table 16, page 18
0x8	RX Interface Sequence Number Register see Table 17, page 18
0xC	TX_Z_0_0_SYNC Register (TX Framer K character Register) see Table 18, page 18
0x10	RX_Z_0_0_SYNC Register (RX Framer K character Register) see Table 19, page 19
0x14	TX_Z_0_1_SYNC Register (TX Framer D character Register) see Table 20, page 19
0x18	RX_Z_0_1_SYNC Register (RX Framer D character Register) see Table 21, page 19
0x1c	TX_Z_0_Y_SYNC Register (TX Framer D character Register) see Table 22, page 19
0x20	RX_Z_0_Y_SYNC Register (RX Framer D character Register) see Table 23, page 19
0x24	TX Protocol Version Register see Table 24, page 20
0x28	RX Protocol Version Register see Table 25, page 20
0x2c	TX Fast Ethernet pointer register see Table 26, page 20
0x30	RX Fast Ethernet pointer register see Table 27, page 20
0x34	Signaling Information Register see Table 28, page 20
0x100	Start Timer Register see Table 29, page 21
0x104	HFN Sync Counter Register see Table 30, page 21
0x31C	CPRI Status Register-1 see Table 31, page 21
0x320	CPRI Status Register -2 see Table 32, page 21
0x324	Received Fast Ethernet Pointer Status Register see Table 33, page 22

2.7.2 Register Description

This section describe the registers used in CPRI IP.

Table 15 • **CPRI Control Register- 0X0**

Bit	Type	Function	Default	Description
31:4	R/W	Reserved	0x0	Reserved
3	R/W	IQ_demapper_en	0x0	The IQ demapper block is enabled when this bit is set to "1".
2	R/W	IQ_mapper_en	0x0	The IQ mapper block is enabled when this bit is set to "1".
1	R/W	L1_sync_en	0x0	The L1 sync state machine is active when `L1_sync_en` bit is set to "1".
0	R/W	cpri_en	0x0	CPRI IP functionality is enabled, when this bit is set to "1".

Table 16 • **TX Interface Sequence Number Register- 0x4**

Bit	Type	Function	Default	Description
31:4	R/W	Reserved	0x0	Reserved
5:0	R/W	TX_SEQ_NUM	0x0	The bit specifies the value of the sequence number for the line rates: Line Rate 1: `TX_SEQ_NUM: 0x3` Line Rate 2: `TX_SEQ_NUM: 0x7` Line Rate 3: `TX_SEQ_NUM: 0xf` Line Rate 4: `TX_SEQ_NUM: 0x13` Line Rate 5: `TX_SEQ_NUM: 0x1f` Line Rate 6: `TX_SEQ_NUM: 0x27` Line Rate 7: `TX_SEQ_NUM: 0x3f`

Table 17 • **RX Interface Sequence Number Register - 0x8**

Bit	Type	Function	Default	Description
31:6	R/W	Reserved	0x0	Reserved
5:0	R/W	RX_SEQ_NUM	0x0	The bit specifies the value of the sequence number for the line rates: Line Rate 1: `RX_SEQ_NUM: 0x3` Line Rate 2: `RX_SEQ_NUM: 0x7` Line Rate 3: `RX_SEQ_NUM: 0xf` Line Rate 4: `RX_SEQ_NUM: 0x13` Line Rate 5: `RX_SEQ_NUM: 0x1f` Line Rate 6: `RX_SEQ_NUM: 0x27` Line Rate 7: `RX_SEQ_NUM: 0x3f`

Table 18 • **TX_Z_0_0_SYNC Register- 0xC**

Bit	Type	Function	Default	Description
31:8	R/W	Reserved	0x0	Reserved
7:0	R/W	TX_Z_0_0_SYNC	0x0	This register specifies the value to be written at location Z.0.0, in the CPRI TX frame. Program this register with a value 0xBC which is K28.5 character.

Table 19 • **RX_Z_0_0_SYNC Register - 0x10**

Bit	Type	Function	Default	Description
31:8	R/W	Reserved	0x0	Reserved
7:0	R/W	RX_Z_0_0_SYNC	0x0	This register specifies the value, which is expected at location Z.0.0 in received CPRI frame. Program this register with a value 0xBC which is K28.5 character.

Table 20 • **TX_Z_0_1_SYNC Register - 0x14**

Bit	Type	Function	Default	Description
31:8	R/W	Reserved	0x0	Reserved
7:0	R/W	TX_Z_0_1_SYNC	0x0	This register specifies the value to be written at location Z.0.1 in the CPRI TX frame. Program this register with a value 0x50 which is D16.2 character or 0xc5 which is D5.6 character.

Table 21 • **RX_Z_0_1_SYNC Register - 0x18**

Bit	Type	Function	Default	Description
31:8	R/W	Reserved	0x0	Reserved
7:0	R/W	RX_Z_0_1_SYNC	0x0	This register specifies the value, which is expected at location Z.0.0 in received CPRI frame. Program this register with a value 0x50 which is D16.2 character or 0xc5 which is D5.6 character.

Table 22 • **TX_Z_0_Y_SYNC Register - 0x1C**

Bit	Type	Function	Default	Description
31:8	R/W	Reserved	0x0	Reserved
7:0	R/W	TX_Z_0_Y_SYNC	0x0	This register specifies the value to be written at location Z.0.Y in the CPRI TX frame. Program this register with a value 0x50 which is D16.2 character or 0xc5 which is D5.6 character.

Table 23 • **RX_Z_0_Y_SYNC Register - 0x20**

Bit	Type	Function	Default	Description
31:8	R/W	Reserved	0x0	Reserved
7:0	R/W	RX_Z_0_Y_SYNC	0x0	This register specifies the value, which is expected at location Z.0.Y in received CPRI frame. Program this register with a value 0x50 which is D16.2 character or 0xc5 which is D5.6 character.

Table 24 • **TX protocol version register - 0x24**

Bit	Type	Function	Default	Description
31:8	R/W	Reserved	0x0	Reserved
7:0	R/W	TX_Z_2_0_SYNC	0x0	This register specifies the value of the Protocol Version to be written at Z.2.0 location in the CPRI TX frame. For CPRI IP to work properly, program this register with value 0x1, as the current version of the IP supports only protocol version 1.

Table 25 • **RX protocol version register - 0x28**

Bit	Type	Function	Default	Description
31:8	R/W	Reserved	0x0	Reserved
7:0	R/W	RX_Z_2_0_SYNC	0x0	This register specifies the value of the Protocol Version which is expected at Z.2.0 location in the received CPRI frame. For CPRI IP to work properly, program this register with value 0x1, as the current version of the IP supports only protocol version 1.

Table 26 • **TX Fast Ethernet Pointer Register - 0x2C**

Bit	Type	Function	Default	Description
31:8	R/W	Reserved	0x0	Reserved
7:0	R/W	TX_Z_194_0	0x0	This register specifies the value of the Fast Ethernet Pointer to be written at location Z.194.0. For the CPRI IP to work properly, program this register with value 0x20, as the current version of the IP expects the Fast Ethernet data to be written from location 0x20.

Table 27 • **RX Fast Ethernet Pointer Register - 0x30**

Bit	Type	Function	Default	Description
31:8	R/W	Reserved	0x0	Reserved
7:0	R/W	RX_Z_194_0	0x0	This register specifies the value of the Fast Ethernet Pointer which is expected at Z.194.0 location in the received CPRI frame. For the CPRI IP to work properly, program this register with value 0x20, as the current version of the IP expects the Fast Ethernet data to be written from location 0x20.

Table 28 • **TX Signaling Information Register - 0x34**

Bit	Type	Function	Default	Description
31:8	R/W	Reserved	0x0	Reserved
7:0	R/W	RX_Z_130_0	0x0	This register specifies the value of the Signalling Information (L1 Inband Protocol information) to be written at location Z.130.0.

Table 29 • **Startup Timer Register - 0x100**

Bit	Type	Function	Default	Description
31:0	R/W	startup_timer	0x0	This register specifies the time out value, which is used by the start-up timer in the L1 Sync State Machine.

Table 30 • **HFN Count Register- 0x104**

Bit	Type	Function	Default	Description
31:0	R/W	HFN_COUNT	0x0	This register specifies Hyperframe Count Value. This value indicates the duration of one CPRI Hyperframe for the selected Line rate Line 1: `HFN_COUNT: 3FF` Line 2: `HFN_COUNT: 7FF` Line 3: `HFN_COUNT: FFF` Line 4: `HFN_COUNT: 13FF` Line 5: `HFN_COUNT: 1FFF` Line 6: `HFN_COUNT: 27FF` Line 7: `HFN_COUNT: 3FFF`

Table 31 • **CPRI Status Register-1 - 0x31C**

Bit	Type	Function	Default	Description
31:3	R	Reserved	0x0	Reserved
2	R	RX_VALID	0x0	The value 0x1 indicates that XCVR RX_VALID signal is high,
1	R	RX_READY	0x0	The value 0x1 indicates that RX_READY signal from XCVR is high.
0	R	cpri_rx_aligned	0x0	The value 0x1 indicates that CPRI HFN Sync is achieved.

Table 32 • **CPRI Status Register-2 - 0x320**

Bit	Type	Function	Default	Description
31:5	R	Reserved	0x0	Reserved
4	R	RE_RESET	0x0	The value 0x1 indicates that RE_RESET signal is received from the CPRI Master
3	R	LOF	0x0	The value 0x1 indicates the LOF signal is received from the CPRI Master
2	R	LOS	0x0	The value 0x1 indicates that LOS signal is received from the CPRI Master
1	R	cm_setup_done	0x0	The value 0x1 indicates that C&M setup is done.
0	R	Protocol_setup_done	0x0	The value 0x1 indicates that protocol setup is done

Table 33 • **Received Fast Ethernet Pointer Status Register- 0x324**

Bit	Type	Function	Default	Description
31:8	R	Reserved	0x0	Reserved
7:0	R	rcvd_fast_ethernet_ pointer	0x0	This register returns the value of the Fast Ethernet pointer received from the CPRI Master.

Note: Enable the CPRI Control register after all other registers are programmed. For enabling the CPRI IP, follow these steps.

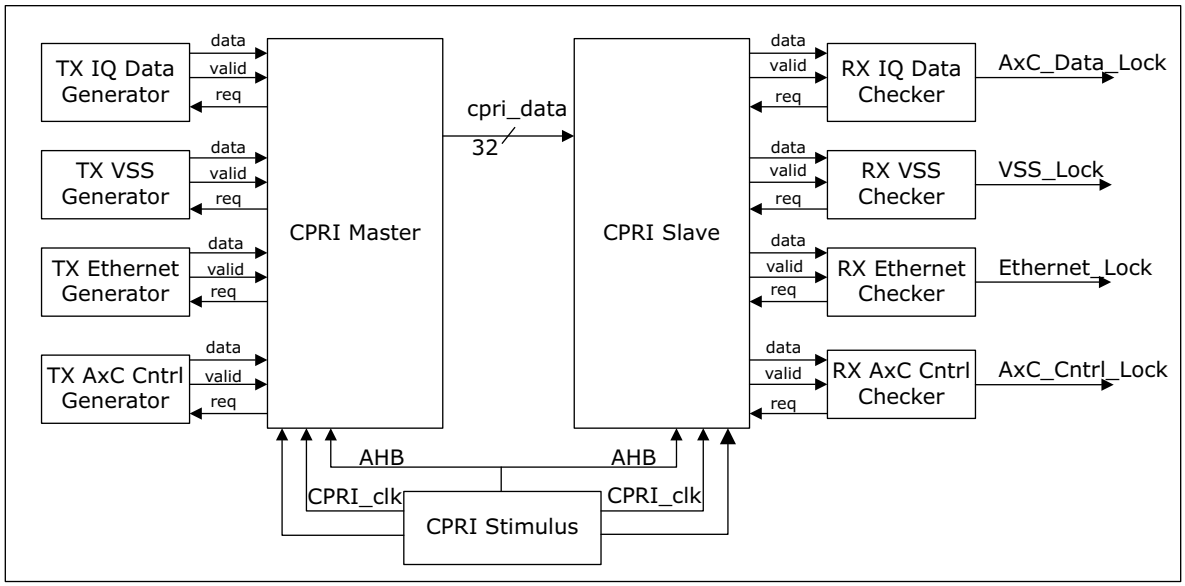
1. First program the respective fields of all the registers from offset 0x4 to 0x104.
2. Write the corresponding bits in the CPRI Control Register at offset 0x0.

2.8 TestBench

Following figure shows the top level block diagram of the testbench which comes along with the CPRI IP. The CPRI master block receives the IQ data from the TX IQ Data Generator and control information such as Ethernet, vendor specific and antenna carrier control from the respective Generator BFMs. CPRI master then frames the incoming data and transmit the 32-bit CPRI frame to the CPRI slave. The CPRI slave then receives the incoming frames and demaps incoming data. The demapped data is then sent to the respective checker blocks.

For example, received IQ data is then transmitted to the RX IQ Data checker block. If the incoming IQ data matches with the expected data, then AxC_Data_Lock signal is asserted. Similarly, when incoming control information matches with the expected control data for vendor specific, Fast Ethernet and antenna carrier control data, then respective lock signals are asserted. Otherwise, the lock signals are low.

Figure 16 • **CPRI IP Top Level TestBench**



A testbench is provided to check the functionality of the CPRI IP. The following table lists the parameters that can be configured according to the application. All the parameters used in the CPRI IP testbench are located in the `core_parameter.v` file, which is included in the top level CPRI testbench.

Table 34 • **CPRI IP TestBench Parameters**

Name	Default Setting	Range	Description
Line_Rate	5	2: Line rate is 1228.8 Mbps 3: Line rate is 2457.6 Mbps 5: Line rate is 4915.2 Mbps 7: Line rate is 9830.4 Mbps	Selects the CPRI Line Rate. Default Setting: 5
no_of_AxC	4	1 to n	Selects the number of antenna carriers. Default Setting: 4 Where *n* is the number of antenna carriers.
PATTERN_TYPE	2	1: Fixed Pattern 2: Incremental Pattern	This parameter defines the type of pattern used while verifying the CPRI IP.
PATTERN_VSS	0xF0F0F0F0	32-bit pattern	32-bit fixed pattern used by TX vendor specific generator when PATTERN_TYPE parameter is set to 0x1.
PATTERN_ETH	0xA0A0A0A0	32-bit pattern	32-bit fixed pattern used by TX Ethernet Generator when PATTERN_TYPE parameter set to 0x1.
PATTERN_AxC_ Cntrl	0xAAAAAAAA	32-bit pattern	32-bit fixed pattern used by TX antenna carrier control generator when PATTERN_TYPE parameter set to 0x1.
PATTERN_Q	0x55aa	15-bit pattern	15-bit Q data when PATTERN_TYPE parameter is set to 0x1.
PATTERN_I	0x33cc	15-bit pattern	15-bit I data when PATTERN_TYPE parameter is set to 0x1.

2.9 SmartDesign

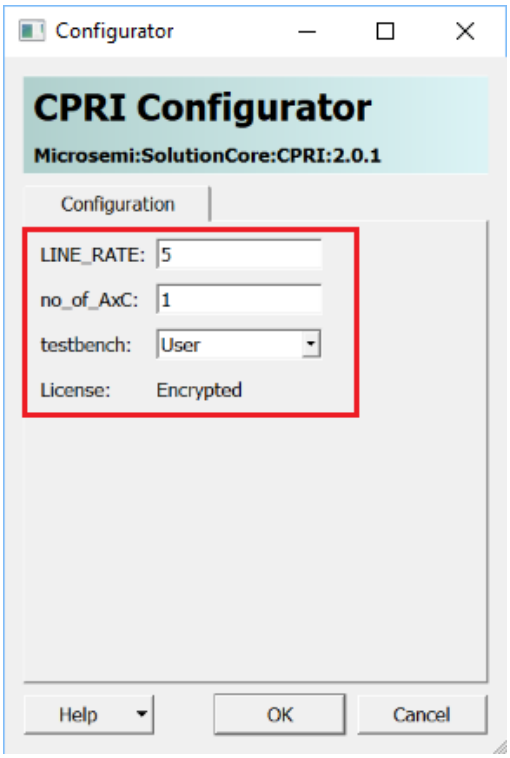
The CPRI IP is available for download in the Libero IP catalog, Solutions-Wireless. Once it is listed in the catalog, then the core can be instantiated using the SmartDesign flow. For more information, on how to use SmartDesign to configure, connect, and generate cores, see to the Libero SoC online help.

After configuring and generating the core instance, basic functionality can be simulated using the testbench supplied with the CPRI IP. The testbench parameters can be updated in the `core_parameter.v` file which is available in *component\Microsemi\SolutionCore\CPRI\2.0.1\stimulus* directory. For more information on testbench parameters see, Table 34, page 23.The CPRI IP can be instantiated as a component of a larger design. CPRI IP is compatible with Libero SoC PolarFire.

2.9.1 Configuring CPRI IP in PolarFire

The CPRI IP can be configured using the configuration user interface within SmartDesign. An example of the user interface for the PolarFire family is shown in the following figure.

Figure 17 • **CPRI IP Configurator**

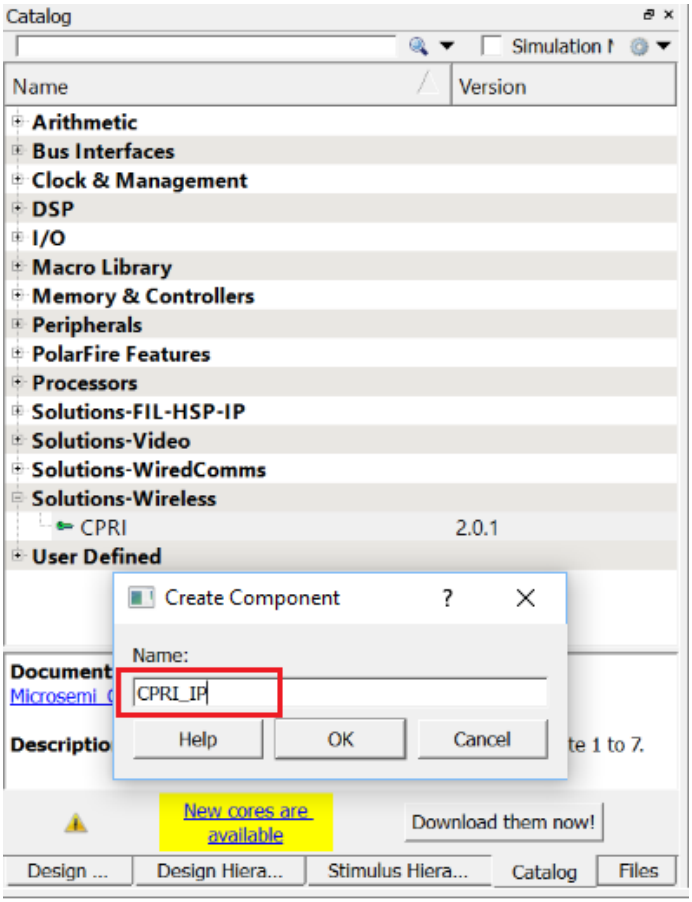


2.9.2 Simulation Flow

The user testbench for CPRI IP is included in the release. The user testbench is selected through the CPRI IP Configurator. When SmartDesign generates the CPRI IP, it installs the user testbench files in **Stimulus Hierarchy** tab. Following steps describe how to run the CPRI IP testbench.

1. Select **Catalog**, expand **Solutions**> **Wireless** and right-click **CPRI**. Select the **Configure Core** and provide the name in **Create Component** window, as shown in following figure.

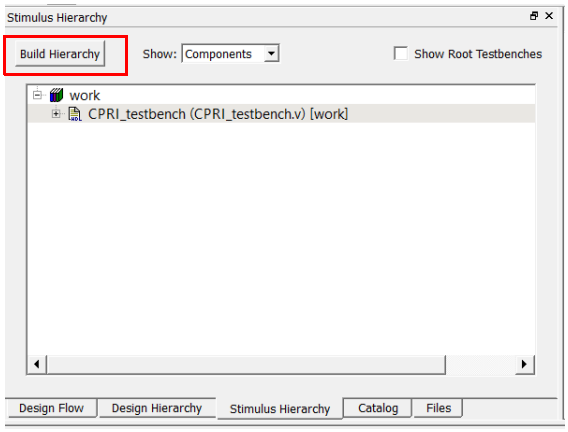
Figure 18 • **Core Configurator**



2. To configure the core, see Figure 17, page 24.

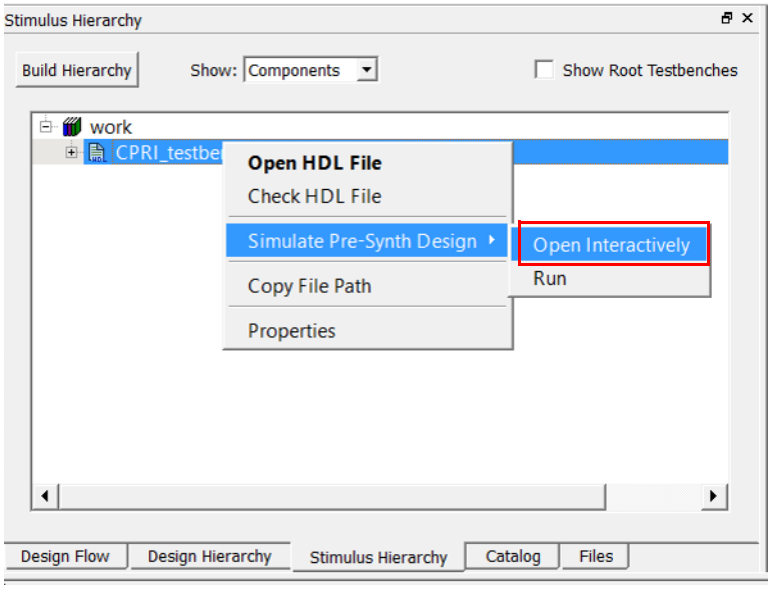
3. Go to **Design Hierarchy** and click **Build Hierarchy** to generate `CPRI_testbench.v` under **Stimulus Hierarchy** as shown in the following figure.

Figure 19 • **Build Hierarchy**



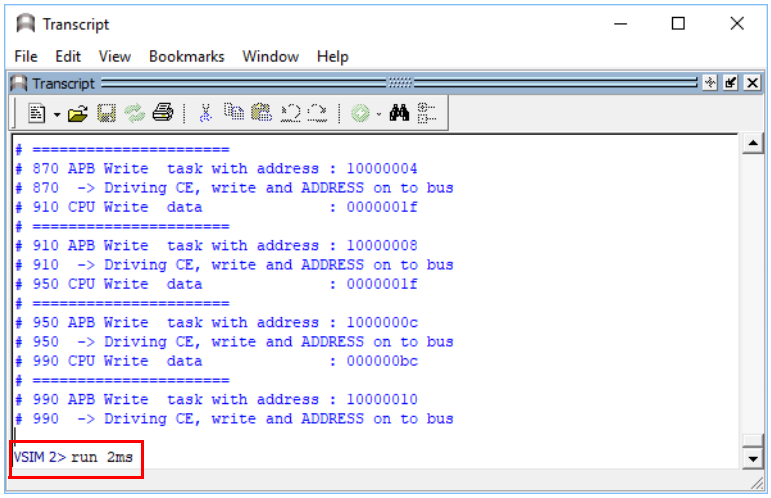
4. Right-Click `CPRI_testbench.v`, select **Simulate Pre-Synth Design** > **Open Interactively**.

Figure 20 • **Simulating the Pre-Synthesis Design Option**



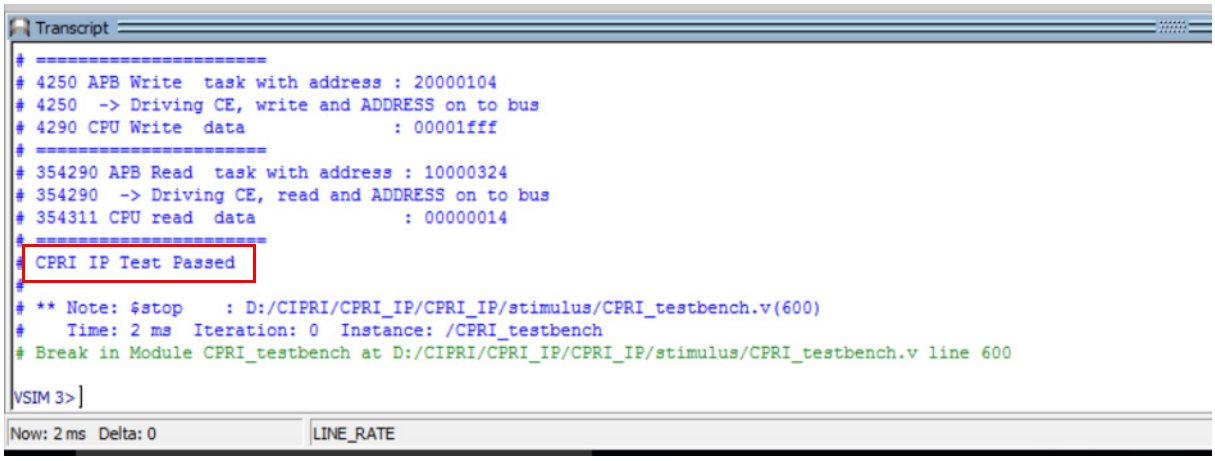
5. ModelSim starts the testbench execution. Run the testbench for 2ms. To do this, enter the command `run 2ms` in **Transcript** window, as shown in the following figure.

Figure 21 • **Command Window**



6. See the results in **Transcript** window, to verify if CPRI IP passed or failed. When the received data matches the expected data, CPRI IP test passes. Otherwise the CPRI IP test fails.

Figure 22 • **Test Results**



2.10 Resource Utilization

CPRI IP is implemented in PolarFire FPGA. The following table lists the resource utilization of CPRI IP in PolarFire FPGA.

Table 35 • **CPRI Resource Utilization Table**

Working Mode		Resource Utilization			
Line Rate	Number of Antenna Carriers	DFF	LUT	uSRAM	LSRAM
2	2	3289	2592	0	10
2	4	4711	3354	0	14
3	2	3821	3654	0	10
3	4	4583	5310	0	14
5	4	5852	8221	0	14
5	8	10795	13469	0	22
7	8	10870	6316	0	22

3 Appendix: Verification

3.1 Use Case: Line Rate 5 and No_of_AxC 4

Follow these steps to configure a CPRI IP in SmartDesign:

1. Configure the CPRI IP in SmartDesign to Line Rate 5 and no_of_AxC 4.
2. Open the `core_prameter.v` in stimulus directory and update the following testbench parameters
   - Set Line_Rate to 5
   - Set No_of_AxC to 4
3. Configure the following registers

```
//Configuring CPRI Master Registers (Base Address 0x20000000)
  AHB_WRITE (32'h20000004, 32'h1f); //TX_SEQ_NUM
  AHB_WRITE (32'h20000004, 32'h1f); //RX_SEQ_NUM
  AHB_WRITE (32'h2000000C, 32'hBC); //TX_Z_0_0_SYNC Register
  AHB_WRITE (32'h20000010, 32'hBC); //RX_Z_0_0_SYNC Register
  AHB_WRITE (32'h20000014, 32'h50); //TX_Z_0_1_SYNC Register
  AHB_WRITE (32'h20000018, 32'h50); //RX_Z_0_1_SYNC Register
  AHB_WRITE (32'h2000001C, 32'h50); //TX_Z_0_Y_SYNC Register
  AHB_WRITE (32'h10000020, 32'h50); //RX_Z_0_Y_SYNC Register
  AHB_WRITE (32'h20000024, 32'h01); //TX protocol version register
  AHB_WRITE (32'h2000002C, 32'h14); //TX fast Ethernet pointer register
  AHB_WRITE (32'h20000030, 32'h14); //RX fast Ethernet pointer register
  AHB_WRITE (32'h20000100, 32'd1000000); //Start Up Timer Register
  AHB_WRITE (32'h20000104, 32'h1fff); //HFN Count Register


//Configuring CPRI Slave Registers (Base Address 0x10000000)
  AHB_WRITE (32'h10000004, 32'h1f); //TX_SEQ_NUM
  AHB_WRITE (32'h10000004, 32'h1f); //RX_SEQ_NUM
  AHB_WRITE (32'h1000000C, 32'hBC); //TX_Z_0_0_SYNC Register
  AHB_WRITE (32'h10000010, 32'hBC); //RX_Z_0_0_SYNC Register
  AHB_WRITE (32'h10000014, 32'h50); //TX_Z_0_1_SYNC Register
  AHB_WRITE (32'h10000018, 32'h50); //RX_Z_0_1_SYNC Register
  AHB_WRITE (32'h1000001C, 32'h50); //TX_Z_0_Y_SYNC Register
  AHB_WRITE (32'h10000020, 32'h50); //RX_Z_0_Y_SYNC Register
  AHB_WRITE (32'h10000024, 32'h01); //TX protocol version register
  AHB_WRITE (32'h1000002C, 32'h14); //TX fast Ethernet pointer register
  AHB_WRITE (32'h10000030, 32'h14); //RX fast Ethernet pointer register
  AHB_WRITE (32'h10000100, 32'd1000000); //Start Up Timer Register
  AHB_WRITE (32'h10000104, 32'h1fff); //HFN Count Register
//Enabling the CPRI Master by writing into CPRI Master Control register
  #500
  AHB_WRITE (32'h20000000, 32'h4);
  AHB_WRITE (32'h20000000, 32'h5);
  AHB_WRITE (32'h20000000, 32'hf);
```

```
  #500
//Enabling the CPRI Slave by writing into CPRI Slave Control register
  AHB_WRITE (32'h10000000, 32'h1);
  AHB_WRITE (32'h10000000, 32'hB);
  #200
  AHB_WRITE (32'h10000000, 32'hf);
```