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Release Notes
CoreColDet v2.0

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

This is the first publication of this document. Created for CoreColDet v2.0.

Contents

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2 CoreColDet

This release notes accompanies the production release of CoreColDet v2.0 IP Core. This document provides details about the features, system requirements, supported families, implementations, and known issues and workarounds.

2.1 Key Features

CoreColDet detects collision when there is simultaneous read/write access to the same location at the same time.

2.2 Delivery Types

CoreColDet is licence free.

2.2.1 Register Transfer Level (RTL)

The complete RTL source code is provided for the core and testbench.

2.3 Supported Families

Supported by all families.

2.4 Supported Tool Flows

Requires Libero® System-on-Chip (SoC) v12.0 or later.

2.5 Installation Instructions

The CoreColDet CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

For more information and instructions on core installation, licensing, and general use, see the *Using DirectCore section in Libero SoC for Classic Constraint Flow User Guide* or *Libero SoC Online Help*.

2.6 Supported Test Environments

Verilog user test bench is the supported test environment.

2.7 Documentation

This release contains a copy of the CorColDet Handbook. The handbook describes the core functionality, and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and implementation suggestions.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit: *http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores*.

2.8 Known Issues and Workarounds

There are no known limitations and workarounds for CoreColDet.

2.9 Resolved Issues

The following table lists the resolved issues in v2.0 Release.

Table 1 • **Resolved SARs in CoreColDet v2.0 Release**

SAR	Description
109049	Collision Detection IP is developed which detects collision and performs write over read.