HB0910

Handbook
CoreColDet v2.0

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Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

This is the first publication of this document. Created for CoreColDet v2.0.

2 Acronyms

The following acronyms are used in this document.

Table 1 • **List of Acronyms**

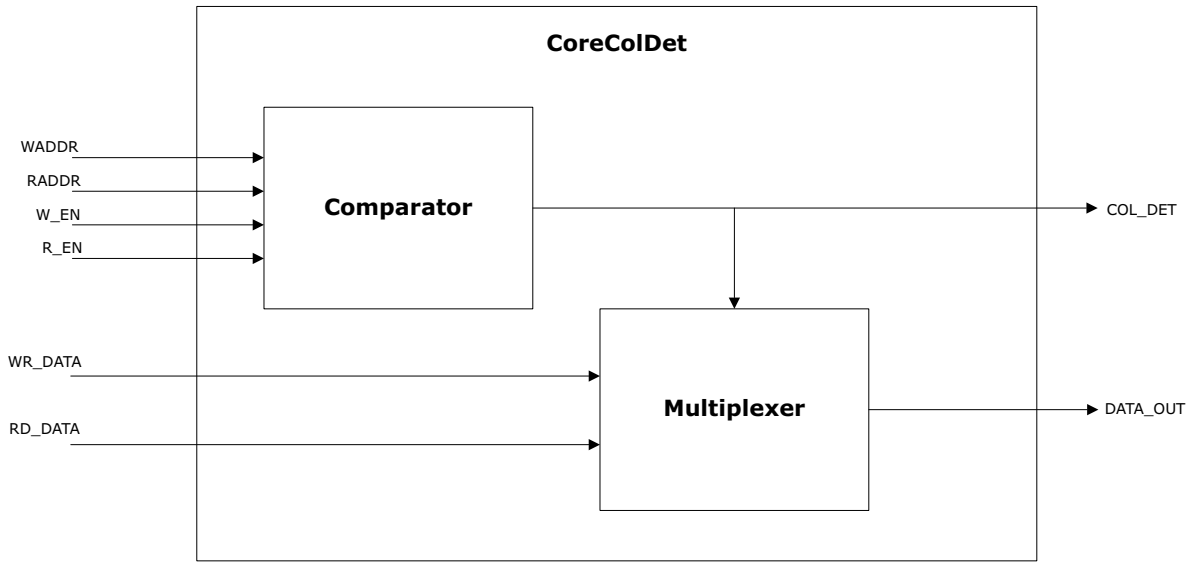
Acronym	Expanded
LSRAM	Large Synchronous Random Accessible Memory
uSRAM	Micro Synchronous Random Accessible Memory
ECC	Error Correcting Codes

3 Introduction

CoreColDet detects collision when there is simultaneous read and write access to the same location. The implementation gives priority to write over read.

This IP generates signal COL_DET, which signifies detection of collision whenever read and write address are same at the same edge of clock and subsequently the logic gives priority to write over read.

Figure 1 • **CoreColDet Block Diagram**



3.1 Key Features

This IP detects a collision of read and write addresses.

3.2 Core Version

This handbook is for CoreColDet version 2.0.

3.3 Supported Families

The following families are supported in this version:

- PolarFire SoC
- PolarFire®
- RTG4™
- SmartFusion®2
- IGLOO®2

3.4 Utilization and Performance

The following tables describe the different configurations.

Table 2 • **Resource Utilization and Performance for Different Families (ECC = Disabled, PIPE = Non-Pipelined)**

	Logic Elements			
Family	**Sequential**	**Combinational**	**Total**	**Performance**
SmartFusion2	66	42	108	525.1 MHz
IGLOO2	66	42	108	525.1 MHz
RTG4	66	42	108	249.8 MHz
PolarFire	66	42	108	557.3 MHz

Note: ADDR_WIDTH = 16, DATA_WIDTH = 32, ECC = Disabled, PIPE = Non-Pipelined.

Table 3 • **Resource Utilization and Performance for Different Families (ECC = Non-Pipelined, PIPE = Pipelined)**

	Logic Elements			
Family	**Sequential**	**Combinatorial**	**Total**	**Performance**
RTG4	99	44	143	249.8 MHz
PolarFire	99	44	143	557.3 MHz

Note: ADDR_WIDTH = 16, DATA_WIDTH = 32, ECC = Non-Pipelined, PIPE = Pipelined.

Table 4 • **Resource Utilization and Performance for Different Families (ECC = Pipelined, PIPE = Non-Pipelined)**

	Logic Elements			
Family	**Sequential**	**Combinatorial**	**Total**	**Performance**
RTG4	115	44	159	249.8 MHz
PolarFire	99	44	143	557.3 MHz

Note: ADDR_WIDTH = 16, DATA_WIDTH = 32, ECC = Pipelined, PIPE = Non-Pipelined.

Table 5 • **Resource Utilization and Performance for Different Families (ECC = Pipelined, PIPE = Pipelined)**

	Logic Elements			
Family	**Sequential**	**Combinatorial**	**Total**	**Performance**
RTG4	148	44	192	249.8 MHz
PolarFire	132	44	176	557.3 MHz

Note: ADDR_WIDTH = 16, DATA_WIDTH = 32, ECC = Pipelined, PIPE = Pipelined.

In Table 5 for RTG4 family, Sequential Logic Elements for different ADDR_WIDTH and DATA_WIDTH can be calculated as: Sequential elements = (4 x DATA_WIDTH + ADDR_WIDTH + 4).

Also, in Table 5 for PolarFire or PolarFire SoC family, Sequential Logic Elements for different ADDR_WIDTH and DATA_WIDTH can be calculated as:

Sequential elements = (3 x DATA_WIDTH + 2 x ADDR_WIDTH + 4)

Note: Resource utilization for PolarFire SoC is same as utilization for PolarFire family.

4 Design Description

The CoreColDet soft IP detects a collision on simultaneously reading and writing into the same locations. Different Configuration has different latencies from memory.

The design compares write address and read address to detect a collision and provide signals COL_DET and DATA_OUT at given latencies as shown in Table 6. When the ECC is pipelined in RTG4, core compares the register version of write address with read address to detect collision as there is a one clock cycle latency during write as shown in Table 7.

When ECC is enabled and collision occurs, SB_CORRECT or DB_DETECT flags coming from the memory may be high. This is not a valid scenario, CoreColDet ignores SB_CORRECT and DB_DETECT flags when collision occurs and drives low to SB_CORRECT_OUT and DB_DETECT_OUT flags. For normal operation, SB_CORRECT_OUT and DB_DETECT_OUT flags are directly assigned to SB_CORRECT and DB_DETECT flag respectively.

When ECC is enabled, the user should use SB_CORRECT_OUT and DB_DETECT_OUT flags to monitor error status.

Table 6 • **Latency Calculation for Different Configuration of Memory (Except RTG4 Family)**

ECC	Memory Configuration	DATA_OUT latency	COL_DET latency
Disabled	Asynchronous	0	0
	Non-Pipelined	1	1
	Pipelined	2	2
Pipelined	Asynchronous	NA	NA
	Non-Pipelined	2	2
	Pipelined	3	3
Non-Pipelined	Asynchronous	0	0
	Non-Pipelined	1	1
	Pipelined	2	2

Table 7 • **Latency Calculation for Different Configuration of Memory for RTG4 Family**

ECC	Memory Configuration	DATA_OUT latency	COL_DET latency
Disabled	Asynchronous	0	0
	Non-Pipelined	1	1
	Pipelined	2	2
Pipelined	Asynchronous	NA	NA
	Non-Pipelined	3 (1 clock for write and 2 clock for read)	3 (1 clock for write and 2 clock for read)
	Pipelined	4 (1 clock for write and 3 clock for read)	4 (1 clock for write and 3 clock for read)
Non-Pipelined	Asynchronous	0	0
	Non-Pipelined	1	1
	Pipelined	2	2

Note:

1. In the PolarFire family, uSRAM does not support the ECC feature.
2. LSRAM does not support memory in the asynchronous configuration.
3. In case when memory is configured in asynchronous mode and ECC is in the nonpipelined, configuration is supported by RTG4 uSRAM only.
4. SmartFusion2 and IGLOO2 family does not support the ECC feature. Also, LSRAM configured in asynchronous mode is not supported while it is supported by uSRAM.

5 Core Interfaces

The following section describes the input / output signals and parameters.

5.1 I/O Signals

The port signals for the CoreColDet is shown in Figure 1, page 3 and defined in Table 8.

Table 8 • **Input and Output Signals for CoreColDet**

Name	Type	Description
CLK	Input	Clock input from system.
W_EN	Input	Write Enable. Synchronous to clock domain.
R_EN	Input	Read Enable. Synchronous to clock domain.
WADDR[ADDR_WIDTH - 1:0]	Input	Write address. Synchronous to clock domain.
RADDR[ADDR_WIDTH - 1:0]	Input	Read Address. Synchronous to clock domain.
WR_DATA[DATA_WIDTH - 1:0]	Input	Data to be written on WADDR of the Memory. Synchronous to clock domain.
RD_DATA[DATA_WIDTH - 1:0]	Input	Data read from RADDR of the Memory. Synchronous to clock domain except when PIPE is asynchronous for SEL_SRAM_TYPE = uSRAM.
SB_CORRECT*	Input	Single bit error Correct Flag input from RAM.
DB_DETECT*	Input	Multiple bit error Detect Flag input from RAM.
SB_CORRECT_OUT*	Output	Single bit error Correct Flag output.
DB_DETECT_OUT*	Output	Multiple bit error Detect Flag output.
DATA_OUT[DATA_WIDTH - 1:0]	Output	Data Output from Core (Combinational).
COL_DET	Output	Output signal detecting Collision. This signal goes HIGH for one clock (CLK) cycle when collision is detected depending on the latency shown in Table 6, page 5/Table 7, page 5.

Note: *Used only when ECC is pipelined or ECC is non-pipelined.

5.2 Core Parameters

The following table describes the CoreColDet parameters for configuring the RTL code. All the parameters are integer types:

Table 9 • **Parameter Descriptions for CoreColDet**

Name	Valid Range	Default	Description
ADDR_WIDTH	1 - 32	10	Address width.
DATA_WIDTH	1 - 512	32	Data width.
SEL_RAM_TYPE	0 - 1	0	0 - LSRAM 1 - uSRAM
PIPE	1, 2 for LSRAM	1	1 - Non-pipelined/transparent read data out 2 - Pipelined read data out
	0, 1, 2 for uSRAM	1	0 - Asynchronous 1 - Non-pipelined/transparent read data out 2 - Pipelined read data out
ECC	0, 1, 2	0	0 - Disabled 1 - Pipelined 2 - Non-pipelined

Note: The parameters for Memory (LSRAM or uSRAM SgCore) and CoreColDet IP must be same.

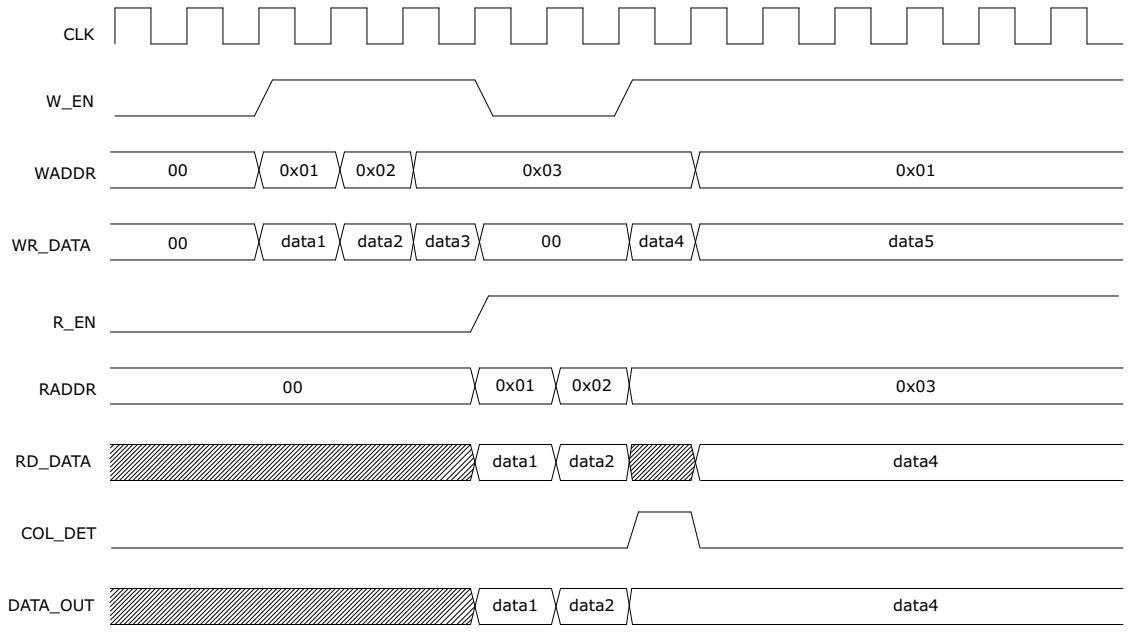
6 Timing Diagrams

From Table 6, page 5/Table 7, page 5 of latency calculation, the inferred RAM is configured in different configurations depending on parameters ECC, PIPE, and SEL_RAM_TYPE.

Different waveforms are depicted by taking all the different cases for ECC and PIPE.

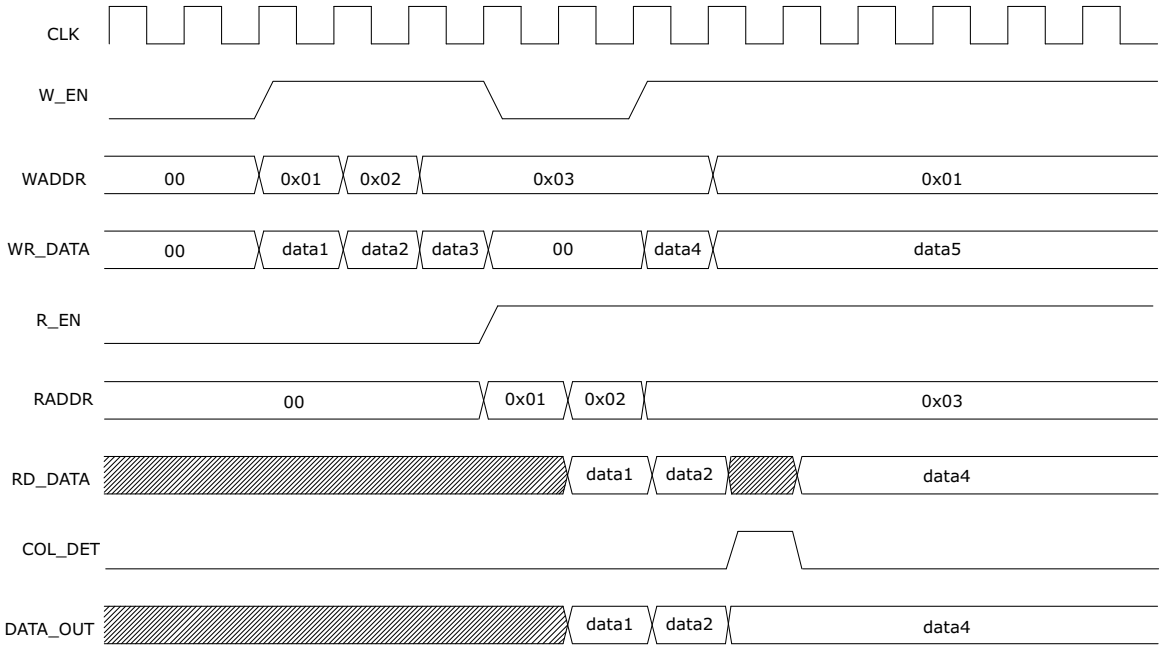
6.1 For (ECC = Disabled and PIPE = Asynchronous) or (ECC = Non-Pipelined and PIPE = Asynchronous)

Figure 2 • **Timing Diagram for CoreColDet with Zero Clock Latency**



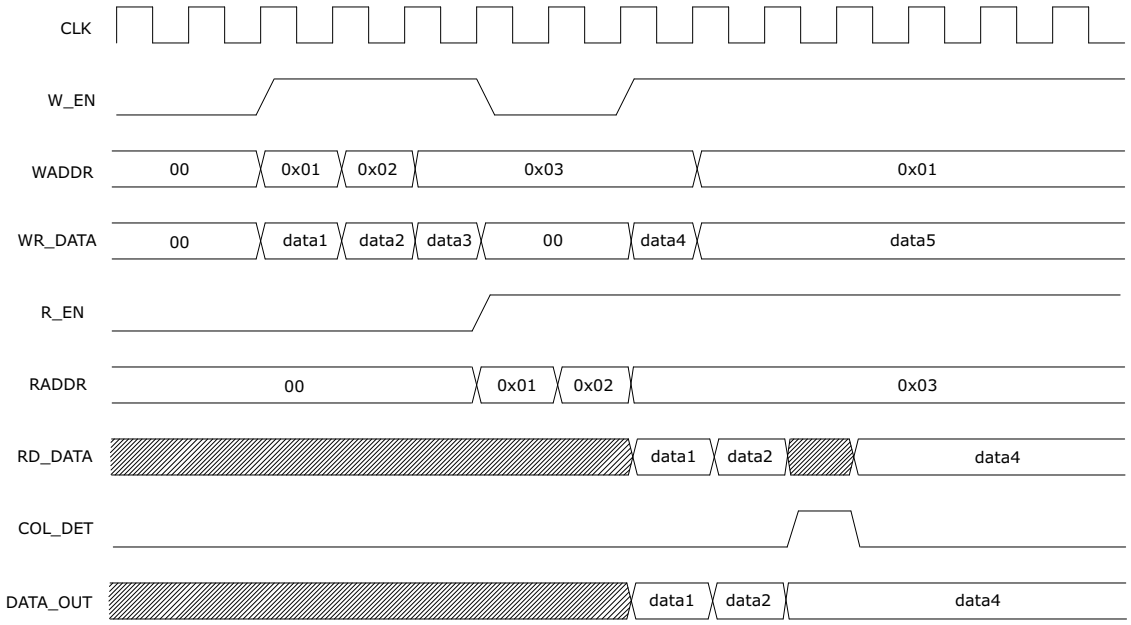
6.2 For (ECC = Disabled and PIPE = Non-Pipelined) or (ECC = Non-Pipelined and PIPE = Non-Pipelined)

Figure 3 • **Timing Diagram for CoreColDet with One Clock Latency**



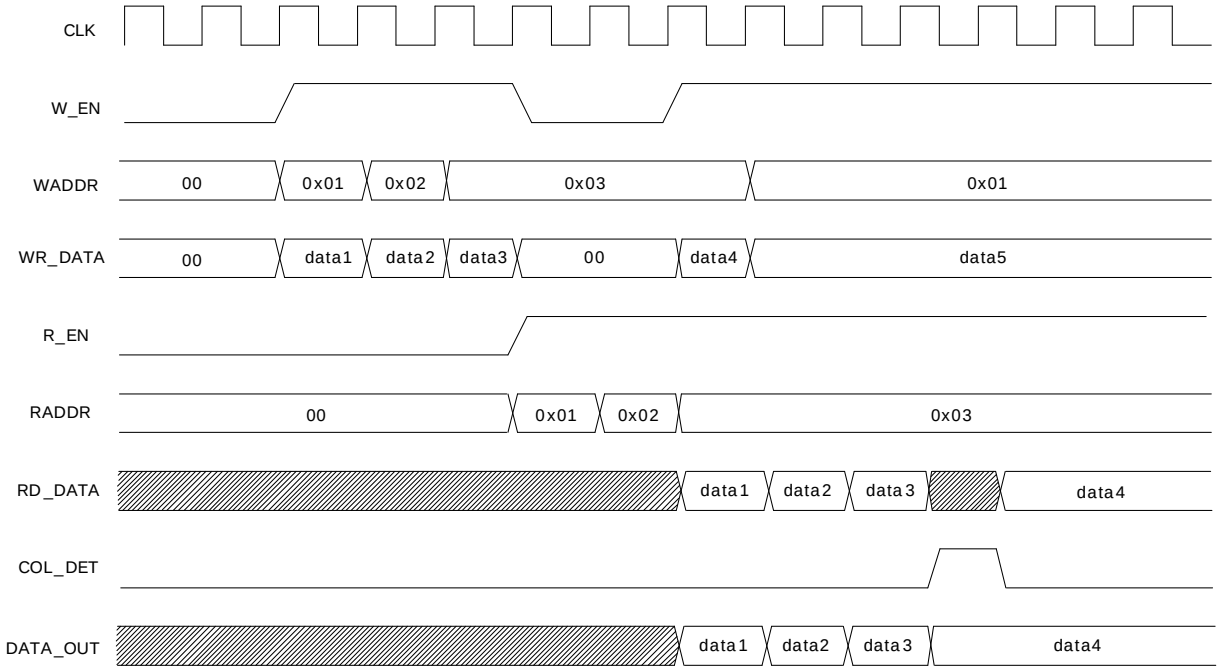
6.3 For (ECC = Disabled and PIPE = Pipelined) or (ECC = Non-Pipelined and PIPE = Pipelined) or (ECC = Pipelined and PIPE = Non-pipelined)

Figure 4 • **Timing Diagram for CoreColDet with Two Cock Latency**



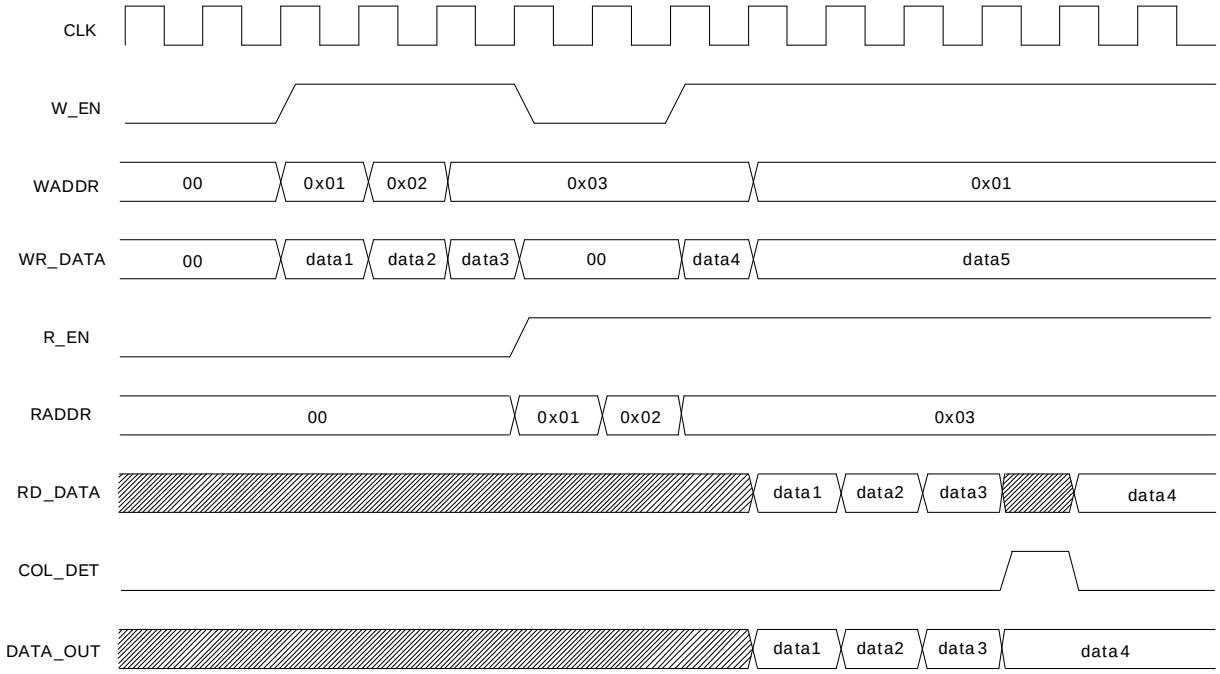
6.4 For ECC = Pipelined and PIPE = Non-Pipelined (For RTG4 Family)

Figure 5 • **Timing Diagram for CoreColDet with Three Clock Latency (1 Clock for Write and 2 Clocks for Read)**



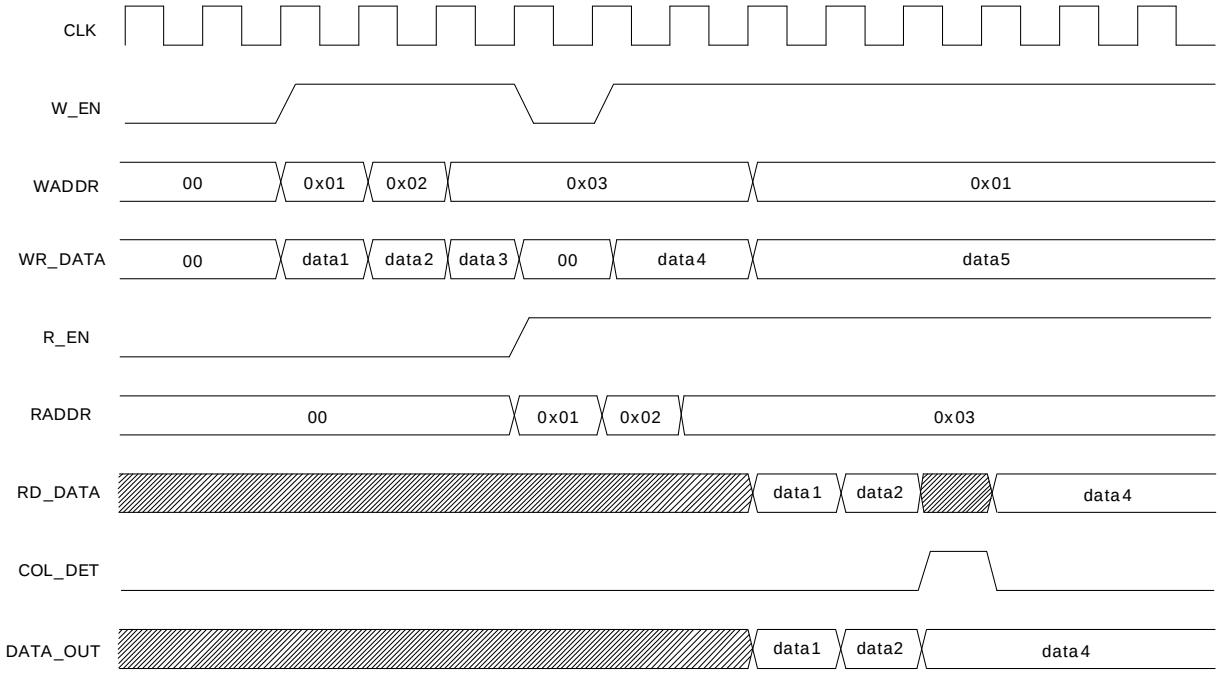
6.5 For ECC = Pipelined and PIPE = Pipelined (For RTG4 Family)

Figure 6 • **Timing Diagram for CoreColDet with Four Clock Latency (1 Clock for Write and 3 Clocks for Read)**



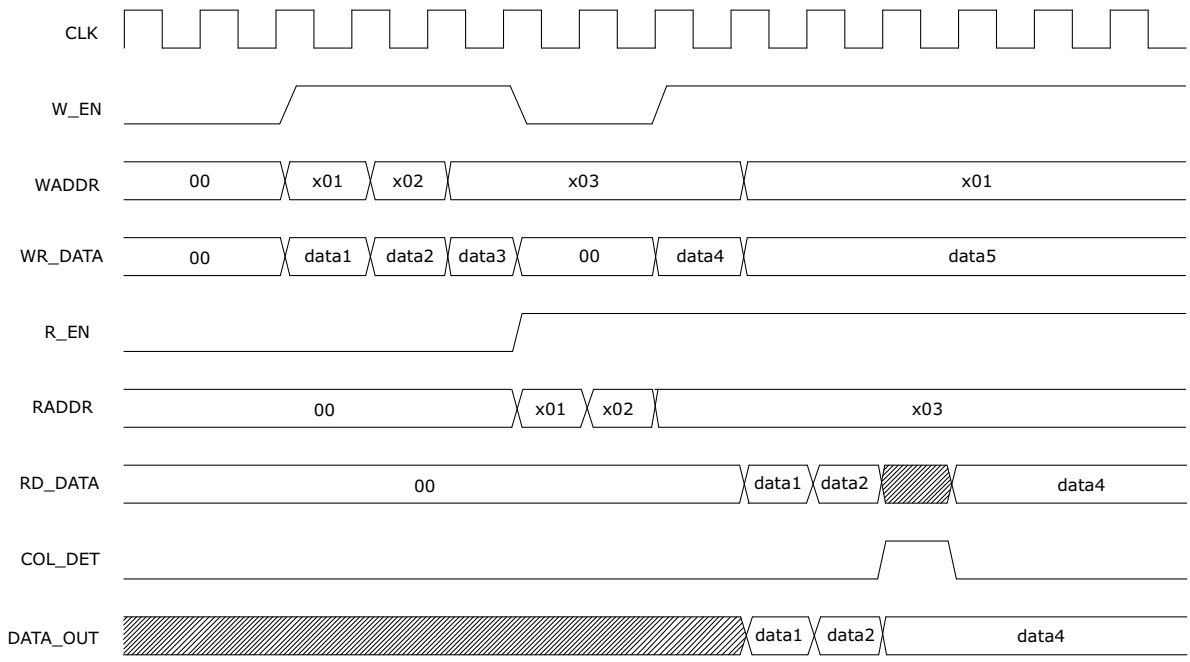
6.6 For ECC = Pipelined and PIPE = Pipelined (For RTG4 Family)

Figure 7 • **Timing Diagram for CoreColDet with Four Clock Latency (1 Clock for Write and 3 Clocks for Read)**



6.7 ECC = Pipelined and PIPE = Pipelined

Figure 8 • **Timing Diagram for CoreColDet with Three Clock Latency**



Note: For RTG4 Family, when ECC is pipelined, read and write will take an extra clock cycle.

7 Tool Flows

7.1 License

The CoreColDet does not require any license.

7.2 RTL

Complete RTL source code is provided for the core and testbench.

7.3 SmartDesign

CoreColDet is preinstalled in the SmartDesign IP Deployment design environment. For information on using the SmartDesign to instantiate and generate cores, refer to the *Using DirectCore in Libero SoC User Guide*.

Figure 9 • **CoreColDet Instance View**

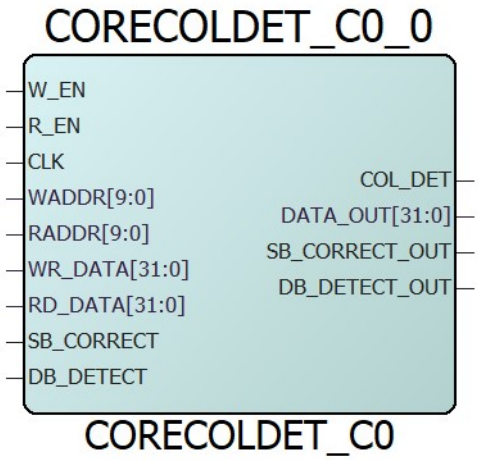
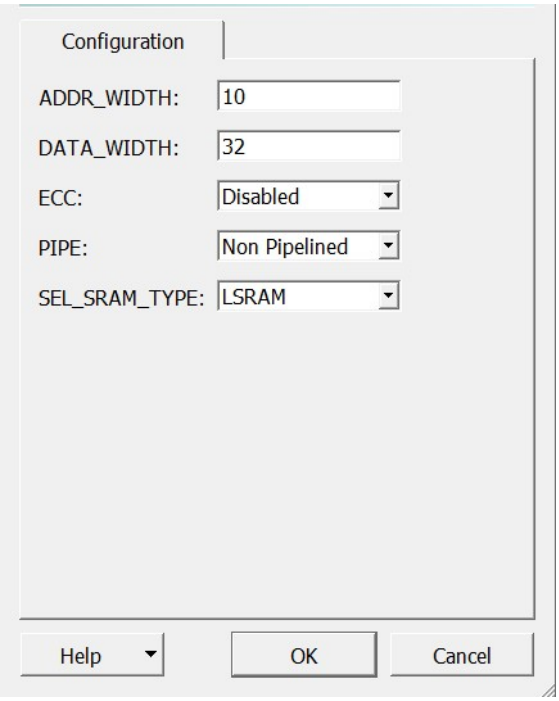


Figure 10 • **SmartDesign Configuration Window**



7.4 Simulation Flow

The User Testbench for CoreColDet is included in all the releases.

To run simulations, select the **User Testbench** flow within **SmartDesign CoreColDet** configuration GUI, right-click the canvas, and select **Generate Design**.

When SmartDesign generates the design files, it will install the user testbench files.

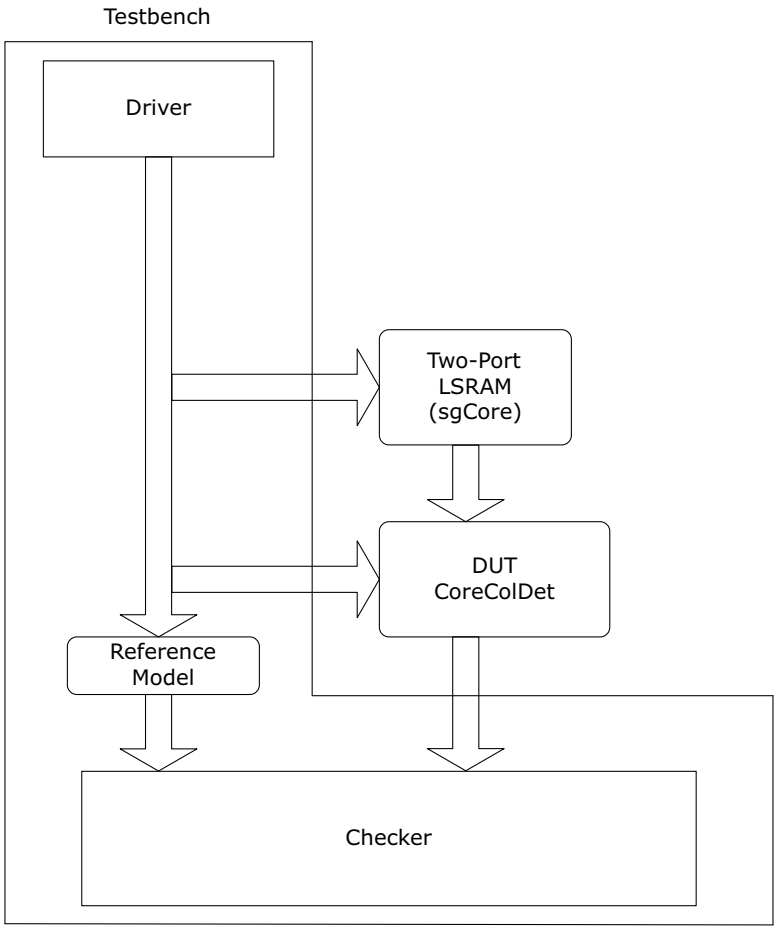
To run the user testbench, set the design root to the CoreColDet instantiation in the Libero® System-on-Chip (SoC) design hierarchy pane and click **Simulation** in the Libero SoC Design Flow window. This will invoke ModelSim® and automatically run the simulation.

7.4.1 User Testbench

The user test bench is designed by using two-port LSRAM (SgCore) of different families with **ADDR_WIDTH** =10 and **DATA_WIDTH** =18 (for RTG4, SmartFusion2, and IGLOO2) or **DATA_WIDTH** = 20 (for PolarFire and PolarFire SoC). Parameters ECC and PIPE are configurable.

The user testbench instantiates a CoreColDet DUT and two-port LSRAM macro as shown in the following figure:

Figure 11 • **CoreColDet User Test-bench**



7.5 Synthesis in Libero SoC

After setting the design root appropriately for the design, use the following steps to run the Synthesis.

1. Click **Synthesis** in the Libero SoC software. The Synthesis window appears displaying the Synplicity project.
2. Set Synplicity to use the Verilog 2001 standard, if Verilog is used.
3. Click **Run.**

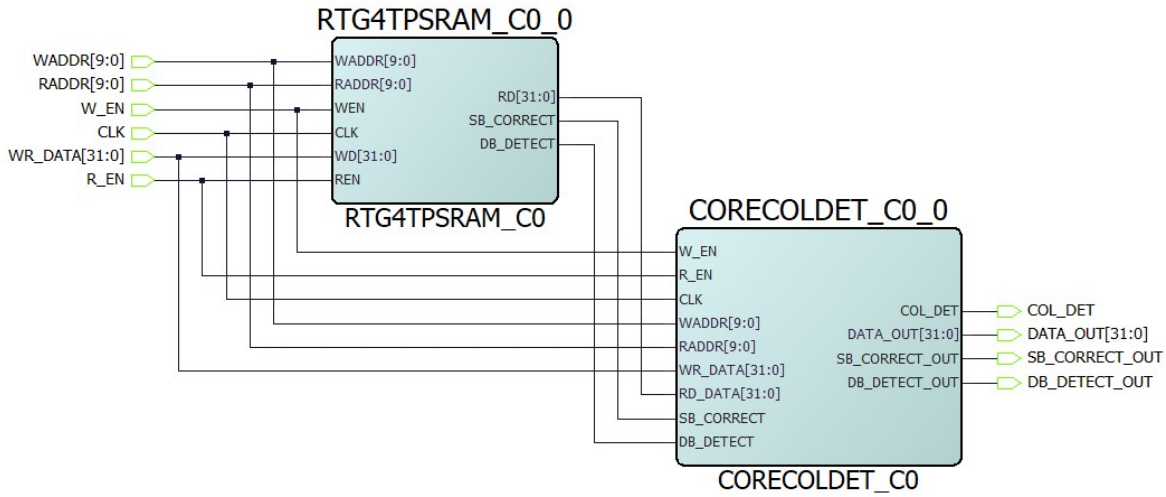
7.6 Place and Route

After setting the design route appropriately for the design, and running Synthesis, click **Layout** in the Libero SoC software to invoke Designer. CoreColDet does not require any special place-and-route settings.

8 System Integration

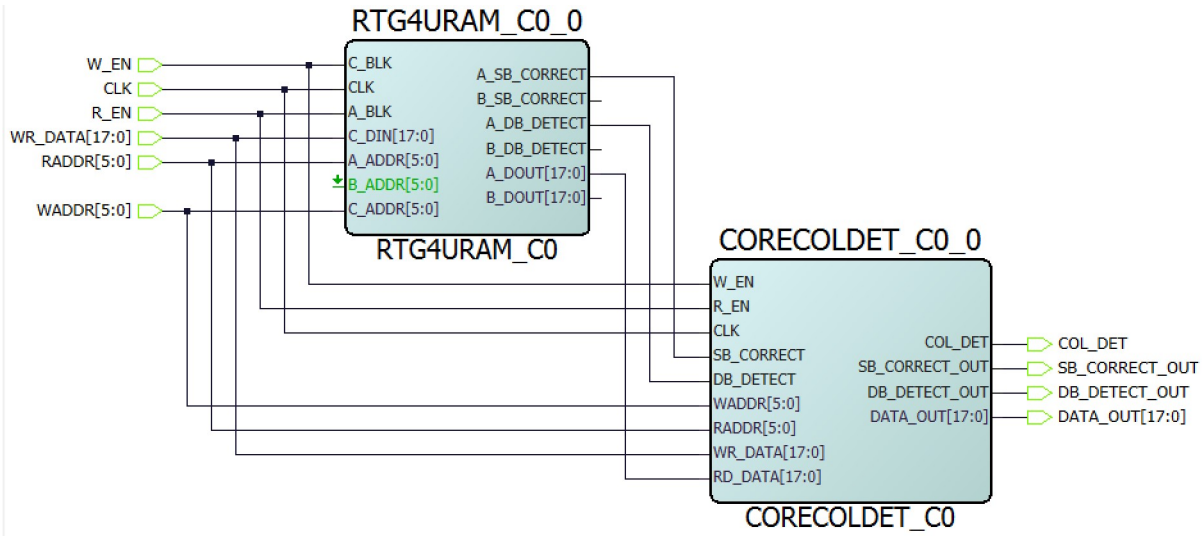
This section provides an example, that shows the integration of CoreColDet.

Figure 12 • **CoreColDet Example Design**



The example design described in this section contains CoreColDet and RTG4 two-port LSRAM (SgCore).

Figure 13 • **CoreColDet Example Design**



The example design described in this section contains CoreColDet and RTG4 Micro SRAM (SgCore).

Note: Micro SRAM (uSRAM) supports two read ports (Port A and Port B) as shown in the preceding figure. In the example design Port A is selected as read port. The user can use either of the two read ports.