RN0175
Release Notes
CoreAXI4Interconnect v2.8

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 8.0

Published in March 2020. The core was updated to v2.8.

1.2 Revision 7.0

Published in September 2019. The core was updated to v2.7.

1.3 Revision 6.0

Published in May 2019. The core was updated to v2.6.

1.4 Revision 5.0

Published in April 2018. The core was updated to v2.5.

1.5 Revision 4.0

Published in November 2017. The core was updated to v2.4.

1.6 Revision 3.0

Published in June 2017. The following were the summary of updates in revision 3.0 of this document.

- The core is updated to v2.3.
- Support to number of slaves is upgraded to 32. For more information, see Key Features, page 2.

1.7 Revision 2.0

Published in April 2017. The core was updated to v2.2.

1.8 Revision 1.0

Published in February 2017. It was the first publication of this document. The core v2.0 was created.

2 CoreAXI4Interconnect

This release notes accompanies the production release of CoreAXI4Interconnect v2.8 IP Core. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.1 Key Features

CoreAXI4Interconnect is a configurable core with the following features:

- AXI protocol compliant. It can be configured to support AXI4, AXI3, and AXI4-Lite protocols on all master or slave ports, and can also be configured to support AHB-Lite protocol on master ports.
- The AXI4 Interconnect core breaks-up burst transactions of more than 16 data beats from AXI4 masters into multiple transactions of not more than 16 beats when addressed to an AXI3 slave.
- The AXI4 Interconnect core breaks-up burst transactions of more than 1 data beats from AXI4 or AXI3 masters into multiple transactions of 1 beats when addressed to an AXI4 slave.
- Interface data widths:
  - AXI4/AXI3/AHB-Lite: 32, 64, 128, 256, or 512 bits
  - AXI4-Lite: 32 or 64 bits
- Address width: Up to 64 bits
- USER width (per channel): Up to 64 bits
- ID width: Up to 8 bits
- Support for Read-only and Write-only masters and slaves, resulting in reduced resource utilization.
- Support for up to 16 masters and 32 slaves
- Support AXI3/AXI4 read interleaving

2.2 Delivery Types

CoreAXI4Interconnect is license free.

2.2.1 Register Transfer Level (RTL)

The complete RTL source code is provided for the core and testbench.

2.3 Supported Families

CoreAXI4Interconnect supports the following families:

- PolarFire SoC
- PolarFire®
- SmartFusion®2
- IGLOO®2
- RTG4

2.4 Supported Tool Flows

This version of CoreAXI4Interconnect requires Libero® SoC v12.2 or later.

2.5 Installation Instructions

The CoreAXI4Interconnect `.CPZ` file must be installed in the Libero SoC. This is automatically installed through the Catalog update function in the Libero software, or the `.CPZ` file can be manually added using the **Add Core** catalog feature. Once installed in the Libero catalog, the core can be instantiated and configured.

For more information and instructions on core installation, licensing, and general use, see the *Using DirectCore section in Libero SoC for Classic Constraint Flow User Guide* or *Libero SoC Online Help*.

2.6 Supported Test Environments

Verilog user test bench is the supported test environment.

2.7 Documentation

This release contains a copy of the *CoreAXI4Interconnect Handbook*. The handbook describes the core functionality, gives step-by step instructions on how to simulate, synthesize, and place-and-route the core, and also provides implementation suggestions. For more information about IP, visit: http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores. For updates and additional information about software, FPGAs, and hardware, see: http://www.microsemi.com.

2.8 Known Issues and Workarounds

The following section describes the known issues and workarounds. The support to migrate from CoreAXI4Interconnect v2.7 to CoreAXI4Interconnect v2.8 can be obtained from the Microsemi technical support team.

2.8.1 Migration Issue

The following is an issue and work around associated with the migration.

2.8.1.1 CoreAXI4Interconnect IP Core may not be Reconfigured after Migrating from v2.7 to v2.8

There is a possibility that the user might not be able to reconfigure the CoreAXI4Interconnect IP Core, if the following configurations are used in CoreAXI4Interconnect v2.7 and migrated to CoreAXI4Interconnect v2.8.

1. Number of Masters configured to 1 or
2. Number of Slaves configured to 1 or
3. Optimization is configured to either **Performance** or **Area**

To fix the issue, the user should delete all the instances of CoreAXI4Interconnect v2.7 and use CoreAXI4Interconnect v2.8 from the scratch to configure the CoreAXI4Interconnect IP Core.

2.9 Resolved Issues

The following table lists the resolved issues in v2.8 Release.

Table 1 • **Resolved SARs in CoreAXI4Interconnect v2.8 Release**

SAR	Description
109370	Configurator Issue with the latest versions of COREAXI4INTERCONNECT.
109518	Enhancement Request: Hide unused parameters from the configurator.
108796	Updated Handbook, which needed more information about simulation section.
107729	Data corruption observed with different ID's.
111135	Enhancement: Throughput improvement for the FIXED burst type (AXI4/AXI3).

The following table lists the resolved issues in v2.7 Release.

Table 2 • **Resolved SARs in CoreAXI4Interconnect v2.7 Release**

SAR	Description
108003	ADDR_WIDTH_INT parameter is not updated correctly.
108232	Getting place and route errors in Libero v12.2 due to AXI4Interconnect core.
107433	Enhance presentation of configuration information.

The following table lists the resolved issues in v2.6 Release.

Table 3 • **Resolved SARs in CoreAXI4Interconnect v2.6 Release**

SAR	Description
88348	Add Support for 64bit address.
91000	Read/write transactions latency is very high when CDC is enabled.
94231	AHB Master: Timings are not meeting.
98837	CoreAXI4Interconnect does not use reset signals for all the flip flops.
100431	IP Core stops passing WLAST from master to slave when slave type is configured to AXI3 and SLAVE_FIFO_ADDRESS_DEPTH and SLAVE_FIFO_DATA_DEPTH parameters are configured to 8.
104032	IP Core stops passing slave AWREADY/ARREADY to master AWREADY/ARREADY when master issues outstanding transactions on multiple threads (ids).
105985	CoreAXI4Interrconnect IP HB missing information and clarifications required.
106185	Enhancement request - Add support for 16 masters.

The following table lists the resolved issues in v2.5 Release.

Table 4 • **Resolved SARs in CoreAXI4Interconnect v2.5 Release**

SAR	Description
94407	Enhanced the address decoding section.
94651	Updated the minimum and maximum vector in the GUI and the Core AXI4 Handbook.
95143	Added RTG4 support to CoreAXI4Interconnect.