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Release Notes
CoreFPU v2.0

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

This is the first publication of this document. Created for CoreFPU v2.0.

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2 CoreFPU v2.0

2.1 Overview

These release notes accompany the production release of CoreFPU v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

The Core Floating Point Unit (CoreFPU) is designed for floating-point arithmetic and conversion operations for single precision floating point numbers. CoreFPU supports conversion operations like fixed-point to floating-point, floating-point to fixed-point and arithmetic operations like addition, subtraction, and multiplication.

CoreFPU has following features:

1. Supports single precision floating numbers as per IEEE-754 standard.
2. Conversions
   - Fixed Point to Floating Point Conversion
   - Floating Point to Fixed Point Conversion
3. Arithmetic Operations
   - Floating Point Addition
   - Floating Point Subtraction
   - Floating point Multiplication
4. Provides flags for Overflow, Infinity, and Not-a-Number (NaN) for floating point numbers.
5. Fully pipelined implementation of arithmetic operations.
6. Provision to configure the core for design requirements.

2.3 Delivery Types

The following is a list of deliverables:

- Verilog Source
- User Testbench
- Core Release Notes
- Core Handbook

2.4 Supported Families

- Polarfire SoC
- PolarFire
- RTG4

2.5 Supported Tool Flows

CoreFPU requires Libero v12.3 or higher.

2.6 Installation Instructions

CoreFPU must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the core Handbook. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

User testbench is provided with the core.

2.9 Release History

Table 1 lists the release history.

Table 1 • **Release History**

Version	Date	Changes
2.0	April 2020	Initial release.

2.10 Discontinued Features and Devices

There are no discontinued features and devices.

2.11 Known Limitations and Workarounds

None.