HB0716

CoreAXI4SRAM v2.1 Handbook

02 2017

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document. Created for CoreAXI4SRAM v2.1.

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2 Preface

2.1 About this Document

This handbook provides details about the CoreAXI4SRAM and how to use it.

2.2 Intended Audience

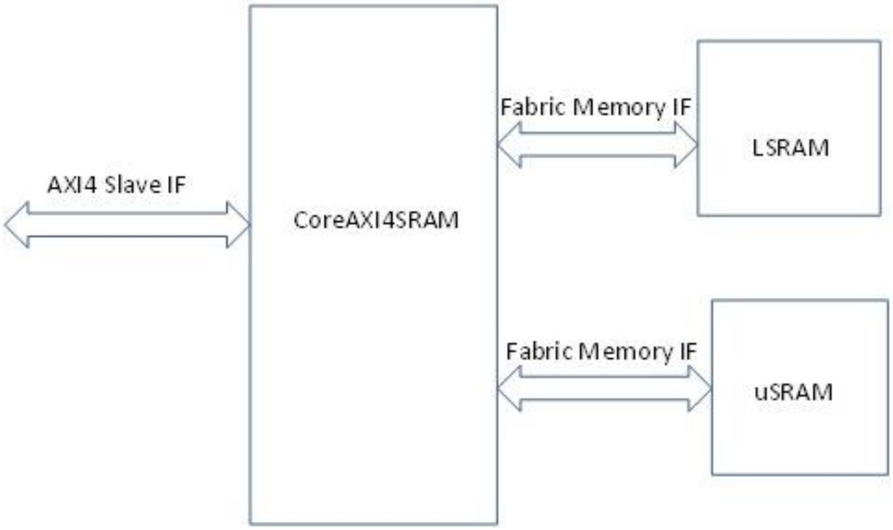
FPGA designers using Libero® System-on-Chip (SoC).

3 Introduction

3.1 Overview

The CoreAXI4SRAM is an AXI4 slave memory controller and provides access to fabric memories on PolarFire devices.

Figure 1 CoreAXI4SRAM Block Diagram



The CoreAXI4SRAM provides access to the embedded large SRAM (LSRAM) and small SRAM (uSRAM) blocks available on the PolarFire system-on-chip (SoC) field programmable gate array (FPGA) family device. The core provides an AXI4 Slave interface for addressing and accessing data from the connected memory devices. It facilitates convenient access to fabric SRAM by AXI4 master. The CoreAXI4SRAM IP is programmable through parameter configuration.

The AXI protocol defines five independent channels, which are: Write address channel, Read address channel, Write data channel, Write response channel, and Read data channel. Refer to the AMBA3 AXI specification document for more details.

3.2 Features

- Supports AXI4 protocol only
- Supports 1:1 synchronous clock
- Interface data widths: 32 and 64-bits
- Supports 32-bit address bus
- Supports single/burst transfers
- Supports AXI4 increment and wrap transfers, except fixed transfers
- Configurable Read / Write, Read-only or Write-only interfaces

The following features are not supported:

- No support for streaming masters
- Does not support AXI4 user and region signals
- Does not support AXI4 QoS signals
- Does not support low power interface signals
- No trust zone security support
- Does not support data width conversion. Microsemi recommends you to use the Microsemi CoreAXI4Interconnect for data width conversion.
- Does not support AXI3 to AXI4 protocol conversion. Microsemi recommends you to use the Microsemi CoreAXI4Interconnect for protocol conversion.

3.3 Core Version

This handbook is for CoreAXI4SRAM version 2.1.

3.4 Supported Families

- PolarFire

3.5 Device Utilization and Performance

Utilization and performance data is listed in Table 1 for the PolarFire device family. The data listed in this table is indicative only. The overall device utilization and performance of the core is system dependent.

Table 1 CoreAXI4SRAM Device Utilization

Family	AXI4_DWIDTH	SEL_SRAM_TYPE	MEM_DEPTH	WRAP_SUPPORT	AXI4_IFTYPE_WR	AXI4_IFTYPE_RD	Logic Elements				Frequency (MHz)
							Sequential	Combinatorial	Total	%	
PolarFire	64	1	512	0	1	1	347	450	797	0.27	172
PolarFire	64	1	1024	0	1	1	346	503	849	0.29	168
PolarFire	32	1	512	1	1	1	383	1143	1526	0.51	117
PolarFire	32	1	4096	0	1	1	513	745	1258	0.42	159
PolarFire	64	0	64	0	1	1	353	454	807	0.27	169
PolarFire	32	0	256	0	1	1	393	550	943	0.31	167
PolarFire	64	0	192	1	1	1	688	1554	2242	0.75	116
PolarFire	32	0	512	0	1	1	591	877	1468	0.49	167

Note: The data in this table is achieved using typical synthesis and layout settings. Frequency (in MHz) was set to 100 and speed grade was -1.

4 Functional Description

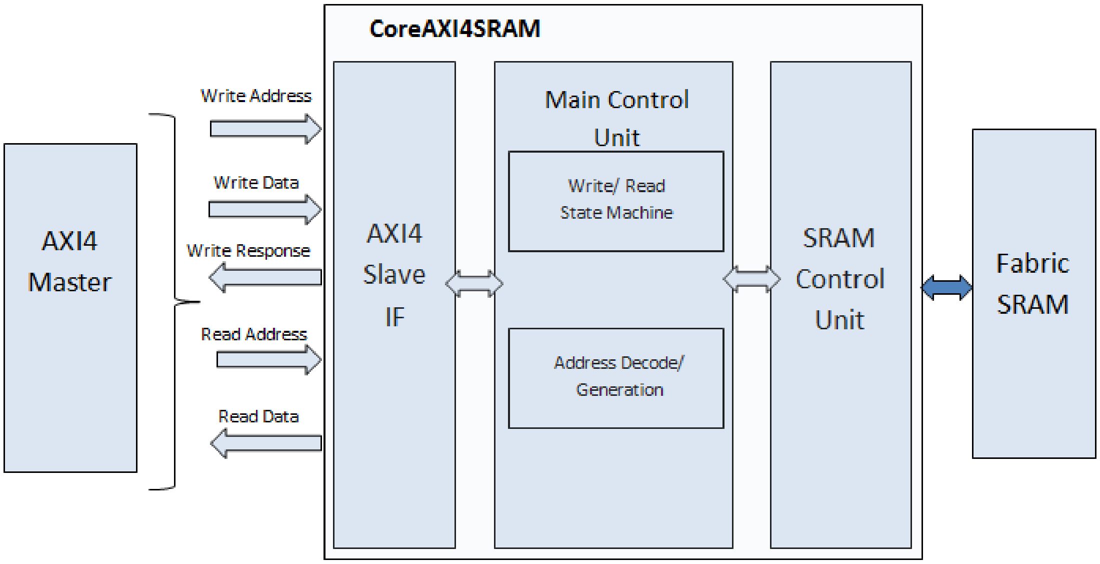
The AXI4 master communicates with CoreAXI4SRAM slave by requesting access by providing transaction details on Write address channel or Read address channel. The CoreAXI4SRAM consists of three major functional blocks, AXI4 Slave Interface block, Main Control logic block, and SRAM Memory Interface logic block. A basic block diagram of the design for CoreAXI4SRAM is as shown in Figure 2.

The connected AXI4 master communicates with the CoreAXI4SRAM slave interface. The master performs requests access to fabric memory by issuing write/read requests on the Write address channel or Read address channel respectively.

Following are the three major functional blocks of CoreAXI4SRAM:

- Slave Interface Logic
- Main Control Logic
- SRAM Interface Control Logic

Figure 2 CoreAXI4SRAM Design Diagram



4.1 AXI4 Slave Interface Logic

The core provides AXI4 slave interface to connect to the AXI4 master or AXI4 interconnect bus interface. The AXI4 slave interface of the core complies with AMBA® AXI4 protocol specifications. The core supports single beat or burst AXI4 transactions. The burst transactions for incremental bursts [INCR] can be from 1 beat to 256 beats and the burst transactions for wrapping burst [WRAP] can be 2, 4, 8, or 16 beats. The CoreAXI4SRAM does not support fixed type of burst transactions.

The core does not support outstanding write/read transactions. It de-asserts the ready to the AXI4 Master and re-asserts only when the current transaction is complete.

4.2 Main Control Logic

The Main Controller block contains control state machines to perform read/write to the fabric memories. This block interfaces between the AXI4 slave interface block and the SRAM Control logic block. It is responsible for the generation of the necessary control signals required to access the fabric memory. The AXI4 interface of the core also performs the write and read channel arbitration and the address decoding functionalities. The channel arbitration implements a round robin algorithm and is applicable only when both AXI4 write channels and AXI4 read channels are active simultaneously. The core responds to read and write transactions in round robin manner. This guarantees that none of the AXI channels are held back in wait mode. The address decoding logic utilizes the address received on the AXI4 slave interface to generate the SRAM read/write address for the selected memory type.

4.3 SRAM Interface Control Logic

The SRAM Control logic block performs read/write to the fabric memories. It generates the necessary memory control signals associated with the selected memory type (based on SEL_SRAM_TYPE configuration). This block is responsible for generation of the address and enables signals to the fabric memories. In addition, it also aligns the address and data received from the AXI4 interface module to match the address and data width configured for the fabric memory.

5 Feature Description

5.1 Write Only Interface

The core supports Write-Only interface resulting in reduced resource utilization. This interface is enabled by default. The parameter AXI4_IFTYPE_WR is used to enable/ disable the interface.

5.2 Read Only Interface

The core supports Read-Only interface resulting in reduced resource utilization. This interface is enabled by default. The parameter AXI4_IFTYPE_RD is used to enable/ disable the interface.

6 Interface

I/O Signal descriptions for CoreAXI4SRAM are defined in Table 2.

Table 2 I/O Signals

Port Name	Width	Direction	Description
Global Signal Ports			
ACLK	1	In	AXI clock. All the AXI signals inside the block are clocked on the rising edge.
ARESETN	1	In	AXI reset signal. The signal is active low. Asynchronous assertion and synchronous de-assertion. This is used to reset all the AXI registers in the Block.
AXI Slave Interface Ports			
AXI Write ADDRESS CHANNEL			
AWID	AXI4_IDWIDTH	In	Write Address ID. This Signal is the Identification tag for the write address group of signals.
AWADDR	AXI4_AWIDTH	In	Write address. The write address bus gives the address of the first transfer in a write burst. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
AWLEN	8	In	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
AWSIZE	3	In	Burst size. This signal indicates the size of each transfer in the burst.
AWBURST	2	In	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated. **Note:** AXI4 fixed type transactions are not supported by the core.
AWLOCK	2	In	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
AWCACHE	4	In	Memory type. This signal indicates how transactions are required to progress through a system.
AWPROT	3	In	Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access.
AWVALID	1	In	Write address valid. This signal indicates that valid write address and control information are available: 1 = Address and control available 0 = Address and control not available
AWREADY	1	Out	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = Slave ready 0 = Slave not ready

AXI Write DATA CHANNEL			
WDATA	AXI4_DWIDTH	In	Write data bus is 64 bits wide.
WSTRB	8	In	Write strobes. This signal indicates, which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. WSTRB[n] corresponds to WDATA [(8 × n) + 7 :(8 × n)].
WLAST	1	In	Write last. This signal indicates the last transfer in a write burst.
WVALID	1	In	Write valid. Indicates that valid write data and strobes are available: 1 = Write data and strobes available 0 = Write data and strobes unavailable
WREADY	1	Out	Write ready. This indicates that the slave can accept the write data: 1 = Slave ready 0 = Slave not ready
AXI Write RESPONSE CHANNEL			
BID	AXI4_IDWIDTH	Out	Response ID. This is the identification tag for the write response. The BID must match the AWID value of the write transaction to which the slave is responding.
BRESP	2	Out	Write response. This signal indicates the status of the write transaction. The allowable responses are: 00 = OKAY 01 = EXOKAY 10 = SLVERR DECERR is not supported.
BVALID	1	Out	Write response valid. Indicates that a valid write response is available: 1 = Write response available 0 = Write response not available
BREADY	1	In	Response ready. This signal indicates that the master can accept the response information: 1 = Master ready 0 = Master not ready

AXI Read ADDRESS CHANNEL			
ARID	AXI4_IDWIDTH	In	Read Address ID. This signal is the identification tag for the read address group of signals.
ARADDR	AXI4_AWIDTH	In	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided.
ARLEN	8	In	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
ARSIZE	3	In	Burst size. This signal indicates the size of each transfer in the burst.
ARBURST	2	In	Burst type. The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated.
ARLOCK	2	In	Lock Type. This signal provides additional information about the atomic characteristics of the transfer.
ARCACHE	4	In	Memory type. This signal indicates how transactions are required to progress through a system
ARPROT	3	In	Protection type. This signal indicates the privilege and security level of the transaction, and whether the transaction is a data access or an instruction access.
ARVALID	1	In	Read address valid. This signal indicates, when HIGH, that the read address and control information is valid: 1 = Address and control valid 0 = Address and control not valid
ARREADY	1	Out	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals: 1 = Slave ready 0 = Slave not ready
AXI Read RESPONSE CHANNEL			
RID	AXI4_IDWIDTH	Out	Read ID Tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding.
RDATA	AXI4_DWIDTH	Out	Read data. Read data bus is 64-bits wide.
RRESP	2	Out	Read Response. This signal indicates the status of the read transfer. The allowable responses are: 00 = OKAY 01 = EXOKAY 10 = SLVERR DECERR is not supported.
RLAST	1	Out	Read Last. This signal indicates the last transfer in a read burst.
RVALID	1	Out	Read Valid. This signal indicates that the required read data is available and the read transfer can complete: 1 = Read data available 0 = Read data not available
RREADY	1	In	Read ready. This signal indicates that the master can accept the read data and response information:

			1= Master ready 0 = Master not ready

6.1 Configuration Parameters

6.1.1 CoreAXI4SRAM Configurable Options

There are a number of configurable options that apply to CoreAXI4SRAM as shown in Table 3. If a configuration other than the default is required, use the configuration dialog box in SmartDesign to select appropriate values for the configurable options.

Table 3 CoreAXI4SRAM Configuration Parameters

Name	Valid Range	Default	Description
FAMILY	26	26	Must be set to the required FPGA family: 26 = PolarFire
AXI4_AWIDTH	32	32	Address Width.
AXI4_DWIDTH	32, 64	64	Write/Read data bus on AXI side.
AXI4_IDWIDTH	4	4	Width of ID field for all AXI channels. Note: AXI4_IDWIDTH is fixed to four.
AXI4_IFTYPE_WR	0-1	1	When 1: Supports write operation. **Note:** AXI4_IFTYPE_WR = 0 and AXI4_IFTYPE_RD = 0 is an illegal selection. Atleast one of the two above parameters needs to be selected to 1.
AXI4_IFTYPE_RD	0-1	1	When 1: Supports read operation. **Note:** AXI4_IFTYPE_WR = 0 and AXI4_IFTYPE_RD = 0 is an illegal selection. Atleast one of the two above parameters needs to be selected to 1.
SEL_SRAM_TYPE	0-1	1	1: Select LSRAM memory 0: Select Small SRAM memory
MEM_DEPTH	512-524288 for LSRAM 64-2048 for uSRAM	512 (LSRAM), 64 (uSRAM)	Memory depth. In steps of 512 bytes when SEL_SRAM_TYPE = 1 (for Large SRAM). **Note:** For LSRAM available depth is 512 in this revision. Step size for uSRAM = 64. Note: For uSRAM available depth is 64 in this revision.
WRAP_SUPPORT	0-1	0	Select AXI wrapping burst transactions. Wrapping burst transactions are disabled by default. **Note:** This option should only be enabled if required as it has a significant impact on logic resource consumption and maximum operating frequency.

7 Timing Diagrams

CoreAXI4SRAM IP complies with the AMBA® AXI4 protocol specifications timings.

8 Tool Flow

8.1 License

CoreAXI4SRAM does not require a register transfer level (RTL) license to be used and instantiated.

8.2 RTL

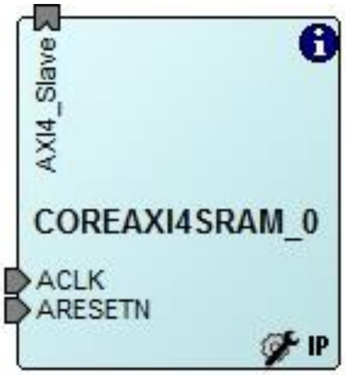
Complete RTL source code is provided for the core and testbenches.

8.3 SmartDesign

CoreAXI4SRAM is preinstalled in the SmartDesign IP Deployment design environment. An example instantiated view is as shown in Figure 3. The core can be configured using the configuration GUI within the SmartDesign, as shown in Figure 4.

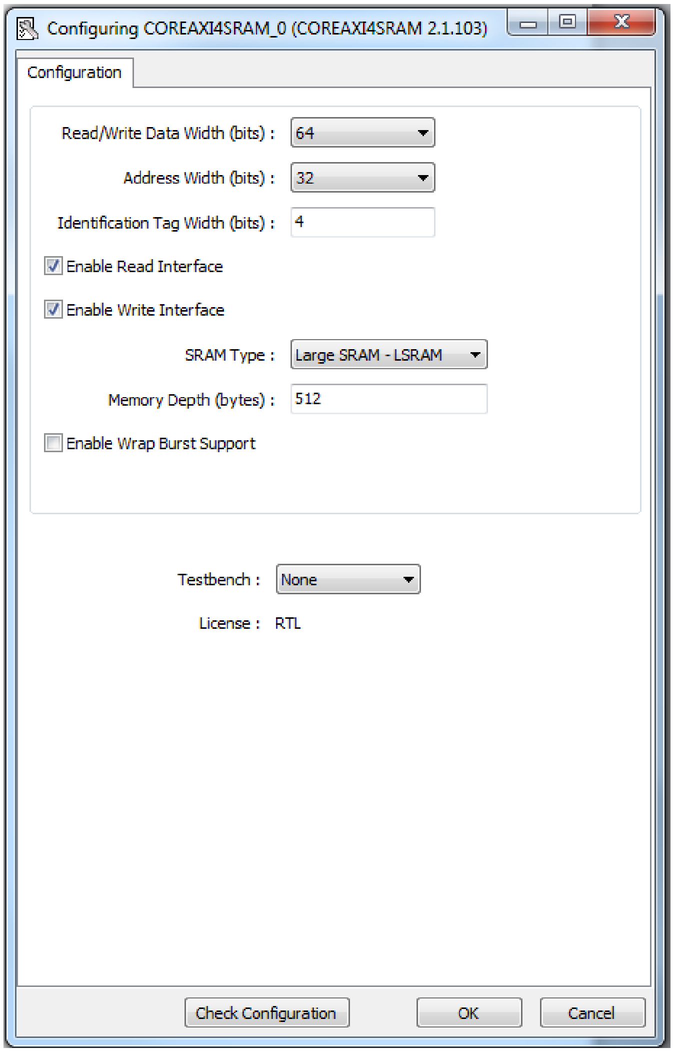
For more information on using SmartDesign to instantiate and generate cores, refer to the Using DirectCore in Libero® SoC User Guide.

Figure 3 SmartDesign CoreAXI4SRAM Instance View



8.4 Configuring CoreAXI4SRAM in SmartDesign

Figure 4 Configuring CoreAXI4SRAM in SmartDesign



Configuring COREAXI4SRAM_0 (COREAXI4SRAM 2.1.103)

Configuration

Read/Write Data Width (bits) : 64

Address Width (bits) : 32

Identification Tag Width (bits) : 4

☑ Enable Read Interface

☑ Enable Write Interface

SRAM Type : Large SRAM - LSRAM

Memory Depth (bytes) : 512

□ Enable Wrap Burst Support

Testbench : None

License : RTL

8.5 Simulation Flows

The User Testbench for CoreAXI4SRAM is included in all releases.

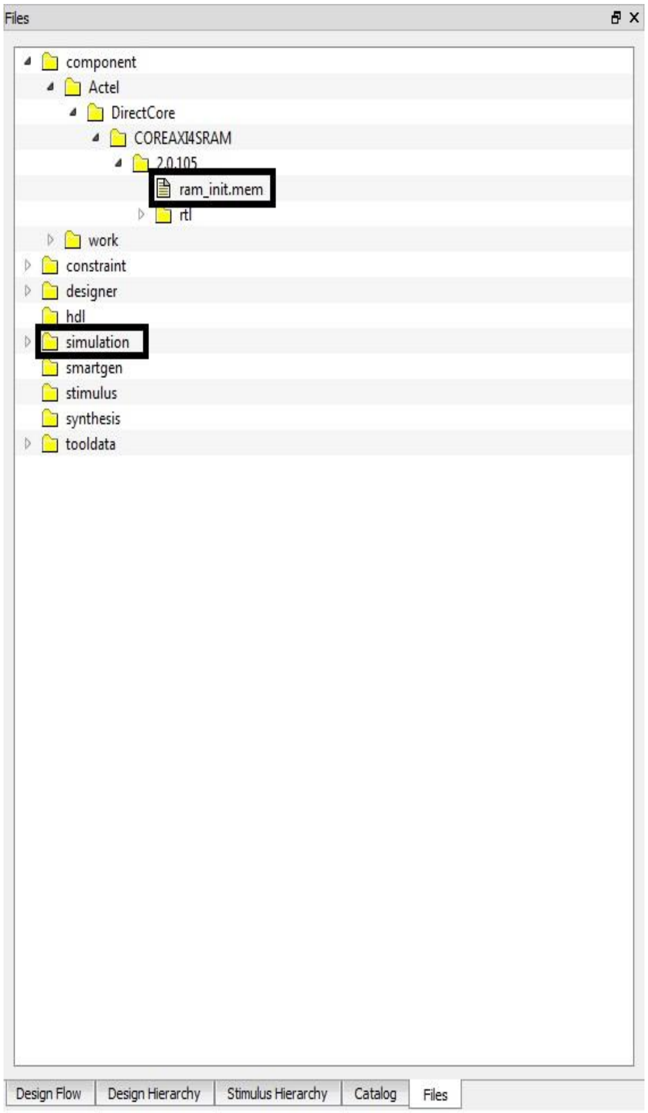
To run simulations, select the User Testbench flow within SmartDesign and click Save and Generate on the Generate pane. The User Testbench is selected through the Core Testbench Configuration GUI.

When SmartDesign generates the Libero SoC project, it installs the user testbench files.

To run the User Testbench, set the design root to the CoreAXI4SRAM instantiation in the Libero SoC design hierarchy pane and click the Simulation icon in the Libero SoC design flow window. This invokes ModelSim® and automatically run the simulation.

Note: To run the User testbench, copy the Libero generated ram_init.mem (/component/Actel/DirectCore/CoreAXI4SRAM/<version_no>/ram_init.mem) file in to Simulation directory in the Libero SoC 'files' pane as shown in the Figure 5.

Figure 5 Simulation Directory in the Libero SoC 'files' Pane



8.6 Synthesis in Libero

To run synthesis on the core, set the design root to the SmartDesign design and click the **Synthesis** icon in Libero SoC. The Synthesis window appears displaying the Synplify® project. To run **Synthesis**, select the **Run** icon.

8.7 Place-and-Route in Libero

After the design is synthesized, run the compilation and then place-and-route the tools. CoreAXI4SRAM requires no special place-and-route settings.

9 Testbench

A unified test-bench is used to verify and test CoreAXI4SRAM called as user test-bench.

9.1 User Test-bench

The user test-bench is included with the releases of CoreAXI4SRAM that verifies few features of the CoreAXI4SRAM.

Figure 6 CoreAXI4SRAM User Test-bench

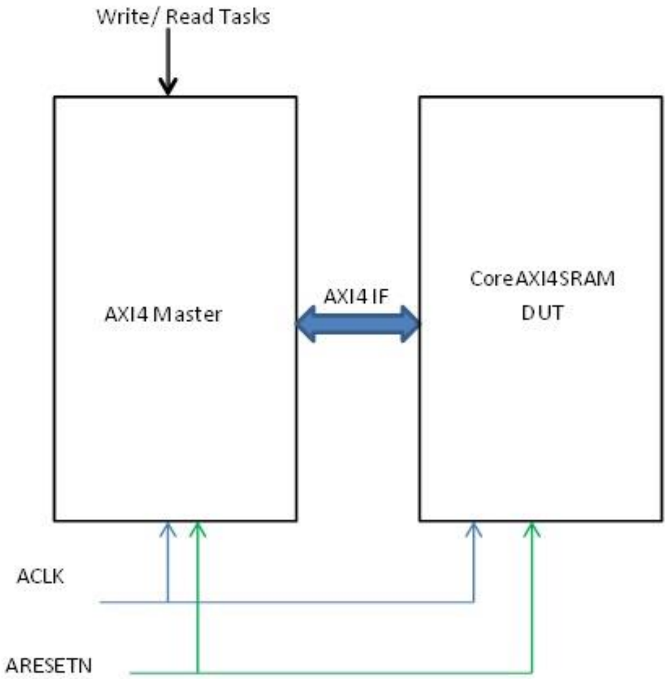


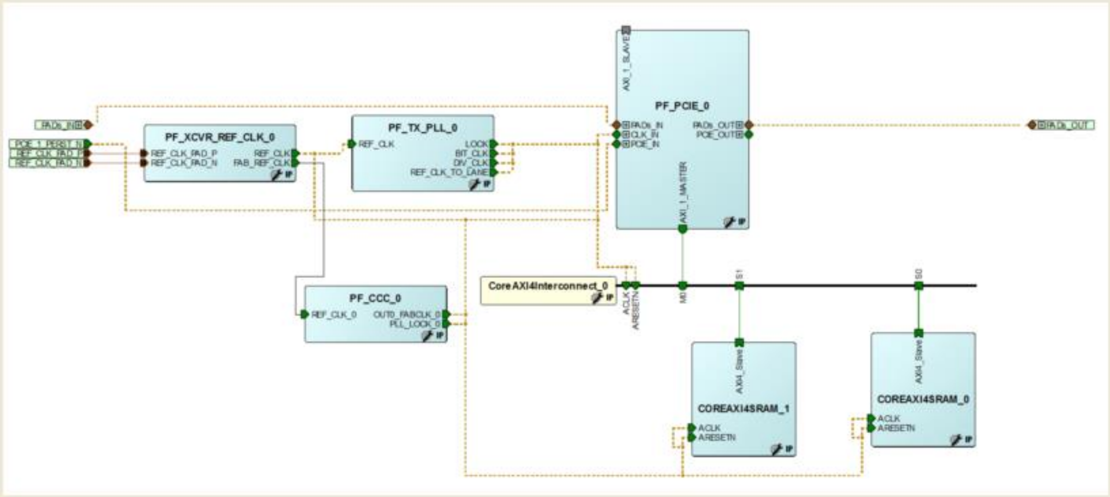
Figure 6 shows the user test bench instantiating a Microsemi® DirectCore CoreAXI4SRAM DUT, the AXI Master model, and an AXI4SRAM DUT. The AXI master model drives the Write and Read transactions to the DUT. The IP core sends the corresponding response and the test bench environment determines whether or not the transaction is successful.

Note: The User testbench for VHDL is fixed to run at AXI4_DWIDTH = 64 only.

10 System Integration

The example design configures the CoreAXI4SRAM IP and tests the PCIe application on the PolarFire device.

Figure 7 CoreAXI4SRAM Example Design



- CoreAXI4SRAM is connected to System clock generated by the PLL.
- Fabric reset is used to reset the core.
- CoreAXI4SRAM is connected to the slave interface of the CoreAXI4Interconnect and accessed by the PCIe controller on the master interface.

The example design can be obtained from the Microsemi technical support team.

11 Ordering Information

11.1 Ordering Codes

Order CoreAXI4SRAM through your local Microsemi sales representative. Use the following number convention when ordering: CoreAXI4SRAM-XX. XX is listed in Table 4.

Table 4·Ordering Codes

XX	Description
RM	RTL for RTL source — multiple-use license.