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CoreXAUI v2.0 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document. Created for CoreXAUI v2.0.

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2 CoreXAUI v2.0 Release Notes

2.1 Overview

These release notes accompany the production release of CoreXAUI v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CoreXAUI v2.0 has the following features:

- Operations frequency of 156.25MHz
- Pseudorandom Idle Insertion using PRBS X7 + X3 + 1
- XAUI (Idle Character) Encoding
- Support 64bit @ SDR in transmitter and receiver path
- Will use PF_XCVR built-in 8B10B Encoder
- Will use PF_XCVR built-in 8B10B Decoder and COMMA word aligner
- Support multichannel alignment and lane deskew in receiver path
- XAUI (Idle Character) Decoding
- Support for 10Gbps data rate across four lanes of SERDES running at 3.125 GHz
- Support for 10Gbps data rate across two lanes of SERDES running at 6.25 GHz (that is, support for RXAUI)

2.3 Delivery Types

CoreXAUI has two delivery types: RTL and Obfuscated.

The RTL source is license locked while the Obfuscated source is available for free.

2.3.1 Obfuscated

- Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign.
- Simulation, Synthesis, and Layout can be performed with Libero software. The RTL code for the core is obfuscated using the IP encryption (encryptP1735.pl) solution.

2.3.2 RTL

Complete RTL source code is provided for the core.

2.4 Supported Families

- PolarFire™

2.5 Supported Tool Flows

This version of the core requires Libero PolarFire SoC v2.0 or later.

2.6 Installation Instructions

The CoreXAUI CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *CoreXAUI Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

- Verilog user testbench
- VHDL user testbench

2.9 Resolved History

Table 1 lists the release history for CoreXAUI.

Table 1 • **Release History**

Version	Date	Changes
2.0	March 2018	• First Production release.

2.10 Known Issues and Workarounds

There are no known limitations or workarounds in the CoreXAUI v2.0 release.