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Release Notes
CoreUSXGMII v2.0

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

This is the first publication of this document. Created for CoreUSXGMII v2.0.

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2 CoreUSXGMII v2.0

2.1 Overview

These release notes accompany the production release of CoreUSXGMII v2.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CoreUSXGMII (Universal Serial Media Independent Interface) IP is used to carry single network port over a single SERDES between the MAC and PHY for Multi-Gigabit technology at 1G/ 2.5G/ 5G/ 10G data rate.

CoreUSXGMII has following features:

- Convey Single network ports over an USXGMII MAC-PHY interface (USXGMII-S Only - USXGMII-Copper PHY: EDCS- 1150953)
- Supports operating speed rates of 1G/2.5G/5G/10G
- MAC side interface is 64-bit XGMII
- Support for MAC side interface for 1G is 8-bit GMII interface and will be added in future release
- System interface operates in full duplex mode only
- Provides a serial 10.3125Gbps serial link on the transceiver side
- Provides 64-bit interface to Microsemi Transceiver operating in PCS 64B66B Clause 49
- Supports Clause 37 Auto-negotiation between MAC and PHY
- APB management interface for configuration/status

2.3 Delivery Types

CoreUSXGMII is available in two versions - Evaluation and Obfuscated.

- **Evaluation:** The Evaluation version is freely available and supports four hours of functionality on silicon.
- **Obfuscated:** Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout can be performed with Libero software. The RTL code for the core is obfuscated using the IP encryption (encryptP1735.pl) solution.

2.4 Supported Families

PolarFire®

2.5 Supported Tool Flows

CoreUSXGMII requires Libero v12.0 or higher.

2.6 Installation Instructions

CoreUSXGMII must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the core Handbook. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

User testbench is not provided with the core.

2.9 Release History

Table 1 lists the release history.

Table 1 • **Release History**

Version	Date	Changes
2.0	September 2019	Initial release.

2.10 Discontinued Features and Devices

There are no discontinued features and devices.

2.11 Known Limitations and Workarounds

This release of the IP does not provide User Test bench.