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CoreSDITX v2.2 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Updated for CoreSDITX v2.2.

1.2 Revision 2.0

Updated for CoreSDITX v2.1.

1.3 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreSDITX v2.0.

Contents

3 CoreSDITX v2.2 Release Notes

3.1 Overview

These release notes accompany the production release of CoreSDITX v2.2. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

3.2 Features

CoreSDITX has the following features:

- Compliant with SMPTE 259 (SD-SDI) standard
- Compliant with SMPTE 292 (HD-SDI) standard
- Compliant with SMPTE 424 (3G-SDI) standard
- Supports data rates 270 Mb/s and 270/1.001 Mb/s for SD-SDI Level C mode
- Supports data rates 1.485 Gb/s and 1.485/1.001 Gb/s for HD-SDI mode
- Supports data rates 2.97 Gb/s and 2.97/1.001 Gb/s for 3G-SDI Level A mode
- Generates and inserts Start of Active Video (SAV) and End of Active Video (EAV) packets from timing reference information.
- Generates and inserts line number (LN) packets (in HD-SDI or 3G-SDI mode only)
- Generates and inserts Cyclic Redundancy Check (CRC) packets (in HD-SDI or 3G-SDI mode only)
- Performs Scrambling and Non-Return-to-Zero Inverted (NRZI) encoding

3.3 Delivery Types

CoreSDITX is available in two versions:

- Obfuscated
- Evaluation

The Evaluation version is freely available and supports four hours of functionality on silicon.

The Obfuscated version is license locked and will be available only with Libero Gold and Platinum Licenses.

3.4 Supported Families

- PolarFire®

3.5 Supported Tool Flows

CoreSDITX v2.2 requires Libero SoC PolarFire.

3.6 Installation Instructions

The CoreSDITX CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

3.7 Documentation

This release contains a copy of the *CoreSDITX Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

3.8 Supported Test Environments

User testbench is provided with CoreSDITX.

3.9 Release History

Table 1 lists the release history for CoreSDITX.

Table 1 • **Release History**

Version	Date	Changes
2.2	November 2018	Refer Table 2.
2.1	August 2018	Refer Table 3.
2.0	May 2018	Initial release.

3.10 Resolved Issues in the v2.2 Release

Table 2 • **Resolved Issues in the v2.2 Release**

SAR Number	Changes
100768	Added SD-SDI mode support.

3.11 Resolved Issues in the v2.1 Release

Table 3 • **Resolved Issues in the v2.1 Release**

SAR Number	Changes
100271	Re-encrypt core as per the VHDL RTL Encryption flow guidelines.

3.12 Known Limitations and Workarounds

There are no known limitations and workarounds for CoreSDITX.